BROADCOM®

Data Sheet

BCM88280

360-Gb/s Integrated Packet Processor and Traffic Manager Single-Chip Device

Overview

The Broadcom® BCM88280 series is an optimized switching solution for fifth generation (5G) mobile backhaul, cell-site routing transport and data center applications, enabling switching platforms with a mix of Ethernet, Optical Transport Network (OTN), and Flex Ethernet (FlexE) ports.

The product series belongs to the seventh generation of the DNX scalable switching product line and processes up to 360 Gb/s of traffic, operating at Layer 1 through Layer 4.

The BCM88280 integrates FlexE. The FlexE core provides an additional way to optimize the uplink bandwidth in backhaul, transport, and data center interconnect (DCI) applications. FlexE clients can manage the bandwidth allocation per service. An integrated FlexE cross-connect unit minimizes the latency of sensitive services, such as ultra-reliable and low-latency communication (URLLC), through a dedicated high-speed switching plane.

Being optimized for 5G mobile backhaul, the BCM88280 implements a fully featured, large-scale network slicing solution at wire speed. It supports the fast creation of slices and the isolation of these services in the converged network. When configuring network slices, the user can leverage the flexible forwarding classification, virtual databases, and large-scale segment routing. Bandwidth management per-slice is programmable, and supports hierarchical quality-of-service (HQoS), scheduling, and shaping. Latency-sensitive slices, such as radio traffic, can be assigned low-latency and lossless resources.

The Elastic Pipe™ packet classification engine is software programmable, with built-in support for carrier and data center networking applications.

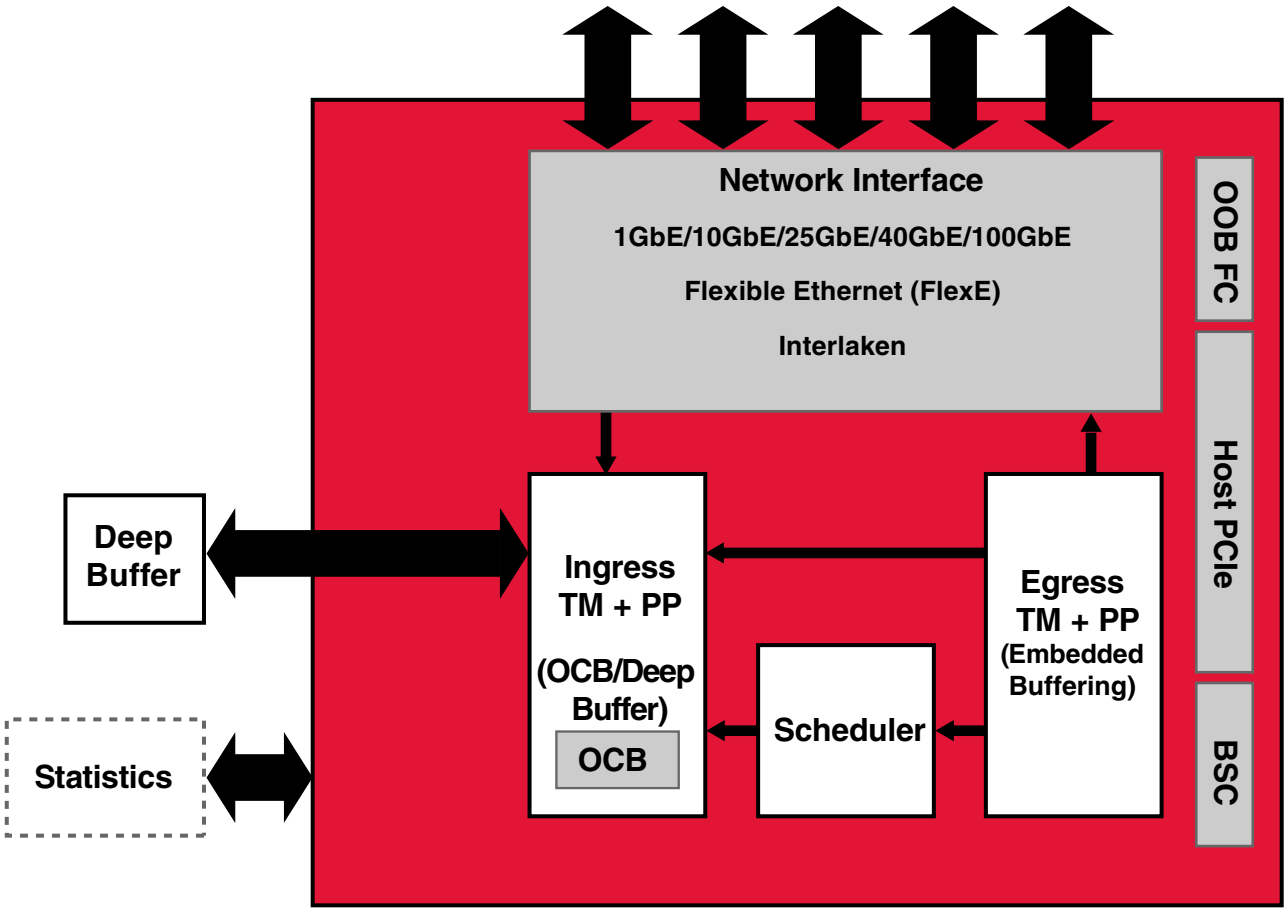
The traffic manager integrates deep-packet buffers with a distributed scheduling scheme that allows state-of-the-art HQoS, transmission scheduling per-customer, and per-service, as well as tunneling and overlay networks. Flexible flow control mechanisms support Priority-based Flow Control (PFC), Enhanced Transmission Selection (ETS), and Explicit Congestion Notification (ECN).

The integrated bypass path delivers latency-sensitive services, such as OTN, Time Division Multiplex (TDM), or mobile traffic.

Features

- Seventh-generation Dune scalable fabric access processor (FAP) product line.
- Flexible network interface:
  - 1GbE, 10GbE, 25GbE, 40GbE, 50GbE, and 100GbE interfaces.
  - Support for a mix of OTN (ODU) and Ethernet ports on the same device.
- FlexE network interface:
  - Flexible line rate.
  - Large number of FlexE clients.
- Traffic manager:
  - On-chip buffer with off-chip deep-buffering option.
  - Hierarchical memory management.
  - Programmable, hierarchical scheduling.
  - Compliant with scheduling and shaping standards, including Metro Ethernet Forum (MEF) and Broadband Forum standards.
- Flexible and software-programmable Elastic Pipe packet processor:
  - Bridging, routing, Multiprotocol Label Switching (MPLS), Virtual Private LAN Service (VPLS), Layer 2 virtual private networks (L2VPNs), Layer 3 virtual private networks (L3VPNs), and Operations, Administration, and Maintenance (OAM).
  - MPLS and IPv6 segment routing.
  - Data center tunneling encapsulations including Virtual Extensible LAN (VXLAN), Network Virtualization using Generic Routing Encapsulation (NVGRE), and Generic Network Virtualization Encapsulation (GENEVE).
  - Built-in support for data center, carrier, and metro.
  - Ethernet and packet transport applications.
  - Large on-chip tables.
- Bypass mode:
  - Delivery of latency-sensitive services, such as OTN, TDM, or mobile traffic.
  - Unified data plane for OTN and Ethernet.
- Precision Time Protocol (PTP) IEEE 1588, Synchronous Ethernet (SyncE).
- Time-sensitive network (TSN) support.
- In-band management.

Figure 1: Functional Block Diagram



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Chapter 1: Introduction

1.1 Features

The Broadcom BCM88280 is an optimized switching solution for 5G mobile backhaul, cell-site routing transport, and data center applications, enabling switching platforms with a mix of Ethernet, OTN, and FlexE ports.

The following features are available with the BCM88280:

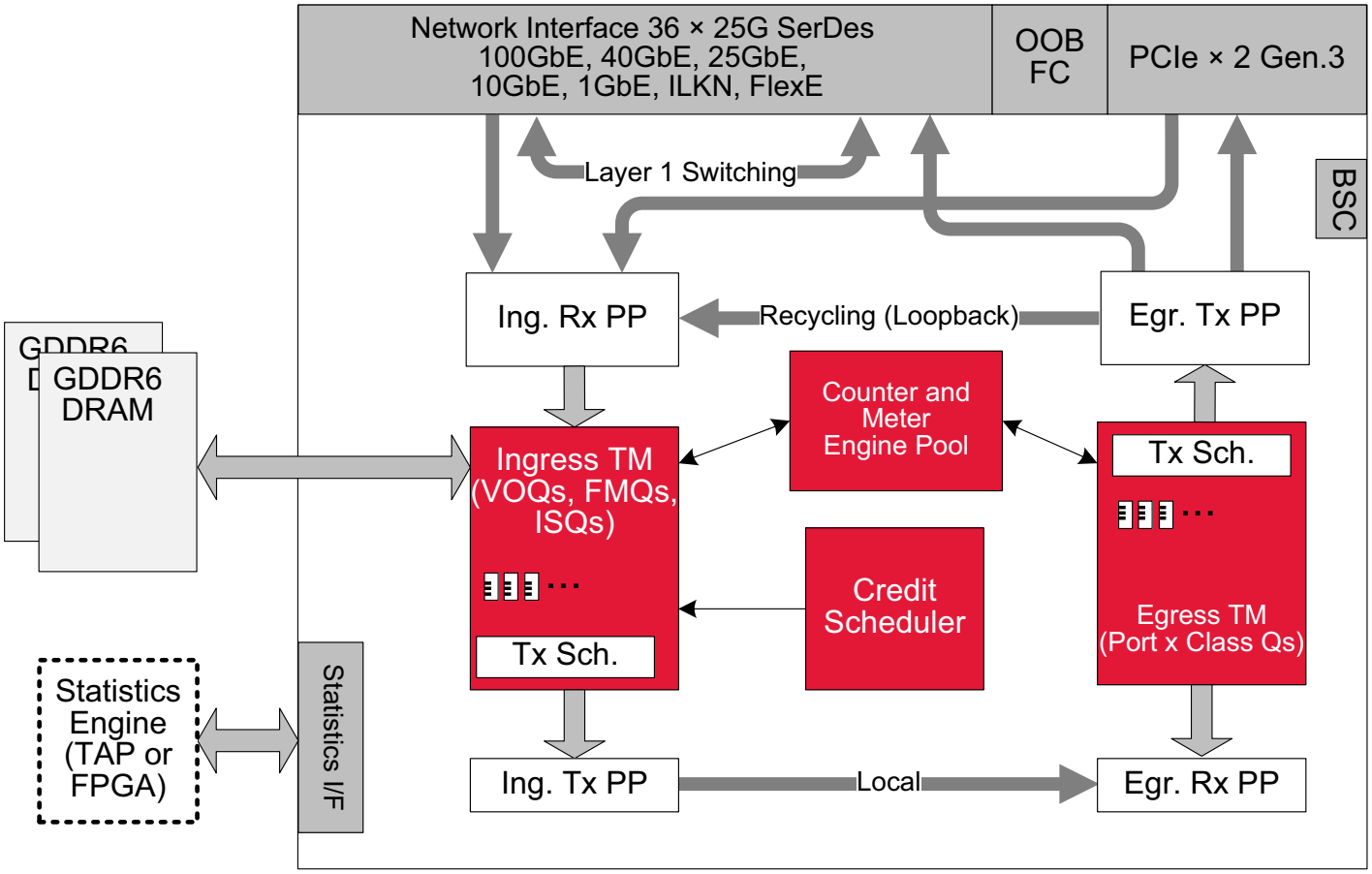
- High performance
  - 360 Gb/s full-duplex, integrated traffic manager, packet processor, and Layer 1 switching device.
  - 300 Mp/s processing rate
- Flexible network interface
  - 36 SerDes with rates up to 25.78125G, supporting the following port configurations:
    - 36 × 1GbE/10GbE/25GbE over one lane
    - 18 × 40GbE/50GbE over two lanes
    - 9 × 40GbE/100GbE over four lanes
  - Up to two Interlaken interfaces
- Flex Ethernet (FlexE)
  - Full support of the Optical Internetworking Forum (OIF) FlexE standard versions 1.x and 2.x
  - Up to 200 Gb/s of total FlexE traffic
  - Bonding of up to four PHYs in a group
  - Up to 40 FlexE clients, with client bandwidth granularity of 5 Gb/s
  - Sub-rating of Ethernet PHYs
  - Accurate time synchronization
  - Switching at Layer 2 through Layer 4 of FlexE and Ethernet traffic
- Packet lengths supported in the range 64B to 10240B
- Traffic Manager
  - 32K programmable wire-rate queues
  - Deep packet buffering using two external GDDR6 DRAM devices.
  - Congestion management
    - Hierarchical WRED and tail-drop policies
    - Congestion notification – CNM generation and CNM reception (proxy)
    - Flow control generation – Fully programmable, in-band and out-of-band
    - Flow control reception-any level – Interface, port, class, flow, traffic type (in-band and out-of-band)
    - Priority flow control (PFC) – Eight levels
    - Congestion tracking statistics
    - Three ingress meter operations per packet
    - Two egress meter operations per packet
  - Hierarchical scheduling and shaping
    - Fully programmable to any depth
    - Support for priority propagation
  - MEF, Broadband Forum TR-059-compliant scheduling and shaping

- Packet processor
  - Bridging, routing, MPLS, VPLS, L2VPNs, L3VPNs, and OAM
  - MPLS and IPv6 segment routing
  - Data center tunneling encapsulations including VXLAN, NV-GRE, and GENEVE
  - Built-in support for data center, carrier and metro Ethernet, and transport applications
  - Large modular on-chip databases, application-oriented with off-chip expandability
  - OAM accelerator engine
  - PEM (flexible pipe)
- Counters, meters, and statistics
  - On-chip counter pool up to 128K counters
  - On-chip meter pool up to 64K meters
  - Statistics interface for expandable, off-chip statistics gathering:
    - The SerDes used for the statistics interface is shared with network interface (NIF) SerDes
    - Efficient packet-based protocol based on Ethernet simplifies connectivity to KBP BCM16K, TAP BCM5235, or FPGAs
    - Seamless connection to KBP BCM16K and TAP BCM5235 devices
- Multicast – Pointer-based ingress and egress multicast replication
- IEEE 1588 support with improved time-stamping accuracy of nanosecond scale
- In-band management
- PCIe × two-lane Gen3 host interface with DMA
- Hardware linkscan engine
- LED processor

1.2 Device Overview

The following figure is a high-level functional block diagram of the BCM88280.

Figure 2: BCM88280 Block Diagram



As shown in Figure 2, the BCM88280 includes the following functional blocks.

Traffic Manager

- Ingress traffic manager (TM):
  - Manages a pool of queues in on-chip SRAM and in off-chip DRAM
  - Replicates packets for multicast, snooping, and mirroring
- Ingress and egress end-to-end credit scheduler – Schedules packets out of the ingress TM
- Egress traffic manager:
  - Manages a pool of egress queues in on-chip memory
  - Schedules traffic toward packet interfaces – Network, PCIe, internal hosts, and recycling (loopback)
  - Replicates multicast packets
- Counter and meter engine pool:
  - Features a general-purpose pool of counters and meters
  - Handles ingress and egress counting and metering
  - Includes configurable counting modes and criteria
  - Applied according to the packet processor command

Packet Processing

- Ingress receive packet processor:
  - Manages the main packet processing stage
  - Identifies incoming interface link layer, tunnel, PWE, and AC
  - Determines where to forward the packet based on packet forwarding header (L2, L3, MPLS, and so on)
  - Appends the packet processor (PP) header
- Ingress transmit packet processor:
  - Edits the packet (or packet copy) before transmitting to egress PP
- Egress receive packet processor:
  - Filters packets according to various criteria
- Egress transmit packet processor:
  - Edits packets according to PP header (from ingress)

Flex Ethernet (FlexE)

- Full support of the OIF FlexE standard versions 1.1 and 2.0
- Up to 200 Gb/s of total FlexE traffic
- Up to four FlexE groups
- Bonding of up to four PHYs in a group
- Up to 40 FlexE clients, with client bandwidth granularity of 5 Gb/s
- Bonding of Ethernet PHYs
- Sub-rating of Ethernet PHYs
- Accurate time synchronization
- Layer 1 switching between FlexE clients to FlexE clients
- Layer 1 switching between FlexE clients to Ethernet ports
- Switching at Layer 2 through Layer 4 of FlexE and Ethernet traffic

Interfaces

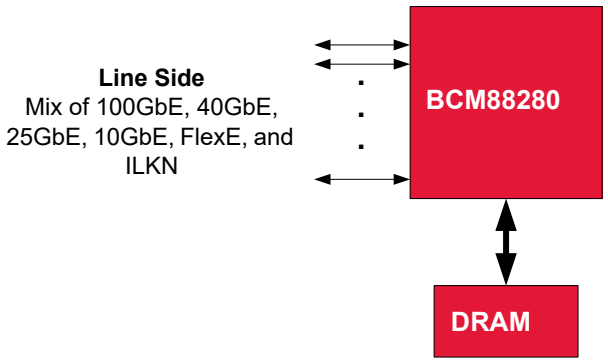
- Network interface:
  - 36 SerDes up to 25.78125 Gb/s
  - Port types supported include 1GbE, 10GbE, 25GbE, 40GbE, 50GbE, and 100GbE
  - Single Interlaken (ILKN) core, which can be configured to use two interfaces
- Statistics interface:
  - Sharing network interface SerDes
  - Use Ethernet ports, up to 100GbE per statistics interface
  - Generate statistics records over packets
- Out-of-band flow control (OOBFC):
  - Transmit and receive flow control
  - SPI 4.2 or ILKN protocol
- PCIe x2 lane Gen3 host interface:
  - Configuration and status register access
  - Packet transfer to and from host memory by using DMA
- Broadcom Serial Control (BSC, which is NXP I^2C-compatible) two-line interface:
  - Basic device debug and register access (PCIe debug)
  - PCIe quad serial peripheral interface (QSPI) flash programming
  - Loading code used for heating when an industrial device is powered-up at a low ambient temperature

Chapter 2: System Configurations

2.1 Stand-Alone or Centralized Switch

The BCM88280 may be used as a stand-alone or centralized switch device with ingress and egress intelligent TM. The integrated TM enables intelligent oversubscription with granular, per-flow (or per-customer-and-traffic-class) scheduling and shaping in the upstream direction, downstream direction, or both.

Figure 3: BCM88280 Switch with Integrated Traffic Manager



As shown in the preceding figure, the BCM88280 offers a flexible set of user interfaces, supporting a mix of 10GbE, 25GbE, 40GbE, 50GbE, and 100GbE Ethernet ports, FlexE, and ILKN interfaces.

Chapter 3: System Interfaces

3.1 Network Interface

The BCM88280 network interface (NIF) includes two PM50s, six PM25s, and one Interlaken (ILKN) core.

Ethernet Port Macros (PMs)

PM50:

- Two Ethernet port macros
- Each PM50 includes an octal SerDes (Blackhawk) supporting up to 25.78125G
- Each PM50 supports the following Ethernet configurations:
  - 2 × 100GbE ports over four lanes
  - 4 × 50GbE ports over two lanes
  - 4 × 40GbE ports over two lanes
  - 2 × 40GbE ports over four lanes
  - 8 × 25GbE ports over one lane
  - 8 × 12GbE ports over one lane
  - 8 × 10GbE ports over one lane

PM25:

- Six Ethernet port macros
- Each PM25 includes a quad SerDes (Falcon16) supporting up to 25.78125G
- Each PM25 supports the following Ethernet configurations:
  - 1 × 100GbE port over four lanes
  - 2 × 50GbE ports over two lanes
  - 2 × 40GbE ports over two lanes
  - 1 × 40GbE port over four lanes
  - 4 × 25GbE ports over one lane
  - 4 × 12GbE ports over one lane
  - 4 × 10GbE ports over one lane
  - 4 × 1GbE ports over one lane

FlexE Core

The BCM88280 supports a 200G FlexE core with the following capabilities:

- Up to 200G FlexE traffic.
- Up to four FlexE groups.
- Up to 40 clients. Client bandwidth can be from 5G to 200G.

Interlaken Cores

The BCM88280 contains a single Interlaken core, supporting 12 lanes that can be partitioned to two interfaces.

ILKN FEC is not supported in the BCM88280.

SerDes Interface Mapping

The following table describes the mapping of PMs and Interlaken cores to SerDes and provides the interface naming conventions.

NOTE: The information in the table applies to the device family in general. Each part number within the device family might support a different subset of options listed in the table.

NOTE: The BCM88280 uses the same package, pin names, and I/O definitions as the BCM88480.

Table 1: BCM88280 NIF SerDes Interface Mapping

PM	SRD Number	Availability	FlexE	STAT	ILKN Core	ILKN Interface
PM50_00	000 to 007	Per part number	+	—	0[a]	0 and 1
PM50_01	008 to 015	Per part number	Per part number	—	0	0 and 1
PM25_02	016 to 019	Available	—	—	—	—
PM25_03	020 to 023	Per part number	—	—	—	—
PM25_04	024 to 027	Available	—	—	—	—
PM25_05	028 to 031	N/A	—	—	—	—
PM25_06	032 to 035	Per part number	—	+	—	—
PM25_07	036 to 039	Per part number	—	+	—	—
PM25_08	040 to 043	Available	—	—	—	—
PM25_09	044 to 047	N/A	—	—	—	—
PM25_10	048 to 051	N/A	—	—	—	—

a. PM50_00 can support ILKN only over SerDes 4 to 7.

NOTE: The total limit of device bandwidth is 360 Gb/s.

3.1.1 Ethernet Ports

Ethernet ports are implemented by the Ethernet port macro (PM). The PMs include the MAC and PCS layers of Ethernet ports. The BCM88280 includes two types of port macros. PM50 is based on an octal SerDes block (Blackhawk). PM25 is based on a quad SerDes block (Falcon16).

The following table depicts the Ethernet port modes supported by PM50 and PM25.

NOTE: BASE-R FEC indicates IEEE 802.3, Clause 74-compliant FEC.

Table 2: Supported Port Modes

Port Speed	No. of Lanes	PM Type	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
100GbE	4	PM50 and PM25	CAUI-4 C2C	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Annex 83D
			CAUI-4 C2M	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Annex 83E
			100GBASE-KR4	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Clause 93
			100GBASE-CR4	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3 Clause 92
		PM50 only	100GAUI-4 C2C	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135D
			100GAUI-4 C2M	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135E
50GbE	2	PM50 and PM25	Consortium 50G C2C	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GE with C2C interface as defined in IEEE 802.3 Annex 83D
			Consortium 50G C2M	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GE with C2M interface as defined in IEEE 802.3 Annex 83E
			LAUI-2 C2C	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3cd Annex 135B
			LAUI-2 C2M	25.78125	25.78125	NRZ	RS-528, no FEC	IEEE 802.3cd Annex 135C
			Consortium 50G KR2	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GbE with KR interface as defined in IEEE 802.3 Clause 93
			Consortium 50G CR2	25.78125	25.78125	NRZ	RS-528, no FEC	Consortium 50GbE with CR interface as defined in IEEE 802.3 Clause 92
		PM50 only	50GAUI-2 C2C	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135D
			50GAUI-2 C2M	26.5625	26.5625	NRZ	RS-544	IEEE 802.3cd Annex 135E

Table 2: Supported Port Modes (Continued)

Port Speed	No. of Lanes	PM Type	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
40GbE	2	PM50 and PM25	XLAUI-2 KR	20.625	20.625	NRZ	No FEC	XLAUI-4, bit-muxed to two lanes, with KR interface as defined in 802.3 Clause 93 (masks scaled to 20.625G)
			XLAUI-2 CR	20.625	20.625	NRZ	No FEC	XLAUI-4, bit-muxed to two lanes, with CR interface as defined in IEEE 802.3 Clause 92 (masks scaled to 20.625G)
			XLAUI-2 C2C	20.625	20.625	NRZ	No FEC	XLAUI-4, bit-muxed to two lanes, with C2C interface as defined in IEEE 802.3 Annex 83D (masks scaled to 20.625G)
			XLAUI-2 C2M	20.625	20.625	NRZ	No FEC	XLAUI-4, bit-muxed to two lanes, with C2M interface as defined in IEEE 802.3 Annex 83E (masks scaled to 20.625G)
40GbE	4	PM50 and PM25	XLAUI	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Annex 83A
			40GBASE-KR4	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Clause 84
			40GBASE-CR4	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Clause 85
			XLPPI	10.3125	20.625	NRZ	BASE-R, no FEC	IEEE 802.3 Annex 86A
25GbE	1	PM50 and PM25	25GAUI C2C	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Annex 109A
			25GAUI C2M	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Annex 109B
			25GBASE-KR/25GBASE-KR-S	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Clause 111
			25GBASE-CR/ 25GBASE-CR-S	25.78125	25.78125	NRZ	RS-528, BASE-R, no FEC	IEEE 802.3 Clause 110
12GbE	1	PM50 and PM25	XFI (Scaled)	12.5	25	NRZ	No FEC	XFI+ (FC-PI-3), scaled to 12.5G

Table 2: Supported Port Modes (Continued)

Port Speed	No. of Lanes	PM Type	Port Mode	SerDes Rate (Gb/s)	VCO Rate (GHz)	SerDes Mode	FEC	Related Standard
10GbE	1	PM50 and PM25	10GBASE-KR	10.3125	PM50: 20.625 PM25: 25.78125	NRZ	BASE-R, no FEC	IEEE 802.3 Clause 72
			XFI	10.3125	PM50: 20.625 PM25: 25.78125	NRZ	BASE-R, no FEC	XFI+ (FC-PI-3)
			SFI	10.3125	PM50: 20.625 PM25: 25.78125	NRZ	BASE-R, no FEC	SFF-8431
			Direct Attached Cable (DAC)	10.3125	PM50: 20.625 PM25: 25.78125	NRZ	BASE-R, no FEC	—
1GbE	1	PM25 only	1000BASE-X, SGMII (1GbE only)	1.25	25.78125	NRZ	No FEC	—

3.1.1.1 100GbE Port

3.1.1.1.1 100GbE over Four Lanes

The BCM88280 device supports standard 100GbE according to IEEE 802.3. This port type is supported on both PM50 and PM25.

The 100GbE port supports the following interfaces:

- CAUI-4 (chip-to-chip IEEE 802.3 Annex 83D and chip-to-module IEEE 802.3 Annex 83E)
- 100GBASE-KR4 (IEEE 802.3 Clause 93)
- 100GBASE-CR4 (IEEE 802.3 Clause 92)
- 100GAUI-4 (chip-to-chip IEEE 802.3cd Annex 135D and chip-to-module IEEE 802.3cd Annex 135E)

When using the 100GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant with IEEE 802.3 Clause 91, both RS(528,514) and RS(544,514).

3.1.1.2 50GbE Port

3.1.1.2.1 50GbE over Two Lanes

The BCM88280 supports 50GbE according to IEEE 802.3cd and the 25G/50G Ethernet consortium. This port type is supported on both PM50 and PM25.

The 50GbE port supports the following interfaces:

- 50GbE over two lanes according to the 25G/50G Ethernet consortium
- LAUI-2 (chip-to-chip IEEE 802.3cd Annex 135B and chip-to-module IEEE 802.3cd Annex 135C)
- 50GBASE-KR2 (this is Ethernet consortium 50GbE with a KR interface as defined in IEEE 802.3 Clause 93)
- 50GBASE-CR2 (this is Ethernet consortium 50GbE with a CR interface as defined in IEEE 802.3 Clause 92)
- 50GAUI-2 (chip-to-chip IEEE 802.3cd Annex 135D and chip-to-module IEEE 802.3cd Annex 135E)

When using the 50GbE port, an optional Reed-Solomon FEC is supported. This FEC is compliant with IEEE 802.3 Clause 134, RS(544,514), or Clause 91, RS(528,514). PM25 supports only Clause 91, RS(528,514).

3.1.1.3 40GbE Port

3.1.1.3.1 40GbE over Two Lanes

The BCM88280 supports standard 40GbE according to IEEE 802.3. This port type is supported on both PM50 and PM25.

The 40GbE ports support the following interfaces:

- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a KR interface as defined in IEEE 802.3 Clause 93 (masks scaled to 20.625G).
- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a CR interface as defined in IEEE 802.3 Clause 92 (masks scaled to 20.625G).
- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a chip-to-chip interface as defined in IEEE 802.3 Annex 83D (masks scaled to 20.625G).
- XLAUI-2 – This is XLAUI-4, bit-muxed to two lanes, with a chip-to-module interface as defined in IEEE 802.3 Annex 83E (masks scaled to 20.625G).

No FEC is supported for the 40GbE port over two lanes.

3.1.1.3.2 40GbE over Four Lanes

The BCM88280 supports standard 40GbE according to IEEE 802.3. This port type is supported on both PM50 and PM25.

The 40GbE ports support the following interfaces:

- XLAUI (IEEE 802.3 Annex 83A)
- 40GBASE-KR4 (IEEE 802.3 Clause 84)
- 40GBASE-CR4 (IEEE 802.3 Clause 85)
- XLPPI (IEEE 802.3 Annex 86A)

When using the 40GbE port in four-lane mode, an optional FEC is supported. The FEC is compliant with IEEE 802.3 Clause 74.

3.1.1.4 25GbE Port

The BCM88280 supports 25GbE according to IEEE 802.3, and the 25G/50G Ethernet consortium. This port type is supported on both PM50 and PM25.

The 25GbE ports support the following interfaces:

- 25GAUI (chip-to-chip IEEE 802.3 Annex 109A and chip-to-module IEEE 802.3 Annex 109B)
- 25GBASE-KR/25GBASE-KR-S (IEEE 802.3 Clause 111)
- 25GBASE-CR/25GBASE-CR-S (IEEE 802.3 Clause 110)

When using the 25GbE port, an optional FEC is supported. The FEC can be either IEEE 802.3 Clause 108, RS(528,514) or IEEE 802.3 Clause 74 FEC.

3.1.1.5 12GbE Port

The BCM88280 supports 12GbE. The 12GbE port is similar to the 10GbE port, with a SerDes rate of 12.5G (scaled up from 10.3125G). This port type is supported on both PM50 and PM25.

The 12GbE port supports XFI+ (FC-PI-3), and the SerDes rate is scaled up to 12.5G from 10.3125G.

The 12GbE port does not support FEC.

3.1.1.6 10GbE Port

The BCM88280 supports 10GbE according to IEEE 802.3. This port type is supported on both PM50 and PM25.

The 10GbE ports support the following interfaces:

- XFI or SFI for direct connect to optical module[1]
- 10GBASE-KR (IEEE 802.3 Clause 72)
- Direct-attached cable (DAC)

When using the 10GbE port with the KR interface, an optional FEC is supported. The FEC is compliant with IEEE 802.3 Clause 74.

3.1.1.7 1GbE Port

The BCM88280 supports 1GbE over an SGMII or a 1000BASE-X interface.

- The GbE port is supported over the PM25 port macro only.
- The GbE port supports 1GbE only (no support for 10-Mb/s and 100-Mb/s speeds).
- The GbE port does not support auto-negotiation.
- The GbE port does not support clock recovery for SyncE.
- Half-duplex mode is not supported.
- No support is available for a 2.5GbE port.

1. Supported: SR (limiting), LR (limiting), ER (limiting).
   Not supported: ZR (limiting), ZR (linear), LRM (linear), DWDM (linear).

3.1.1.8 Mixed Port Types on PM50

Different port types can be supported on the same Blackhawk port macro (PM50). Mixing port types is allowed when all ports in the same PM50 are derived from one or two PLL rates. The following table defines the PLL (VCO) combinations and available ETH ports on each combination.

NOTE: For Ethernet ports, TVCO (PLL1) and OCVO (PLL0) do not have the same functionality. (See Section 3.1.1.8.1, PM50 Mixed Port-Type Limitations.)

NOTE: When FlexE is used, PM50 TVCO must be configured to 26.5625G.

Table 3: PM50 PLL VCO Combinations and Supported Port Types

			TVCO	25.78125G	25.78125G	25.78125G	26.5625G	26.5625G	26.5625G
			OVCO	20.625G	25.000G	26.5625G	20.625G	25.000G	25.78125G
VCO Rate (Gb/s)	**Port BW**	**Lanes**	**SRD Rate**						
26.5625	100GbE	4	26.5625			+	+	+	+
26.5625	50GbE	2	26.5625			+	+	+	+
25.78125	100GbE	4	25.78125	+	+	+			+
25.78125	50GbE	2	25.78125	+	+	+			+
25.78125	25GbE	1	25.78125	+	+	+			+
25.000	12.5GbE[a]	1	12.5000		+			+	
20.6250	40GbE	2	20.6250	+			+		
20.6250	40GbE	4	10.3125	+			+		
20.6250	10GbE	1	10.3125	+			+		

a. 12.5GbE data bandwidth is 12.12G. This is a non-standard ETH rate.

3.1.1.8.1 PM50 Mixed Port-Type Limitations

The main limitations of the PM50 are as follows:

- Up to eight lanes can be supported.
- Up to two VCO rates can be supported. An ETH application on PM50 requires a TVCO rate of 25.78125G or 26.5625G. This requirement prevents using a combination of 20.625G and 25.0000G PLL rates if ETH is used.
- Any modification of TVCO causes ETH ports based on OVCO to be reset as well.
- When FlexE is used, TVCO is set to 26.5625G.

3.1.1.8.2 Software Sequence and Rules for Port Allocation

This section describes the software sequence and rules for port allocation. The goal is to provide a better understanding of the device options. For more information and updates regarding PMx50 mixed ports, refer to the *BCM88690 Traffic Manager Programming Guide* (88690-PG2xx).

Ports can be allocated to the PM8x50 by a single port assignment or by a multi-port assignment using the following APIs:

- `bcm_port_resource_set()`
- `bcm_port_resource_multi_set()`

Ports are allocated only if the new configuration meets the TVCO and OVCO combinations in Table 3 and the following software limitations are met.

For the initial allocation (there are no active ports on the PM), VCO rates are defined according to the following table.

Table 4: Initialization Options Table

Requested PLL Rate	Port Requirement for PM50 Initialization	TVCO	OVCO
Initialization with One Rate			
20.625G	At least one ETH port	25.78125G[a]	20.625G
20.625G	ILKN only (no ETH)	Shut-down	20.625G
25.000G	At least one ETH port	25.78125G[a]	25.000G
25.000G	ILKN only (no ETH)	Shut-down	25.000G
25.78125G	No restrictions	25.78125G	Shut-down
26.5625G	No restrictions	26.5625G	Shut-down
Initialization with Two Rates			
25.000G + 20.625G[b]	ILKN only (no ETH)	20.625G	25.000G
25.78125G + 20.625G	No restrictions	25.78125G	20.625G
25.78125G + 25.000G	No restrictions	25.78125G	25.000G
26.5625G + 20.625G	No restrictions	26.5625G	20.625G
26.5625G + 25.000G	No restrictions	26.5625G	25.000G
26.5625G + 25.78125G	No restrictions	26.5625G	25.78125G

a. The default rate is 25.78125G for the dynamic addition of 25.78125G ports. A software flag can configure the TVCO to 26.5625G if that rate is expected.

b. This combination cannot work with ETH. It works only with ILKN.

For an allocation update (there are active ports on the PM), the following information applies:

- If all ports in the PM are included in the update command, the SW treats the update as if this is the initial allocation.
- If only some of the PM ports are included in the update command, the SW tries to perform the PLL update without impacting used resources.
- To update TVCO, all ETH ports using TVCO and OVCO, as well as all ILKN ports using TVCO, should be included in the update command. All of these ports will go through the port-down and port-up sequence. (Only ILKN ports using OVCO are not affected.)
- To update OVCO, all ETH ports using OVCO and all ILKN ports using OVCO should be included in the update command. All of these ports will go through the port-down and port-up sequence. (Ports using TVCO are not affected.)

3.1.1.8.3 PM50 Mixed Port Type Allocation Restrictions

The scenarios in this section show examples of configuration restrictions.

Scenario 1

If a PM is configured using a 40GbE port (four lanes, VCO = 20.6250G) and a 50GbE port (two lanes, VCO = 25.78125G), a dynamic configuration adding a 100GbE port (four lanes, VCO = 25.78125G) results in an error indication because more than eight lanes are required.

Scenario 2

If a PM is configured using a 40GbE port (four lanes, VCO = 20.6250G) and a 50GbE port (two lanes, VCO = 26.5625G), a dynamic configuration that adds a 50GbE port (two lanes, VCO = 25.78125G) results in an error indication because three VCO rates are required.

3.1.1.9 Mixed Port Types on PM25

The 25GbE (25.78125G), 10GbE (10.3125G), and 1GbE (1.25G) port types can coexist simultaneously on the same PM25. Any combination of other rates is not allowed.

For example, when using 12GbE (12.5G), other rates can not be used on the same PM25.

3.1.2 FlexE

The BCM88280 includes a FlexE core with the following features:

- Full support of the OIF FlexE standard versions 1.1 and 2.0.
- Up to 200 Gb/s of total FlexE traffic.
- Up to four FlexE groups.
- 50G, 100G, and 200G PHY rates. 26.5625G and 25.78125G SerDes rates.
- Bonding of up to four PHYs in a group.
- Up to 40 FlexE clients, with client bandwidth granularity of 5 Gb/s.
- Dynamic configuration of adding and removing FlexE groups and clients.
- Insertion and extraction of FlexE overhead.
- IEEE1588 over FlexE overhead.
- OAM insertion, extraction, and monitoring.
- 1+1 and 1:1 protection.
- Bonding of Ethernet PHYs.
- Sub-rating of Ethernet PHYs.
- Accurate time synchronization.
- Layer 1 switching between FlexE clients to FlexE clients.
- Layer 1 switching between FlexE clients to Ethernet ports.
- Switching at Layer 2 through Layer 4 of FlexE and Ethernet traffic.

The BCM88280 FlexE core shares SerDes with PM50-0 and PM50-1. Depending on the device part-number, up to eight SerDes from either PM50-0 or PM50-1 can be used for FlexE.

For more information about BCM88280 support for FlexE, refer to the application note, *FlexE Interface* (88480-AN2xx).

NOTE: When FlexE is used, the TVCO of the PM50 that is used must be configured to 26.5625G.

3.1.3 Interlaken

The BCM88280 has one Interlaken core.

The BCM88280 Interlaken core supports SerDes rates of up to 25.78125G. For the defined ILKN rates, see Section 3.1.3.1, Interlaken SerDes Supported Rates and Electrical Standards.

The ILKN core has 12 lanes and can support two interfaces (ILKN_0 and ILKN_1). The ILKN core shares SerDes with PM50-0 (lanes 4 to 7) and PM50-1.

When FlexE is used, ILKN_0 and ILKN_1 cannot be used for data.

For information about PM assignment to ILKN cores, see Table 1. When making assignments, use the following guidelines:

- If the RX (or TX) of a specific physical SerDes is used for ILKN, the TX (or RX) of the same SerDes should go to the same ILKN interface.
- For a logical ILKN lane, RX SerDes and TX SerDes should be on the same PM.

3.1.3.1 Interlaken SerDes Supported Rates and Electrical Standards

The ILKN interface is targeted to comply with the electrical specifications of the standards as listed in the following table.

Table 5: ILKN Supported Rates and Electrical Specifications Standards

SerDes Rate (Gb/s)	SerDes Mode	Standard Electrical Specifications
25.78125	NRZ	25GBASE-KR-S IEEE 802.3 Clause 111
		CAUI-4 C2C: IEEE 802.3 Annex 83D
		CAUI-4 C2M: IEEE 802.3 Annex 83E
25.0	NRZ	25GBASE-KR-S IEEE 802.3 Clause 111[a]
		CAUI-4 C2C: IEEE 802.3 Annex 83D[a]
12.5	NRZ	10G XFI: XFI+ (FC-PI-3)[a]
10.3125	NRZ	10GBASE-KR IEEE 802.3 Clause 72
		10G XFI: XFI+ (FC-PI-3)

a. Scaled to the appropriate rate.

3.1.3.2 Interlaken Receive Burst Rules

Packets are transmitted across the Interlaken interface in bursts. The BCM88280 requires that burst sizes and burst intervals (Interlaken BurstShort) conform to certain rules.

The BCM88280 Interlaken receive supports both burst interleaving and full packet mode. If the peer device is configured to burst interleaving, assign a separate ingress reassembly context for each active channel.

Receive (into the BCM88280) burst interleaving rules are as follows:

- Supported BurstMax size is 256B.
- Start-of-packet (SOP) bursts should be 192B or larger.
- Bursts that are not end-of-packet (EOP) bursts may be either 128B, 192B, or 256B.
- EOP bursts may be any size (up to the configured BurstMax).
- BurstShort (the minimum interval between burst control words) should be at least 96B.

3.1.3.3 Interlaken Transmit Burst Rules

When the StrataDNX™ TM is operational (stand-alone or central switch mode), the BCM88280 ILKN TX supports only full-packet mode (burst-interleaving occurs only when TDM packets preempt data packets).

When transmitting across an Interlaken interface, the BCM88280 supports configurations consistent with the following:

- BurstShort (minimum interval between burst control words):
  - Configuration is from 96B to 256B in increments of 32B.
- BurstMax options:
  - BurstMax = 256B, normal scheduling:
    - Non-EOP bursts are 256B.
    - EOP burst can be from 1B to 256B.
  - BurstMax = 256B, enhanced scheduling (not supported in FlexE adapter mode):
    - Configurable BurstMin of 64B or 128B.
    - Non-EOP bursts are 256B.
    - Penultimate burst when BurstMin is 128B: 128B or 256B.
    - Penultimate burst when BurstMin is 64B: 192B or 256B.
    - EOP bursts are from 64B to 256B.

3.1.3.4 Interlaken In-Band Flow Control

Each Interlaken interface supports in-band flow control according to the Interlaken protocol definition.

The flow-control (FC) information is carried over the control words sent across the interface. Each control word includes a 16-bit flow-control field and a reset calendar bit. Each flow-control bit indicates the flow-control status (ON/OFF) of a specific Interlaken calendar channel. The BCM88280 supports a configurable calendar length between 16 to 256 channels (16, 32, 64, 128, and 256).

The BCM88280 supports two options for link level flow control (LLFC) mapping:

- Map the LLFC to flow control calendar channel #0.
- Map the LLFC to the first flow-control calendar channel in every control word (that is, entries 0, 16, 32, and so on). This option is useful for faster reaction times for LLFC, at the expense of flow-control channels.

The BCM88280 is flexible in flow-control processing, and each calendar entry can be mapped to one of the following flow-control reaction points:

- Link level (mapped to Interlaken NIF port)
- Channel level (mapped to OTM port)
- Egress queue pair level

Flow-control generation (flow-control transmission) – The BCM88280 can assign each calendar entry with flow control information or indications that may represent the following:

- Status of Interlaken port receive buffer (useful for link level).
- Status of the global resources (in other words, DRAM buffers).
- Status of a virtual-statistics queue – May be programmed to generate flow control per Interlaken channel but enables more fine-grain flow-control indications; for example, per port and traffic class, per flow, and so on.

3.1.4 Bandwidth Provisioning of the Network Interface

The NIF of the BCM88280 allows flexible and oversubscribed connectivity that exceeds the switching capacity of the device.

When provisioning the device NIF ports, use the following calculations to avoid misconfiguration and unpredictable packet loss. In the equations, *INT* is the reserved bandwidth for internal ports (such as recycling, CPU, and so on), and *L1* is L1 switching between any FlexE group client and any Ethernet or ILKN interface.

NOTE: L1 switching between a FlexE group client and other FlexE group clients has no impact on the NIF provisioning and is not considered in this calculation.

The maximum bandwidth provisioned to NIF ports (Ethernet, FlexE, and Interlaken), is calculated by the following equation:

Maximum provisioned NIF bandwidth = 900 Gb/s – INT – (3 × L1)

For example, with FlexE active, 30 Gb/s reserved for internal ports, and 50-Gb/s L1 switching, the maximum bandwidth provisioned for NIF (ETH, ILKN, and L2 FlexE) is 720 Gb/s.

720 Gb/s = 900G – 30G – (3 × 50G)

3.2 Out-of-Band Flow Control

The BCM88280 supports out-of-band flow control (OOBFC) from the user to the BCM88280 (egress flow control or reception) and from the BCM88280 to the user (ingress flow control or generation).

The BCM88280 has two independent bidirectional OOBFC interfaces. Each interface can work in SPI-4.2 mode or Interlaken mode.

In all modes, the OOBFC interface supports the following:

- Reception – Each calendar entry is mapped to a flow-control reaction point that is either:
  - Link-level (NIF port)
  - Channel-level (OTM port)
  - Priority-level (egress queue pair)
- Generation (flow-control transmission) – Each calendar entry represents a flow-control generation point that is either:
  - Status of a virtual-statistics queue
  - Status of the global resources, in other words, DRAM buffers
  - Status of the port (MAC) receive buffer (link level)
- XON/XOFF signaling (no concept of credits, such as SPI-4.2)

In SPI-4.2 mode, the OOBFC interface has the following characteristics:

- SPI-4.2 status channel-like framing
- Calendar length of up to 512 entries
- Three-wire signaling for each direction – Two data and one clock to support the following XON/XOFF indications:
  - On TX STARVING = XON and SATISFIED = XOFF
  - On RX XON = (HUNGRY or STARVING) and XOFF = SATISFIED
- SDR operation for data signals
- Transmission clock rate – Core frequency divided by 6, 8, 10, 12, 14, or 16 (maximum rate is 166 MHz)
- Reception clock rate – DC to 200 MHz

In Interlaken mode, the OOBFC interface has the following characteristics:

- Interlaken protocol
- Calendar length of up to 512 entries
- Reception and generation of Interlaken retransmit requests
- Three-wire signaling for each direction – One each for clock, data, and sync
- 4b CRC protection
- DDR operation for data and sync signals
- Transmission clock rate – Core frequency divided by 6, 8, 10, 12, 14, or 16 (maximum rate is 166 MHz)
- Reception clock rate – Up to 180 MHz

NOTE: In-band and out-of-band flow-control signaling may be used simultaneously.

3.3 Synchronous Ethernet

The BCM88280 supports Synchronous Ethernet (SyncE) applications. The support includes two functions: controlling the transmit clock of network ports, and recovering a clock from a network port.

3.3.1 Transmit Clock

The transmit clock of each SerDes is locked to one of the NIF_[3:0]_REFCLK_P/N input reference clocks (for mapping information, see the NIF_[3:0]_REFCLK_P/N description in Section 4.3, Pin Description – Grouped by Function).

By connecting the system transmit clock to the NIF_[3:0]_REFCLK_P/N inputs, it is possible to control the transmit clock of the SerDes.

3.3.2 Recovered Clock

The BCM88280 provides up to two recovered clocks that may be used as reference clocks for an external synchronization unit. The source for the recovered clocks can be any of the NIF SerDes configured as an Ethernet port. The BCM88280 drives two recovered clocks (SYNCE[1:0]_CLK_OUT) and a valid indication per clock (SYNCE[1:0]_CLK_OUT_VALID).

NOTE: Support for clock recovery is as follows:

- Clock recovery is supported for a NIF interface configured as an Ethernet port or FlexE interface.
- Clock recovery is not supported for a 1G Ethernet interface.

The valid indication is asserted when the recovered clock is synchronized to the selected SerDes RX signal and can be used for system synchronization. The valid indication is based on a PCS lock and a link-up indication.

Each of the recovered clocks works as either a normal clock or a squelched clock. In normal clock mode, the CLK_OUT is the recovered clock of the selected SerDes. In squelched mode, the CLK_OUT halts if the RX of the selected link is not synced.

For multilane ports (for example, 40GbE or 100GbE), the recovered clock is derived from the first SerDes of the relevant port, and the valid signal is according to the linkup status of the entire port.

The recovered clock frequency is 25 MHz.

A fractional divider is used for generating an average clock of 25 MHz.

The following example describes how the average output frequency of 25 MHz is generated for a 100GbE port (4 × 25.78125 Gb/s).

The 25.78125 GHz is divided by 40, and the fractional divider, over 32 clock cycles, uses 7 clock cycles of a 25 divider [(25.78125 ÷ 40) ÷ 25] and 25 clock cycles of a 26 divider [(25.78125 ÷ 40) ÷ 26], as shown in the following equation.

$$\frac{25.78125\ \text{GHz}}{40} \div \frac{(7 \times 25) + (25 \times 26)}{32} = 25\ \text{MHz}$$

Similarly:

- A fractional divider of 26.5625 GHz uses 14 clock cycles of a 26 divider and 18 clock cycles of a 27 divider.
- A fractional divider of 20.625 GHz uses 12 clock cycles of a 20 divider and 20 clock cycles of a 21 divider.

NOTE: An external jitter attenuator is required to clean the recovered clock before using it as a reference for the rest of the system.

3.4 IEEE 1588

The BCM88280 is a highly integrated device with many hardware hooks for designs that require network time synchronization with improved time-stamping accuracy on a nanosecond scale. The following features make the device ideally suited for time synchronization applications that comply with IEEE 1588.

- Supported modes:
  - E2E and P2P transparent clock (TC).
  - Boundary clock (BC).
  - TC + OC timeReceiver, BC + OC timeReceiver.
- One-step clock features:
  - On-the-fly egress packet modification including UDP checksum update and CRC update.
  - All modifications to the correction field are handled in hardware.
  - Very short residence time.
  - All packets timestamped on ingress.
  - Switch-packet processing engines identify IEEE 1588 packets.
- Two-step features:
  - Egress timestamps are stored in per-port FIFO, along with IEEE 1588 sequence number.
  - The CPU indicates which packets should generate a timestamp on egress.
  - All packets are timestamped on ingress.
  - Uses switch packet processing engines to identify IEEE 1588 packets and trap to CPU.
- Synchronizable timestamp counter:
  - Can be phase-locked to external source.
  - BroadSync® (timecode + event clock) interface.
  - Broadcom PHY sync interface.
  - Timestamped GPIOs.
- Frequency synthesizer:
  - Additional clock divider: 10 MHz + 1 p/s.
  - Low jitter.

NOTE: PTP/IEEE 1588 functionality is supported over Ethernet ports only. Timestamping is not supported over Interlaken interfaces.

NOTE: For information about PTP/IEEE 1588 over FlexE, refer to the *BCM88480 FlexE Overhead, OAM, and IEEE 1588 Handling* (88480-AN3xx).

3.4.1 BroadSync External Interfaces

The BroadSync block provides the following external interfaces for providing timing information to off-chip devices or for retrieving timing information from external devices:

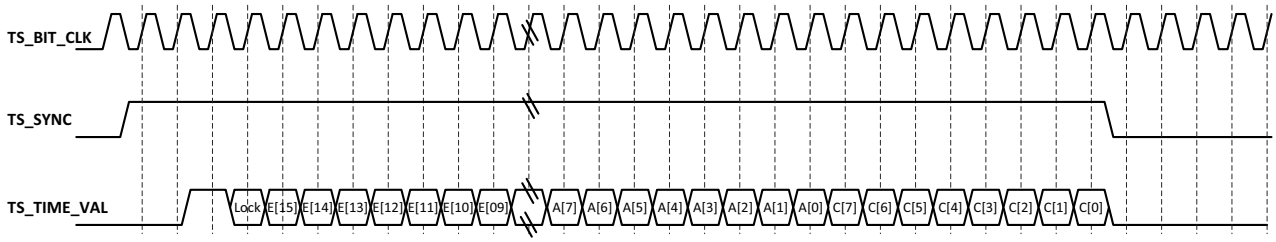
- Reference clock (input)
- External Sync 1 (input or output)
- External Sync 2 (input or output)
- Three-pin BroadSync interface (input or output):
  - TS_BIT_CLK
  - TS_SYNC
  - TS_TIME_VAL

The reference clock input is used for the clocking of all of the logic in the BroadSync block. The BroadSync block operates on a separate clock domain than the rest of the switch logic. The reference clock input should be driven from a low-jitter source to ensure that all time-related functions are accurate.

The External Sync 1 and 2 signals can be used as either inputs or outputs. When the signals are being used as inputs, a rising edge on the signal can be used to sample the current value of the internal timer, which can then be retrieved by the CPU. When these signals are used as outputs, the signal can be programmed to toggle based on a configurable interval.

The BroadSync interface is configured through the CMIC_BS_CONFIG register and is composed of three signals: the clock, the heartbeat, and the time code. The BroadSync interface can be configured to operate as either a timeTransmitter (output) or timeReceiver (input). The interface clocks out or takes in serial data as shown in the following figure.

Figure 4: BroadSync Interface I/O



When the BroadSync interface is operating in timeReceiver mode, an external device is used to clock a time code into the BCM88280. External hardware provides the TS_BIT_CLK, TS_SYNC, and TS_TIME_VAL signals. During each heartbeat period, the external hardware shifts in a time code value, which consists of the following:

- Start bit
- Lock bit
- 16-bit epoch
- 32-bit seconds
- 2-bit zero
- 30-bit nanoseconds
- 8-bit accuracy
- CRC8 (covers all bits from LOCK to ACCURACY[0])

The time value shifted in corresponds to the time of the most recent rising edge of the heartbeat signal. All of the bits clocked in from the time code are stored in the CMIC_BS_INPUT_TIME[0:2] registers. Additionally, the received CRC8 is compared against the computed CRC8, and the result of the comparison is present in the CHECKSUM_ERROR field in the CMIC_BS_INPUT_TIME_2 register.

The internal time value is calibrated to the external signals through the following process:

1. The rising edge of TS_SYNC is used to sample the device's internal free-running clock value.
2. The sampled free-running clock value is compared to the time value subsequently shifted in using the TS_TIME_VAL signal.
3. These pairs of values (shifted-in time and sampled free-running time) are provided to the CPU on an occasional basis.
4. The differences and rates of change of the differences of the two time bases are used to derive a drift value.
5. The computed drift value is used to correct the internal time counter.

When the BroadSync interface is operating in timeTransmitter mode, the interface drives a time code to external devices. How frequently a new time code is clocked out depends on how often the heartbeat signal goes high. The heartbeat signal toggling frequency can be configured through the CMIC_BS_HEARTBEAT_CTRL register. When the heartbeat goes high, the contents of the CMIC_BS_OUTPUT_TIME memory is clocked out. The BCM88280 automatically computes and appends the correct CRC8 value immediately after the 8-bit accuracy field is clocked out. The TS_BIT_CLK used to clock out the time code is synthesized from the BroadSync Clock domain.

The BCM88280 can optionally synthesize the TS_BIT_CLK from a highly accurate internal PLL. The PLL generates an extremely low-jitter clock that is ITU-T G.824 and ITU-T G.823 compliant.

3.5 Statistics Interface

The statistics interface is an event-driven interface through which statistics are pushed out. Statistics records are continuously reported at a maximum rate of one record per clock in ingress and egress, for a maximum rate of two records per clock. The BCM88280 supports one of the following global configurable options:

- Queue-Size – The statistics interface reports the queue size of ingress enqueue actions and ingress dequeue actions. This mode can be used to build an image of queue sizes, infer congestion, and enable congestion management by an ingress PP.
- Billing – The statistics interface reports ingress received packets and egress transmitted packets. Packets are tagged with information that maps into counters at the external statistic processing device.
- Ingress-Enqueue/Dequeue – In this mode, the statistics interface reports per each ingress packet enqueued and dequeued. Packets are tagged with information that map into counters at the external statistic processing device.

The statistics interface has two modes:

- Single mode – The statistics interface is a single port up to 100GbE. Each packet contains records from ingress and egress. This mode allows different record sizes for the ingress and the egress. Thus, it is possible to mix larger ingress records with shorter egress records without compromising the rate of the statistics interface.
- Dual mode – The statistics interface is made of two ports, each up to 100GbE. Each interface caters to the ingress or egress. In this mode, mixing larger ingress record with shorter egress records would compromise the statistics interface bandwidth.

The external statistics processor can be Broadcom KBP or TAP devices, or a custom FPGA. When connecting to the Broadcom KBP or TAP as an external statistics processor, the statistics interface should be configured to single mode.

The BCM88280 statistics interface can use NIF ports from PM25-6 or PM25-7 (SerDes 32 to 39), as described in Table 1.

NOTE: Only the TX direction of the Ethernet port is used for the statistics interface. The RX direction is unused in this case. However, if the link partner (KBP or FPGA) can spare the TX SerDes, connect these lines to the BCM88280 RX to facilitate system debugging.

An Ethernet-like MAC is used to send statistics packets with the following characteristics:

- Standard Ethernet 8-byte preamble.
- 32b FCS, which is the same as standard Ethernet.
- Average interpacket gap (IPG) of 12B.

3.6 External DRAM Packet Buffer

The BCM88280 uses off-chip DRAM to queue packets.

There are two GDDR6 interfaces, and each interface has two 16b-wide channels.

The BCM88280 GDDR6 controller supports a data rate of 6.8G (per DQ pin).

To meet application requirements, the BCM88280 can operate with two external DRAM devices, one external DRAM device, or no external DRAM. Additional DRAM usage guidelines are as follows:

- When using a single DRAM, use DDR0.
- Each DDR interface can support up to 8 Gb of the GDDR6 memory.

3.7 CPU Interface

The Broadcom iProc block provides an interface between the host CPU and the internal registers and tables within the switch device, enabling complete management of the switch.

The iProc block is made up of the following components:

- PCIe x2 lane Gen3 interface at up to 8 Gb/s:
  - Compatible with x1 lane PCIe.
  - Compatible with PCIe Gen1 at 2.5 Gb/s or Gen2 at 5 Gb/s.
- BSC (I^2C-compatible) two-line interface.
  - Basic device debug and register access (PCIe debug).
  - PCIe QSPI flash programming.
  - Loading code used for heating when an industrial device is powered-up at a low ambient temperature.
- Microcontroller subsystem:
  - Two Arm Cortex-R5 microcontrollers, running at 875 MHz (independent of core clock).
  - 32-KB I-Cache, 32-KB D-Cache for each microcontroller core.
  - 128-KB I-tightly coupled memory, 128-KB D-tightly coupled memory for each microcontroller core.
  - 1-MB internal system memory.
- MIIM interface:
  - MDIO compatible interface.
- LED interface.
- SBUS DMA: Enables the BCM88280 to read from host memory and update the BCM88280 tables, and to read BCM88280 tables and write to the host memory.
- FIFO DMA.
- Packet TX/RX DMA.
- Remote CPU over network interface.
- Miscellaneous (endian order, reset controls).

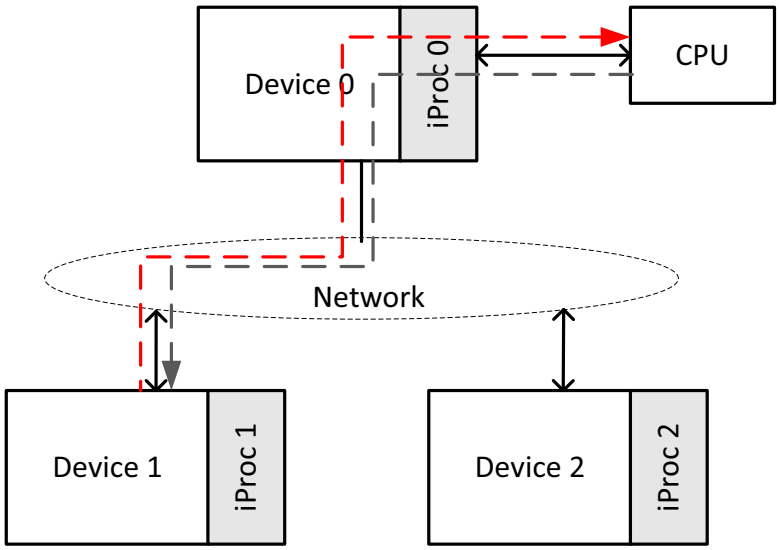
3.7.1 Remote CPU Support

The BCM88280 can be programmed from a remote CPU after initialization. Upon power-up, the device must be initialized using the PCIe interface. After the device has been initialized, the following functions are supported:

- iProc register access
- Generating RCPU packets when interrupts are triggered
- SCHAN register access
- SCHAN table access

The BCM88280 can operate in a system that is managed by a remote CPU. The CPU management interface controller (CMIC) communicates with the remote CPU through Ethernet packets with a special EtherType. These packets are referred to as remote CPU packets. The following figure represents a system managed by a remote CPU.

Figure 5: System Managed by Remote CPU



For the CPU to generate an S-channel operation in Device 1, the following events must occur:

1. The CPU generates an Ethernet packet with MACDA addressed to iProc1 with a special EtherType value reserved for remote CPU packets. The packet is an SCHAN_REQUEST.
2. iProc0 injects this packet into the ingress pipeline of Device 0. The packet is forwarded based on the MACDA.
3. The packet is received at Device 1 and is forwarded to iProc1.
4. iProc1 interprets the packet and performs the S-channel operation.
5. iProc1 creates a new SCHAN_REPLY packet based on the result of the S-channel operation. This is also an Ethernet packet with MACDA addressed to the CPU with a special EtherType. This packet is injected into the ingress pipeline of Device 1.
6. Device 1 forwards the SCHAN_REPLY packet based on the MACDA and the packet is sent to Device 0.
7. Device 0 receives the packet and forwards it to iProc0.
8. iProc 0 sends the packet to the CPU.

3.7.2 Remote Packet Operations

Remote packets are those that are sent or received by the iProc without a local CPU (whether internal or external) being involved. The iProc receives a remote packet from the switch egress pipe. The iProc matches this packet and performs some operations based on the packet data. The iProc may then send a packet back to the sender of the original packet.

The remote CPU performs certain SCHAN operations without the local CPU's intervention. This is especially useful in stacks where the master CPU in the stack may want to perform L2 insert or delete operations. The means for having the CMIC match incoming packets and perform an SCHAN operation is provided. The CMIC may then send a reply packet back to the requesting remote CPU with the SCHAN operation's status and result data.

Although remote CPUs can send arbitrary SCHAN control packets to the device using this mechanism, it does not remove the requirement for a local CPU to configure the switch (either internal or external). The remote CPU SCHAN packets contain control information to match a reply to a request, but higher layer software must be provided to deal with lost packets, whether they are request or reply packets. Some SCHAN operations are potentially destructive in that they cannot easily be replayed if a reply is lost. No mechanism exists in this device to handle such situations.

3.7.3 PCIe Interface

The PCIe interface of the BCM88280 switch conforms to PCIe 3.1 specifications. The BCM88280 supports two lanes of Gen3 PCIe (8G in each direction). No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

3.7.4 MIIM

The iProc supports the IEEE 802.3 standard MII Management (MIIM) interface. This is a two-wire serial bus controlled by the iProc that allows register access to external PHYs in the system. The two signals for MIIM are MDC (clock) and MDIO (bidirectional data).

The CPU programs the external PHY registers using this interface. The MIIM interface can be configured to support Clause 22 or Clause 45.

The BCM88280 supports seven MIIM interfaces (MDIO_0 and MDC_0 are not available for user applications).

3.7.5 UART

The BCM88280 has two UART interfaces. UART interfaces are used for debugging software running on the microcontrollers (one UART for each microcontroller). The UART interfaces can be used for time-of-day (ToD) synchronization

The UART interface includes only the following two data lines:

- One RxData line
- One TxData line

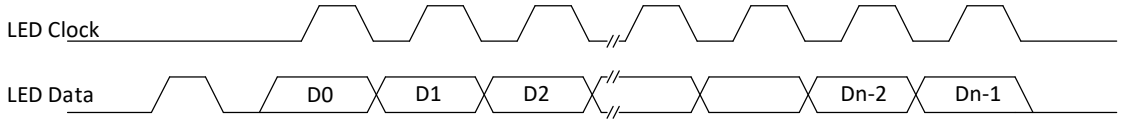
3.7.6 LED Interface

The device provides five serial LED output interfaces. An Arm Cortex-M0 microcontroller has control of all five interfaces, allowing the user to select which interfaces are used to provide serial LED bitstreams. A user can write code for the microcontroller that collects status for Ethernet ports, forms streams of status bits, and then shifts them out using any one of the LED interfaces.

The output frequency and refresh rate are user-configurable. These parameters are common across all five of the LED status interface outputs.

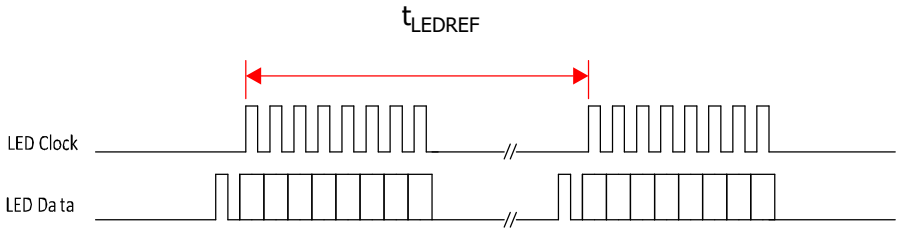
A two-wire (clock and data) LED interface controls system LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle (see the following figure).

Figure 6: Single LED Refresh Cycle



The LED refresh cycle is repeated periodically to refresh the LEDs (see the following figure).

Figure 7: LED Refresh Timing



Chapter 4: Pin Signal Description

4.1 Pin List and Pin Map

The BCM88280 pin list and pin map are provided in spreadsheet format on the Broadcom Engineering Support Portal (ESP) for collateral distribution. The spreadsheet serves as the official document containing the device's signal mapping. Refer to the *BCM88480 PinList* file (see Related Documents).

NOTE: The BCM88280 uses the same package, pin names, and I/O definitions as the BCM88480.

4.2 Pin I/O Type Description

The following table lists the conventions that are used to describe the I/O nature of the pins.

Table 6: Signal I/O Type Description

I/O	Description
B	Bidirectional signal
B_{OD}	Open drain bidirectional signal
B_{PD}	Bidirectional signal, with internal pull-down[a]
B_{PU}	Bidirectional signal, with internal pull-up[a]
I	Input signal
I_{OD}	Open drain input signal
I_{PD}	Input signal, with internal pull-down[a]
I_{PU}	Input signal, with internal pull-up[a]
NC	No Connect
O	Output signal
O_{OD}	Open drain output signal
O_{PD}	Output, with internal pull-down[a]
O_{PU}	Output, with internal pull-up[a]

a. Pull-up and pull-down values are minimum = 40 kΩ, maximum = 60 kΩ.

4.3 Pin Description – Grouped by Function

The following table provides an overview of the pins on the BCM88280.

NOTE: The BCM88280 uses the same package, pin names, and I/O definitions as the BCM88480.

NOTE: Information about connectivity and filters for some of the signals is available in the *Hardware Design Guidelines for StrataDNX 16-nm Devices* (DNX16-AN1xx). In the following table, this document is referred to as the HWDG.

Table 7: Pin List by Function

Signal/Bus Name	Qty.	Type	Tech	Description
PCIe Interface				PCIe interface supporting Gen1, Gen2, and Gen3. According to connectivity (x1, or x2), use lanes [0], or [1:0].
PCIE_TX_[1:0]_P/N	2 × 2	O	Differential	PCIe differential TX pairs. The lanes should be AC coupled. When not in use, leave open.
PCIE_RX_[1:0]_P/N	2 × 2	I	Differential	PCIe differential RX pairs. The lanes should be AC coupled. RX is internally terminated. When not in use, leave open.
PCIE_REFCLK_P/N	2	I	Differential CML	PCIe reference clock inputs. 100 MHz. External 100Ω termination is required between P and N pins. For connectivity, refer to the HWDG.
PCIE_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
PCIE_RST_N	1	I_{PD}	CMOS 1.8V	PCIe reset, active low. Follow the functionality described in Section 5.5, Power-Up, Power-Down, and Reset Sequence. (This function is required for PCIe Gen1, Gen2, and Gen3.) Use external pull down to force 0 while control logic is not initiated.
PCIE_PVDD0P8	1	PWR	0.8V	PCIe PLL power supply. For the recommended filter, refer to the HWDG.
PCIE_RTVDD0P8	2	PWR	0.8V	PCIe SerDes analog power supply. For the recommended filter, refer to the HWDG.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
QSPI				The QSPI interface accesses a serial flash memory device. The flash memory holds the PCIe SerDes firmware and configuration that is required in all PCIe modes (Gen1, Gen2, and Gen3). Output pins are driven even when the device is in reset.
QSPI_CS_N	1	O_{PD}	CMOS 1.8V	Chip select (active low) from device to flash.
QSPI_HOLD_N	1	O_{PD}	CMOS 1.8V	Hold (active low) from device to flash. Can be used to pause the serial communication with the initiator device without resetting the serial sequence.
QSPI_MISO	1	I_{PD}	CMOS 1.8V	Serial data from flash (SO) to device (MI).
QSPI_MOSI	1	O_{PD}	CMOS 1.8V	Serial data from device (MO) to flash (SI).
QSPI_SCK	1	O_{PD}	CMOS 1.8V	Serial clock from device to flash.
QSPI_WP_N	1	O_{PD}	CMOS 1.8V	The write protect (WP_N) allows normal read/write operations when held high. When the WP_N is brought low, all write operations are blocked.
BSC/I^{2}C Interface				The BSC/I^{2}C is an alternate management interface that can be used for PCIe debugging, QSPI image programming, and for loading code used for heating when an industrial device is powered up at a low ambient temperature.
I2C_SCL	1	I_{OD}	CMOS 1.8V	BSC/I^{2}C CPU interface (responder only). Clock. Open drain. Must be pulled up externally to 1.8V.
I2C_SDA	1	B_{OD}	CMOS 1.8V	BSC/I^{2}C CPU interface (responder only). Data in/out. Open drain. Must be pulled up externally to 1.8V.
Miscellaneous Signals				
INT_N	1	O	CMOS 1.8V	CPU interrupt output. Pseudo open drain, active low. Must be pulled up externally to 1.8V.
SYS_RST_N	1	I_{PD}	CMOS 1.8V	Device reset input. Active low. Use external pull down to force 0 when control logic is not initiated.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
MIIM Interface				
MDC_[7:0]	8	O_{PU}	CMOS 1.8V	Clock output of MIIM interface chains. Enables controlling external PHY (initiator mode only). Supports Clause 22/45 protocol formats with CMOS 1.8V signaling. When not in use, leave open. MDC_0 is for factory test only. Leave open.
MDIO_[7:0]	8	B_{PU}	CMOS 1.8V	Data in and data out of MIIM interface chains. Enables controlling external PHY (initiator mode only). Supports Clause 22/45 protocol formats with CMOS 1.8V signaling. When not in use, leave open. MDIO_0 is for factory test only. Leave open.
Power-Up Configuration Word				
PUC_[29:0]	30	I	CMOS 1.8V	Power up configuration (PUC) word. For PUC bus information, see Section 5.5, Power-Up, Power-Down, and Reset Sequence and Section 5.6, Power-Up Configuration Word.
Recommended Operating Voltage (ROV)				
ROV_[2:0]	3	O	CMOS 1.8V	Recommended operating voltage. Pull to GND, R < 5 kΩ. These pins define the required VDDC voltage levels with which the specific device should work. Working with a VDDC level that is different from the value required by the ROV may cause the device to fail normal operation or exceed power limits. For ROV information, see Section 5.2.1, Recommended Operating Voltage.
LED Controller				
LED_CLK[4:0]	5	O_{PD}	CMOS 1.8V	LED clock of the five LED buses. Used to latch the LED output data. When not in use, leave open.
LED_DATA[4:0]	5	O_{PD}	CMOS 1.8V	LED data of the five LED buses. Serially indicates port status. When not in use, leave open.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
UART				
UART[1:0]_RX	2	I_{PD}	CMOS 1.8V	UART data receive, one for each UART interface. Might be used for on-chip Arm debug. Usage options: ■ When using the Broadcom IEEE 1588 stack, both UART[1:0]_RX can be used as input of Time of Day (ToD) for Grandmaster (GM) clock. ■ When not in use, leave open.
UART[1:0]_TX	2	O_{PU}	CMOS 1.8V	UART data transmit, one for each UART interface. Might be used for on-chip Arm debug. Usage options: ■ When using Broadcom IEEE 1588 stack, both UART[1:0]_TX can be used as output of Time of Day (ToD) for timeReceiver clock. ■ When not in use, leave open.
BroadSync and Broadcom IEEE 1588 Stack Interfaces				
TS_GPIO_[5:0]	6	B_{PU}	CMOS 1.8V	User-programmable general-purpose I/Os. Each pin can be individually configured to act as input or output. Usage options: ■ When not in use, leave open. ■ When using BroadSync, TS_GPIO_1 can be used as 1 PPS for testing. ■ When using the Broadcom IEEE 1588 stack, TS_GPIO_[5:0] can be used as 1 PPS input or 1 PPS output.
TS_PLL_BYP	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
BS_PLL_BYP	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
TS_PLL_REFCLK_P/N	2	I	Differential CML	TSPLL (time stamp PLL) and BSPLL (BroadSync PLL) reference clock differential input. Clock rate is 25 MHz. For connectivity, refer to the HWDG. Usage options: ■ When not in use, leave open. ■ When using BroadSync, can be sourced from a simple free-running local oscillator. ■ When using Broadcom IEEE 1588 stack, must be sourced from TDPLL, which is sourced from oven-controlled crystal oscillator (OCXO).

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
TS_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
TS_PLL_LOCK	1	O_{PD}	CMOS 1.8V	TS PLL lock indication. High indicates PLL is locked. Lock indication is available only after software initializes and enables the PLL.
BS_PLL_LOCK	1	O_{PD}	CMOS 1.8V	BS PLL lock indication. High indicates PLL is locked. Lock indication is available only after software initializes and enables the PLL.
TS_PLL_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. For the recommended filter, refer to the HWDG.
TS[1:0]_BIT_CLK	2	B_{PD}	CMOS 1.8V	Usage options: ■ When not in use, leave open. ■ When using BroadSync: – TS0_BIT_CLK is used as BroadSync bit clock, usually 10 MHz. This signal can be configured as input for a BroadSync timeReceiver or output for a BroadSync timeTransmitter. – TS1_BIT_CLK is not used. ■ When using Broadcom IEEE 1588 stack, both TS[1:0]_BIT_CLK are optional 10-MHz output.
TS[1:0]_SYNC	2	B_{PD}	CMOS 1.8V	Usage options: ■ When not in use, leave open. ■ When using BroadSync: – TS0_SYNC is used as BroadSync heartbeat pulse, 4 kHz. – Marks the start of the transmission of the synchronize time value. This signal can be configured as input for a BroadSync timeReceiver or output for a BroadSync timeTransmitter. – TS1_SYNC is not used. ■ When using Broadcom IEEE 1588 stack, both TS[1:0]_SYNC are optional 4-kHz input or output.
TS[1:0]_TIME_VAL	2	B_{PD}	CMOS 1.8V	Usage options: ■ When not in use, leave open. ■ When using BroadSync – TS0_TIME_VAL is used as BroadSync synchronized time value and serially shifts the time value 1 bit per rising edge of the TS0_BIT_CLK. This signal can be configured as input for a BroadSync timeReceiver or output for a BroadSync timeTransmitter. – TS1_TIME_VAL is not used. ■ When using Broadcom IEEE 1588 stack, both TS[1:0]_TIME_VAL are not used.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
Synchronized Ethernet (SyncE)				
SYNCE[1:0]_CLK_OUT	2	O	CMOS 1.8V	SyncE recovered clock. With an additional external circuit, these signals can be used for system-level clock synchronization for SyncE applications. See Section 3.3.2, Recovered Clock.
SYNCE[1:0]_CLK_OUT_VALID	2	O	CMOS 1.8V	SyncE valid indication. With an additional external circuit, these signals can be used for system-level clock synchronization for SyncE applications. See Section 3.3.2, Recovered Clock.
Out-of-Band Flow Control				
FC_A_RX_CLK	1	I_{PD}	CMOS 1.8V	Flow control interface A, RX clock. When not in use, leave open or place a pull-down resistor.
FC_A_RX_STAT	1	I_{PD}	CMOS 1.8V	Flow control interface A, RX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.
FC_A_RX_SYNC	1	I_{PD}	CMOS 1.8V	Flow control interface A, RX synchronization signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.
FC_A_TX_CLK	1	O	CMOS 1.8V	Flow control interface A, TX clock. When not in use, leave open.
FC_A_TX_STAT	1	O	CMOS 1.8V	Flow control interface A, TX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
FC_A_TX_SYNC	1	O	CMOS 1.8V	Flow control interface A, TX synchronization signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.
FC_B_RX_CLK	1	I_{PD}	CMOS 1.8V	Flow control interface B, RX clock. When not in use, leave open or place a pull-down resistor.
FC_B_RX_STAT	1	I_{PD}	CMOS 1.8V	Flow control interface B, RX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.
FC_B_RX_SYNC	1	I_{PD}	CMOS 1.8V	Flow control interface B, RX synchronization signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.
FC_B_TX_CLK	1	O	CMOS 1.8V	Flow control interface B, TX clock. When not in use, leave open.
FC_B_TX_STAT	1	O	CMOS 1.8V	Flow control interface B, TX status information. Usage options: ■ When operating in ILKN mode, the functionality is xx_STAT. ■ When operating in SPI mode, the functionality is xx_STAT[0]. ■ When not in use, leave open.
FC_B_TX_SYNC	1	O	CMOS 1.8V	Flow control interface B, TX synchronization signal. Usage options: ■ When operating in ILKN mode, the functionality is xx_SYNC. ■ When operating in SPI mode, the functionality is xx_STAT[1]. ■ When not in use, leave open.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
GDDR6 Interfaces				
DDR_RES_NEG	1	B	Analog	DDR interface calibration pin. An external calibration resistor of 60.4Ω, 1%, should be connected between this pin and DDR_RES_VSS.
DDR_RES_POS	1	B	Analog	DDR interface calibration pin. An external calibration resistor of 40.2Ω, 1% should be connected between this pin and DDR_RES_VDD.
DDR_RES_VDD	1	B	Analog	DDR interface calibration pin. An external calibration resistor of 40.2Ω, 1%, should be connected between this pin and DDR_RES_POS.
DDR_RES_VSS	1	B	Analog	DDR interface calibration pin. An external calibration resistor of 60.4Ω, 1%, should be connected between this pin and DDR_RES_NEG.
DDR_VDDC	12	PWR	0.88V	Power supply to the DDR PHY core.
DDR_VDDO	93	PWR	1.3V	Power supply to the DDR PHY I/Os. DDR_VDDO is shared with the GDDR6 VDDQ. Should be set to 1.3V.
DDR0_RST_N	1	O	POD 1.3V	Drives GDDR6 RESET_N.
DDR0_CK_T/C	2	O	POD 1.3V	Clock CK_T (true) and CK_C (complementary).
DDR0_PLL_CLK_MON	1	O	Analog	Analog monitor output. Leave open.
DDR0_CAUX	1	O	POD 1.3V	Leave open.
DDR0_V_ANALOG	2	PWR	PWR	1.8V analog supply for DDR interface.
DDR0_VREF_MON	1	O	Analog	Analog monitor output. Leave open.
DDR0_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. For the recommended filter, refer to the HWDG.
DDR0_AVSS	1	GND	GND	PLL analog ground. On the board, it should share the same common GND plane as the VSS pins.
DDR0_A_AUX[1:0]	2	O	POD 1.3V	Leave open.
DDR0_A_CA[10:00]	11	O	POD 1.3V	Command address. For CA[10] external termination, refer to the HWDG.
DDR0_A_CABI_N	1	O	POD 1.3V	Command address bus inversion.
DDR0_A_CKE_N	1	O	POD 1.3V	Clock enable.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
DDR0_A_DBI[1:0]_N	2	B	POD 1.3V	Data bus inversion. DBI0_N is associated with DQ[7:0]. DBI1_N is associated with DQ[15:8].
DDR0_A_EDC[1:0]	2	I	POD 1.3V	Error Detection Code from GDDR6 to controller. EDC0 is associate with DQ[7:0]. EDC1 is associate with DQ[15:8].
DDR0_A_DQ[15:00]	16	B	POD 1.3V	Data input/output.
DDR0_A_WCK[1:0]_T/C	2 × 2	O	POD 1.3V	Write clock differential clocks used for *write* data capture and *read* data output. WCK0_T and WCK0_C are associated with DQ[7:0], DBI0_N, and EDC0. WCK1_T and WCK1_C are associated with DQ[15:8], DBI1_N, and EDC1. For WCK per word, WCK0 is used for channel A, and WCK1 is used for channel B.
DDR0_B_AUX[1:0]	2	O	POD 1.3V	Leave open.
DDR0_B_CA[10:00]	11	O	POD 1.3V	Command address. For CA[10] external termination, refer to the HWDG.
DDR0_B_CABI_N	1	O	POD 1.3V	Command address bus inversion.
DDR0_B_CKE_N	1	O	POD 1.3V	Clock enable.
DDR0_B_DBI[1:0]_N	2	B	POD 1.3V	Data bus inversion. DBI0_N is associated with DQ[7:0]. DBI1_N is associated with DQ[15:8].
DDR0_B_EDC[1:0]	2	I	POD 1.3V	Error detection code from GDDR6 to controller. EDC0 is associated with DQ[7:0]. EDC1 is associated with DQ[15:8].
DDR0_B_DQ[15:00]	16	B	POD 1.3V	Data input/output.
DDR0_B_WCK[1:0]_T/C	2 × 2	O	POD 1.3V	Write clock differential clocks used for *write* data capture and *read* data output. WCK0_T and WCK0_C are associated with DQ[7:0], DBI0_N, and EDC0. WCK1_T and WCK1_C are associated with DQ[15:8], DBI1_N, and EDC1. For WCK per word, WCK0 is used for channel A, and WCK1 is used for channel B.
DDR1_RST_N	1	O	POD 1.3V	Drives GDDR6 RESET_N.
DDR1_CK_T/C	2	O	POD 1.3V	Clock CK_T (true) and CK_C (complementary).
DDR1_PLL_CLK_MON	1	O	Analog	Analog monitor output. Leave open.
DDR1_CAUX	1	O	POD 1.3V	Leave open.
DDR1_V_ANALOG	2	PWR	PWR	1.8V Analog supply for DDR interface.
DDR1_VREF_MON	1	O	Analog	Analog monitor output. Leave open.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
DDR1_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. For the recommended filter, refer to the HWDG.
DDR1_AVSS	1	GND	GND	PLL analog ground. On the board, it should share the same common GND plane as the VSS pins.
DDR1_A_AUX[1:0]	2	O	POD 1.3V	Leave open.
DDR1_A_CA[10:00]	11	O	POD 1.3V	Command address. For CA[10] external termination, refer to the HWDG.
DDR1_A_CABI_N	1	O	POD 1.3V	Command address bus inversion.
DDR1_A_CKE_N	1	O	POD 1.3V	Clock enable.
DDR1_A_DBI[1:0]_N	2	B	POD 1.3V	Data bus inversion. DBI0_N is associated with DQ[7:0]. DBI1_N is associated with DQ[15:8].
DDR1_A_EDC[1:0]	2	I	POD 1.3V	Error detection code from GDDR6 to controller. EDC0 is associated with DQ[7:0]. EDC1 is associated with DQ[15:8].
DDR1_A_DQ[15:00]	16	B	POD 1.3V	Data input/output.
DDR1_A_WCK[1:0]_T/C	2 × 2	O	POD 1.3V	Write clock differential clocks used for *write* data capture and *read* data output. WCK0_T and WCK0_C are associated with DQ[7:0], DBI0_N, and EDC0. WCK1_T and WCK1_C are associated with DQ[15:8], DBI1_N, and EDC1. For WCK per word, WCK0 is used for channel A, and WCK1 is used for channel B.
DDR1_B_AUX[1:0]	2	O	POD 1.3V	Leave open.
DDR1_B_CA[10:00]	11	O	POD 1.3V	Command address. For CA[10] external termination, refer to the HWDG.
DDR1_B_CABI_N	1	O	POD 1.3V	Command address bus inversion.
DDR1_B_CKE_N	1	O	POD 1.3V	Clock enable.
DDR1_B_DBI[1:0]_N	2	B	POD 1.3V	Data bus inversion. DBI0_N is associated with DQ[7:0]. DBI1_N is associated with DQ[15:8].
DDR1_B_EDC[1:0]	2	I	POD 1.3V	Error detection code from GDDR6 to controller. EDC0 is associated with DQ[7:0]. EDC1 is associated with DQ[15:8].
DDR1_B_DQ[15:00]	16	B	POD 1.3V	Data input/output.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
DDR1_B_WCK[1:0]_T/C	2 × 2	O	POD 1.3V	Write clock differential clocks used for *write* data capture and *read* data output. WCK0_T and WCK0_C are associated with DQ[7:0], DBI0_N, and EDC0. WCK1_T and WCK1_C are associated with DQ[15:8], DBI1_N, and EDC1. For WCK per word, WCK0 is used for channel A, and WCK1 is used for channel B.
Calibration Resistors				
NIF_RESCAL_[2:0]	3	Analog	Analog	Resistor calibration terminal for SerDes. Connect each pin through an external resistor of 4.53 kΩ (1%) to SRD_AGND. The resistor should be located between this signal via and the nearest SRD_AGND via. NIF_RESCAL_0: Calibrate SerDes NIF50_[15:8] and NIF25_[27:16]. NIF_RESCAL_1: Calibrate SerDes NIF25_[51:28]. NIF_RESCAL_2: Calibrate SerDes NIF50_[7:0] and PCIe.
NIF_RESCAL_0_AVDD0P8	1	PWR	0.8V	RESCAL analog power 0.8V. For the recommended filter, refer to the HWDG.
Thermal Diode				
THERM_DIODE_N	1	Analog	Analog	Cathode (N) pin for the thermal diode. Use an external thermal diode reader. When not in use, connect to GND.
THERM_DIODE_P	1	Analog	Analog	Anode (P) pin for the thermal diode. Use an external thermal diode reader. When not in use, connect to GND.
THERM_DIODE_VDD3P3	1	PWR	3.3V	Thermal diode 3.3V supply.
PLLs and Clocks				
CLOCK25	1	I	CMOS 1.8V	25-MHz clock.
C_PLL_REFCLK_P/N	2	I	Differential CML	Core PLL reference clock inputs. 25 MHz. For connectivity, refer to the HWDG.
C_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
C_PLL_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. For the recommended filter, refer to the HWDG.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
C_PLL_AGND	2	GND	GND	PLL analog ground. On the board, it should share the same common GND plane as the VSS pins.
C_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Core PLL lock indication. High indicates PLL is locked.
U_PLL_REFCLK_P/N	2	I	Differential CML	Microcontroller PLL reference clock inputs. 25 MHz. For connectivity, refer to the HWDG.
U_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
U_PLL_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. For the recommended filter, refer to the HWDG.
U_PLL_LOCK	1	O_{PD}	CMOS 1.8V	Microcontroller PLL lock indication. High indicates PLL is locked.
NIF_PLL_REFCLK_P/N	2	I	Differential CML	NIF PLL reference clock inputs. 156.25 MHz. Used for NIF SerDes digital section. For connectivity, refer to the HWDG.
NIF_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
NIF_PLL_LOCK	1	O_{PD}	CMOS 1.8V	NIF_PLL lock indication. High indicates PLL is locked. Lock indication is available only after software initialize and enable the PLL.
FLEXE_8K_REFCLK	1	I	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FLEXE_PLL_REFCLK_P/N	2	I	Differential CML	Connect to 156.25 MHz or 155.52 MHz (either frequency is acceptable).
FLEXE_PLL_TESTOUT_P/N	2	O	Differential CML	Factory test only. Leave open.
FLEXE_PLL_AVDD1P8	1	PWR	1.8V	PLL analog power 1.8V. For the recommended filter, refer to the HWDG.
FLEXE_PLL_LOCK	1	O_{PD}	CMOS 1.8V	FlexE PLL lock indication. High indicates PLL is locked. Lock indication is available only after software initializes and enables the PLL.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
DDR_REFCLK_P/N	2	I	LVDS	DDR PLL reference clock inputs. 100 MHz. For connectivity, refer to the HWDG. The input buffer includes an internal differential termination of 100Ω. **NOTE:** No signal or clock should be on the LVDS inputs if DDR0_AVDD1P8 is not present.
C_PLL_BYP	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
U_PLL_BYP	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
C_PLL_BYP_CLK	1	I_{PD}	CMOS 0.8V	Factory test only. Leave open.
U_PLL_BYP_CLK[1:0]	2	I_{PD}	CMOS 0.8V	Factory test only. Leave open.
NIF_PLL_BYP	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FLEXE_PLL_BYP	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
NIF SerDes REFCLK and 1.8V PLL Supply				
NIF_[3:0]_REFCLK_P/N	4 × 2	I	Differential CML	NIF SerDes analog reference clock inputs. 156.25 MHz. ■ 0: PM50_00. ■ 1: PM50_01. ■ 2: PM25_02 to PM25_07. ■ 3: PM25_08 to PM25_10. These clocks should share the same source. For connectivity, refer to the HWDG.
NIF_[4:0]_PVDD1P8	5	PWR	1.8V	NIF SerDes PLL analog power 1.8V. For the recommended filter, refer to the HWDG.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
NIF50 SerDes Links, Power, and Test Outputs				
NIF50_TX_[15:0]_P/N	2 × 16	O	Differential	NIF SerDes (50G) differential TX pairs. (The BCM88280 supports up to 25.78125G.) The link should be AC coupled and have a termination on the link partner receiver. Verify that the link partner includes this circuitry.
NIF50_RX_[15:0]_P/N	2 × 16	I	Differential	NIF SerDes (50G) differential RX pairs. (The BCM88280 supports up to 25.78125G.) The SerDes receiver includes internal serial AC coupling and termination. If external AC coupling is required, see Chapter 5, Electrical Specifications.
NIF50_[1:0]_PLL[1:0]_PVDD0P8	2 × 2	PWR	0.8V	SerDes PLL power 0.8V. For the recommended filter, refer to the HWDG.
NIF50_[1:0]_RVDD0P8	2 × 4	PWR	0.8V	SerDes receiver power 0.8V. For the recommended filter, refer to the HWDG.
NIF50_[1:0]_TVDD0P8	2 × 3	PWR	0.8V	SerDes transmitter power 0.8V. For the recommended filter, refer to the HWDG.
NIF50_[1:0]_TVDD1P2	2 × 2	PWR	1.2V	SerDes transmitter power 1.2V. For the recommended filter, refer to the HWDG.
NIF50_[1:0]_PLL0_TESTOUT_P/N	2 × 2	O	Differential CML	Factory test only. Leave open.
NIF50_[1:0]_PLL0_LOCK	2	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
NIF25 SerDes Links, Power, and Test Outputs				
NIF25_TX_[51:16]_P/N	2 × 36	O	Differential	NIF SerDes (25G) differential TX pairs. (The BCM88280 supports up 20 SerDes from this group.) The link should be AC coupled and have a termination on the link partner receiver. Verify that the link partner includes this circuitry.
NIF25_RX_[51:16]_P/N	2 × 36	I	Differential	NIF SerDes (25G) differential RX pairs. (The BCM88280 supports up 20 SerDes from this group.) The SerDes receiver includes internal serial AC coupling and termination. If external AC coupling is required, see Chapter 5, Electrical Specifications.
NIF25_[10:02]_PVDD0P8	9	PWR	0.8V	SerDes PLL power 0.8V. For the recommended filter, refer to the HWDG.
NIF25_RTVDD0P8	66	PWR	0.8V	NIF25 SerDes analog power supply. For the recommended filter, refer to the HWDG.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
NIF25_TVDD1P2	18	PWR	1.2V	SerDes transmitter power 1.2V For the recommended filter, refer to the HWDG.
NIF25_##_PLL_TESTOUT_P/N	4 × 2	O	Differential CML	Factory test only. Leave open.
NIF25_##_PLL_LOCK	3	O_{PD}	CMOS 1.8V	Factory test only. Leave open.
Flex Ethernet				
FLEXE_RX_FP_[7:0]	8	O_{PD}	CMOS 1.8V	FlexE RX frame pulse. Use for FlexE debug.
FLEXE_RX_MFP_[7:0]	8	O_{PD}	CMOS 1.8V	FlexE RX multi-frame pulse. Use for FlexE debug.
FLEXE_TX_FP_[7:0]	8	O_{PD}	CMOS 1.8V	FlexE TX frame pulse. Use for FlexE debug.
FLEXE_TX_MFP_[7:0]	8	O_{PD}	CMOS 1.8V	FlexE TX multi-frame pulse. Use for FlexE debug.
Broadcom Internal Test and Debug				
SCAN_MODE	1	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
TEST_[4:0]	5	I_{PD}	CMOS 1.8V	Factory test only. Pull to GND, R ≤ 1 kΩ.
FTEST_[24:7, 4:0]	23	B	CMOS 1.8V	Factory test only. Required connectivity: ■ FTEST_[14:12]: Connect to GND. ■ Other FTEST pins: Leave open. FTEST_5 and FTEST_6 do not exist.
AVS_PVTMON_AIO	1	B	Analog	Factory test only. Pull to GND, R = 0Ω.
C_VTMON_AIO	1	B	Analog	Factory test only. Pull to GND, R = 0Ω.
NIF_VTMON[2:0]_AIO	3	B	Analog	Factory test only. Pull to GND, R = 0Ω.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
SPI				
SPI_MISO	1	O_{PU}	CMOS 1.8V	Factory test only. Leave open.
SPI_MOSI	1	I_{PU}	CMOS 1.8V	Factory test only. Leave open.
SPI_SCK	1	I_{PU}	CMOS 1.8V	Factory test only. Leave open.
SPI_SSN	1	I_{PU}	CMOS 1.8V	Factory test only. Leave open.
JTAG				
JTAG_TCE	1	I	CMOS 1.8V	JTAG test enable. 0 during normal device operation. 1 to enable JTAG functionality. An option is to connect with JTAG_TRST_N.
JTAG_TCK	1	I	CMOS 1.8V	JTAG, clock input.
JTAG_TDI	1	I	CMOS 1.8V	JTAG, input data.
JTAG_TDO	1	O	CMOS 1.8V	JTAG, output data.
JTAG_TMS	1	I	CMOS 1.8V	JTAG, TMS test mode input.
JTAG_TRST_N	1	I_{PD}	CMOS 1.8V	JTAG TAP controller reset. Pull down to GND. (R = < 10 kΩ.)
Power				
VDDC	116	PWR	VDDC	Core power supply. Must be adjusted according to ROV. Working with a VDDC level different from the value required by the ROV may cause the device to fail normal operation or exceed power limits.
VDDO	17	PWR	1.8V	I/O 1.8V power supply.
VSS	298	GND	GND	Connect to ground.
SRD_AGND	443	GND	GND	Analog ground (return path) for Blackhawk, Falcon, and PCIe SerDes and their supplies (PVDD, RTVDD, RVDD, and TVDD). On the board, these pins should connect to the same common GND plane as the VSS pins.

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
VDDC_SENSE	1	O	Analog	Core VDDC sense, from the VDDC supply grid. Used by the system as a feedback to the voltage supply monitor.
VSS_SENSE	1	O	Analog	Core VSS sense, from the VSS ground grid. Used by the system as a feedback to the voltage supply monitor.
NC_OCHK	1	NC	None	Orientation check for Broadcom testing systems. Leave not connected on customer board.
NB	4	None	None	No ball. The device has one free position in each corner.

Chapter 5: Electrical Specifications

5.1 Absolute Maximum Ratings

The specifications shown in the following table indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect the long-term reliability of the device.

Table 8: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply voltage 1.8V	–0.25	+2.0	V
DDR VDDO supply voltage (1.3V)	–0.3	+1.5	V
DDR VDDC supply voltage (0.88V)	–0.25	+1.04	V
Supply voltage 1.2V (SerDes TX driver)	–0.25	+1.38	V
Supply voltage 0.8V, digital core	–0.25	+1.04	V
Supply voltage 0.8V, SerDes analog	–0.25	+0.92	V
Thermal diode 3P3 supply voltage	–0.25	+3.8	V
Storage temperature	–40	+125	°C
Maximum junction temperature (T_J)	—	+110	°C

5.2 Recommended Operating Conditions

This section provides information about the recommended operating conditions for the BCM88280 device.

5.2.1 Recommended Operating Voltage

The BCM88280 is equipped with a preprogrammed recommended operating voltage (ROV) stamp indicating the nominal voltage at which the core (VDDC) of the specific BCM88280 device must be operated. The ROV stamp indicates the silicon process of this specific device. Working with a VDDC level that is different from the value required by the ROV may cause the device to fail normal operation or exceed power limits.

Power-up the BCM88280 with the initial state voltage level (according to the following table) for the VDDC. Next, read the ROV stamp from the ROV_[2:0] pins. Then, trim the VDDC power supply to the ROV stamp voltage. Perform VDDC trimming before the BCM88280 is initialized. ROV does not change from power-up to power-up.

NOTE: If more than one device is on the card, make sure each device has its own VDDC power supply. This VDDC power rail cannot be shared with any other supply rail.

Table 9: VDDC Voltage Level According to ROV Stamp

ROV_[2:0]	VDDC Voltage Level (V)	Comments
000	0.82	Initial state, detected before device power-up.
001	0.82	—
010	0.9	—
011	0.78	—
100	0.80	—
101	0.84	—
110	0.86	—
111	0.88	—

5.2.2 Recommended Operating Voltage Range for DC Supplies

The following table shows the operating voltage range of the DC supplies.

Table 10: Supply Voltage Range

Parameter	Symbol	Min.[a] (%)	Typ. (V)	Max.[a] (%)
Core 0.8V ROV digital supply	VDDC	–0.5	VDDC according to ROV[b]	+0.5
SerDes 0.8V PLL supply	NIF50_[##]_PLL[##]_PVDD0P8 NIF25_[##]_PVDD0P8	–3	0.80	+3
SerDes 0.8V RX supply	NIF##_RVDD0P8	–3	0.80	+3
SerDes 0.8V TX supply	NIF##_TVDD0P8	–3	0.80	+3
SerDes 1.2V TX driver supply	NIF##_TVDD1P2	–3	1.20	+3
PCIe SerDes 0.8V PLL supply	PCIe_PVDD0P8	–3	0.80	+3
PCIe SerDes 0.8V RX/TX supply	PCIe_RTVDD0P8	–3	0.80	+3
xPLL 1.8V supply[c]	xPLL_xVDD1P8	–3	1.80	+3
I/O 1.8V digital supply	VDDO	–5	1.80	+5
DDR PHY VDDO supply voltage	DDR_VDDO	–1	1.3	+1
DDR core voltage (Fixed, not related to ROV VDDC)	DDR_VDDC	–1	0.88	+1

a. The minimum and maximum values are the percentage deviation from the typical value.

b. Recommended operating voltage (ROV).

c. xPLL_xVDD1P8 is defined for the following signals:
   – C_PLL_AVDD1P8
   – U_PLL_AVDD1P8
   – NIF_x_PVDD1P8
   – TS_PLL_AVDD1P8
   – FLEXE_PLL_AVDD1P8
   – DDR[1:0]_AVDD1P8

5.3 Device Power Consumption

NOTE: Under the worst-case process, voltage, and temperature conditions, the target power consumption for an application based on the BCM88280 device is 50W. This target is for an application that includes full Ethernet NIF (36 × 25G), 360 Gb/s, and no ILKN.

Broadcom does not provide a separate value for thermal power. Use the maximum power as the thermal power as well.

The following table shows the current drawn by the different supply rails.

Table 11: Supply Rails and Their Drawn Current

Power Rail	Related Ball	Nominal Voltage (V)	BCM88280 Instances	Max. Current per Instance (mA)	Max. Current from Power Supply (mA)
Device core supply	VDDC	0.82	1	50,000	50,000
General CMOS IO supply	VDDO	1.8	1	600	600
System PLLs and analog	C_PLL_AVDD1P8, U_PLL_AVDD1P8	1.8	2	70	1680
	FLEXE_PLL_AVDD1P8, TS_PLL_AVDD1P8 (+ internal BS_PLL_AVDD1P8), NIF_PLL_AVDD1P8	1.8	4	10	
	DDRx_AVDD1P8	1.8	2	250	
	DDRx_V_ANALOG	1.8	2	500	
Thermal diode supply	THERM_DIODE_VDD3P3	3.3	1	1.3	1.3
DRAM PHY					
DRAM_PHY_VDDC	DDR_VDDC	0.88	1	2000	2000
DRAM_PHY_VDDO	DDR_VDDO	1.3	1	4000	4000
PCIe SerDes					
PCIe core PVDD0P8 (PLL)	PCIE_PVDD0P8	0.8	1	32.5	32.5
PCIe lane RTVDD0P8	PCIE_RTVDD0P8	0.8	2	38.75	77.5
Blackhawk SerDes					
Blackhawk core PVDD1P8	NIF_[1:0]_PVDD1P8	1.8	2	1	2
Blackhawk core PVDD0P8	NIF50_[1:0]_PLL[1:0]_PVDD0P8	0.8	2	282	564
Blackhawk lane RVDD0P8	NIF50_[1:0]_RVDD0P8	0.8	16	250	4000
Blackhawk lane TVDD0P8	NIF50_[1:0]_TVDD0P8	0.8	16	43	688
Blackhawk lane TVDD1P2	NIF50_[1:0]_TVDD1P2	1.2	16	20.5	328
SerDes rescal unit	NIF_RESCAL_0_AVDD0P8	0.8	1[a]	0.75	0.75
Falcon SerDes					
Falcon core PVDD1P8	NIF_[4:2]_PVDD1P8	1.8	6	0.625	3.75
Falcon core PVDD0P8	NIF25_[10:2]_PVDD0P8	0.8	6	122.5	735
Falcon lane RTVDD0P8	NIF25_RTVDD0P8	0.8	24	165.625	4000
Falcon lane TVDD1P2	NIF25_TVDD1P2	1.2	24	18.75	450

a. NIF_RESCAL_0_AVDD0P8 if supplied from an external pin. NIF_RESCAL_[2:1]_AVDD0P8 are supplied from other NIFxx_xVDD0P8 inside the package.

5.4 Power Supply Filtering

The following table lists the magnitude of supply noise allowed on the different supply rails.

Table 12: Supply Noise Specifications (AC)

Description	Symbol	Condition	Max.	Unit
Core 0.8V digital supply	VDDC	< 1.2 mΩ; 10 kHz to 10 MHz	30	mVpp
SerDes 0.8V PLL supply	NIF50_[##]_PLL[##]_PVDD0P8 NIF25_[##]_PVDD0P8	100 kHz to 20 MHz	3	mVpp
SerDes 0.8V RX supply	NIF50_RVDD0P8	100 kHz to 20 MHz	10	mVpp
SerDes 0.8V TX supply	NIF50_TVDD0P8	100 kHz to 20 MHz	10	mVpp
SerDes 1.2V TX driver supply	NIF##_TVDD1P2	100 kHz to 20 MHz	10	mVpp
PCIe SerDes 0.8V PLL supply	PCIe_PVDD0P8	100 kHz to 20 MHz	3	mVpp
PCIe SerDes 0.8V supply	PCIe_RTVDD0P8	100 kHz to 20 MHz	10	mVpp
PLL 1.8V supply[a]	xPLL_xVDD1P8	100 kHz to 20 MHz	3	mVpp
1.8V I/O supply	VDDO	100 kHz to 20 MHz	100	mVpp
DDR PHY I/O supply (1.3V)	DDR_VDDO	100 kHz to 20 MHz	10	mVpp
DRAM PHY core supply	DDR_VDDC	100 kHz to 20 MHz	10	mVpp
DDR analog voltage	DDR#_V_ANALOG	100 kHz to 20 MHz	10	mVpp
DDR PLL voltage	DDR#_AVDD1P8	100 kHz to 20 MHz	10	mVpp

a. xPLL_xVDD1P8 is defined for the following signals:
   – C_PLL_AVDD1P8
   – U_PLL_AVDD1P8
   – NIF_x_PVDD1P8
   – TS_PLL_AVDD1P8
   – FLEXE_PLL_AVDD1P8
   – DDR[1:0]_AVDD1P8

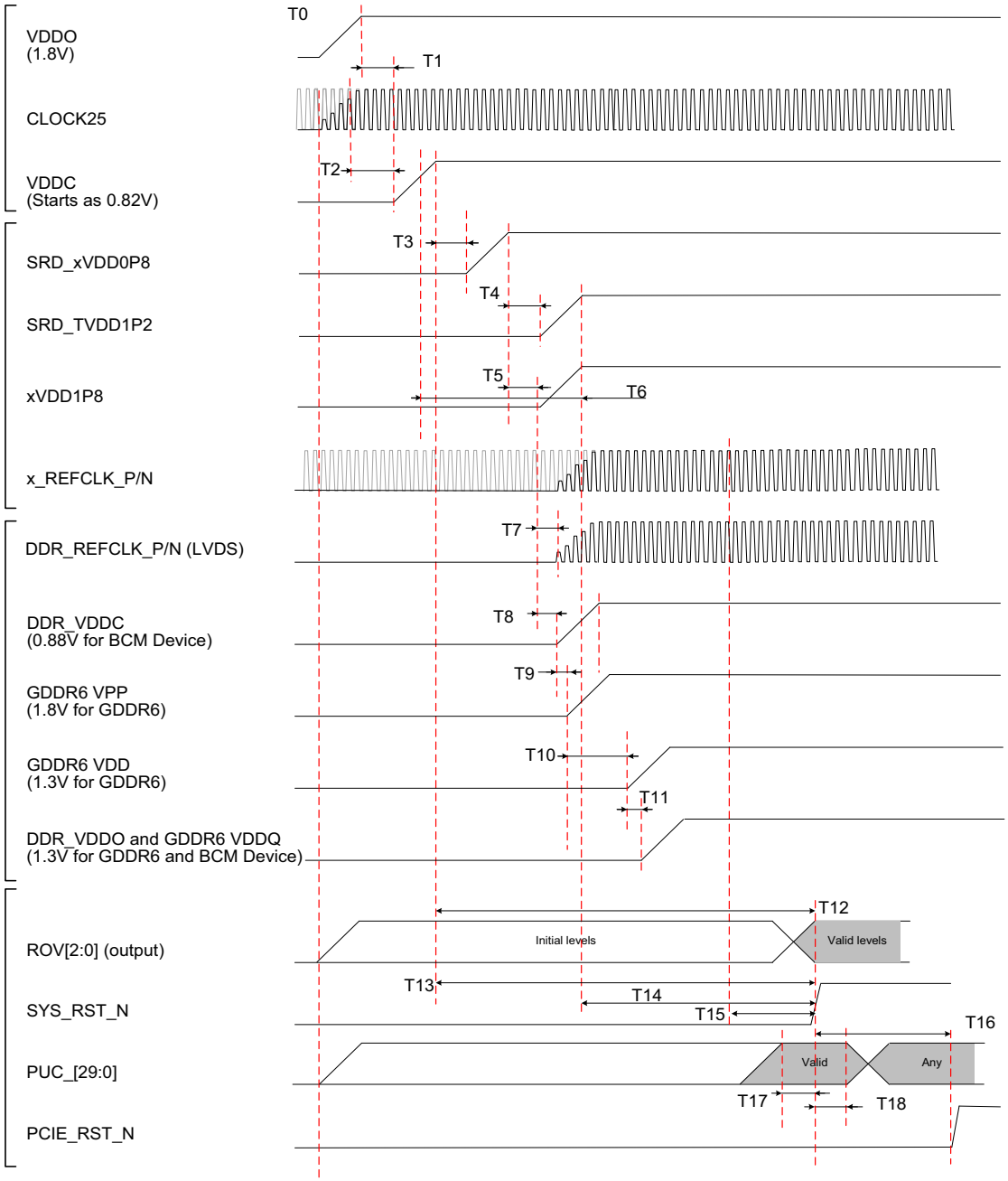
5.5 Power-Up, Power-Down, and Reset Sequence

NOTE: Compliance with the power-up and power-down requirements is mandatory for proper operation and long-term reliability.

5.5.1 Power-Up Sequence

The following figure illustrates the power-up sequence.

Figure 8: Power-Up Sequence



SRD_xVDD0P8 represents the following rails:

- PCI_PVDD0P8
- PCI_TRVDD0P8
- NIF50_[1:0]_PLL[1:0]_PVDD0P8, NIF50_[1:0]_RVDD0P8, and NIF50_[1:0]_TVDD0P8
- NIF25_[##]_PVDD0P8 and NIF25_RTVDD0P8

SRD_TVDD1P2 represents the following rails:

- NIF50_[1:0]_TVDD1P2 and NIF25_TVDD1P2

xVDD1P8 represents the following rails:

- TS_PLL_VDD1P8
- DDR[1:0]_AVDD1P8 and DDR#_V_ANALOG
- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- NIF_[4:0]_PVDD1P8
- FLEXE_PLL_AVDD1P8

x_REFCLK_P/N represents the differential reference clocks:

- PCIE_REFCLK_P/N
- TS_PLL_REFCLK_P/N
- C_PLL_REFCLK_P/N
- U_PLL_REFCLK_P/N
- NIF_PLL_REFCLK_P/N
- NIF_[3:0]_REFCLK_P/N
- FLEXE_PLL_REFCLK_P/N

NOTE: The power-up sequence can be easily met for voltage ramp-ups as slow as 1V/3 ms.

Table 13: Power-Up Sequence Timing

T Number	Description	Min.	Max.	Unit
T0	Initial condition: ■ All voltage rails are below 100 mV. ■ SCAN_MODE, TEST_[4:0], and JTAG_TCE are 0. ■ SYS_RST_N and PCIE_RST_N are 0.			
Vramp	Voltage ramp-up rate. The ramp-up rate should be between 50 µs/V and 5 ms/V.	50	5000	µs/V
T1	(VDDO > 95%) to (VDDC start).	0	15	ms
T2	(CLOCK25 Valid) to (VDDC start).	0	—	ms
T3	(VDDC > 95%) to (SRD_xVDD0P8 start).	0	3	ms
T4[a,b]	(SRD_xVDD0P8 > 95%) to (SRD_TVDD1P2 start).	0	3	ms
T5[a,c]	(SRD_xVDD0P8 > 95%) to (xVDD1P8 start).	0	3	ms
T6	(VDDC = 0.55V) to (xVDD1P8 > 95%).	—	10	ms
T7	(xVDD1P8 start) to (DDR_REFCLK_P/N start).	0	—	ms
T8	(xVDD1P8 start) to (DDR_VDDC start).	0	—	ms
T9	(DDR_VDDC start) to (GDDR6 VPP 1.8V start).	0	—	ms
T10[d]	(GDDR6 VPP 1.8V start) to (GDDR6 VDD start).	0	10	ms
T11[e]	(GDDR6 VDD start) to (DDR_VDDO and GDDR6 VDDQ start).	0	—	ms
T12	(VDDC > 95%) to ROV valid.	—	60	ms
T13	(VDDC > 95%) to SYS_RST_N de-assertion (rising from 0 to 1).	60	—	ms
T14[f]	(Last power to reach 95%) to SYS_RST_N de-assertion (rising from 0 to 1).	10	—	ms
T15	x_REFCLK_P/N valid to SYS_RST_N de-assertion.	10	—	ms
T16	SYS_RST_N =1 to PCIE_RST_N de-assertion (rising from 0 to 1).	100	—	ms
T17	PUC set-up time to SYS_RST_N de-assertion.	160	—	ns
T18	PUC hold time after SYS_RST_N de-assertion.	160	—	ns

a. There is no required timing between xVDD1P8 and SRD_TVDD1P2.

b. SRD_TVDD1P2 should *not* exceed SRD_xVDD0P8 by more than 0.6V (SRD_TVDD1P2 – SRD_xVDD0P8 < 0.6V).

c. xVDD1P8 should *not* exceed SRD_xVDD0P8 by more than 1.2V (xVDD1P8 – SRD_xVDD0P8 < 1.2V).

d. VPP must be equal to or greater than VDD and VDDQ at all times the device is powered up.

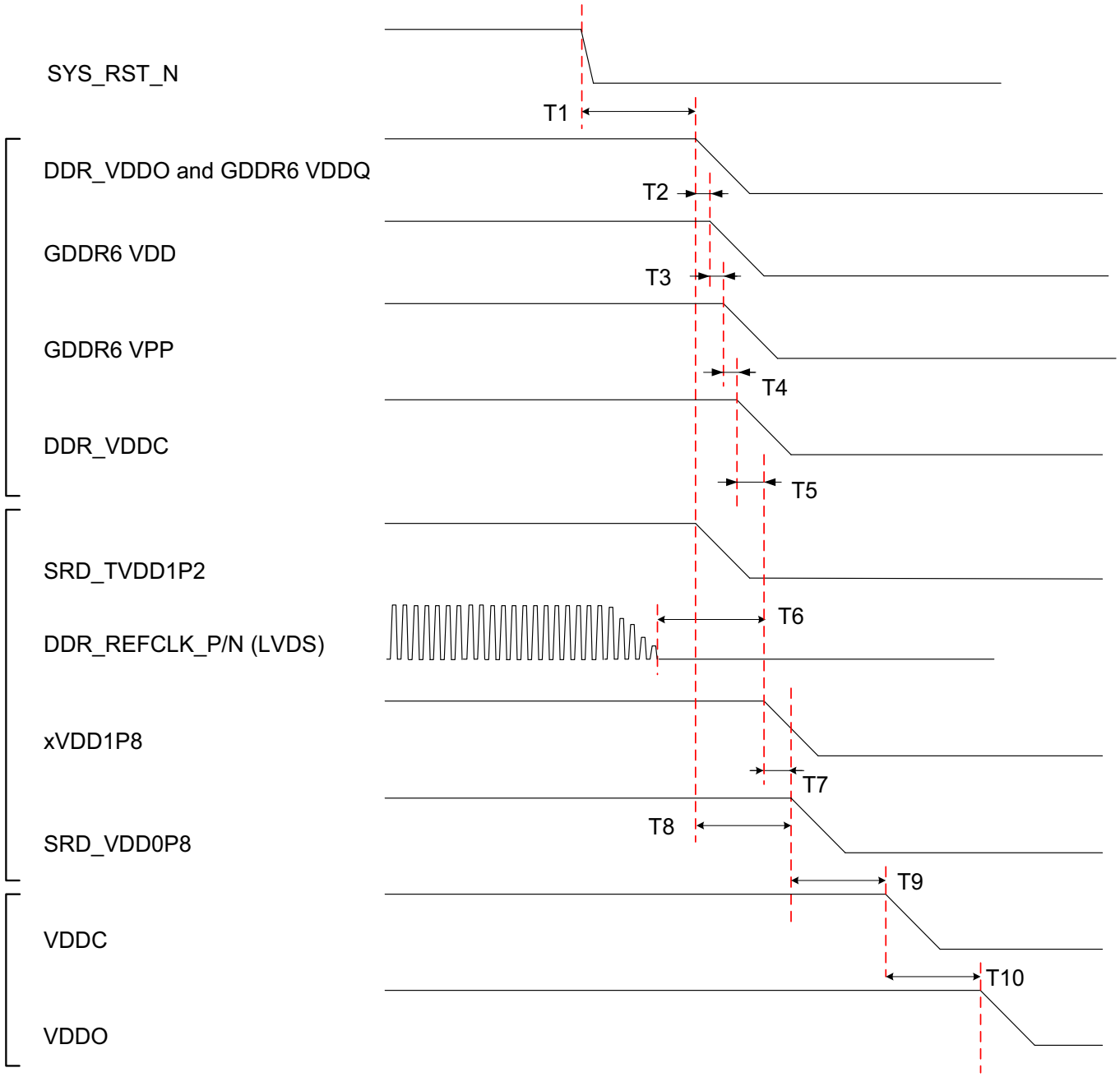
e. VDD and VDDQ must be within 300 mV of each other at all times the device is powered up.

f. The last power rail out of xVDD1P8, SRD_TVDD1P2, or DDR_VDDC.

5.5.2 Power-Down Sequence

The following figure illustrates the power-down sequence.

Figure 9: Power-Down Sequence



SRD_xVDD0P8 represent the following rails:

- PCI_PVDD0P8 and PCI_TRVDD0P8
- NIF50_[1:0]_PLL[1:0]_PVDD0P8, NIF50_[1:0]_RVDD0P8, and NIF50_[1:0]_TVDD0P8
- NIF25_[##]_PVDD0P8 and NIF25_RTVDD0P8

SRD_TVDD1P2 represents the following rails:

- NIF50_[1:0]_TVDD1P2 and NIF25_TVDD1P2

xVDD1P8 represents the following rails:

- TS_PLL_VDD1P8
- DDR[1:0]_AVDD1P8 and DDR#_V_ANALOG
- C_PLL_AVDD1P8
- U_PLL_AVDD1P8
- NIF_[4:0]_PVDD1P8
- FLEXE_PLL_AVDD1P8

Table 14: Power-Down Sequence Timing

T Number	Description[a]	Min.	Max.	Unit
T1	SYS_RST_N asserted to first power drop start. (DDR_VDDO and GDDR6_VDDQ, or SRD_TVDD1P2). This period is optional and is needed to minimize the number of packets with errors during reset.	5	—	µs
T2[b]	DDR_VDDO (+ GDDR6 VDDQ) drop start to GDDR6_VDD drop start.	0	—	ms
T3[c]	GDDR6_VDD drop start to GDDR6_VPP drop start.	0	—	ms
T4	GDDR6_VPP drop start DDR_VDDC drop start.	0	—	ms
T5	DDR_VDDC drop start to xVDD1P8 drop start.	0	—	ms
T6	DDR_REFCLK_P/N drop start to xVDD1P8 drop start.	0	—	ms
T7[d, e]	xVDD1P8 drop start to SRD_xVDD0P8 drop start.	0	—	ms
T8[d, f]	SRD_TVDD1P2 drop start to SRD_xVDD0P8 drop start.	0	—	ms
T9	SRD_xVDD0P8 drop start to VDDC drop start.	0	—	ms
T10	VDDC drop start to VDDO drop start.	0	—	ms

a. Power rails can start drop without delay; however, the requirements in the following footnotes must be met.

b. VDD and VDDQ must be within 300 mV of each other at all times the device is powered up.

c. VPP must be equal to or greater than VDD and VDDQ at all times the device is powered up.

d. Timing is not required between xVDD1P8 and SRD_TVDD1P2.

e. xVDD1P8 should not exceed SRD_xVDD0P8 by more than 1.2V (xVDD1P8 – SRD_xVDD0P8 < 1.2V).

f. SRD_TVDD1P2 should not exceed SRD_xVDD0P8 by more than 0.6V (SRD_TVDD1P2 – SRD_xVDD0P8 < 0.6V).

5.5.3 Fail-Safe Considerations

The CMOS I/Os of the BCM88280 are powered by 1.8V VDDO. Input signals can be driven before VDDO (1.8V) is supplied.

5.5.4 Warm Reset

It is possible to reset the device during normal device operation and not just during power-up. To place the device in reset, assert SYS_RST_N and PCIE_RST_N to low. Keep SYS_RST_N low for at least 10 µs before setting it high (releasing the device from the reset condition). The PCIE_RST_N should go high 100 ms after the SYS_RST_N.

When taking the device from the reset condition, all the requirements for logic signals that are part of the Power-Up, Power-Down, and Reset Sequence should be met.

5.6 Power-Up Configuration Word

The following table describes the power-up configuration word (PUC) functionality for PUC_[29:0]. When needed, use pull-up or pull-down resistors where R < 5 kΩ.

Table 15: Power-Up Configuration Signal Description

PUC	Function	Description
PUC_[9:0]	CORE_PLL_N_DIV[9:0]	For 450 MHz operation, set to PUC_[19:0] = 0x38FC.
PUC_[18:10]	CORE_PLL_M_DIV[8:0]	
PUC_[19]	Factory test	
PUC_[21:20]	I2C_SA[1:0]	Device I^2C (BSC) responder address LSB. When the I^2C (BSC) interface is used, the device physical address is made up of the following 7 bits: ■ [A6, A5, A4, A3, A2] fixed as 0x10001. ■ [A1, A0] set according to [PUC_21, PUC_20]. Available addresses are 0x44, 0x45, 0x46, and 0x47.
PUC_[25:22]	Factory test	Set to 0x0.
PUC_[26]	PCIE_QSPI_ENABLE	Set to 1.
PUC_[29:27]	Factory test	Set to 0x0.

5.7 DC Electrical Specifications

5.7.1 1.8V Digital I/Os

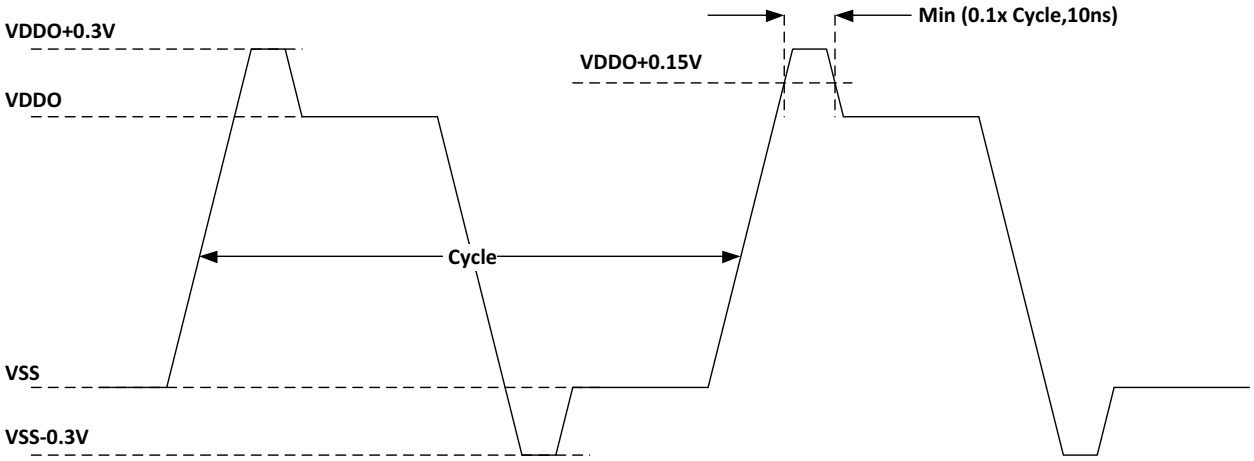
The following table lists the DC specifications of the CMOS1.8V I/Os.

Table 16: DC Specification for CMOS 1.8V I/O

Parameters	Symbol	Conditions	Min.	Max.	Unit
Input low-level voltage	V_{IL}	—	See Figure 10	VDDO × 0.32	V
Input high-level voltage	V_{IH}	—	VDDO × 0.65	See Figure 10	V
Output low-level voltage	V_{OL}	I_{OUT} = 4 mA	—	0.4	V
Output high-level voltage	V_{OH}	I_{OUT} = –4 mA	VDDO – 0.4	—	V

The following figure shows CMOS 1.8V overshoot definitions.

Figure 10: CMOS 1.8V Overshoot Definitions



The high overshoot can be up to VDDO + 0.3V, and the low overshoot can be down to GND – 0.3V. The duration, measured on a level of half the peak, should be less of 10% of the duty cycle and less than 10 ns.

5.7.2 BSC/I^{2}C

The following table lists the DC specifications of the BSC I/Os.

Table 17: DC Specification for CMOS 1.8V BSC/I^{2}C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input low level voltage	V_{IL}	—	—	—	0.3 × VDD	V
Input high level voltage	V_{IH}	—	0.7 × VDD	—	—	V
Output low level current	V_{OL}	V_{OL} = 0.4V	8	—	—	mA

5.8 AC Electrical Specifications

5.8.1 BSC/I^{2}C Interface Timing

The BSC (I^{2}C-compatible) interface supports standard I^{2}C mode and can operate at up to 100 kHz.

The BSC interface of the BCM88280 can operate in responder mode only.

The BCM88280 samples BSC_SDA during a write operation and drives BSC_SDA during a read operation.

Figure 11: BSC Timing Diagram

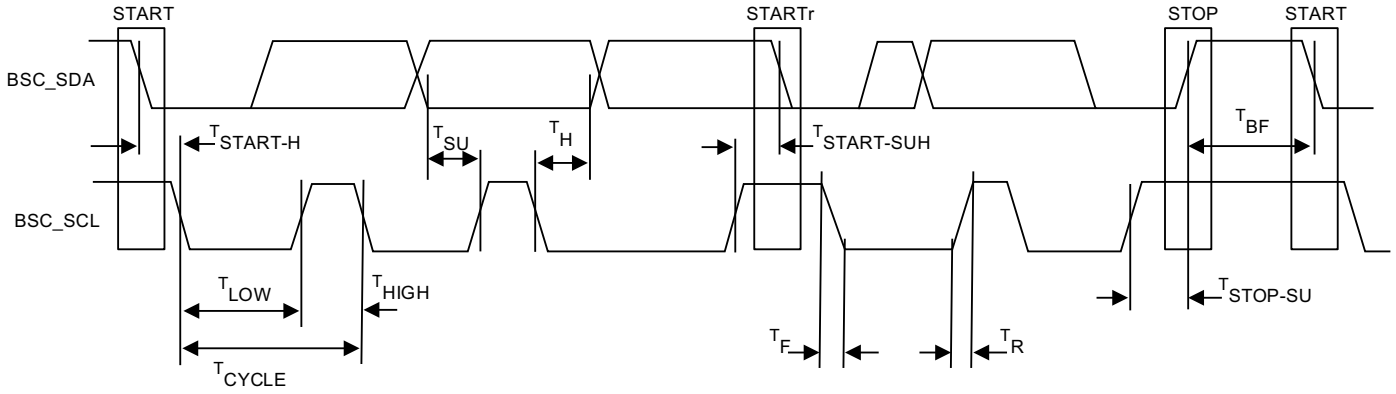


Table 18: BSC Responder Standard-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	100	kHz
BSC_SCL cycle time	T_{CYCLE}	10	—	—	µs
BSC_SCL low time	T_{LOW}	4.7	—	—	µs
BSC_SCL high time	T_{HIGH}	4.0	—	—	µs
Data hold time	T_H	0.0	—	—	µs
Data setup time	T_{SU}	250	—	—	ns
Rise time, data[a]	T_R	—	—	1000	ns
Fall time, data	T_F	—	—	300	ns
Hold time, start, or repeated start	$T_{START–H}$	4.0	—	—	µs
Setup time, repeated start	$T_{START–SU}$	4.7	—	—	µs
Setup time, stop	$T_{STOP–SU}$	4.0	—	—	µs
Bus free time (between stop and start)	T_{BF}	4.7	—	—	µs

a. BSC_SCL is an open-drain input, and BSC_SDA is an open-drain input/output. The rise time is dependent on the strength of the external pull-up resistor, which must be chosen to meet the rise time requirement.

5.8.2 Management Interface Timing

5.8.2.1 MDIO AC Characteristics

Figure 12: MIIM Interface Timing Diagram

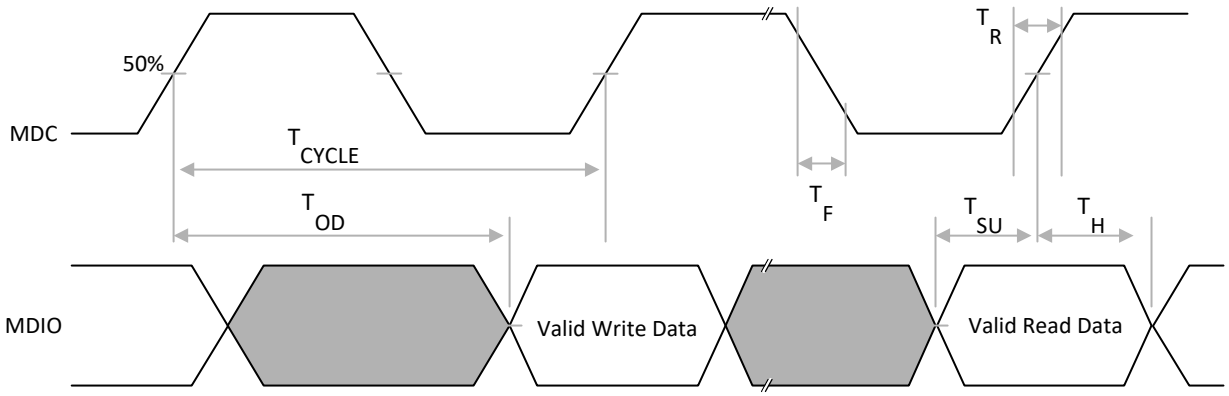


Table 19: MDC and MDIO Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
MDC clock frequency	f_{CLK}	—	2.5	12.5	MHz
MDC cycle time	T_{CYCLE}	80	400	—	ns
MDC duty cycle	—	40	—	60	%
MDIO setup time	T_{SU}	20	—	—	ns
MDIO hold time	T_{H}	0	—	—	ns
MDIO output delay	T_{OD}	10	—	35	ns

NOTE:
- Output load conditions = 25 pF.
- The external device to conform to the IEEE specifications.
- The MDC rate and the MDIO output delay are configurable.

5.8.3 SyncE Recovered Clocks

The SYNCE_[1:0]_CLK_OUT recovered clocks are single-ended 1.8V CMOS outputs.

Table 20: SYNCE_[1:0]_CLK_OUT Output Clock Timing

Parameters	Symbol	Min.	Typ.	Max.	Unit
Recovered clock frequency	F_{CLKOUT_AVG}	—	25	—	MHz

5.8.4 LED Timing

LED[4:0]_CLK and LED[4:0]_DATA are outputs. LED[4:0]_CLK output clock period is 200 ns (5.0 MHz).

Figure 13: LED Timing Diagram

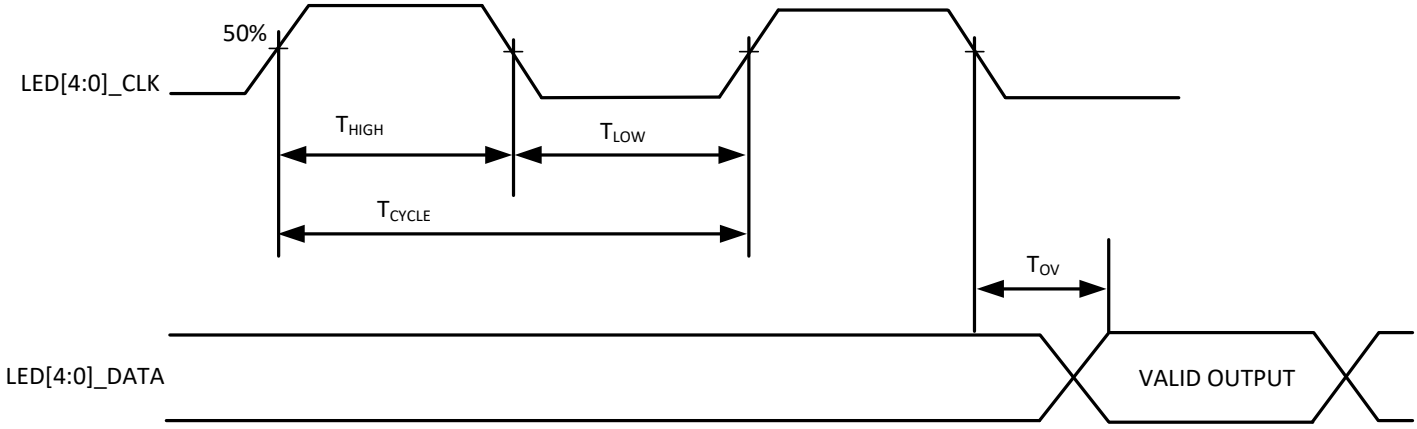


Table 21: LED Timing[a]

Parameter	Symbol	Min.	Typ.	Max.	Unit
LED frequency	F_{TCK}	—	5	—	MHz
LED period	T_{CYCLE}	200	—	—	ns
LED clock HIGH	T_{HIGH}	70	100	130	ns
LED clock LOW	T_{LOW}	70	100	130	ns
LED data output valid	T_{OV}	–15	—	15	ns

a. Timing figures are specified at the 50% crossing thresholds.

5.8.5 Out-of-Band Flow Control Timing

The out-of-band flow-control (OOBFC) interfaces support two modes of operation, which impacts both the protocol and the low-level timing.

5.8.5.1 SPI4.2 Flow-Control Mode

Figure 14: OOB Flow-Control Timing in SPI4.2 Mode

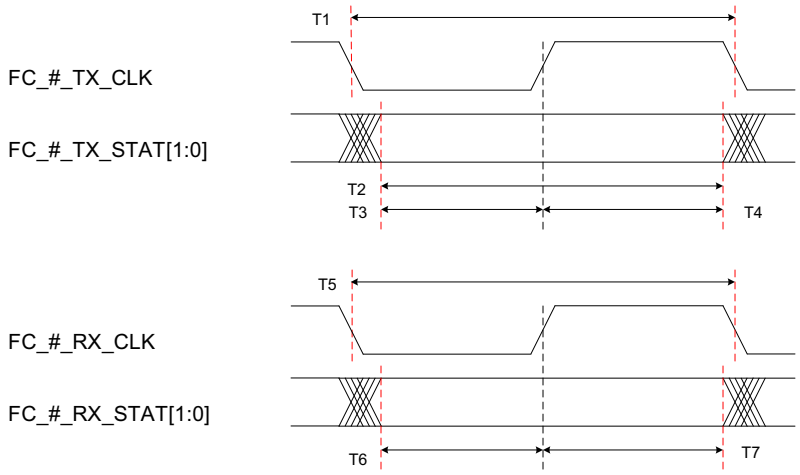


Table 22: OOB Flow-Control Timing Specifications in SPI4.2 Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
FC_#_T_CLK, OOB output clock frequency[a]	1/T1	56.25	FCORE / n	112.5	MHz
FC_#_T_CLK, OOB output clock duty cycle	—	45	—	65	%
FC_#_T_STAT[1:0] output stable window size[b]	T2	5	T1 – 1	20	ns
FC_#_T_STAT[1:0] output stable before clock[c]	T3	—	Programmable	—	ns
FC_#_T_STAT[1:0] output stable after clock[c]	T4	—	Programmable	—	ns
FC_#_R_CLK, OOB input clock frequency	1/T5	—	—	200	MHz
FC_#_R_CLK, OOB input clock duty cycle	—	40	—	60	%
FC_#_R_STAT[1:0] input setup time[d]	T6	0.5	—	—	ns
FC_#_R_STAT[1:0] input hold time[d]	T7	0.5	—	—	ns

a. FC_#_T_CLK output interface clock frequency is user-programmable. Supported rates are core clock divided by 2*n*. For a 450-MHz core clock, values can be 112.5 MHz, 75 MHz, and 56.25 MHz.

b. The given value is for FC_#_T_CLK at F(core / 4).

c. The phase of FC_#_T_CLK in relation to FC_#_T_STAT[1:0] is programmable.

d. The sampling clock edge of the input FC_#_R_STAT[1:0] with respect to the input clock can be programmed to either the rising or falling edge. Figure 14 illustrates a rising edge configuration.

5.8.5.2 Interlaken Flow-Control Mode

Figure 15: OOB Flow-Control Timing in Interlaken Mode

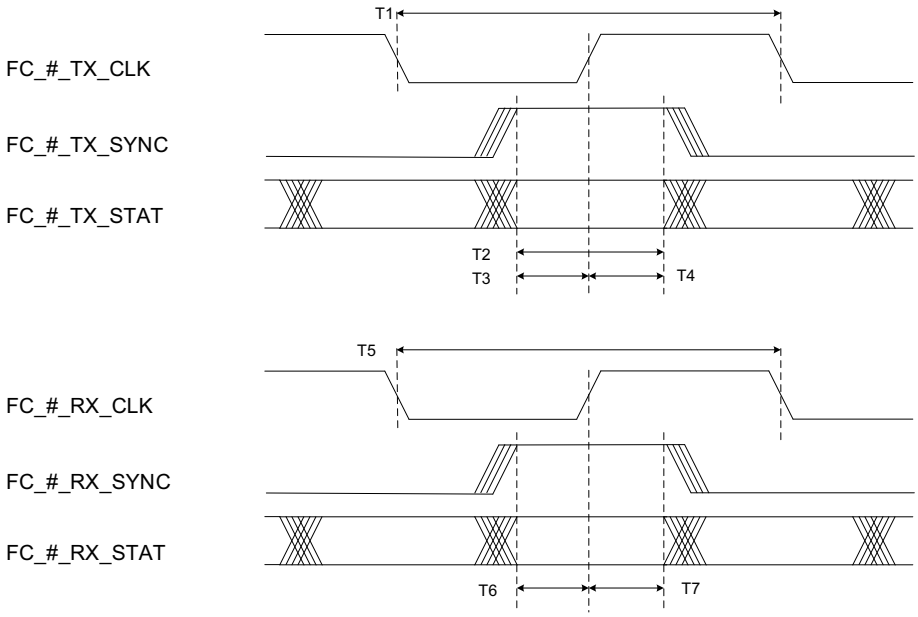


Table 23: OOB Flow-Control Timing Specifications in Interlaken Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
FC_#_T_CLK, OOB output clock frequency[a]	1/T1	56.25	FCORE / n	112.5	MHz
FC_#_T_CLK, OOB output clock duty cycle	—	45	—	65	%
FC_#_T_STAT and FC_#_T_SYNC output stable window size[b]	T2	2	0.5 × T1 – 1	9	ns
FC_#_T_STAT and FC_#_T_SYNC output stable before clock[c]	T3	—	Programmable	—	ns
FC_#_T_STAT and FC_#_T_SYNC output stable after clock[c]	T4	—	Programmable	—	ns
FC_#_R_CLK, OOB input clock frequency	1/T5	—	—	200	MHz
FC_#_R_CLK, OOB input clock duty cycle	—	45	—	65	%
FC_#_R_STAT and FC_#_R_SYNC input setup time	T6	0.5	—	—	ns
FC_#_R_STAT and FC_#_R_SYNC input hold time	T7	0.5	—	—	ns

a. FC_#_T_CLK output interface clock frequency is user-programmable. Supported rates are core clock divided by 2*n*. For a 450-MHz core clock, values can be 112.5 MHz, 75 MHz, and 56.25 MHz.

b. ILKN FC mode is DDR. The value is for FC_#_T_CLK at F(core / 4).

c. The phase of FC_#_T_CLK in relation to FC_#_T_STAT and FC_#_T_SYNC is programmable.

5.8.6 BroadSync and Time Sync Timing

The following figure and table show the timeReceiver mode input timing.

Figure 16: BroadSync Input Timing – timeReceiver Mode

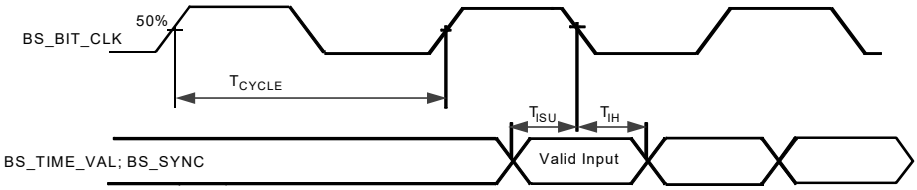


Table 24: BroadSync Input Timing – timeReceiver Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	—	100	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	ns
BS_TIME_VAL; BS_SYNC input setup time	t_{ISU}	20	—	—	ns
BS_TIME_VAL; BS_SYNC input hold time	t_{IH}	0	—	—	ns

The following figure and table show the timeTransmitter mode input timing.

Figure 17: BroadSync Output Timing – timeTransmitter Mode

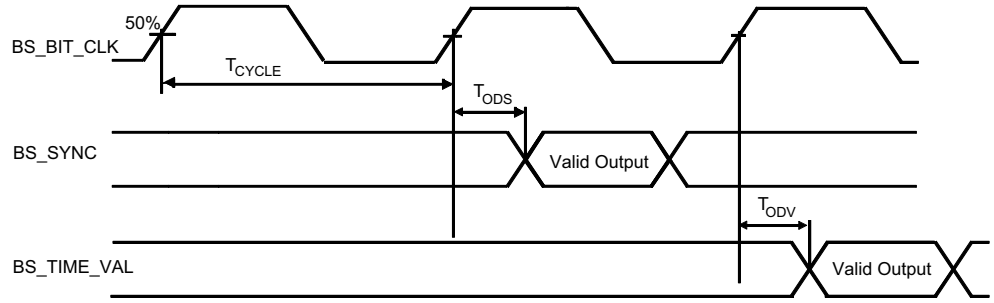


Table 25: BroadSync Output Timing – timeTransmitter Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	—	100	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	ns
BS_SYNC output delay	t_{ODS}	0	—	25	ns
BS_TIME_VAL output delay	t_{ODV}	0	—	25	ns

5.8.7 PCIe Interface

The PCIe core of the BCM88280 supports PCIe Gen1 (2.5G), Gen2 (5G), and Gen3 (8G). The following sections provide basic electrical specifications.

5.8.7.1 PCIe Receiver

The following table lists the specifications of the PCIe SerDes receiver.

Table 26: PCIe SerDes RX Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input differential swing[a]	$V_{IN-DIFF}$	85	—	1200	mVppd
Input differential termination	R_{TERM}	80	100	120	Ohm

a. The receiver input should be externally AC coupled

5.8.7.2 PCIe Transmitter

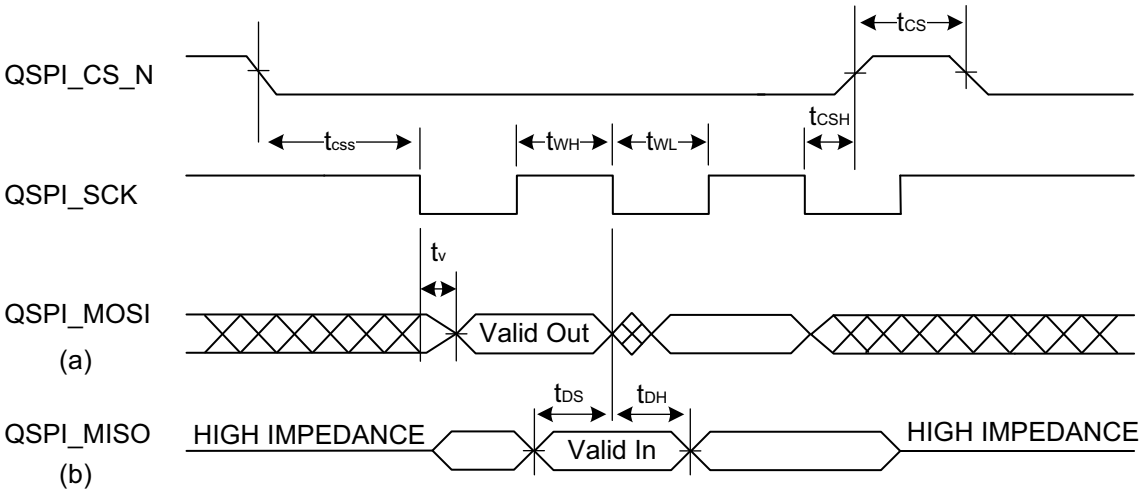
The following table lists the specifications of the PCIe SerDes transmitter.

Table 27: PCIe SerDes TX Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output differential termination	R_{TERM}	80	100	120	Ohm
Output differential swing (programmable)	$V_{OUT-DIFF}$	400	—	1200	mVppd
Output common mode	V_{OUT-CM}	—	400	—	mV

5.8.8 QSPI Flash Interface

Figure 18: QSPI Timing (Boot Read Mode Using BSPI Controller)



(a): Also valid for QSPI_MISO in dual/quad mode; also valid for QSPI_WP_N and QSPI_HOLD_N in quad mode
(b): Also valid for QSPI_MOSI in dual/quad mode; also valid for QSPI_WP_N and QSPI_HOLD_N in quad mode

Table 28: QSPI Timing (Boot Read Mode Using BSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	62.5[a]	—	MHz
SCK clock LOW period	t_{WL}	$0.5/F_{SCK} – 0.5$	—	—	ns
SCK clock HIGH period	t_{WH}	$0.5/F_{SCK} – 0.5$	—	—	ns
CS lead time	t_{CSS}	$1/F_{SCK} – 2.9$	—	—	ns
CS trail time	t_{CSH}	–1.6	—	—	ns
MOSI output valid	t_V	–1.6	—	3	ns
MISO input setup	t_{SU}	4	—	—	ns
MISO input hold	t_H	1.3	—	—	ns

a. The QSPI controller issues only FAST_READ commands, as opposed to READ (03h) commands. Therefore, the QSPI device's operating frequency should be based on the Fast Read commands rather than Read (03h) commands.

5.9 Reference Clocks

5.9.1 CLOCK25 Reference Clock

The CLOCK25 is a CMOS 1.8V input. This is a free-running clock (without an internal PLL) that is used for SYS_RST_N propagation and other basic operation. The required parameters are specified in Table 16, DC Specification for CMOS 1.8V I/O.

Table 29: CLOCK25 Specifications

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	—	25	—	MHz
Reference clock accuracy	ACC_{REF}	—	–100	—	+100	PPM
Reference duty cycle	F_{DC}	—	40	—	60	%
Rise/fall time	T_R/T_F	20% to 80%	—	—	4.0	ns
Input jitter cycle-to-cycle, peak-to-peak,10K samples	J_{IN}	—	—	—	100	ps

5.9.2 Core and Microcontroller PLL Reference Clocks

The BCM88280 holds two PLLs that drive the internal data path and logic. These PLLs are the core clock PLL (C_PLL) and the microcontroller clock PLL (U_PLL). The C_PLL_REFCLK_P/N and U_PLL_REFCLK_P/N, respectively drive these PLLs.

The following table lists the specifications of the core PLL (C_PLL) and the microcontroller PLL (U_PLL) reference clocks.

Table 30: C_PLL and U_PLL Reference Clock Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	25	—	MHz
Reference clock accuracy, total stability	ACC_{REF}	–50	—	+50	PPM
Duty cycle	F_{DC}	45	50	55	%
CML input reference clock swing (diff.)[a]	—	500	—	2000	mVppd
Input CML differential termination	—	80	100	120	Ohm
Input CML clock slew. Based on rise/fall time (10% to 90%)	T_R/T_F	—	—	0.8[b]	ns/Vppd
Input jitter (12 kHz to 5 MHz, RMS)	J_{IN}	—	—	0.35	ps

a. Input should have external AC coupling. The device has an internal 100Ω differential termination.

b. There is a 0.4-ns rise/fall time for a 500-mV swing and 1.6-ns rise/fall time for a 2000-mV swing.

5.9.3 PCIe PLL Reference Clock

The following table lists the specifications of the PCIe PLL reference clock.

Table 31: PCIe PLL Reference Clock Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	100	—	MHz
Reference clock accuracy	ACC_{REF}	–300	—	+300	PPM
Reference duty cycle	F_{DC}	40	—	60	%
Input differential swing[a]	$V_{IN-DIFF}$	600	—	1200	mVppd
Rise/fall time (20% to 80%)	T_R/T_F	200	—	900	ps
Reference clock jitter (RMS, up to 100 MHz)	—	—	—	Follow PCIe specifications	ps

a. Should be AC coupled, and external 100Ω termination is required.

5.9.4 SerDes Reference Clock

The following reference clocks drive SerDes-related PLLs:

- NIF_PLL_REFCLK_P/N – Drive internal logic for NIF
- NIF_[3:0]_REFCLK_P/N – Drive NIF Blackhawk and Falcon SerDes PLLs

The following table lists the specifications of the SerDes-related reference clock.

Table 32: SerDes Reference Clock Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	156.25	—	MHz
Reference clock accuracy, total stability	ACC_{REF}	–50	—	+50	PPM
Duty cycle	F_{DC}	40	50	60	%
CML input reference clock swing (diff)[a]	—	800	—	1400	mVppd
Input CML differential termination	—	80	100	120	Ohm
Differential rise/fall time (20% to 80% for minimum amplitude)	T_R/T_F	50	—	400	ps
Input jitter (12 kHz to 20 MHz, RMS)	J_{IN}	—	—	0.15	ps
Requirement for NIF_PLL_REFCLK only[b] input jitter (12 kHz to 20 MHz, RMS)	J_{IN}	—	—	10	ps

a. Input should have external AC coupling. Device has an internal 100Ω differential termination and internal bias circuit for CM.

b. The loose requirement is only for NIF_PLL_REFCLK if it is using a source or path different from other clocks referenced in the table.

5.9.5 TS_PLL Reference Clock

Table 33: TS_PLL Reference Clock Definitions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	25	—	MHz
Reference clock accuracy	ACC_{REF}	–25	—	+25	PPM
Reference clock duty cycle	F_{REF_DC}	40	—	60	%
CML input reference clock differential swing[a]	$V_{DIFF-PK-PK}$	0.5	—	1.8	Vppd
Input reference clock rise time/fall time (10% to 90%)	T_R/T_F	—	—	1	ns/Vppd
Input jitter (12 kHz to 20 MHz, RMS)	J_{IN}	—	—	10	ps

a. Input should have external AC coupling.

NOTE: For some IEEE 1588 applications, OCXO is required. For more information, contact Broadcom support.

5.9.6 DRAM PLL Reference Clock

Table 34: DRAM PLL Reference Clock Definitions (DDR_REFCLK_P/N)

Parameters	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	100	—	MHz
Reference clock accuracy	ACC_{REF}	–100	—	+100	PPM
Reference clock duty cycle	F_{REF_DC}	45	—	55	%
Differential input voltage (absolute)	V_{DIFF_ABS}	247	350	454	mV
Input offset voltage (For 1.8V supply)	V_{OFFSET}	0.8	0.875	0.95	V
Input reference clock rise time/fall time (10% to 90%)	T_R/T_F	—	—	500	ps
Input reference clock jitter (RMS, integration range 12 kHz to 20 MHz)	R_J	—	—	1	ps

5.9.7 FlexE PLL Reference Clock

Table 35: FlexE PLL Reference Clock Definitions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Reference clock frequency	F_{REF}	—	156.25	—	MHz
Reference clock accuracy	ACC_{REF}	–100	—	+100	PPM
Reference clock duty cycle	F_{REF_DC}	40	—	60	%
CML input reference clock differential swing[a]	$V_{DIFF-PK-PK}$	0.5	—	1.8	Vppd
Input reference clock rise time/fall time (10% to 90%)	T_R/T_F	—	—	500	ps
Input jitter (12 kHz to 20 MHz, RMS)	J_{IN}	—	—	10	ps

a. The input should have external AC coupling.

5.9.8 FlexE 8K Clock

FLEXE_8K_REFCLK is a regular CMOS input, without any requirements for PLL inputs. It must be generated from the same clock source as the FLEXE_PLL_REFCLK_P/N PLL inputs.

5.10 Blackhawk SerDes Operating Conditions

The following table lists the Blackhawk (also known as BH) SerDes operating conditions.

Table 36: Blackhawk SerDes Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data rate, Ethernet	F_{b_NIF}	10.3125	—	25.78125	Gb/s
Data rate, ILKN	F_{b_ELK}	10.3125	—	25.78125	Gb/s

Each Blackhawk core includes eight SerDes. Each one of the eight SerDes is an independent lane suitable for optical and backplane applications, operating in NRZ line coding.

Each SerDes octet (Blackhawk) has two PLLs. Each transmitter and receiver for each lane can select between the two VCO clocks. In this document, the two PLLs inside an octet are referred to as BHPLL0 and BHPLL1.

5.10.1 Blackhawk SerDes Features

The following sections describe the main features of the Blackhawk SerDes.

5.10.1.1 General Features

Blackhawk supports the following general features:

- A block of eight SerDes supporting eight serial links.
- Line rates (depending on the application) from 10.3125 Gb/s to 25.78125 Gb/s).
- Two independent PLLs in each Blackhawk.
- Integrated Arm micro subsystem: Monitors the signal and adaptively adjusts the gain, peaking-filter, and DFE coefficients to optimally equalize and restore the signal. During IEEE 802.3 Clause 72 and Clause 93 TX/RX link-training, this microcontroller is also responsible for returning feedback to the far-link partner to optimally tune its transmitter.

5.10.1.2 Debug Features

Blackhawk supports the following debugging features:

- PRBS 7, 9, 10, 11, 13 15, 20, 23, 31, 49, and 58 generator and checker with burst error length measurement.
- Digital loopback: Turns around the transmit data before it goes into the analog front-end (this is a digital data path loopback for the data coming from the PCS/MAC transmit side).
- AC-JTAG for both TX and RX.
- Full-range horizontal and vertical eye diagnostics.

5.10.2 Blackhawk SerDes Receiver

The Blackhawk receiver features are as follows:

- Integrated AC coupling on RX inputs.
- Three-stage analog peaking filter (PF).
- Three-stage controlled variable gain amplifier (VGA).
- 14-tap DFE (six fixed and eight floating) with adaptive control slicer.
- Clock-phase interpolation in receiver timing recovery.
- Programmable RX polarity inversion.

The following table lists the electrical characteristics of the SerDes receiver.

Table 37: SerDes Receiver Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Input common mode	V_{IN-CM}	—	530	900	mV	Higher than the max V_{IN-CM} requires external AC capacitor on board, 100 nF.
Input differential swing	$V_{IN-DIFF}$	85	—	1600	mVppd	—
Absolute maximum RX input	V_{IN-Abs}	0	—	1100	mV	Measured RX_P to GND and RX_N to GND.

5.10.3 Blackhawk SerDes Transmitter

The Blackhawk transmitter features are as follows:

- Transmitter with fully programmable six-tap FIR.
- IEEE 802.3 link-training.
- Programmable TX polarity inversion.
- TX disable.
- Controlled peak-to-peak amplitude.

The following table lists the electrical characteristics of the SerDes transmitter.

Table 38: SerDes Transmitter Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Output common mode	V_{OUT-CM}	—	0.45	—	V	When terminated with a 100Ω differential
Output differential swing	$V_{OUT-DIFF}$	0	—	1050	mVppd	Programmable

5.11 Falcon16 SerDes Operating Conditions

The following table lists the Falcon16 SerDes operating conditions.

Table 39: Falcon16 SerDes Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data rate, NIF Ethernet	F_{b_NIF}	1.25	—	25.78125	Gb/s

Each Falcon16 core includes four SerDes. Each one of the four SerDes is an independent lane, operating in NRZ line coding. Each core has one PLL.

Every group of Falcon16 cores receives its reference clock from the NIF_[x]_REFCLK_P/N as described in Section 5.11.2, Falcon16 SerDes Supported Rates.

5.11.1 Falcon16 SerDes Features

The following sections describe the main features of the Falcon16 SerDes.

5.11.1.1 General Features

Falcon16 supports the following general features:

- A block of four SerDes supporting four serial links.
- Line rates (depending on the application) from 1.25 Gb/s to 25.78125 Gb/s per serial link.
- One PLL in each Falcon16.
- Integrated Arm micro subsystem: Monitors the signal and adaptively adjusts the gain, peaking filter, and DFE coefficients to optimally equalize and restore the signal. During IEEE 802.3 Clause 72 and Clause 93 TX/RX link-training, this microcontroller is also responsible for returning feedback to the far-link partner to optimally tune its transmitter.

5.11.1.2 Debug Features

Falcon16 supports the following debugging features:

- PRBS 7, 9, 11, 15, 23, 31, and 58 generator and checker.
- Digital loopback: Turns around the transmit data before it goes into the analog front-end (this is a digital data path loopback for the data coming from the PCS/MAC transmit side).
- AC-JTAG for both TX and RX.
- Full-range horizontal and vertical eye diagnostics.

5.11.2 Falcon16 SerDes Supported Rates

For the rates the NIF supports, see Table 2, Supported Port Modes.

5.11.3 Falcon16 SerDes Receiver

The Falcon16 receiver features are as follows:

- Integrated AC coupling on RX inputs.
- Two-stage RX equalizer.
- Two-stage controlled variable gain amplifier (VGA).
- 14-tap DFE (six fixed and eight floating) with adaptive control slicer.
- Programmable RX polarity inversion.

The following table lists the electrical characteristics of the SerDes receiver.

Table 40: SerDes Receiver Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Input common mode	V_{IN-CM}	—	750	900	mV	Higher than the maximum VIN-CM requires an external AC capacitor on the board, 100 nF.
Input differential swing	$V_{IN-DIFF}$	85	—	1600	mVppd	—
Absolute maximum RX input	V_{IN-Abs}	0	—	1100	mV	Measured RX_P to GND and RX_N to GND.

5.11.4 Falcon16 SerDes Transmitter

The Falcon16 transmitter features are as follows:

- Transmitter with fully programmable five-tap FIR.
- IEEE 802.3 link-training.
- Programmable TX polarity inversion.
- TX disable.
- Controlled peak-to-peak amplitude.

The following table lists the electrical characteristics of the SerDes transmitter.

Table 41: SerDes Transmitter Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Output common mode	V_{OUT-CM}	—	0.45	—	V	When terminated with a 100Ω differential.
Output differential swing	$V_{OUT-DIFF}$	0	—	1050	mVppd	Programmable.

Chapter 6: Thermal Specifications

6.1 Absolute and Operational Thermal Specifications

The following table shows the specifications for the absolute thermal limits.

Table 42: Absolute Thermal Limit Specifications

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	—	–40	+110	°C
Maximum junction	T_J	—	+110[a]	°C

a. Operating at a temperature above the maximum T_J may cause permanent damage to the device.
A maximum excursion temperature of T_J = 125°C for 15 days per year (less than 96 consecutive hours) is allowed.
Proper functionality and performance cannot be guaranteed when the device operates above the maximum junction temperature.

Table 43: SerDes Core Operating Temperatures (Junction)

Parameter	Symbol	Min. (Industrial-Grade Devices)[a]	Min. (Commercial-Grade Devices)	Max.	Unit
PCIe operating temperature	PCIE_T_N	–20	0	+110	°C
Blackhawk operating temperature	BLACKHAWK_T_N	–10	0	+110	°C
Falcon16 operating temperature	FALCON16_T_N	–10	0	+110	°C

a. Lowest temperature for operation. For powering up at temperatures between –40°C and 0°C, refer to the *Hardware Design Guidelines for StrataDNX 16-nm Devices (*DNX16-AN1xx), Chapter 10, Thermal Aspects, Industrial-Grade Devices.

Table 44: Ambient Temperature Conditions

Parameter	Min.	Max.	Unit
Commercial temperature grade	0	+70	°C
Industrial temperature grade	–40	+85	°C

NOTE: For additional thermal information (including information about the temperature excursion), refer to the *Thermal Considerations for High-Power Switching Devices* (StrataDNX-StrataXGS-AN1xx).

6.2 Package Block Thermal Model Specifications

The BCM88280 block thermal model is available on the Broadcom Engineering Support Portal (ESP). For more information regarding block models, refer to the `Block_Thermal_Model_Brief.pdf` file, which is part of the block model package available on the ESP.

Use only the block thermal model to perform thermal simulations. The block thermal model replaces all previous models, such as the 2R model, modified 2R model, and Delphi model. Accordingly, Broadcom does not provide θ_{JC} and θ_{JB} values for the device.

6.3 Temperature Monitoring

6.3.1 VTMON

The BCM88280 has four internal on-die temperature sensors that can be accessed by the software API. These monitors (VTMONs) can be used only while the device is operational. They have an accuracy of ±3°C.

6.3.2 Thermal Diode

The BCM88280 has an on-die thermal diode that is not coupled to any of the BCM88280 power sources nor associated with any of its logic. This enables the temperature to be read while the device is powered off or in a nonoperational condition (such as during a reset).

The diode circuit has an independent supply rail, THERM_DIODE_VDD3P3.

To measure and read the on-die thermal diode indications, external circuitry is required.

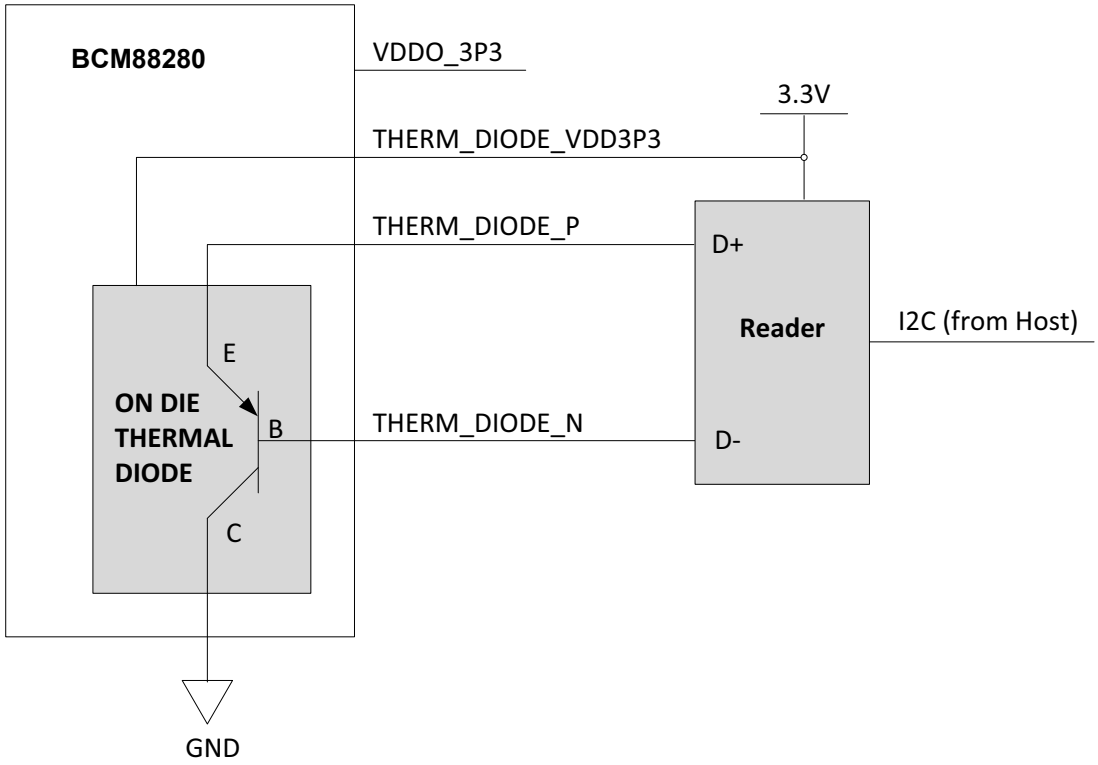
The following table shows the specifications of the on-die thermal diode.

Table 45: On-Die Thermal Diode Specifications

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating temperature	T	—	–40	—	+125	°C
Force current	I_D	—	5	—	120	µA
Forward voltage	VBE	Minimum at 5 µA	0.25	—	—	V
		Maximum at 120 µA	—	—	0.95	V
Ƞ – Ideality factor	—	—	—	1.008	—	—
Base bias (informative)	—	—	—	0.6	—	V
Accuracy[a]	—	–40°C to 110°C	–2.5	—	+2.5	°C
		110°C to 125°C	–1.5	—	+1.5	°C

a. The accuracy figures are for diode currents of 120 µA and 6 µA.

Figure 19: Example Application Using the On-Die Thermal Diode



6.4 Reflow Temperature

Broadcom offers a lead-free package.

NOTE: For additional reflow process recommendations, refer to the PCB Land Pattern and Reflow Process Recommendations section in the *Hardware Design Guidelines for StrataDNX 16-nm Devices* (DNX16-AN1xx).

The following table provides information about the solder ball composition, recommended reflow temperature, and maximum reflow temperature.

Table 46: Solder Ball Composition and Recommended and Maximum Reflow Temperature

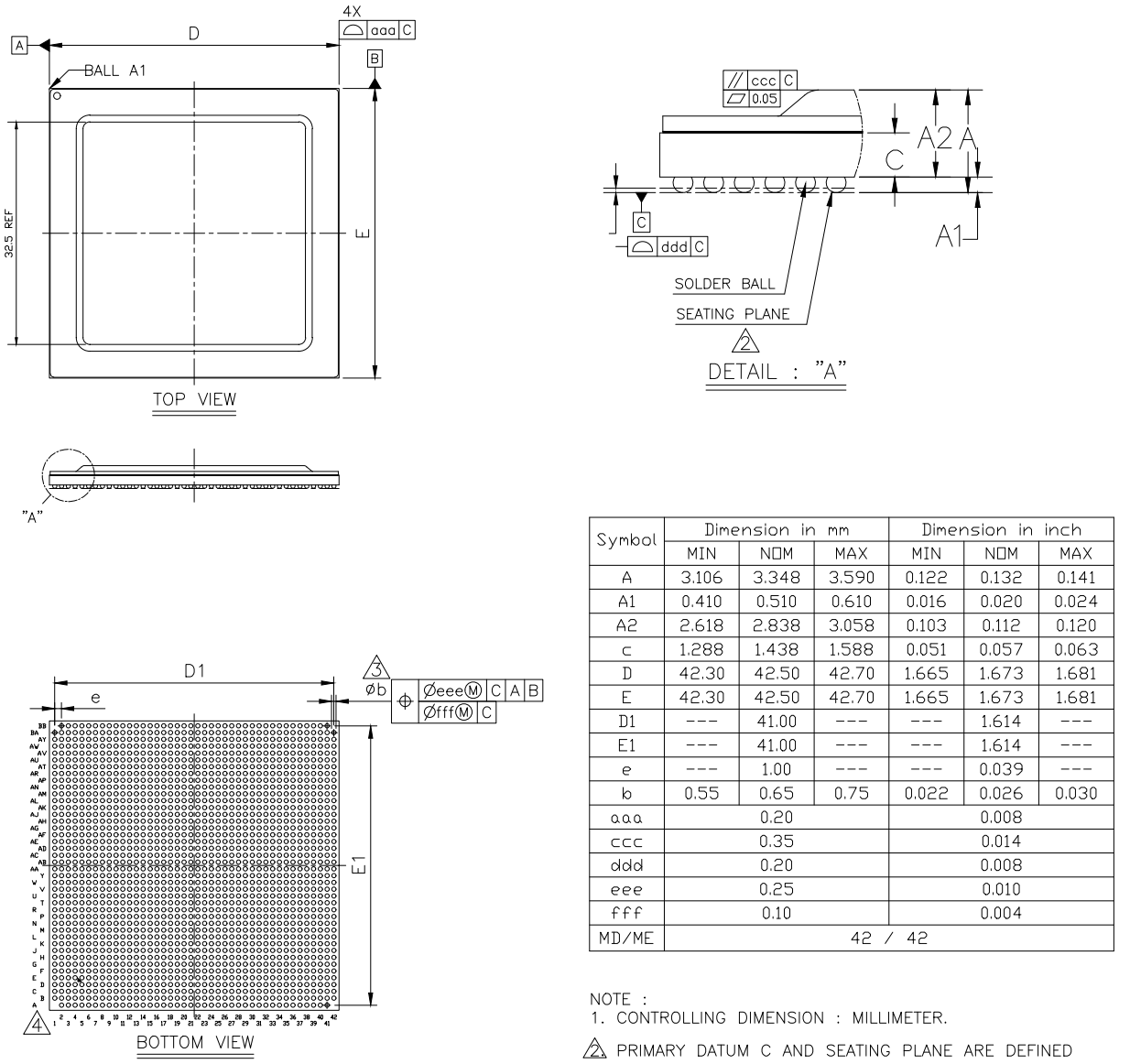
Part Number	Solder Ball Composition	Recommended Reflow Peak Temperature	Maximum Allowed Reflow Peak Temperature
Pb-free RoHS-compliant package	96.5% Sn, 3% Ag, 0.5% Cu	232°C to 237°C	245°C

6.5 Heat Sink Considerations

For information about the heat sink, refer to the *Hardware Design Guidelines for StrataDNX 16-nm Devices* (DNX16-AN1xx).

Chapter 7: Packaging

Figure 20: BCM88280 Packaging



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.106	3.348	3.590	0.122	0.132	0.141
A1	0.410	0.510	0.610	0.016	0.020	0.024
A2	2.618	2.838	3.058	0.103	0.112	0.120
c	1.288	1.438	1.588	0.051	0.057	0.063
D	42.30	42.50	42.70	1.665	1.673	1.681
E	42.30	42.50	42.70	1.665	1.673	1.681
D1	---	41.00	---	---	1.614	---
E1	---	41.00	---	---	1.614	---
e	---	1.00	---	---	0.039	---
b	0.55	0.65	0.75	0.022	0.026	0.030
aaa	0.20			0.008		
ccc	0.35			0.014		
ddd	0.20			0.008		
eee	0.25			0.010		
fff	0.10			0.004		
MD/ME	42 / 42					

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. BALL PLACEMENT USE 0.635 mm SOLDER BALL.
BGA PAD SOLDER MASK OPENING = 0.50 mm.

NOTE: The heat spreading size and flatness information is for reference only.

Related Documents

The references in this section may be used with this document.

NOTE: Broadcom provides customer access to technical documentation and software through its Engineering Support Portal (ESP) at esp.broadcom.com.

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Broadcom Items		
Hardware Design Guidelines for StrataDNX 16-nm Devices	DNX16-AN1xx	Broadcom ESP
BCM88690 Traffic Manager Programming Guide	88690-PG2xx	Broadcom ESP
BCM88480 PinList RevXX[a]	BCM88480_PinList_RevXX.zip	Broadcom ESP
Thermal Considerations for High-Power Switching Devices	StrataDNX-StrataXGS-AN1xx	Broadcom ESP
FlexE Interface Application Note	88480-AN2xx	Broadcom ESP
BCM88480 FlexE Overhead, OAM, and IEEE 1588 Handling	88480-AN3xx	Broadcom ESP
BCM88280 Device Errata	88280-ER1xx	Broadcom ESP
BCM88280 Block Thermal Model	BCM88280_Block_Thermal_Model_vXX.zip	Broadcom ESP
Other Items		
Two-Resistor Compact Thermal Model Guideline	JESD15-3	https://www.jedec.org/

a. The BCM88280 uses the same package, pin names, and I/O definitions as the BCM88480.