BROADCOM®

Product Brief

BCM87840

7-nm CMOS 400G (4:4) PAM-4 PHY

Applications

- Hyperscale data center deployments inside 400G QSFP112 optical modules
- 400G DR4/FR4/LR4
- Co-packaged optical solutions

Overview

The Broadcom® BCM87840 is the industry's highest-performance and lowest-power single-chip 400GbE PAM-4 PHY transceiver capable of driving four lanes of 106-Gb/s PAM-4 at 53 Gbaud, while supporting DR4, FR4, LR4, and QSFP112 optical links.

The BCM87840 leverages Broadcom's market-leading 7-nm PAM-4 PHY transceiver technology platform already proven with BCM8740X PHY plus provides a path to accelerating 400G QSFP-DD/OSFP optical module availability. Broadcom's advanced DSP technology and equalization techniques compensate for optical impairments while maintaining the world's lowest power to enable the deployment of 12.8-Tb/s and higher-density switch ASICs inside pluggable optical modules and co-packaged optical solutions.

The BCM87840 incorporates a highly differentiated feature set, including integrated voltage regulators, 400G FEC capability, and crossbar functionality to provide unmatched competitive advantage to the market.

In 400GbE mode, the BCM87840 converts four lanes of 106 Gb/s (at 53-Gbaud PAM-4) from the system side into four lanes of 106 Gb/s (at 53-Gbaud PAM-4) to drive next-generation high-density optical PAM-4 links inside QSFP-DD and OSFP form-factor modules.

The BCM87840 also features crossbar on both the system and line sides for easier routing in PCBs.

The on-chip clock synthesis is performed by a low-cost 156.25-MHz reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

The BCM87840 is available in a 12 mm × 13 mm, 0.5-mm pitch, 575-ball BGA, RoHS-compliant package.

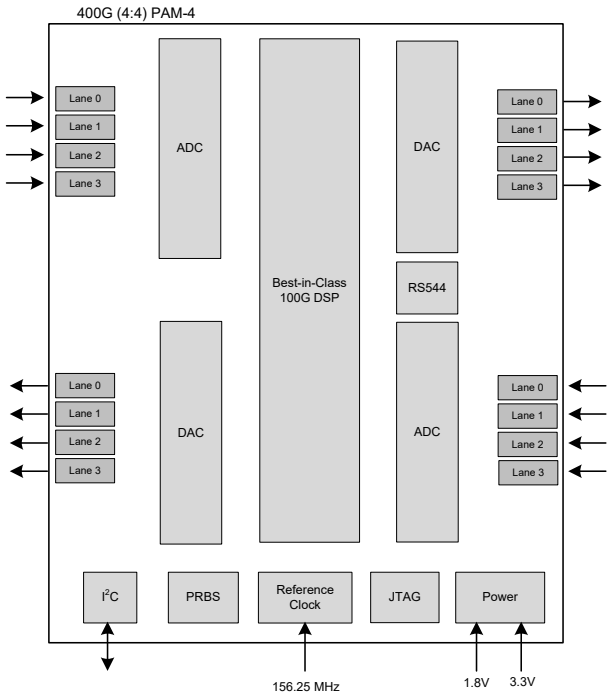
Features

- Single-chip 4 × 100G PAM-4 PHY drives 400GbE over optics:
  - System side: 4 × 106G PAM-4
  - Line side: 4 × 106G PAM-4
- Supports system-side and line-side crossbar for flexible routing to various standards
- Supports 100G, 50G, and 25G repeater modes
- Supports differential line-side output

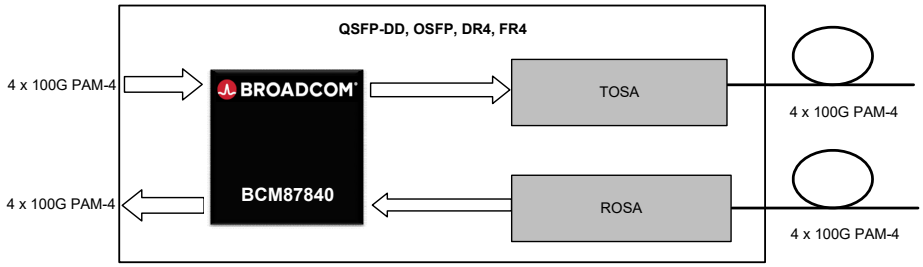
Features (cont.)

- Client-side interface compliance with CEI-28G/56G VSR and MR specifications
- IEEE 802.3bs/bj standard-compliant KP4 and end-to-end FEC bypass operation:
  - 400G/200G/100G/50G KP4 FEC
- Integrated voltage regulators for best-in-class power efficiency, reduced PCB routing, and lowest BOM costs
- Link training support available
- Line-side and system-side loopbacks
- Lowest-power 7-nm CMOS design

Block Diagram



Application Diagram



Ordering Information

Part Number	Package	Ambient Temperature
BCM87840A0KEFBG	12 mm × 13 mm, 0.5-mm pitch, 575-ball BGA, RoHS-compliant	0°C to 70°C

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For more product information: broadcom.com

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