

Product Brief



Key Features

- 8 × 100G PAM-4 PHY drives 800GbE over optics:
 - System side: 8 × 106G PAM-4
 - Line side: 8 × 106G PAM-4
- Supports system-side and line-side crossbar for flexible routing to various standards
- Supports forward gearbox for backward compatibility with 400G optical modules:
 - System side: 8 × 53G PAM-4
 - Line side: 4 × 106G PAM-4
- Supports OTN rates
 - FlexO/FOIC1.2/2.4/4.8 with Line 111.8G PAM4 and Client 27.95G NRZ/55.9G and 111.8G PAM-4
 - OTUCn/OTLC1.4 with Line 112.3G PAM-4 and Client 28.07G NRZ/56.15G and 112.3G PAM-4
- Supports 100G, 50G, and 25G repeater modes
- Supports differential line-side output

BCM87812

7-nm CMOS 800G (8:8) PAM-4 Transceiver PHY with Integrated TIA and Laser Driver

Overview

The Broadcom® BCM87812 is a high-performance, low-power 800GbE PAM-4 transceiver PHY capable of driving eight lanes of 106-Gb/s PAM-4 at 53 Gbaud, while supporting DR8, 2x FR4, and 2x LR4 optical links.

The BCM87812 leverages market-leading 7-nm PAM-4 PHY transceiver technology platform, already proven with the BCM87400 and BCM87800 PHYs, and provides a path to accelerating 800G QSFP-DD/OSFP optical module availability. The advanced Broadcom DSP technology and equalization techniques compensate for optical impairments while maintaining the world's lowest power pluggable optical modules and co-packaged optical solutions and help enable the deployment of 51.2-Tb/s and higher-density switch ASICs.

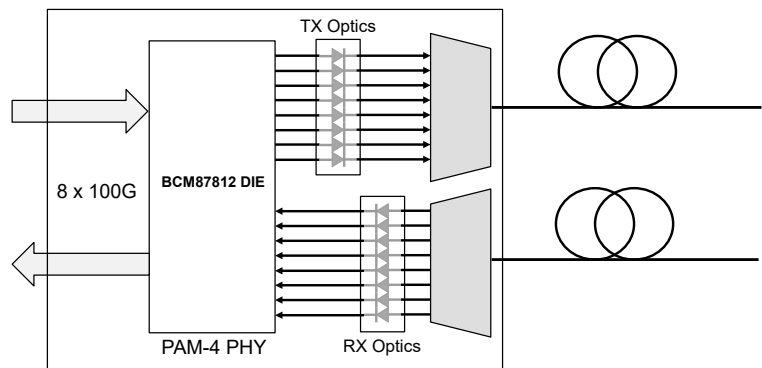
The BCM87812 incorporates a highly differentiated feature set, including integrated TIA, laser drivers, market-leading FEC capability options, and system-side switch ASIC SerDes interoperability to provide an unmatched competitive advantage to the market.

In 800GbE mode, the BCM87812 converts eight lanes of 106 Gb/s (at 53-Gbaud PAM-4) from the system side into eight lanes of 106 Gb/s (at 53-Gbaud PAM-4) to drive next-generation high-density optical PAM-4 links inside QSFP-DD and OSFP form-factor modules.

The BCM87812 also features crossbar on both the system and line sides for easier routing in PCBs.

The on-chip clock synthesis is performed by a low-cost 156.25-MHz reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

Application Diagram



Key Features (cont.)

- Client-side interface compliant with:
 - IEEE 802.3ck C2C specification supporting medium-reach channels
 - IEEE 802.3ck C2M specification supporting chip-to-module channels
- CEI-112G-MR and CEI-112G-VSR specification
- IEEE 802.3bs/bj standard-compliant KP4 and end-to-end FEC bypass operation:
 - 400G/200G/100G/50G KP4 FEC
- Supports integrated laser driver with TIA
- Line-side and system-side loopbacks
- Lowest-power 7-nm CMOS design

Applications

- 800G QSFP-DD/OSFP optical modules
- 800G DR8
- 2 × 400G DR4/FR4/LR4

Ordering Information

Part Number	Package	Ambient Temperature
BCM87812A0-DIE	—	0°C to +70°C