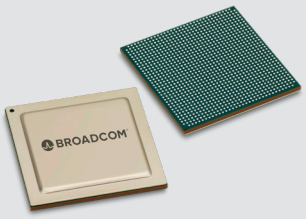
BROADCOM®

Product Brief

BCM87728

7-nm 8 x 53.125-Gb/s PAM-4 to 16 x 25.78125-Gb/s NRZ Reverse Gearbox PHY



Applications

- ASIC-to-module 8 × 56-Gb/s to 16 × 25-Gb/s front-panel interface
- High-density 10G, 25G, 40G, 50G, 100G, 200G, and 400G front-panel and backplane line-card applications

Overview

The Broadcom® BCM87728 is a single-chip 8 × 53.125-Gb/s PAM-4 to 16 × 25.78125 Gb/s NRZ reverse gearbox PHY that supports both the PAM-4 and NRZ data formats. It also supports various operation modes, such as the Retimer, Forward, and Reverse Gearbox modes. It also supports the 10G, 25G, 40G, 50G, 100G, 200G, and 400G line-card applications.

The on-chip clock synthesis is performed by a low-cost reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

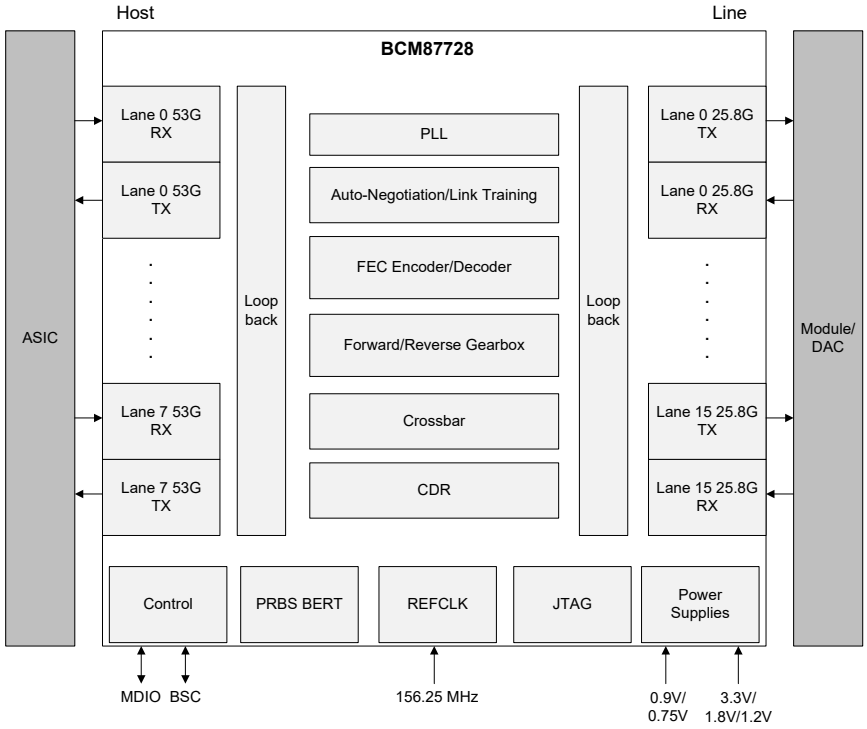
The BCM87728 is fabricated in advanced low-power 7-nm CMOS technology.

The BCM87728 is available in a 23 mm × 23 mm, 0.8-mm pitch, 729-ball BGA, RoHS-compliant package.

Features

- Host-side interface:
  - Long reach (LR): ~30 dB
- Line-side interface:
  - KR
  - CR
  - Chip-to-module (C2M) compliant
- Retimer, Forward, and Reverse Gearbox modes
- Flexible crossbar
- Supports forward error correction (FEC)
- Supports Mux and Broadcasting modes
- Supports 400G-CR8 mode
- Integrated AC-coupling capacitors at host-side and line-side receiver
- Multiple standard and line rate support for both PAM-4 and NRZ
- Continuous auto-adaptive equalizer
- Line- and system-side loopbacks
- PRBS generator/error checker
- Eye monitoring per lane accessed through MDIO
- Dual low-cost REFCLK inputs
- Recovered clock output
- Interoperates with Broadcom ASIC and merchant switch silicon
- Low-power 7-nm CMOS design
- 23 mm × 23 mm BGA, 0.8-mm ball pitch package

Block Diagram



Ordering Information

Part Number	Package	Ambient Temperature
BCM87728A0KFSBG	23 mm × 23 mm, 0.8-mm ball pitch, 729-ball BGA, RoHS-compliant	0°C to 70°C

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For more product information: broadcom.com

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