BROADCOM®

Product Brief

# BCM87416

## 400GbE PAM-4 (8:4) PHY with Integrated TIA and Laser Driver


## Applications

- Wired network infrastructure
- Hyperscale data center
- 400G QSFP-DD/OSFP optical modules
- 400G DR4/FR4/LR4

## Overview

The Broadcom® BCM87416 is a high-performance, low-power, single-chip 400GbE PAM-4 transceiver PHY capable of directly driving four lanes of 106-Gb/s PAM-4 at 53 Gbaud, while supporting DR4/FR4/LR4 optical links. The BCM87416 leverages market-leading PAM-4 transceiver PHY technology platform and represents the industry's first monolithic 400G PAM-4 PHY with integrated transimpedance amplifier (TIA) and laser driver, developed in 7-nm CMOS. The Broadcom advanced DSP technology and equalization techniques compensate for optical impairments inside pluggable optical modules while maintaining the world's lowest power to enable the deployment of 12.8 Tb/s and higher-density switch ASICs.

The BCM87416 incorporates a highly differentiated feature set, including integrated TIA, laser drivers, market-leading FEC capability options, and system-side switch ASIC SerDes interoperability to provide an unmatched competitive advantage in the market.

In 400GbE mode, the BCM87416 converts eight lanes of 53 Gb/s (at 26-Gbaud PAM-4) from the system side into four lanes of 106 Gb/s (at 53-Gbaud PAM-4) to directly drive next-generation high-density optical PAM-4 links inside QSFP-DD and OSFP form-factor modules. The BCM87416 is compliant with industry standards, including 400GBASE-DR4 and 100G-MSA draft 1.0 with KP4 FEC and FEC bypass capability.

The on-chip clock synthesis is performed by a low-cost 156.25-MHz reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

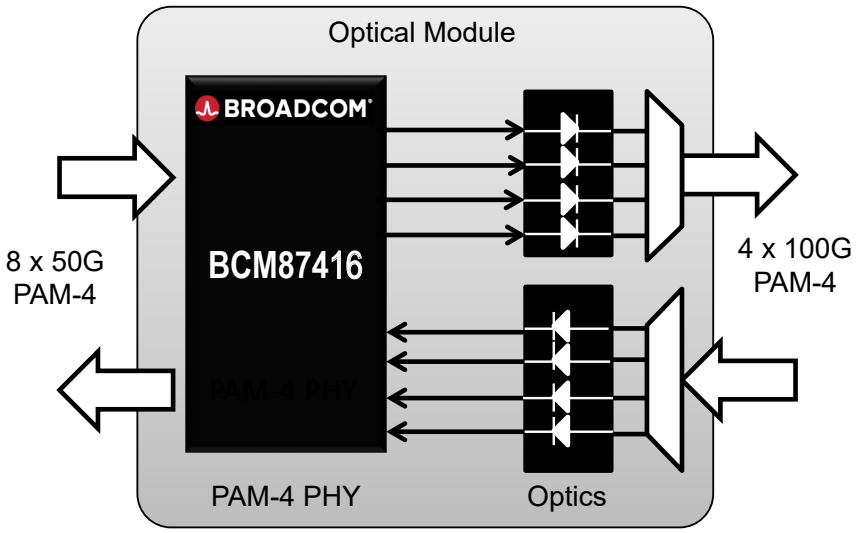
## Features

- Single-chip 4 × 100G PAM-4 PHY drives 400GbE over optics
  - System side: 8 × 53G PAM-4
  - Line side: 4 × 106G PAM-4
- Supports DR4 to DR1 break-out mode with independent lane operation capability
- Supports industry standards, including 100G-MSA draft 1.0
- Supports integrated TIA

## Features (cont.)

- Client-side interface compliance:
  - IEEE 802.3 400GAUI-8 C2C (Annex 120D) specification supporting medium-reach channels
  - IEEE 802.3 400GAUI-8 C2M (Annex 120E) specification supporting chip-to-module channels
- IEEE 802.3bs standard-compliant KP4 and end-to-end FEC bypass operation
- Built-in negotiation and detection engine
- Line-side and system-side loopbacks
- Low-power 7-nm CMOS design

**Block Diagram**



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