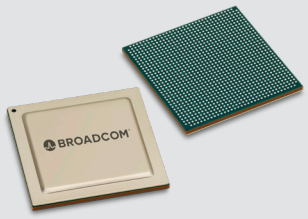
BROADCOM®

Product Brief

BCM87402

400GbE PAM-4 (8:4) with Direct-Drive



Applications

- Wired network infrastructure
- Hyperscale data center deployments inside 400G QSFP-DD/OSFP optical modules
- 400G DR4/FR4/LR4
- Co-packaged optical solutions

Overview

The Broadcom® BCM87402 is the industry's lowest power single-chip 400GbE PAM-4 PHY transceiver capable of directly driving four lanes of 106-Gb/s PAM-4 at 53 Gbaud, while supporting DR4/FR4/LR4 optical links. The BCM87402 leverages Broadcom's market-leading PAM-4 PHY transceiver technology platform and represents the industry's first monolithic 400G PAM-4 PHY Direct-Drive transceiver available in 7-nm CMOS. Broadcom's advanced DSP technology and equalization techniques compensate for optical impairments while maintaining the world's lowest power to enable the deployment of 12.8 Tb/s and higher-density switch ASICs inside pluggable optical modules and co-packaged optical solutions.

The BCM87402 incorporates a highly differentiated feature set, including integrated voltage regulators, Direct-Drive capability, market-leading FEC capability options, and system-side switch ASIC SerDes interoperability to provide an unmatched competitive advantage to the market.

In 400GbE mode, the BCM87402 converts eight lanes of 53 Gb/s (at 26-Gbaud PAM-4) from the system side into four lanes of 106 Gb/s (at 53 Gbaud PAM-4) to directly drive next-generation high-density optical PAM-4 links inside QSFP-DD and OSFP form-factor modules. The BCM87402 is compliant with industry standards, including 400GBASE-DR4 and100G-MSA draft 1.0 with KP4 FEC and FEC bypass capability.

The on-chip clock synthesis is performed by a low-cost 156.25-MHz reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

The BCM87402 device is available in an 11 mm × 12.5 mm, 0.5-mm pitch, 460-ball BGA, RoHS-compliant package. The BCM87402 is pin-to-pin compatible with the BCM87400 device.

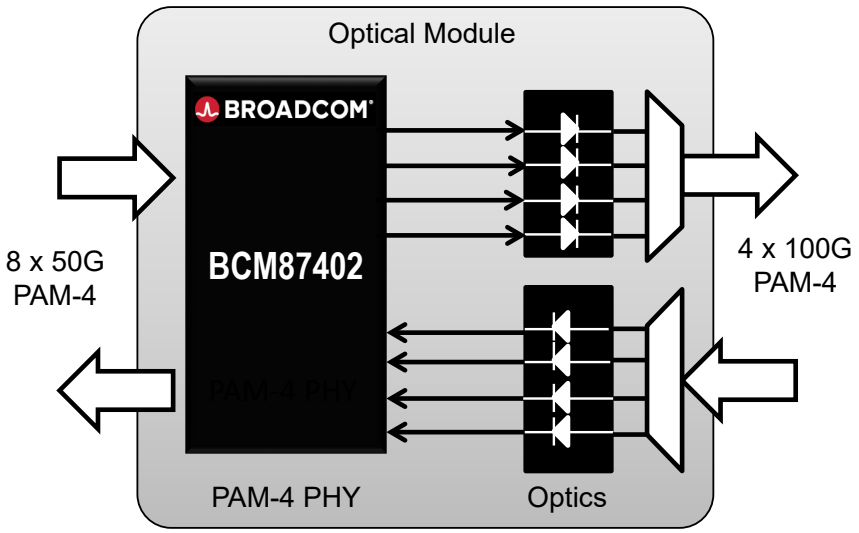
Features

- Single-chip 4 × 100G PAM-4 PHY drives 400GbE over optics
  - System side: 8 × 53G PAM-4
  - Line side: 4 × 106G PAM-4
- Supports DR4 to DR1 break-out mode with independent lane operation capability
- Supports industry standards, including 100G-MSA draft 1.0
- Supports Direct-Drive with 1.5-Vpp single-ended or 3.0-Vpp differential line-side output

Features (cont.)

- Client-side interface compliance:
  - IEEE 802.3 400GAUI-8 C2C (Annex 120D) specification supporting medium-reach channels
  - IEEE 802.3 400GAUI-8 C2M (Annex 120E) specification supporting chip-to-module channels
- IEEE 802.3bs standard-compliant KP4 and end-to-end FEC bypass operation
- Integrated voltage regulators for best-in-class power efficiency, reduced PCB routing, and lowest BOM costs
- Built-in negotiation and detection engine
- Line-side and system-side loopbacks
- Lowest-power 7-nm CMOS design

Block Diagram



Ordering Information

Part Number	Package	Ambient Temperature
BCM87402A2KREBG	Direct-Drive, 11 mm × 12.5 mm, 460-ball BGA, RoHS-compliant t	0°C to 70°C

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For more product information: broadcom.com

87402-PB100 May 26, 2021