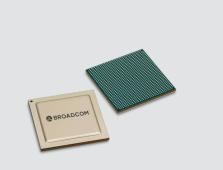


### **Product Brief**



## **Applications**

- 16 × 56-Gb/s front-panel and backplane PHY for Switch/ASIC line cards
- High-density 10G, 25G, 40G, 50G, 100G, 200G, and 400G frontpanel and backplane line-card applications

# BCM87326

# 7-nm 16 x 56 Gb/s PAM-4 PHY

### Overview

The Broadcom® BCM87326 is a single-chip 16 × 56-Gb/s full-duplex PHY that supports both the PAM-4 and NRZ data formats. It supports various operation modes, such as the Retimer, Forward and Reverse Gearbox modes. It also supports the 10G, 25G, 40G, 50G, 100G, 200G, and 400G line-card applications.

The on-chip clock synthesis is performed by a low-cost reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

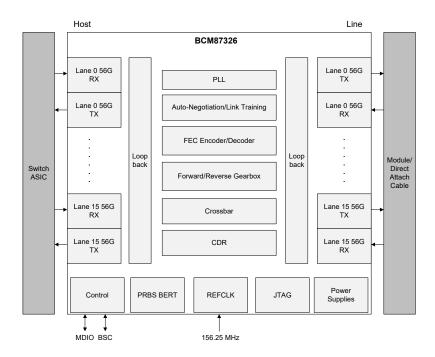
The BCM87326 is fabricated in advanced low-power 7-nm CMOS technology.

The BCM87326 is available in a 23 mm  $\times$  23 mm, 0.8-mm pitch, 729-ball BGA, RoHS-compliant package.

### **Features**

- · Host-side interface:
  - Long reach (LR): >30 dB
  - Chip-to-chip (C2C) compliant
- Line-side interface:
  - Long reach (LR): >30 dB for cable (CR) and backplane (KR) application
  - Chip-to-module (C2M) compliant
- Retimer, Forward and Reverse Gearbox modes
- Flexible crossbar
- Supports forward error correction (FEC)
- Supports Mux and Broadcasting modes
- Supports 400G-CR8 mode
- Integrated AC-coupling capacitors at host-side and line-side receiver
- Multiple standard and line rate support for both PAM-4 and NRZ
- Continuous auto-adaptive equalizer
- Line- and system-side loopbacks
- PRBS generator/error checker
- Eye monitoring per lane accessed through MDIO
- Recovered clock output
- Interoperates with Broadcom ASIC and merchant switch silicon
- Low-power 7-nm CMOS design
- 23 mm × 23 mm BGA, 0.8-mm ball pitch package

#### **Block Diagram**



Ordering Information	
Part Number	Package
BCM87326A0KFSBG	23 mm × 23 mm, 0.8-mm ball pitch, 729-ball BGA, RoHS-compliant

