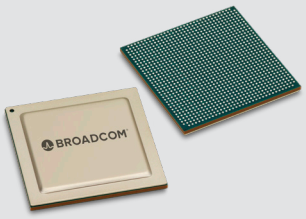
BROADCOM®

Product Brief

BCM87106

100GbE PAM-4 PHY (4:1)



Applications

- Wired network infrastructure
- Hyperscale data center deployments inside 100G QSFP28 optical modules
- 100G DR/FR/LR
- Co-packaged optical solutions

Overview

The Broadcom® BCM87106 is the industry's lowest power single-chip 100GbE PAM-4 PHY transceiver capable of driving 112-Gb/s PAM-4 at 56 Gbaud, while supporting DR/FR/LR optical links. The BCM87106 leverages market-leading PAM-4 PHY transceiver technology platform and represents the industry's first 100G PAM-4 PHY transceiver available in 7-nm CMOS. The Broadcom advanced DSP technology and equalization techniques compensate for optical impairments while maintaining the world's lowest power to enable the deployment of 12.8 Tb/s and higher-density switch ASICs inside pluggable optical modules and co-packaged optical solutions.

The BCM87106 incorporates a highly differentiated feature set, including integrated voltage regulators, market-leading FEC capability options, and system-side switch ASIC SerDes interoperability to provide an unmatched competitive advantage to the market.

In 100GbE mode, the BCM87106 supports functionality to accept 25G NRZ host-side inputs. The BCM87106 supports gearbox mode supporting QSFP28 module form factors. In gearbox mode, the BCM87102 can encode four lanes of 25.7815-Gb/s NRZ from the system side into one lane of 106.26 Gb/s (at 53 Gbaud PAM-4) with standard-compliant KP4 FEC.

The on-chip clock synthesis is performed by a low-cost 156.25-MHz reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

The BCM87106 device is available in an 11 mm × 12.5 mm, 0.5-mm pitch, 460-ball BGA, RoHS-compliant package. The BCM87106 is pin-to-pin compatible with the BCM87102 device.

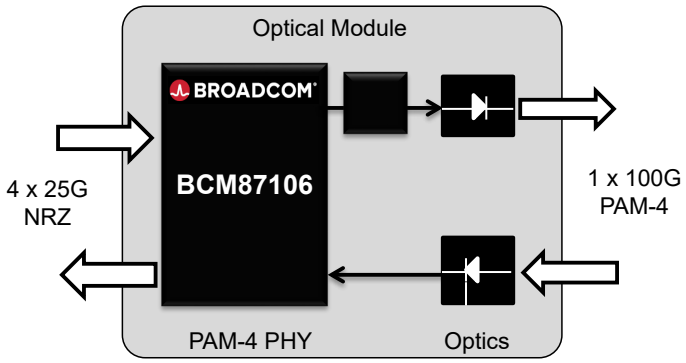
Features

- Single-chip 1 × 100G PAM-4 PHY drives 100GbE over optics
  - System side: 4 × 25G NRZ
  - Line side: 1 × 100G PAM-4
- Supports industry standards, including 100G-MSA draft 1.0
- Supports differential line-side output
- Client-side interface compliance:
  - IEEE 802.3 CAUI-4 C2C (Annex 83D) specification supporting medium-reach channels
  - IEEE 802.3 CAUI-4 C2M (Annex 83E) specification supporting chip-to-module channels
- IEEE 802.3bs standard-compliant KP4, KR4, and end-to-end FEC bypass operation

Features (cont.)

- Optimized-performance proprietary FEC modes available
- Integrated voltage regulators for best-in-class power efficiency, reduced PCB routing, and lowest BOM costs
- Built-in negotiation and detection engine
- Line-side and system-side loopbacks
- Lowest-power 7-nm CMOS design

Block Diagram



Ordering Information

Part Number	Package	Ambient Temperature
BCM87106A1KRFBG	9 mm × 8 mm, 255-ball BGA, RoHS-compliant	0°C to 70°C

BROADCOM®
connecting everything®

For more product information: broadcom.com

87106-PB100 May 26, 2021