BROADCOM®

Product Brief

BCM85828-DIE

5-nm CMOS 800G (4:4) PAM-4 Transceiver PHY with Integrated Laser Driver

Key Features

- Supports various chip modes:
  - 4:4 retimer mode with client 212.5G PAM-4 and line 212.5G PAM-4
  - 4:4 retimer mode with client 212.5G PAM-4 and line 226.875G PAM-4 with IEEE-compliant (128,120) Hamming inner code
  - Backward 4:4 retimer modes comparability to 106G/lane and 53G/lane Ethernet and HDR/NDR interface
- Proven interoperability with the Broadcom 200G electro-absorption modulated laser (EML)
- Supports 200G silicon photonics (SiPh) optics with 3.0V differential high-swing driver
- Client side supports 35 dB+ channel
- Supports client-side crossbar for flexible routing
- Supports FEC monitoring in the repeater modes with a subsampling feature available for reduced power

Overview

The Broadcom® BCM85828-DIE is the industry's highest-performance and lowest-power 200G/lane PAM-4 PHY. It enables 1.6T DR8 and 800G DR4 pluggable transceivers for next-generation AI/ML clusters and Ethernet networking of hyperscale data centers.

The BCM85828-DIE when paired with the BCM85826-DIE, helps reduce routing congestion and makes power network design simpler on the 1.6T paddle cards.

The BCM85828-DIE leverages the market-leading 5-nm PAM-4 PHY transceiver technology platform, already proven with the BCM85822. The advanced Broadcom DSP technology and equalization techniques compensate for optical impairments while delivering best-in-class module performance in BER and power consumption.

The BCM85828-DIE incorporates a highly differentiated feature set, including multiple line-side FEC options:

- Bypass mode
- Segmented mode
- Concatenated mode

This feature set also includes client-side switch ASIC SerDes interoperability to provide an unmatched competitive advantage to the market.

The BCM85828-DIE is a monolithic 800G (4:4) PAM-4 DSP. It converts four lanes of 212.5 Gb/s from the client side into four lanes of 212.5 Gb/s to drive next-generation high-density optical PAM-4 links inside an octal small form-factor pluggable (OSFP) modules.

The BCM85828-DIE also features crossbar on the client side for easier routing in the PCBs.

The on-chip clock synthesis is performed by a low-cost 312.5/625-MHz reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

Key Features (cont.)

- Fourteen-tap TX FIR support on both line and client sides
- IEEE 802.3cd standard-compliant KP4 and end-to-end FEC bypass operation:
  - 800G/400G/200G/100G KP4 FEC
- Lowest-power 5-nm CMOS design
- Lowest latency solution (~80 ns)

Applications

- 1.6T OSFP DR8 pluggable for InfiniBand XDR in AI/ML clusters
- 1.6T OSFP DR8/800G OSFP DR4 pluggable for Ethernet 200G per-lane switch ASIC in hyperscale data centers

Figure 1: Block Diagram

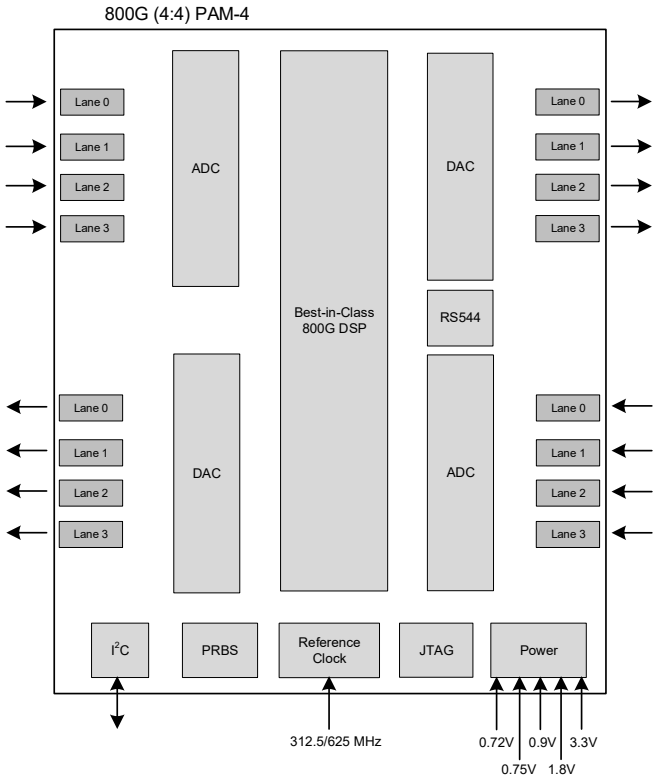
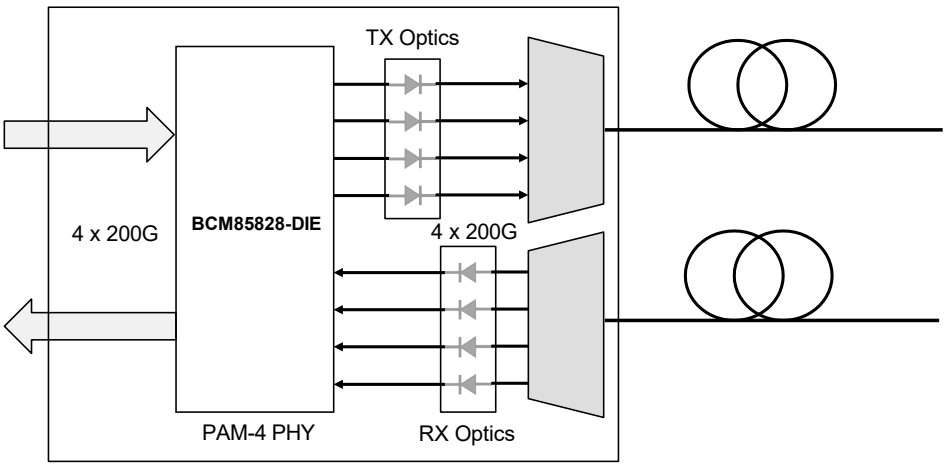


Figure 2: Application Diagram



For more product information: broadcom.com

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