BROADCOM®

Product Brief

BCM85822

5-nm CMOS 800G (8:4) PAM-4 Transceiver PHY with Integrated Laser Driver

Applications

- 1.6T OSFP-XD and 800G OSFP optical module deployments inside hyperscale data center
- 400G DR1.2
- 1.6T DR4.2

Overview

The Broadcom® BCM85822 is the industry's highest-performance and lowest-power 800GbE PAM-4 PHY transceiver capable of driving four lanes of 226-Gb/s PAM-4 at 113 Gbaud, while supporting 400G DR1.2 and 1.6T DR4.2.

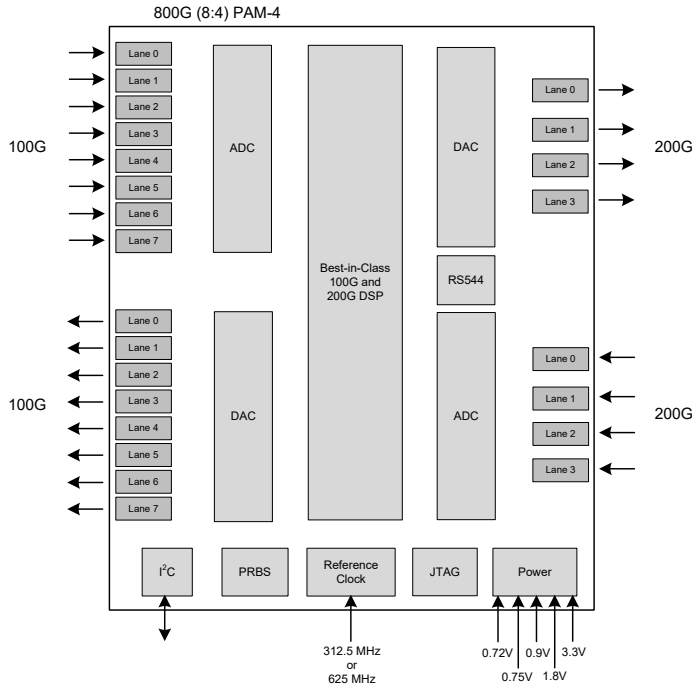
The BCM85822 leverages the market-leading 5-nm PAM-4 PHY transceiver technology platform, already proven with the BCM85812, and provides a path to accelerating 1.6T OSFP-XD optical module availability. The advanced Broadcom DSP technology and equalization techniques compensate for optical impairments while maintaining the world's lowest-power pluggable optical modules and co-packaged optical solutions to enable the deployment of 51.2-Tb/s and higher-density switch ASICs.

The BCM85822 incorporates a highly differentiated feature set, including integrated laser drivers, market-leading FEC capability options, and client-side switch ASIC SerDes interoperability to provide an unmatched competitive advantage to the market.

In 800GbE mode, the BCM85822 converts eight lanes of 106 Gb/s from the client side into four lanes of 226 Gb/s to drive next-generation high-density optical PAM-4 links inside OSFP-XD form-factor modules.

The BCM85822 also features crossbar on the client side for easier routing in the PCBs. The on-chip clock synthesis is performed by a low-cost 312.5-MHz or 625-MHz reference clock through high-frequency, low-jitter phase-locked loops.

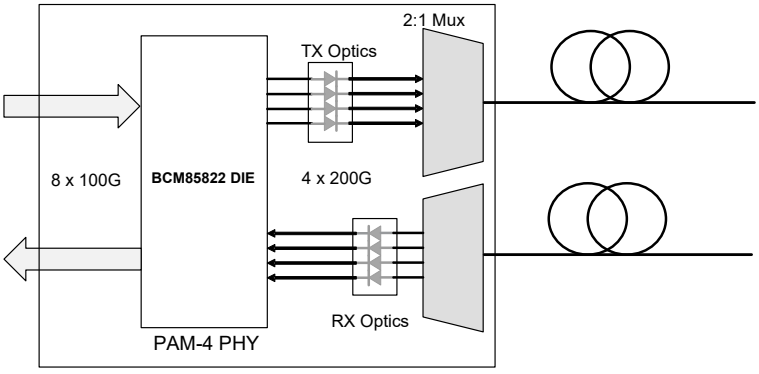
Block Diagram



Key Features

- Single-chip 4 × 200G PAM-4 PHY drives 800GbE over optics:
  - Client side: 8 × 106G PAM-4
  - Line side: 4 × 226G PAM-4 (128,120 inner code with 2-bit padding)
- Supports forward gearbox for backward compatibility with 400G optical modules:
  - Client side: 8 × 53G PAM-4
  - Line side: 4 × 106G PAM-4
- Supports client-side crossbar for flexible routing to various standards
- Supports 100G repeater mode
- Supports FEC monitoring in the repeater modes with a subsampling feature available for reduced power
- Supports FEC termination and generation
- Supports differential line-side output
- TX FIR support on both sides, line side (10 tap) and client side (7 tap)
- Client-side interface compliant with:
  - IEEE 802.3ck C2C (Annex 135F) specification supporting medium-reach channels
  - IEEE 802.3ck C2M (Annex 135G) specification supporting chip-to-module channels
  - CEI-112G-VSR/MR specification supporting shortreach (VSR) and medium-reach (MR) channels
- IEEE 802.3cd standard-compliant KP4 and end-to-end FEC bypass operation:
  - 800G/400G/200G/100G KP4 FEC
- Link-training support available on client side
- Line-side and client-side loopbacks
- Lowest-power 5-nm CMOS design
- Integrated AVS regulator
- Supports Direct-Drive with 1.5-Vpp single-ended or 3.0-Vpp differential line-side output

Application Diagram



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