BROADCOM

Product Brief

BCM85657

5-nm 16-Lane PCIe Gen5 and CXL 2.0 Retimer

Key Features

- Compatible with PCIe Gen5/Gen4/Gen3/Gen2/Gen1 and Compute Express Link (CXL 2.0) standards
- Operates at 32, 16, 8, 5, and 2.5 GT/s
- Supports parallel lane groupings per transfer:
  - Sixteen lanes can be statically configured as a selected subset of the following combinations:
  - One 16-lane link (1x 16)
  - Two 8-lane links (2x 8)
  - Four 4-lane links (4x 4)
  - Eight 2-lane links (8x 2)
- Supports low-latency mode
- Extends reach to >40 dB at 32 GT/s
- RX integrates multistage linear EQ and adaptive 16-tap DFE; TX uses 4-tap FIR taps
- Receiver is capable of operating at data rates with REFCLK, independent of transmitter
- Provides clock and data recovery (CDR) tolerance of spread inputs up to 6000 ppm relative to the reference clock
- Supports LT when connected with an LT-capable link partner

Overview

The Broadcom® BCM85657 is a 16-lane, low-power, low-latency, symmetrical PCIe Gen5, and CXL integrated MAC and PHY retimer. This device extends the reach between a root complex (RC) and endpoint (EP) by >40 dB of loss on both the sides at 32 GT/s. Each lane is capable of multiple data rates, including Gen5 (32G), Gen4 (16G), Gen3 (8G), Gen2 (4G), and Gen1 (2.5G). The bifurcation mux and MAC support groups of 1x 16 lanes, 4x 4 lanes, and 8x 2 lanes.

For a low-latency application, the user can bypass the mux and MAC. The data path goes directly from SerDes to SerDes.

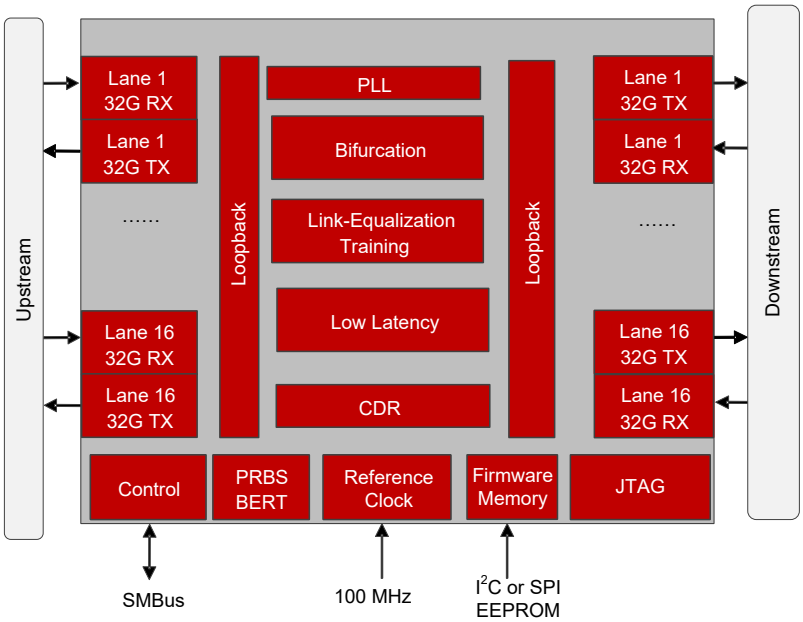
To compensate for link loss, the BCM85657 performs link training (LT) to automatically set the optimal TX-FIR settings.

The receiver features integrated and dynamic peaking filter, VGA, DFE, and CDR for signal recovery.

The BCM85657 uses a low-cost standard PCIe 100-MHz reference clock.

The pinout is compatible with the Intel PCIe 5.0 Retimer Supplemental Footprint, Revision 1.0.

Block Diagram



Applications

- HPC and AI servers for hyperscalers and data centers
- PCIe storage servers
- PCIe riser cards, interposer cards, and backplane

Key Features (cont.)

- Provides an adjustable loss-of-signal (LOS) detector
- Supports low-power modes
- Supports PCIe L0, L1, and L1 substates power modes
- Supports proprietary low-latency (LL) modes:
  - Intel proprietary inband LL entry and exit
  - Broadcom proprietary inband LL entry and exit
- CC, SRNS, and SRIS clock mechanism
- Receiver lane (eye) margining
- Receiver detect bypass
- Dynamic pseudo port and polarity orientation
- I^2C or SPI master for external EEPROM configuration
- Reference clock output
- Secured bootloader of firmware from the ROM
- Line-side and system-side loopbacks
- PRBS generator and checker
- Single low-cost reference clock input
- JTAG and embedded logic analyzer
- Interoperability with the Broadcom PCIe switches series switch/storage silicon
- Low-power 5-nm CMOS design
- Integrated AC-coupling on high-speed lanes
- Only three power supplies needed

Ordering Information

Part Number	Package	Ambient Temperature	Integrated AC-Capacitor Option
BCM85657A1IEFB1G	Industrial-rated A1 silicon, 8.9 mm × 22.8 mm, 354-ball BGA, RoHS-compliant	–40°C to 85°C	1
BCM85657A1IEFB2G	Industrial-rated A1 silicon, 8.9 mm × 22.8 mm, 354-ball BGA, RoHS-compliant	–40°C to 85°C	2

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For more product information: broadcom.com

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