BCM85344

Dual 800G MACsec/IPsec Retimer PHY

Key Features

- Supports IEEE 802.1AE (dataplane), IEEE 802.1X-2010 (MKA), IEEE 802.1AEbw, IEEE 802.1AEbn, including all cipher suites: GCM_AES_128/256 and GCM_AES_XPN_128/256
- Supports 25G/50G/100G/200G/400G/800G Ethernet applications
- Dual 800GbE port supports FR8, LR8 QSFP-DD, and OSFP retimer/equalization/MACsec/IPsec encryption
- Dual 400GbE port with CDAUI8-to-CDAUI8 port support FR8, LR8 QSFP-DD retimer/equalization MACsec encryption
- Dual 200GbE port with CDAUI4-to-CDAUI4 port support FR4, LR4 QSFP56 retimer/equalization/MACsec encryption
- Supports MACsec encryption in Reverse Gearbox mode:
  - 1 × 100G PAM-4 to 2 × 50G PAM-4
  - 2 × 50G PAM-4 to 4 × 25G NRZ
- Dual 100GbE channels with CAUI4-to-CAUI4 port support SR4/LR4/CR4 QSFP28 retimer/equalization/MACsec encryption
- Supports failover mux for both Retimer and Gearbox modes
- Supports IEEE 1588 timestamping with Synchronous Ethernet (SyncE) recovered clock outputs
- Supports FEC terminate/regenerate for all rates up to 800G
- MDC and MDIO host interface
- Integrated AC-coupling capacitors on all high-speed receivers on the line and system side
- Interoperates with Broadcom ASIC and merchant switch silicon

Overview

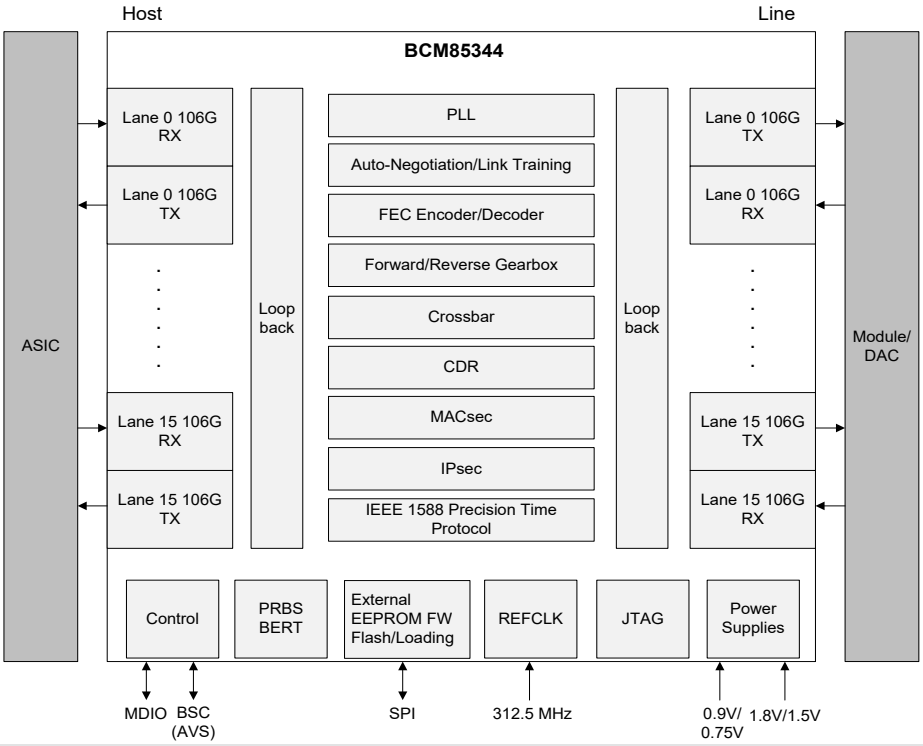
The Broadcom® BCM85344 is a 5-nm low-power, high-density PHY that integrates IEEE 801.1AE MACsec, IPsec GCM-AES-256b encryption, IEEE 1588, retimer, and equalizer functions.

The BCM85344 supports 800-Gigabit Ethernet (GbE), 400GbE, 200GbE, 100GbE, 50GbE, and 25GbE applications. The device also supports both PAM-4 and NRZ data formats as well as MACsec encryption in Reverse Gearbox mode.

The on-chip clock synthesis is performed by a single low-cost 312.5-MHz reference clock (for all IEEE standard 50G/100G/200G/400G/800G rates) through high-frequency, low-jitter, phase-locked loops (PLLs). Individual clock recovery is performed on the device by synchronizing directly to the respective incoming data streams.

The BCM85344 is designed in 5-nm CMOS technology to provide a low-power solution with integrated AC-coupling capacitors.

Block Diagram



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