Data Sheet

BCM81724

8 x 56 Gb/s PAM-4 to 16 x 25 Gb/s NRZ Forward and Reverse Gearbox with 8 x 56 Gb/s PAM-4 Pass-Through Mode PHY

Overview

The Broadcom® BCM81724 is a single-chip 8 × 56 Gb/s to 16 × 25 Gb/s NRZ forward and reverse gearbox with 8 × 56 Gb/s PAM-4 Pass-Through mode PHY. It supports both the PAM-4 and NRZ data formats. It supports Retimer, Forward, and Reverse Gearbox modes. It also supports 1G, 10G, 25G, 40G, 50G, 100G, 200G, and 400G line-card applications.

On-chip clock synthesis is performed by a low-cost 156.25-MHz reference clock through high-frequency, low-jitter phase-locked loops (PLLs).

The BCM81724 is fabricated in advanced low-power 16-nm CMOS technology.

The BCM81724 is available in a 19 mm × 19 mm, 0.8-mm pitch, 484-ball BGA, RoHS-compliant package.

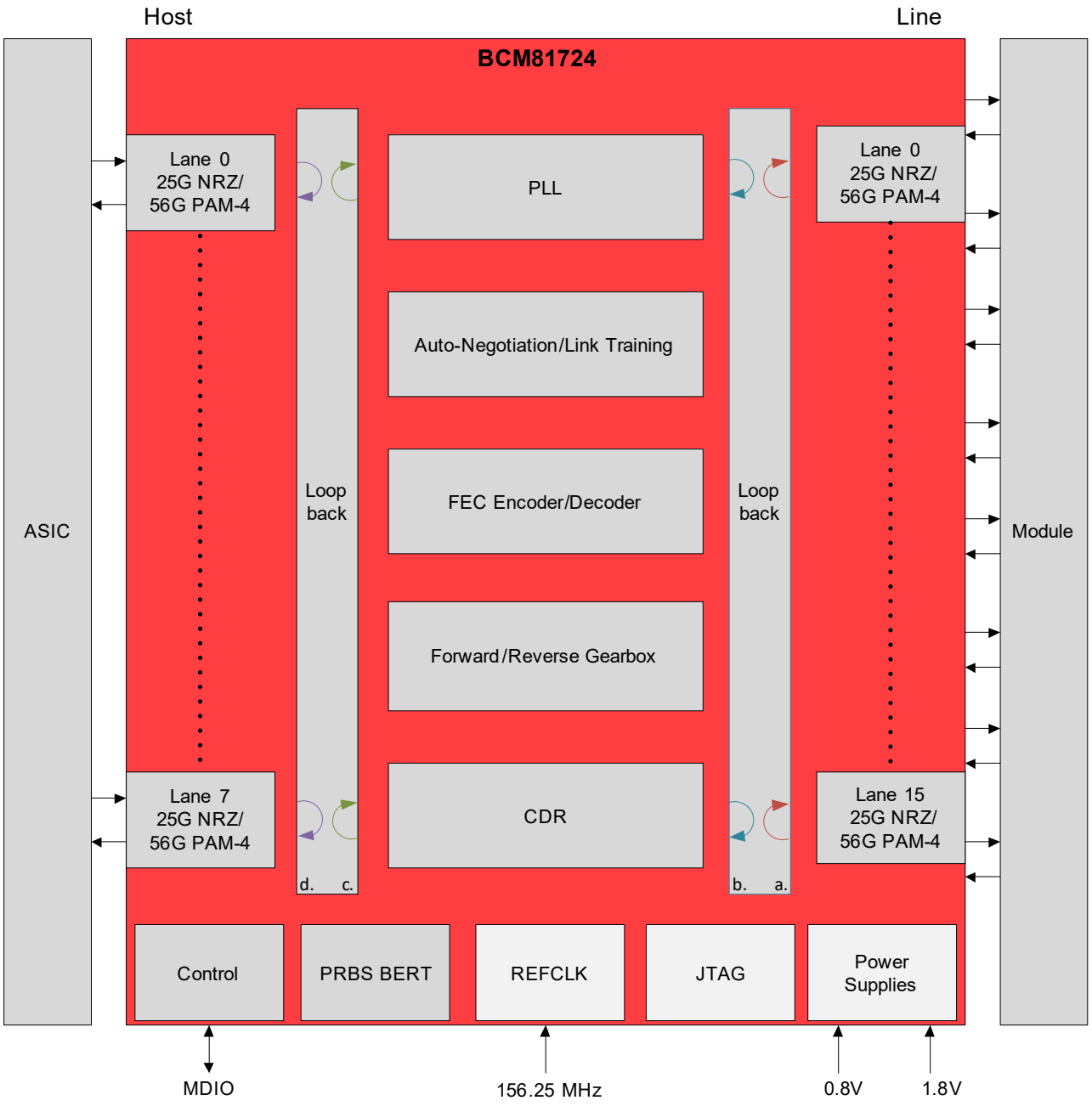
Applications

- ASIC-to-module interface 16 × 25 Gb/s front-panel application
- ASIC-to-module interface 8 × 56 Gb/s front-panel application
- High-density 10G, 25G, 40G, 50G, 100G, 200G, and 400G front-panel line-card applications

Features

- Host-side interface: 30 dB (both NRZ and PAM-4 modes)
- Line-side interface:
  - 35 dB (NRZ mode)
  - 20 dB (PAM-4 mode)
  - Chip-to-module (C2M) compliant
- Forward and Reverse Gearbox mode and Retimer mode
- Supports forward error correction (FEC)
- Supports CR mode in Reverse Gearbox mode
- Integrated AC-coupling capacitors on the system-side and line-side receivers
- Multiple standard and line rate support for both PAM-4 and NRZ
- Continuous auto-adaptive equalizer
- Line- and system-side loopbacks
- PRBS generator/error checker
- Eye monitoring per lane on the line side, accessed through MDIO
- SNR measurements per lane on the host side, accessed through MDIO
- Single low-cost REFCLK input
- Single-ended and differential recovered clock outputs
- Supports SGMII pass-through
- Interoperates with Broadcom ASIC and merchant switch silicon
- Low-power 16-nm CMOS design
- 19 mm × 19 mm BGA, 0.8-mm ball pitch package

Figure 1: BCM81724 Block Diagram for Reverse Gearbox and Retimer Modes



NOTE:

a. Line-side remote loopback (line-side shallow loopback).

b. Line-side digital loopback (acting host-side deep loopback).

c. Host-side digital loopback (acting line-side deep loopback).

d. Host-side remote loopback (host-side shallow loopback).

Loopbacks can be configured on a per-lane basis.

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Chapter 1: Functional Description

For the BCM81724, lane 0 and lane 1 are grouped together and share the same PLL. Although they share one PLL, lane 0 and lane 1 can operate at different frequencies with each using different OSR settings (1, 2, or 4). For example, when lane 0 is set to 25G, lane 1 can be set only to 25G, 12.5G, or 6.25G. The same is true for lane 2/lane 3, lane 4/lane 5, and lane 6/lane 7 pairs.

1.1 Reverse, Retimer, and Forward Gearbox Modes

Table 1 describes the Reverse, Retimer, and Forward Gearbox modes of the BCM81724.

Table 1: Reverse, Retimer, and Forward Gearbox Operating Modes for 400G Slice (Host-Side 8 × 50G/8 × 25G to Line-Side 8 × 50G/16 × 25G)

Operating Mode (Front-Panel Ports)	Logical Function (Per Port)	Host-Side SerDes Mode Per Port	FEC on Host ASIC	Line-Side SerDes Mode Per Port	FEC Required for Line Side	FEC Function Inside PHY
1 port of 400GbE	Reverse gearbox	400GAUI-8 (8 × 50G)	CL-119 FEC (RS-544 over 8 lanes)	400GAUI-16 (16 × 25G)	CL-119 FEC (RS-544 over 16 lanes)	Retiming (bit mux)
2 ports of 200GbE	Reverse gearbox	200GAUI-4 (4 × 50G)	CL-119 FEC (RS-544 over 4 lanes)	200GAUI-8 (8 × 25G)	CL-119 FEC (RS-544 over 8 lanes)	Retiming (bit mux)
4 ports of 100GbE	Reverse gearbox	100GAUI-2 (2 × 50G)	CL-91 FEC (RS-544 over 2 lanes)	CAUI-4 and 100GAUI-4 (4 × 25G) (optics) 100G-CR4 (4 × 25G) (copper) with AN/LT	No FEC/CL-91 FEC (RS-528)/CL-91 FEC (RS-544) over 4 lanes	Terminate CL-91 FEC (RS-544) from host side, and generate no FEC/CL-91 FEC (RS-528) for line side or retiming (bit mux)
8 ports of 50G/C	Reverse gearbox (50G Consortium)	50GAUI-1 (50G)	CL-134 (RS-544 over 1 lane)	LAUI-2 (2 × 25G) (optics) 50G-CR2 (2 × 25G) (copper) with AN/LT	No FEC/FC-FEC/ RS-528 over 2 lanes	Terminate CL-134 FEC from host side, and generate no FEC/FC-FEC/ RS-528 for line side
4 ports of 40GbE	Reverse gearbox	XLPPI-2 (22 × 20G)	(No FEC)	XLPPI-4 (4 × 10G) (optics) 40G-CR4 (4 × 10G) (copper) with AN/LT	(No FEC)	Retiming (bit mux)
1 port of 400GbE	Retimer	400GAUI-8 (8 × 50G)	CL-119 FEC (RS-544 over 8 lanes)	400GAUI-8 (8 × 50G) (optics) 400G (8 × 50G) (copper) with AN/LT	CL-119 FEC (RS-544 over 8 lanes)	Retiming

Table 1: Reverse, Retimer, and Forward Gearbox Operating Modes for 400G Slice (Host-Side 8 × 50G/8 × 25G to Line-Side 8 × 50G/16 × 25G) (Continued)

Operating Mode (Front-Panel Ports)	Logical Function (Per Port)	Host-Side SerDes Mode Per Port	FEC on Host ASIC	Line-Side SerDes Mode Per Port	FEC Required for Line Side	FEC Function Inside PHY
2 ports of 200GbE	Retimer	200GAUI-4 (4 × 50G)	CL-119 FEC (RS-544 over 4 lanes)	200GAUI-4 (4 × 50G) (optics) 200G (4 × 50G) (copper) with AN/LT	CL-119 FEC (RS-544 over 4 lanes)	Retiming or RS544 FEC terminate and regenerate
1 port of 200GbE	Retimer	200GAUI-8 (8 × 25G)	CL-119 FEC (RS-544 over 8 lanes)	200GAUI-8 (8 × 25G) (optics)	CL-119 FEC (RS-544 over 8 lanes)	Retiming
4 ports of 100GbE	Retimer	100GAUI-2 (2 × 50G)	CL-91 FEC (RS-544 over 2 lanes)	100GAUI-2 (2 × 50G) (optics) 100G (2 × 50G) (copper) with AN/LT	CL-91 FEC (RS-544 over 2 lanes)	Retiming or RS544 FEC terminate and regenerate
2 ports of 100GbE	Retimer	CAUI-4 and 100GAUI-4 (4 × 25G)	No FEC/CL-91 FEC (RS-528)/CL-91 FEC (RS-544), over 4 lanes	CAUI-4 and 100GAUI-4 (4 × 25G) (optics) 100G (4 × 25G) (copper) with AN/LT	No FEC/CL-91 FEC (RS-528)/CL-91 FEC (RS-544) over 4 lanes	Retiming
2 ports of 40GbE	Retimer	XLPPI-4 (4 × 10G)	(No FEC)	XLPPI-4 (4 × 10G) (optics) 40G (4 × 10G) (copper) with AN/LT	(No FEC)	Retiming
8 ports of 50GbE	Retimer	50GAUI-1 (50G)	CL-134 (RS-544 over 1 lane)	50GAUI-1 (optics) 50G (copper) with AN/LT	CL-134 (RS-544 over 1 lane)	Retiming or RS544 FEC terminate and regenerate
4 ports of 50G/C	Retimer (50G Consortium)	LAUI-2 (2 × 25G)	No FEC/FC-FEC/RS-FEC over 2 lanes	LAUI-2 (2 × 25G) (optics) 50G (2 × 25G) (copper) with AN/LT	No FEC/FC-FEC/ RS-FEC over 2 lanes	Retiming
8 ports of 25GbE	Retimer (IEEE and Consortium)	25GAUI (25G)	No FEC/FC-FEC/RS-FEC over 1 lane	25GAUI (optics) 25G (copper) with AN/LT	No FEC/FC-FEC/ RS-FEC over 1 lane	Retiming
8 ports of 10GbE	Retimer	SFI (10G)	(No FEC)	10G SFI (optics) 10G SFI (copper)	(No FEC)	Retiming
1 port of 400GbE	Forward gearbox	400GAUI-16 (16 × 25G)	CL-119 FEC (RS-544 over 16 lanes)	400GAUI-8 (8 × 50G)	CL-119 FEC (RS-544 over 8 lanes)	Retiming (bit mux)
2 ports of 200GbE	Forward gearbox	200GAUI-8 (8 × 25G)	CL-119 FEC (RS-544 over 8 lanes)	200GAUI-4 (4 × 50G)	CL-119 FEC (RS-544 over 4 lanes)	Retiming (bit mux)

Table 1: Reverse, Retimer, and Forward Gearbox Operating Modes for 400G Slice (Host-Side 8 × 50G/8 × 25G to Line-Side 8 × 50G/16 × 25G) (Continued)

Operating Mode (Front-Panel Ports)	Logical Function (Per Port)	Host-Side SerDes Mode Per Port	FEC on Host ASIC	Line-Side SerDes Mode Per Port	FEC Required for Line Side	FEC Function Inside PHY
4 ports of 100GbE	Forward gearbox	CAUI-4 and 100GAUI-4 (4 × 25G) (optics)	No FEC/CL-91 FEC (RS-528)/CL-91 FEC (RS-544) over 4 lanes	100GAUI-2 (2 × 50G)	CL-91 FEC (RS-544 over 2 lanes)	Terminate CL-91 FEC (RS-544) from host side, and generate no FEC/CL-91 FEC (RS-528) for line side or retiming (bit mux)
				100G (4 × 25G) (copper) with AN/LT		
8 ports of 50GbE	Forward gearbox (50G Consortium)	LAUI-2 (2 × 25G) (optics)	No FEC/FC-FEC/ RS-528 over 2 lanes	50GAUI-1 (50G)	CL-134 (RS-544 over 1 lane)	Terminate CL-134 FEC from host side, and generate no FEC/FC-FEC/ RS-528 for line side
				50G (2 × 25G) (copper) with AN/LT		
4 ports of 40GbE	Forward gearbox	XLPPI-4 (4 × 10G) (optics)	(No FEC)	XLPPI-2 (22 × 20G)	(No FEC)	Retiming (bit mux)
				40G (4 × 10G) (copper) with AN/LT		

Table 2 and Table 3 show the SerDes mapping of the BCM81724 working as Reverse Gearbox, Retimer, and Gearbox modes.

Table 2: SerDes Mapping, Reverse Gearbox Mode

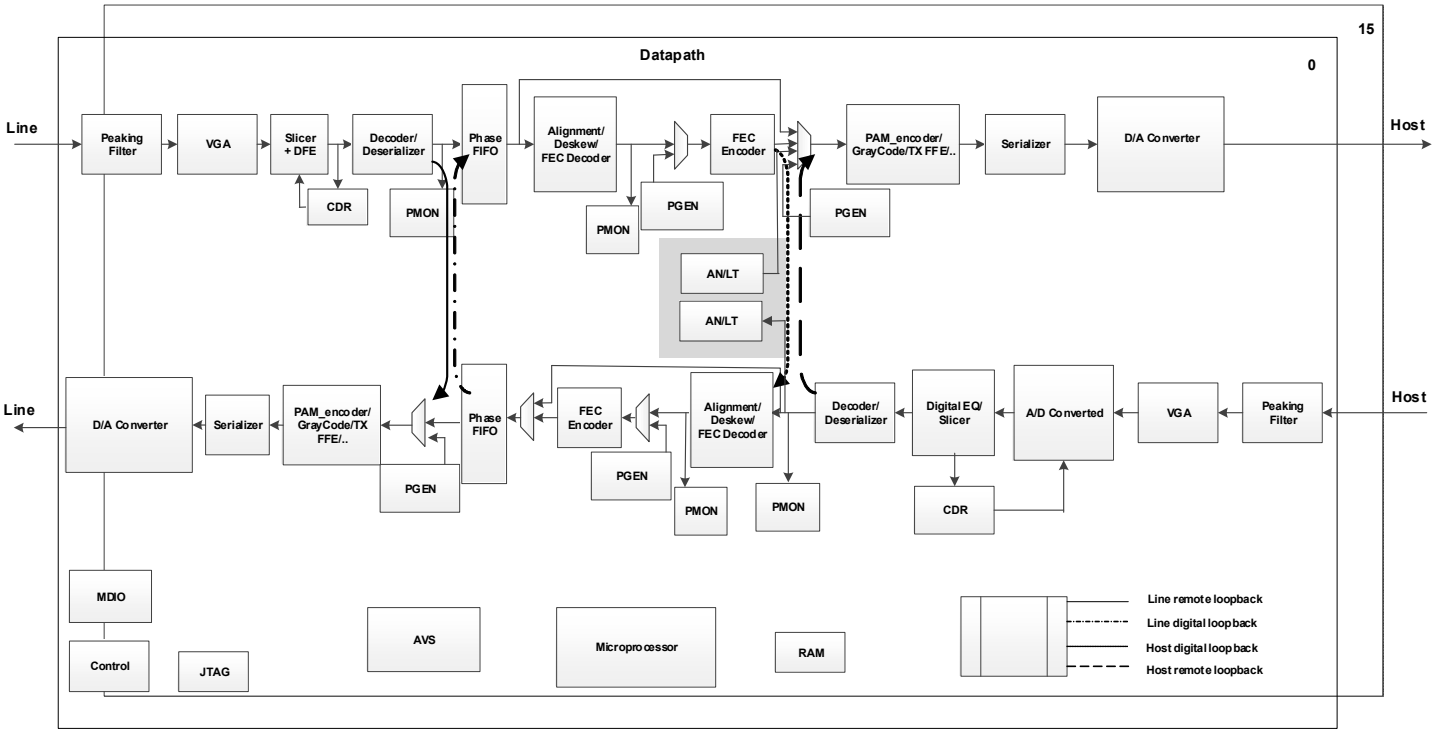
Operating Mode (Front-Panel Ports)	Logical Function (Per Port)	Port Number	Host-Side SerDes Lanes	Line-Side SerDes Lanes
1 port of 400GbE	Reverse gearbox (PAM-4 to NRZ)	Port 1	H0 to H7	L0 to L15
2 ports of 200GbE	Reverse gearbox (PAM-4 to NRZ)	Port 1	H0 to H3	L0 to L7
		Port 2	H4 to H7	L8 to L15
4 ports of 100GbE	Reverse gearbox (PAM-4 to NRZ)	Port 1	H0 to H1	L0 to L3
		Port 2	H2 to H3	L4 to L7
		Port 3	H4 to H5	L8 to L11
		Port 4	H6 to H7	L12 to L15
8 ports of 50G/C	Reverse gearbox (PAM-4 to NRZ)	Port 1	H0	L0 to L1
		Port 2	H1	L2 to L3
		Port 3	H2	L4 to L5
		Port 4	H3	L6 to L7
		Port 5	H4	L8 to L9
		Port 6	H5	L10 to L11
		Port 7	H6	L12 to L13
		Port 8	H7	L14 to L15
4 ports of 40GbE	Reverse gearbox (NRZ to NRZ)	Port 1	H0 to H1	L0 to L3
		Port 2	H2 to H3	L4 to L7
		Port 3	H4 to H5	L8 to L11
		Port 4	H6 to H7	L12 to L15
1 port of 400GbE	Retimer (PAM-4 to PAM-4)	Port 1	H0 to H7	L8 to L15
2 ports of 200GbE	Retimer (PAM-4 to PAM-4)	Port 1	H0 to H3	L0 to L3
		Port 2	H4 to H7	L8 to L11
1 port of 200GbE	Retimer (NRZ to NRZ)	Port 1	H0 to H7	L0 to L3 and L8 to L11
4 ports of 100GbE	Retimer (PAM-4 to PAM-4)	Port 1	H0 to H1	L0 to L1
		Port 2	H2 to H3	L2 to L3
		Port 3	H4 to H5	L8 to L9
		Port 4	H6 to H7	L10 to L11
2 ports of 100GbE	Retimer (NRZ to NRZ)	Port 1	H0 to H3	L0 to L3
		Port 2	H4 to H7	L8 to L11
2 ports of 40GbE	Retimer (NRZ to NRZ)	Port 1	H0 to H3	L0 to L3
		Port 2	H4 to H7	L8 to L11
8 ports of 50GbE	Retimer (PAM-4 to PAM-4)	Ports 1 to 8	H0 to H7	L0 to L3 and L8 to L11
4 ports of 50G/C	Retimer (NRZ to NRZ)	Port 1	H0 to H1	L0 to L1
		Port 2	H2 to H3	L2 to L3
		Port 3	H4 to H5	L8 to L9
		Port 4	H6 to H7	L10 to L11
8 ports of 25GbE	Retimer (NRZ to NRZ)	Ports 1 to 8	H0 to H7	L0 to L3 and L8 to L11
8 ports of 10GbE	Retimer (NRZ to NRZ)	Ports 1 to 8	H0 to H7	L0 to L3 and L8 to L11

Table 3: SerDes Mapping, Forward Gearbox Mode

Operating Mode (Front-Panel Ports)	Logical Function (Per Port)	Port Number	Host-Side SerDes Lanes	Line-Side SerDes Lanes
1 port of 400GbE	Forward gearbox (NRZ to PAM-4)	Port 1	L0 to L15	H0 to H7
2 ports of 200GbE	Forward gearbox (NRZ to PAM-4)	Port 1	L0 to L7	H0 to H3
		Port 2	L8 to L15	H4 to H7
4 ports of 100GbE	Forward gearbox (NRZ to PAM-4)	Port 1	L0 to L3	H0 to H1
		Port 2	L4 to L7	H2 to H3
		Port 3	L8 to L11	H4 to H5
		Port 4	L12 to L15	H6 to H7
8 ports of 50GbE	Forward gearbox (NRZ to PAM-4)	Port 1	L0 to L1	H0
		Port 2	L2 to L3	H1
		Port 3	L4 to L5	H2
		Port 4	L6 to L7	H3
		Port 5	L8 to L9	H4
		Port 6	L10 to L11	H5
		Port 7	L12 to L13	H6
		Port 8	L14 to L15	H7
4 ports of 40GbE	Forward gearbox (NRZ to PAM-4)	Port 1	L0 to L3	H0 to H1
		Port 2	L4 to L7	H2 to H3
		Port 3	L8 to L11	H4 to H5
		Port 4	L12 to L15	H6 to H7
1 port of 400GbE	Retimer (PAM-4 to PAM-4)	Port 1	H0 to H7	L8 to L15
2 ports of 200GbE	Retimer (PAM-4 to PAM-4)	Port 1	L0 to L3	H0 to H3
		Port 2	L8 to L11	H4 to H7
1 port of 200GbE	Retimer (NRZ to NRZ)	Port 1	L0 to L3 and L8 to L11	H0 to H7
4 ports of 100GbE	Retimer (PAM-4 to PAM-4)	Port 1	L0 to L1	H0 to H1
		Port 2	L2 to L3	H2 to H3
		Port 3	L8 to L9	H4 to H5
		Port 4	L10 to L11	H6 to H7
2 ports of 100GbE	Retimer (NRZ to NRZ)	Port 1	L0 to L3	H0 to H3
		Port 2	L8 to L11	H4 to H7
2 ports of 40GbE	Retimer (NRZ to NRZ)	Port 1	L0 to L3	H0 to H3
		Port 2	L8 to L11	H4 to H7
8 ports of 50GbE	Retimer (PAM-4 to PAM-4)	Ports 1 to 8	L0 to L3 and L8 to L11	H0 to H7
4 ports of 50G/C	Retimer (NRZ to NRZ)	Port 1	L0 to L1	H0 to H1
		Port 2	L2 to L3	H2 to H3
		Port 3	L8 to L9	H4 to H5
		Port 4	L10 to L11	H6 to H7
8 ports of 25GbE	Retimer (NRZ to NRZ)	Ports 1 to 8	L0 to L3 and L8 to L11	H0 to H7
8 ports of 10GbE	Retimer (NRZ to NRZ)	Ports 1 to 8	L0 to L3 and L8 to L11	H0 to H7

Figure 2 shows the detailed block diagram of the BCM81724.

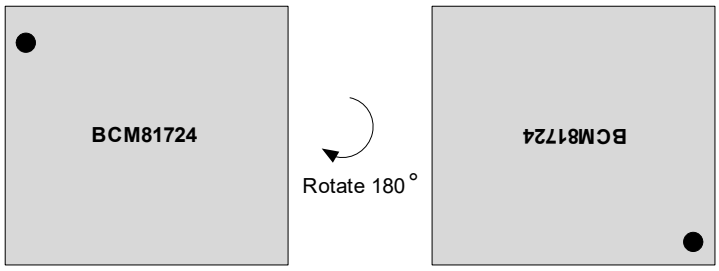
Figure 2: Detailed Block Diagram



1.2 Device Functions

The BCM81724 can function as a reverse gearbox or a forward gearbox. To operate in the Reverse Gearbox mode, use the device as is. To operate in the Forward Gearbox mode, the chip must be physically rotated by 180 degrees as shown in Figure 3.

Figure 3: Reverse Gearbox Mode to Forward Gearbox Mode



Reverse Gearbox Mode Forward Gearbox Mode

In the BCM81724, lane 0 and lane 1 are grouped together and share the same PLL. Although they share one PLL, lane 0 and lane 1 can operate at different frequencies with each using different OSR settings (1, 2, or 4). For example, when lane 0 is set to 25G, lane 1 can be set only to 25G, 12.5G, or 6.25G. The same is true for the lane 2/lane 3, lane 4/lane 5, and lane 6/lane 7 pairs.

In all operating modes, the transmitter clock frequency is locked to the opposite side recovered clock frequency. For example, the system-side transmitter clock frequency is locked to the line-side recovered clock frequency, and the line-side transmitter clock frequency is locked to the system-side recovered clock frequency.

NOTE: The lane-swap feature is not available on the BCM81724. However, P/N polarity swaps are available on both the system-side and line-side transmitter and receiver paths to help with PCB routing.

1.2.1 Host-Side Interface

The host-side interface receiver is a high-performance, ADC-based digital equalizer, which includes an analog peaking filter (PF) and a variable gain amplifier (VGA) in analog front end as well as a high-performance analog-to-digital converter (ADC) with digital equalizer of feed-forward equalizer (FFE) and a clock and data recovery (CDR) circuitry.

The analog PF, enabled by a programmable continuous-time linear equalizer (CTLE), provides first-order equalization by boosting the high-frequency content to compensate for the intersymbol interference (ISI) on the incoming data. The peak of the peaking filter can be adjusted by the registers for various backplane channel characteristics. After the analog PF, the signal is further enhanced through a VGA, and the gain is automatically controlled by a gain control loop for best ADC performance.

A high-performance ADC is implemented after the PF and VGA stages. The incoming data is sampled at baud rate, and the digitalized samples are subsequently postprocessed by the digital equalizer (EQ) prior to slicing. The digital equalizer has a multiple-taps baud rate FFE, which equalizes the sampled signal. The equalizer is continuously adapted to the incoming signal variation with the least mean squared (LMS) algorithm.

The timing recovery block recovers both the phase and frequency of the incoming data stream. Further, it determines the optimal sampling phase for obtaining the best-recovered signal after equalization. Data is determined at the slicer with optimal timing by a fully adapted timing recovery block. All RX EQ and analog parameters are automatically configured and adapted for best CDR and EQ operation using a combination of hardware and firmware running in a microcontroller.

There is an integrated on-die AC-coupling capacitor on the host-side receiver (see Section 2.1, Functional Ball Descriptions, for the common-mode and maximum peaking voltage restrictions).

The host-side interface can support backplane channels with 30-dB insertion loss (in Nyquist frequency). The transmitters are based on a high-resolution digital-to-analog converter (DAC) and are compliant to the CEI-28G/56G-LR specifications. The TX equalization is provided by a conventional multiple-tap TXFIR structure.

Host-side interfaces have a pseudorandom bit sequence (PRBS) generator as well as checker capability.

1.2.2 Line-Side Interface

The analog PF, enabled by a programmable continuous-time linear equalizer (CTLE), provides first-order equalization by boosting the high-frequency content to compensate for the intersymbol interference (ISI) on the incoming data. The peak of the peaking filter can be adjusted by the registers for various backplane channel characteristics. After the analog PF, the signal is further enhanced through a VGA, and the gain is automatically controlled by a gain control loop for best ADC performance.

A multitap decision feedback equalizer (DFE)/timing recovery is implemented after the PF and VGA stages, where it continuously adapts to the incoming signal with the least mean squared (LMS) algorithm, and together with a CDR block, recover both the phase and frequency of the incoming data stream and determine the optimal sampling phase for obtaining the best-recovered signal after equalization.

The line-side interface receiver is an analog equalizer, including a PF, a VGA, and a multiple-tap decision feedback equalizer (DFE) with a CDR circuit synchronizing the receiver with the incoming data stream.

There is an integrated on-die AC-coupling capacitor on the line-side receiver (see Section 2.1, Functional Ball Descriptions, for the common-mode and maximum peaking voltage restrictions). The line-side interface is compliant to the CEI-28G/56G-LR specifications and can support long-reach (LR) 35-dB insertion loss (at Nyquist frequencies) in NRZ mode and 20-dB insertion loss (at Nyquist frequencies) in PAM-4 mode.

The line-side interface transmitters are based on a high-resolution digital-to-analog converter (DAC) and are compliant to the CEI-28G/56G-LR specifications. The TX equalization is provided by a conventional multiple-tap TXFIR structure.

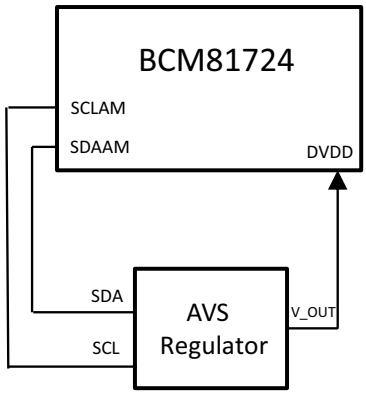
Line-side interfaces have a pseudorandom bit sequence (PRBS) generator as well as checker capability.

1.3 Adaptive Voltage Scaling

The BCM81724 implements Broadcom Serial Control (BSC) interface to achieve lower digital power consumption through adaptive voltage scaling (AVS). The BSC master interface is compatible with the I^2C standard. The hardware configuration (as shown in Figure 4) is realized by connecting an AVS voltage regulator, with a slave I^2C-compatible port, to the BCM81724 master BSC pins (SCLAM, SDAAM), and by connecting the output of the AVS regulator to the BCM81724 DVDD power rail. The AVS process is controlled automatically by the firmware, where the AVS algorithm is part of firmware and, when enabled, the firmware controls the AVS regulator's output voltage to adapt to the lowest DVDD voltage possible, at chip live operating condition, while still ensuring proper chip operation. The lowest digital power consumption is achieved by maintaining the lowest DVDD voltage possible at live chip operating condition.

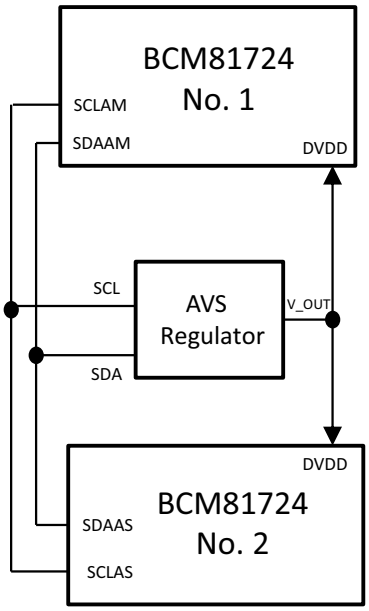
NOTE: The BSC is I^2C compliant and supports both standard I^2C mode (100 kHz) and fast I^2C mode (400 kHz).

Figure 4: AVS Configuration (One Regulator for One Package)



Multiple packages can share one AVS regulator. The configuration example where one regulator is shared by two packages is shown in Figure 5. The BCM81724 no. 1 is the master package that controls both the AVS regulator and the BCM81724 no. 2, where the BCM81724 no. 2 slave AVS BSC port should be connected to the AVS master BSC ports of the BCM81724 no. 1.

Figure 5: AVS Configuration (One Regulator for Two Packages)



For optimized power, Broadcom recommends connecting one AVS regulator per BCM81724 device. When more than one BCM81724 devices are connected to an AVS regulator, the power savings are less optimal because the power consumed by each BCM81724 device is dictated by the maximum power consumed by the most power hungry device.

NOTE: AVS requires an update every 1 second. Ensure you can meet this requirement when controlling AVS with an external FPGA or CPU.

1.4 Loss of Signal and Signal Detector

The BCM81724 contains a loss-of-signal (LOS) detect circuit that monitors the energy of the receiving signal. A peak detector looks for a minimum amplitude swing. The LOS status is observable in the RX status register.

Whenever there is there is an LOS detected on the line-side RX, the host-side TX is squelched. Similarly, whenever there is an LOS detected on the host-side RX, the line-side TX is squelched.

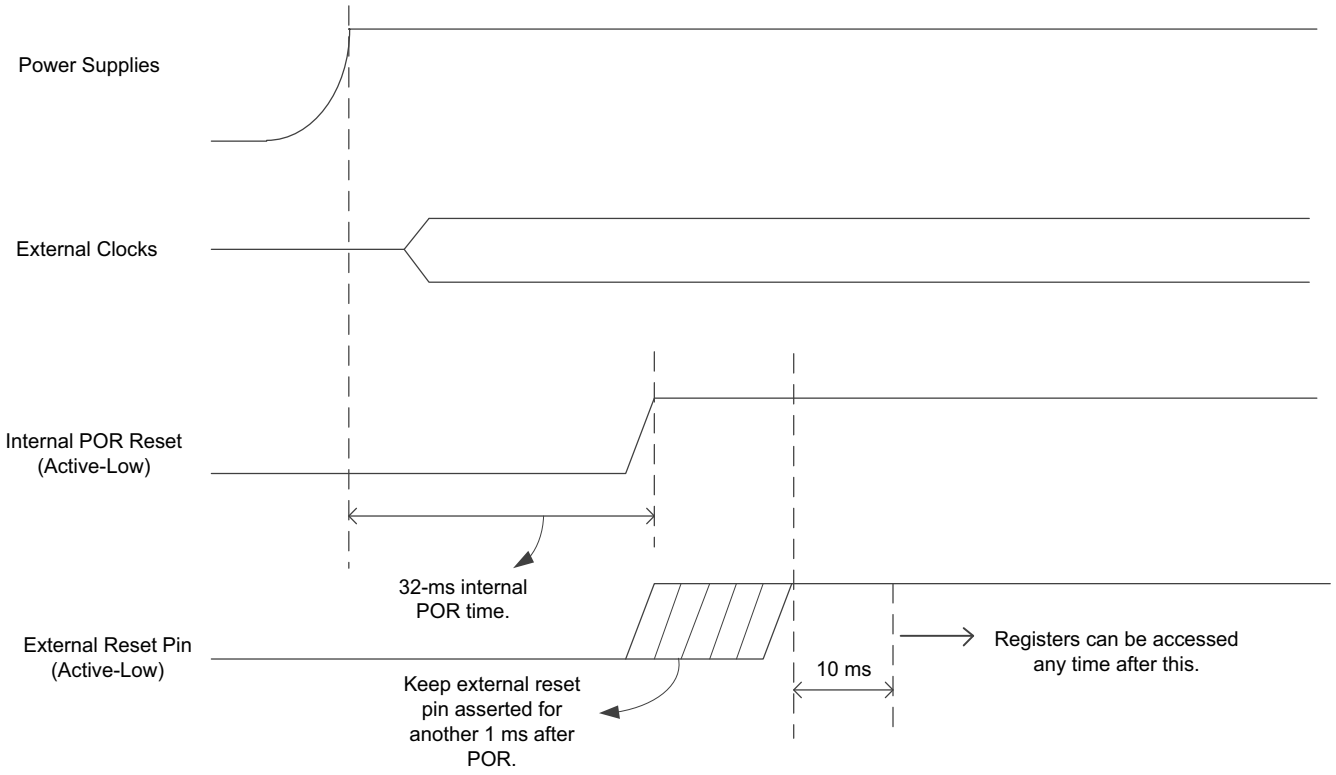
1.5 Reset

The RESET_L is a global hardware reset pin that is used to clear the entire chip, including all registers and data path. The RESET_L pin has an internal pull-up resistor to VDDIO. The reset timing diagram is shown in Figure 6.

The RESET_L pins must be held low for at least 1 ms after internal POR release. The management interface requires 10 ms after the application of the reset to be in the ready state.

NOTE: The RESET_L pins must be held low until the power rails and reference clock become ready.

Figure 6: Reset Timing Diagram



1.6 Microcode Loading

The microcode (or firmware) must be loaded into the microcontroller's RAM for PHY's operation. The microcode download is possible using one of the following methods:

- Downloading the microcode from the external SPI-ROM.
- Downloading the microcode directly over the management interface (MDIO).

It is also possible to program the external SPI-ROM over the MDIO with updated microcode.

External 24-bit addressing, 256-KB SPI-EEPROM, is used to store the microcode. The microcode is automatically downloaded from the SPI-EEPROM, through the SCK, SS_N, MOSI, and MISO pins, into the PHY's microcontrollers RAM when the PHY comes out of reset.

Chapter 2: Ball Assignments and Descriptions

2.1 Functional Ball Descriptions

Table 4: I/O Pin Functional Descriptions

Ball Number	Ball Name	Ball Type	Level	Description
L1	MRX_0P	I	Differential input Internal AC capacitor	Line port 0 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
M1	MRX_0N			
M3	MRX_1P	I	Differential input Internal AC capacitor	Line port 1 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
N3	MRX_1N			
R3	MRX_2P	I	Differential input Internal AC capacitor	Line port 2 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
T3	MRX_2N			
V3	MRX_3P	I	Differential input Internal AC capacitor	Line port 3 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W3	MRX_3N			
V5	MRX_4P	I	Differential input Internal AC capacitor	Line port 4 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W5	MRX_4N			
V7	MRX_5P	I	Differential input Internal AC capacitor	Line port 5 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W7	MRX_5N			
V9	MRX_6P	I	Differential input Internal AC capacitor	Line port 6 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W9	MRX_6N			
V11	MRX_7P	I	Differential input Internal AC capacitor	Line port 7 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W11	MRX_7N			
V13	MRX_8P	I	Differential input Internal AC capacitor	Line port 8 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W13	MRX_8N			
V15	MRX_9P	I	Differential input Internal AC capacitor	Line port 9 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W15	MRX_9N			
V17	MRX_10P	I	Differential input Internal AC capacitor	Line port 10 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W17	MRX_10N			
W19	MRX_11P	I	Differential input Internal AC capacitor	Line port 11 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W20	MRX_11N			
U19	MRX_12P	I	Differential input Internal AC capacitor	Line port 12 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
U20	MRX_12N			
R19	MRX_13P	I	Differential input Internal AC capacitor	Line port 13 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
R20	MRX_13N			

Table 4: I/O Pin Functional Descriptions (Continued)

Ball Number	Ball Name	Ball Type	Level	Description
M19	MRX_14P	I	Differential input Internal AC capacitor	Line port 14 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
N19	MRX_14N			
L21	MRX_15P	I	Differential input Internal AC capacitor	Line port 15 ingress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
L22	MRX_15N			
P1	MTX_0P	O	Differential output	Line port 0 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
R1	MTX_0N			
U1	MTX_1P	O	Differential output	Line port 1 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
V1	MTX_1N			
Y1	MTX_2P	O	Differential output	Line port 2 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AA1	MTX_2N			
AA3	MTX_3P	O	Differential output	Line port 3 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB3	MTX_3N			
AA5	MTX_4P	O	Differential output	Line port 4 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB5	MTX_4N			
AA7	MTX_5P	O	Differential output	Line port 5 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB7	MTX_5N			
AA9	MTX_6P	O	Differential output	Line port 6 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB9	MTX_6N			
AA11	MTX_7P	O	Differential output	Line port 7 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB11	MTX_7N			
AA13	MTX_8P	O	Differential output	Line port 8 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB13	MTX_8N			
AA15	MTX_9P	O	Differential output	Line port 9 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB15	MTX_9N			
AA17	MTX_10P	O	Differential output	Line port 10 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB17	MTX_10N			
AA19	MTX_11P	O	Differential output	Line port 11 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB19	MTX_11N			
AA21	MTX_12P	O	Differential output	Line port 12 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
AB21	MTX_12N			
V22	MTX_13P	O	Differential output	Line port 13 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
W22	MTX_13N			

Table 4: I/O Pin Functional Descriptions (Continued)

Ball Number	Ball Name	Ball Type	Level	Description
R22	MTX_14P	O	Differential output	Line port 14 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
T22	MTX_14N			
N21	MTX_15P	O	Differential output	Line port 15 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
N22	MTX_15N			
E1	HRX_0P	I	Differential input Internal AC capacitor	Host-side port 0 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
F1	HRX_0N			
C4	HRX_1P	I	Differential input Internal AC capacitor	Host-side port 1 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
C3	HRX_1N			
C7	HRX_2P	I	Differential input Internal AC capacitor	Host-side port 2 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
C6	HRX_2N			
C10	HRX_3P	I	Differential input Internal AC capacitor	Host-side port 3 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
C9	HRX_3N			
C13	HRX_4P	I	Differential input Internal AC capacitor	Host-side port 4 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
C12	HRX_4N			
C16	HRX_5P	I	Differential input Internal AC capacitor	Host-side port 5 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
C15	HRX_5N			
C19	HRX_6P	I	Differential input Internal AC capacitor	Host-side port 6 egress serial data input at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
C18	HRX_6N			
D22	HRX_7P	I	Differential input Internal AC capacitor	Host-side port 7 egress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
E22	HRX_7N			
B1	HTX_0P	O	Differential output	Host-side port 0 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
C1	HTX_0N			
A4	HTX_1P	O	Differential output	Host-side port 1 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
A3	HTX_1N			
A7	HTX_2P	O	Differential output	Host-side port 2 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
A6	HTX_2N			
A10	HTX_3P	O	Differential output	Host-side port 3 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
A9	HTX_3N			
A13	HTX_4P	O	Differential output	Host-side port 4 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
A12	HTX_4N			
A16	HTX_5P	O	Differential output	Host-side port 5 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
A15	HTX_5N			

Table 4: I/O Pin Functional Descriptions (Continued)

Ball Number	Ball Name	Ball Type	Level	Description
A19	HTX_6P	O	Differential output	Host-side port 6 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
A18	HTX_6N			
A21	HTX_7P	O	Differential output	Host-side port 7 ingress serial data output at 56-Gb/s PAM-4 or 25-Gb/s NRZ based on the mode configuration.
B21	HTX_7N			
H1	REF_CLK_P	I	Differential Input 100Ω differential External AC-coupling required	Reference Clock Input. Used as reference for the internal clock frequency synthesizer. Biased with internal differential 100Ω termination. Frequency must be 156.25 MHz. See Chapter 6, Reference Clock.
J1	REF_CLK_N			
G12	REF_SEL1	I	1.8V internal pull-down	Reference Clock Select. Default value to use the 156.25-MHz reference clock: ■ REF_SEL1 = 0 ■ REF_SEL0 = 0 See Chapter 6, Reference Clock.
G6	REF_SEL0			
J21	CLK_OUT_DIFF_P	O	Differential output	High-Speed Differential Recovered Clock Output. This clock can be used for Synchronous Ethernet. Externally AC-coupled. Needs external clock cleanup. See Chapter 7, Recovered Clock.
J22	CLK_OUT_DIFF_N			
J4	RCLK0	O	1.8V	Low-Speed Single-Ended Recovered Clock Output. This clock can be used for Synchronous Ethernet. Needs external clock cleanup. See Chapter 7, Recovered Clock.
K4	RCLK1			
N5	RESET_N	I	1.8V Schmitt trigger Internal pull-up	PHY Reset Input. Active-low. A minimum low period of 1 ms is required. Applied during and after power-up to initialize and to synchronize the SPI download.
H14	MDC	I	1.8V Schmitt trigger	Management Data Clock. MDIO data is centered on the rising edge of the clock signal MDC.
J17	MDIO	I/O	1.8V open-drain	Management Data Input/Output for MDIO Slave. Data written into the chip on rising edge of MDC. Chip transitions its output on rising edge of MDC when driving MDIO. A pull-up resistor is required on this pin.
M7	PRTAD4	I	1.8V internal pull-down	Port Address 4:2. MSB of MDIO port address [4:0]. Bits 1:0 are hardwired internally.
M13	PRTAD3			
M9	PRTAD2			
H6	SCLAS	I/O	1.8V	BSC Slave Serial Clock Input. For AVS support only. BSC is I^2C compliant.
M5	SDAAS	I/O	1.8V open-drain External pull-up required	BSC Slave Serial Data Input/Output. Open-drain output. For AVS support only. BSC is I^2C compliant.

Table 4: I/O Pin Functional Descriptions (Continued)

Ball Number	Ball Name	Ball Type	Level	Description
H12	SCLAM	I/O	1.8V open-drain External pull-up required	BSC Master Serial Clock Output. For AVS support only.
H11	SDAAM	I/O	1.8V open-drain External pull-up required	BSC Master Serial Data Input/Output. For AVS support only. BSC is I^2C compliant.
H13	INTR_N	O	1.8V	Open-drain output for interrupts is in the chip. Requires an external pull-up resistor.
H9	SCK	O	1.8V	SPI Serial Clock Output to SPI ROM Slave. Control register available for 2 mA/4 mA/6 mA/8 mA/10 mA/12 mA/14 mA/16 mA current strength.
M6	SS_N	O	1.8V	SPI Chip Select Output to SPI ROM Slave. Control register available for 2 mA/4 mA/6 mA/8 mA/10 mA/12 mA/14 mA/16 mA current strength.
H7	MISO	I	1.8V	SPI Master Data Input from SPI ROM Slave Output.
H8	MOSI	O	1.8V	SPI Master Data Output to SPI ROM Slave Input. Control register available for 2 mA/4 mA/6 mA/ 8 mA/10 mA/12 mA/14 mA/16 mA current strength.
H18	BOOT_EN_IN	I	1.8V	Set high to load firmware from external SPI-ROM.
H19	BOOT_EN_OUT	O	1.8V	Sets high after firmware load from external SPI-ROM has completed.
L17	GPIO5	I/O	1.8V internal pull-up	General-Purpose I/O.
M14	GPIO4			
H5	GPIO3			
G7	GPIO2			
G14	GPIO1			
H15	GPIO0			
M8	TRSTB	I	1.8V Schmitt trigger Internal pull-up	JTAG Test Reset Input. Active-low. Resets the JTAG controller. This signal must be pulled low during normal operation.
K18	TCK	I	1.8V Schmitt trigger Internal pull-up	JTAG Test Clock Input.
H10	TMS	I	1.8V internal pull-up	JTAG Test Mode Select Input.
J19	TDI	I	1.8V internal pull-up	JTAG Serial Test Data Input.
K19	TDO	O	1.8V tristate	JTAG Serial Test Data Output.
R11, T11	PVDD1P8	Pwr	1.8V	Line-Side 1.8V PLL Power Supply.
N11, N17, T5, T16	PVDD0P8_0	Pwr	0.8V	Line-side PLL Power Supply.
P11, P17, T6, T17	PVDD0P8_1	Pwr	0.8V	Line-Side PLL Power Supply.
N7, N9, N13, N15, P7, P9, P13, P15	RVDD0P8	Pwr	0.8V	Line-Side Receive Power Supply.
T8, T13	TVDD0P8	Pwr	0.8V	Line-Side Transmit Power Supply.
T9, T14	TVDDDRV	Pwr	0.8V to 1.0V	Line-Side Analog Driver TX Power. **NOTE:** The voltage can be 0.8V to 1.0V. The differential voltage of the analog transmitter is 0.8V peak-to-peak with 0.8V.

Table 4: I/O Pin Functional Descriptions (Continued)

Ball Number	Ball Name	Ball Type	Level	Description
E9, E16	H_PVDD1P8	Pwr	1.8V	Host-Side 1.8V PLL Power Supply.
E8, F9	H_PVDD0P8_A	Pwr	0.8V	Host-Side PLL Power Supply.
E15, F16	H_PVDD0P8_B	Pwr	0.8V	Host-Side PLL Power Supply.
E6, F6, G3, G4	H_RVDD0P8_A	Pwr	0.8V	Host-Side Receive Power Supply.
E13, F13, G18, G19	H_RVDD0P8_B	Pwr	0.8V	Host-Side Receive Power Supply.
E4, F11	H_TVDD0P8_A	Pwr	0.8V	Host-Side Transmit Power Supply.
E18, F20	H_TVDD0P8_B	Pwr	0.8V	Host-Side Transmit Power Supply.
E3, E11	H_TVDDDRV_A	Pwr	0.8V to 1.0V	Host-Side Analog Driver TX Power. **NOTE:** The voltage can be 0.8V to 1.0V. The differential voltage of the analog transmitter is 0.8V peak-to-peak with 0.8V.
E19, E20	H_TVDDDRV_B	Pwr	0.8V to 1.0V	Host-Side Analog Driver TX Power. **NOTE:** The voltage can be 0.8V to 1.0V. The differential voltage of the analog transmitter is 0.8V peak-to-peak with 0.8V.
J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, L8, L9, L14, L15	VDD	Pwr	0.8V	Digital VDD Supply. Can be controlled with AVS to reduce supply level to ~0.65V and lower power.
L12	VDDM	Pwr	0.8V	Digital memory supply.
L5	VDD_MDIO	Pwr	1.8V/1.2V	MDIO Interface Supply. When VDD_MDIO = 1.8V, When VDD_MDIO = 1.2V, only 1.2V signaling is supported. 3.3V MDIO is not supported.
J5, K5	VDDIO	Pwr	1.8V	I/O Supply.

Table 4: I/O Pin Functional Descriptions (Continued)

Ball Number	Ball Name	Ball Type	Level	Description
A1, A2, A5, A8, A11, A14, A17, A20, A22, AA2, AA4, AA6, AA8, AA10, AA12, AA14, AA16, AA18, AA20, AA22, AB1, AB2, AB4, AB6, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AB22, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B22, C2, C5, C8, C11, C14, C17, C20, C21, C22, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, E2, E5, E7, E10, E12, E14, E17, E21, F2, F3, F4, F5, F7, F8, F10, F12, F14, F15, F17, F18, F19, F21, F22, G1, G2, G5, G8, G9, G10, G11, G13, G15, G16, G17, G20, H2, H3, H4, H20, H21, H22, J2, J6, J20, K1, K2, K6, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, K20, K21, K22, L2, L3, L4, L6, L7, L10, L11, L13, L16, L18, L19, L20, M2, M4, M10, M11, M12, M16, M17, M18, M20, M21, M22, N1, N2, N4, N6, N8, N10, N12, N14, N16, N18, N20, P2, P3, P4, P5, P6, P8, P10, P12, P14, P16, P18, P19, P20, P21, P22, R2, R4, R5, R6, R7, R8, R9, R10, R12, R13, R14, R15, R16, R17, R18, R21, T1, T2, T4, T7, T10, T12, T15, T18, T19, T20, T21, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U21, U22, V2, V4, V6, V8, V10, V12, V14, V16, V18, V19, V20, V21, W1, W2, W4, W6, W8, W10, W12, W14, W16, W18, W21, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y22	VSS	GND	0V	Ground.
G21, G22, H16, H17, J3, J18, K3, K17, M15	NC	N/A	Do not connect	—

2.2 Ballout Location Diagram

Figure 7: Ballout Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	VSS	HTX_1N	HTX_1P	VSS	HTX_2N	HTX_2P	VSS	HTX_3N	HTX_3P	VSS	HTX_4N	HTX_4P	VSS	HTX_5N	HTX_5P	VSS	HTX_6N	HTX_6P	VSS	HTX_7P	VSS	**A**
B	HTX_0P	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HTX_7N	VSS	**B**
C	HTX_0N	VSS	HRX_1N	HRX_1P	VSS	HRX_2N	HRX_2P	VSS	HRX_3N	HRX_3P	VSS	HRX_4N	HRX_4P	VSS	HRX_5N	HRX_5P	VSS	HRX_6N	HRX_6P	VSS	VSS	VSS	**C**
D	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	HRX_7P	**D**
E	HRX_0P	VSS	H_TVDD DRV_A	H_TVDD 0P8_A	VSS	H_RVDD 0P8_A	VSS	H_PVDD 0P8_A	H_PVDD 1P8	VSS	H_TVDD DRV_A	VSS	H_RVDD 0P8_B	VSS	H_PVDD0 P8_B	H_PVDD 1P8	VSS	H_TVDD0 P8_B	H_TVDDD RV_B	H_TVDD DRV_B	VSS	HRX_7N	**E**
F	HRX_0N	VSS	VSS	VSS	VSS	H_RVDD 0P8_A	VSS	VSS	H_PVDD 0P8_A	VSS	H_TVDD 0P8_A	VSS	H_RVDD 0P8_B	VSS	VSS	H_PVDD 0P8_B	VSS	VSS	VSS	H_TVDD0 P8_B	VSS	VSS	**F**
G	VSS	VSS	H_RVDD 0P8_A	H_RVDD 0P8_A	VSS	REF_SEL 0	GPIO2	VSS	VSS	VSS	VSS	REF_SEL 1	VSS	GPIO1	VSS	VSS	VSS	H_RVDD0 P8_B	H_RVDD0 P8_B	VSS	NC	NC	**G**
H	REF_CLK _P	VSS	VSS	VSS	GPIO3	SCLAS	MISO	MOSI	SCK	TMS	SDAAM	SCLAM	INTR_N	MDC	GPIO0	NC	NC	BOOT_EN _IN	BOOT_EN _OUT	VSS	VSS	VSS	**H**
J	REF_CLK _N	VSS	NC	RCLK0	VDDIO	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	MDIO	NC	TDI	VSS	CLK_OUT _DIFF_P	CLK_OUT _DIFF_N	**J**
K	VSS	VSS	NC	RCLK1	VDDIO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	TCK	TDO	VSS	VSS	VSS	**K**
L	MRX_0P	VSS	VSS	VSS	VDD_MDI O	VSS	VSS	VDD	VDD	VSS	VSS	VDDM	VSS	VDD	VDD	VSS	GPIO5	VSS	VSS	VSS	MRX_15P	MRX_15N	**L**
M	MRX_0N	VSS	MRX_1P	VSS	SDAAS	SS_N	PRTAD4	TRSTB	PRTAD2	VSS	VSS	VSS	PRTAD3	GPIO4	NC	VSS	VSS	VSS	MRX_14P	VSS	VSS	VSS	**M**
N	VSS	VSS	MRX_1N	VSS	RESET_ N	VSS	RVDD0P8	VSS	RVDD0P8	VSS	PVDD0P 8_0	VSS	RVDD0P8	VSS	RVDD0P8	VSS	PVDD0P8 _0	VSS	MRX_14N	VSS	MTX_15P	MTX_15N	**N**
P	MTX_0P	VSS	VSS	VSS	VSS	VSS	RVDD0P8	VSS	RVDD0P8	VSS	PVDD0P 8_1	VSS	RVDD0P8	VSS	RVDD0P8	VSS	PVDD0P8 _1	VSS	VSS	VSS	VSS	VSS	**P**
R	MTX_0N	VSS	MRX_2P	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PVDD1P 8	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MRX_13P	MRX_13N	VSS	MTX_14P	**R**
T	VSS	VSS	MRX_2N	VSS	PVDD0P 8_0	PVDD0P 8_1	VSS	TVDD0P8	TVDDDRV	VSS	PVDD1P 8	VSS	TVDD0P8	TVDD DRV	VSS	PVDD0P 8_0	PVDD0P8 _1	VSS	VSS	VSS	VSS	MTX_14N	**T**
U	MTX_1P	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MRX_12P	MRX_12N	VSS	VSS	**U**
V	MTX_1N	VSS	MRX_3P	VSS	MRX_4P	VSS	MRX_5P	VSS	MRX_6P	VSS	MRX_7P	VSS	MRX_8P	VSS	MRX_9P	VSS	MRX_10P	VSS	VSS	VSS	VSS	MTX_13P	**V**
W	VSS	VSS	MRX_3N	VSS	MRX_4N	VSS	MRX_5N	VSS	MRX_6N	VSS	MRX_7N	VSS	MRX_8N	VSS	MRX_9N	VSS	MRX_10N	VSS	MRX_11P	MRX_11N	VSS	MTX_13N	**W**
Y	MTX_2P	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	**Y**
AA	MTX_2N	VSS	MTX_3P	VSS	MTX_4P	VSS	MTX_5P	VSS	MTX_6P	VSS	MTX_7P	VSS	MTX_8P	VSS	MTX_9P	VSS	MTX_10P	VSS	MTX_11P	VSS	MTX_12P	VSS	**AA**
AB	VSS	VSS	MTX_3N	VSS	MTX_4N	VSS	MTX_5N	VSS	MTX_6N	VSS	MTX_7N	VSS	MTX_8N	VSS	MTX_9N	VSS	MTX_10N	VSS	MTX_11N	VSS	MTX_12N	VSS	**AB**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Chapter 3: Management Interfaces

3.1 MDIO Access

The BCM81724 can operate in MDIO with indirect MDIO access.

For a write transfer, follow this procedure:

1. Program the indirect control register IND_CTRL for the desired data type and address mode.
2. Write two indirect address registers, IND_ADDRL and IND_ADDRH, for a 32-bit address.
3. Write one or two indirect data registers, IND_DATAL and IND_DATAH. In the case of a word transfer, program IND_DATAL first then IND_DATAH; otherwise, write only to IND_DATAL.

For a read transfer, follow this procedure:

1. Program the indirect control register IND_CTRL for the desired data type and address mode.
2. Write two indirect address registers, IND_ADDRL and IND_ADDRH, for a 32-bit address.
3. Read from one or two indirect data registers, IND_DATAL and IND_DATAH. In the case of a word transfer, read IND_DATAL first then IND_DATAH; otherwise, read only IND_DATAL.

Table 5: MDIO Indirect Address Descriptions

Name	MDIO Address	APB Offset Address	Bit	Access	Description
IND_ADDRL	0x0000	—	15:0	R/W	Indirect access address low [15:0]. Address must be aligned with the data types.
IND_ADDRH	0x0001	—	15:0	R/W	Indirect access address high [31:16].
IND_DATAL	0x0002	—	15:0	R/W	Indirect access data low [15:0]: ■ Write this register to start DMA byte data for IND_DATAL[7:0] write transfer when IND_CTRL[5:4]=00. ■ Write this register to start DMA half-word data for IND_DATAL[15:0] write transfer when IND_CTRL[5:4]=01. ■ Read this register to start DMA data read transfer. When IND_CTRL[5:4]=00, IND_DATAL[7:0] is valid. When IND_CTRL[5:4]=01/10, IND_DATAL[15:0] is valid.
IND_DATAH	0x0003	—	15:0	R/W	Indirect access data high [31:16]: ■ Write this register to start DMA byte data for both IND_DATAL[15:0] and IND_DATAH[15:0] write transfer when IND_CTRL[5:4]=10. ■ Read this register to get higher 16-bit read data when IND_CTRL[5:4]==10.

Table 5: MDIO Indirect Address Descriptions (Continued)

Name	MDIO Address	APB Offset Address	Bit	Access	Description
IND_CTRL	0x0004	—	6:0	R/W	Indirect access control: Bits 3 through 0: Reserved Bits 5 through 4: Indirect access data type/size ■ 00: Byte (8-bit) ■ 01: Half-word (16-bit) ■ 11: Reserved Bit 6: Indirect address auto post increment: ■ 0: Fixed address ■ 1: Address post auto increment by the size of IND_CTRL[5:4] on writes, by word on reads
MDIO_STAT	0x0005	0x000	1:0	R/W	MDIO status: Bit 0: DMA transfer error Bit 1: MDIO read data late error

3.2 MDIO (Slave) Interface

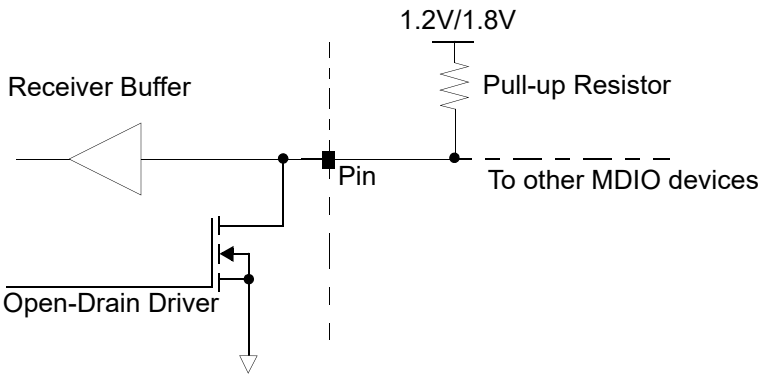
The PHY supports IEEE 802.3 Clause 45 Station Management Interface. Clause 22 is not supported. The PHY acts as an MDIO manageable slave device (MMD) and responds to the host when it receives frames with a matching PRTAD and DEVAD, and it provides access to Device 1 (PMA/PMD) only.

When an MDIO write/read operation is executed, the PHY compares the PRTAD field with its own PHY address. The operation is executed only when the PRTAD matches the PHY's port address.

MDIO is a two-wire interface standard, using the MDIO signal for serial data and the MDC for the serial clock. A 16-bit shift register receives data from the MDIO pin on the rising edge of the MDC clock. The frame format begins with a preamble for clock synchronization followed by the start-of-frame sequence. The read or write opcode, PRTAD, and DEVAD fields follow next. Only one device type is supported for DEVAD: 11111. Depending on the read/write opcode, data is either received or transmitted by the PHY. Once the 16-bit data field is transferred, the MDIO signal is returned to a high-impedance state (idle).

Figure 8 shows the MDIO interface.

Figure 8: MDIO Interface



3.2.1 MDIO Frame Format

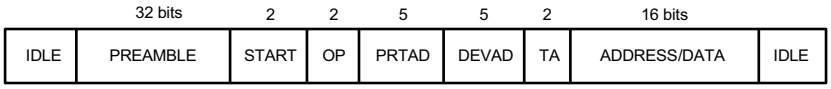
The MDIO frame format begins with a preamble and then is followed by the start-of-frame sequence. The read or write opcode, PRTAD, and DEVAD fields follow next. Depending on the read/write opcode, data is either received or transmitted by the PHY. After the 16-bit data field is transferred, the MDIO signal is returned to a high-impedance state (idle).

Figure 9 shows the MDIO frame format. This format is used for both read and write operations.

MDIO frame format descriptions are listed here:

- Preamble = 32-bit 1s (optional)
- START = Start of frame indicated by 00 pattern
- OP = Opcode (access type)
  - 00: Address
  - 01: Read
  - 11: Write
  - 10: Postread increment address
- TA = Turnaround
  - Z0: Read
  - 01: Write
- PRTAD = Physical port address
- DEVAD = Device address
  - 11111: PMA/PMD
- Address/data = 16-bit address or data

Figure 9: MDIO Frame Format



NOTE: The BCM81724 operates with indirect MDIO access 32-bit address/data. See Section 3.1, MDIO Access, indirect addressing details.

Any read or write operation to a PHY register requires the transmission of at least two MDIO frames from the host. The first frame tells the PHY the address of the target register (with opcode = 00), and the second frame performs the actual read or write operation (with opcode = 01 for read and opcode = 11 for write).

Chapter 4: Register Summary

These tables describe the chip-level, system-side, and line-side registers of the BCM81724.

4.1 Chip-Level Registers

Table 6: CHIP ID REG LSB (0x5200_cb20)

Bits	Name	Type	Default	Description
31:16	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
15:0	chip_id_lower_word	RO	0x1724	Chip ID[15:0].

Table 7: CHIP ID REG MSB (0x5200_cb24)

Bits	Name	Type	Default	Description
31:4	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
3:0	chip_id_high_nibble	RO	0x0008	Chip ID[19:16].

Table 8: REV ID REG (0x5200_cb28)

Bits	Name	Type	Default	Description
31:8	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
7:0	rev_id	RO	0xa0	Revision ID.

Table 9: PKG ID REG LSB (0x5200_cb2c)

Bits	Name	Type	Default	Description
31:16	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
15:0	pkg_id_lower_word	RO	0x0	Package ID lower word.

Table 10: PKG ID REG MSB (0x5200_cb30)

Bits	Name	Type	Default	Description
31:4	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
3:0	pkg_id_high_nibble	RO	0x0	Package ID high nibble.

Table 11: JTAG REV ID REG (0x5200_cb34)

Bits	Name	Type	Default	Description
31:4	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
3:0	jtag_rev_id	RO	0x0	JTAG revision ID.

Table 12: JTAG CHIP ID REG (0x5200_cb38)

Bits	Name	Type	Default	Description
31:16	Reserved	RSVD	0x0	Reserved bits must be written with 0. A read returns an unknown value.
15:0	jtag_chip_id	RO	0x0	JTAG revision ID.

4.2 System-Side Registers

Table 13: PAM TX FIR MICRO CONTROL0 (0x5800_34c0)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	tx_eee_alert_en	R/W	TX EEE alert mode control. 1 = Enable EEE alert mode when pmd_tx_mode (input pins) == 2'b10 0 = Disable EEE alert mode Reset value is 1.
14	tx_eee_quiet_en	R/W	TX EEE quiet mode control. 1 = Enable EEE quiet mode when pmd_tx_mode (input pins) == 2'b01 0 = Disable EEE quiet mode Reset value is 1.
13:10	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.

Table 13: PAM TX FIR MICRO CONTROL0 (0x5800_34c0) (Continued)

Bits	Name	Type	Description
9:4	tx_disable_timer_ctrl	R/W	tx_disable timer value controls. tx_disable_timer_ctrl[5] (MSB) selects the timer units. 0 = 2 µs units 1 = 1 ms units tx_disable_timer_ctrl[4:0] (LSB[4:0]) = controls the number of units per this list: 0 = 0 units 1 = 1 units 2 = 2 units 3 = 3 units 4 = 4 units 5 = 5 units 6 = 6 units 7 = 7 units 8 = 8 units 9 = 10 units 10 = 12 units 11 = 14 units 12 = 16 units 13 = 20 units 14 = 24 units 15 = 28 units 16 = 32 units 17 = 40 units 18 = 48 units 19 = 56 units 20 = 64 units 21 = 80 units 22 = 96 units 23 = 112 units 24 = 128 units 25 = 160 units 26 = 192 units 27 = 224 units 28 = 256 units 29 = 320 units 30 = 384 units 31 = 448 units Reset value is 0x16.
3	pmd_tx_disable_pkill	R/W	TX disable using the pmd_tx_disable pin disable control. 0 = Enable TX disable from pmd_tx_disable pin 1 = Disable TX disable from pmd_tx_disable pin Reset value is 0.

Table 13: PAM TX FIR MICRO CONTROL0 (0x5800_34c0) (Continued)

Bits	Name	Type	Description
2	dp_reset_tx_disable_dis	R/W	TX disable based on data path reset. 0 = Enable TX disable based on data path reset 1 = Disable TX disable based on data path reset Need to set this bit to 1 if tx_disable_output_sel = 2'b01 (send TX power-down). Reset value is 0.
1	tx_disable_trigger	SC	TX disable trigger. When this bit is set to 1, it triggers a TX disable with timer starting at 0. No matter where the TX disable state is, it starts a new timer and applies TX disable. This bit is self-clearing. Reset value is 0.
0	micro_tx_disable	R/W	Micro TX disable This field is used by the Microcontroller for TX disable control during CL93N72 forced mode Reset value is 0.

Table 14: PAM TXFIR MISC CONTROL0 (0x5800_34c4)

Bits	Name	Type	Description
31:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
3:2	tx_disable_output_sel	R/W	These bits select TX disable output function: 2'b00 = Send electrical idles 2'b01 = Send power-down 2'b10 = Send ones 2'b11 = Send zeroes Reset value is 0.
1	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
0	sdk_tx_disable	R/W	SDK TX disable. This TX disable control field is for SDK use during TX programming. Reset value is 0.

Table 15: PAM TX FIR TAP CONTROL0 (0x5800_34cc)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	txfir_test_data_en	R/W	TXFIR DAC test data enable. 1 = Test mode. Enables test data path from the DAC memory to the DAC for characterization. 0 = Normal modes. TXFIR DAC driver is used to drive the DAC. Reset value is 0.
14	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
13:12	txfir_tap_en	R/W	TXFIR taps enable. 2'd0 = tap2:tap0 2'd1 = tap5:tap0 2'd2 = tap8:tap0 2'd3 = tap11:tap0 Reset value is 3.
11	txfir_tap_load	SC	Load TXFIR tap values. The sequence to load the taps is: 1. Set taps values in the txfir_tap*_coeff fields as needed. 2. Set txfir_tap_load field to 1'b1. This field is self-clearing; always reads back 0. Reset value is 0.
10	txfir_nrz_tap_range_sel	R/W	TXFIR NRZ tap range select. 0 = PAM-4 tap range –170 to +170 1 = NRZ tap range –127 to +127 Reset value is 0.
9	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
8:0	txfir_tap0_coeff	R/W	TXFIR tap 0 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 16: PAM TX FIR TAP CONTROL1 (0x5800_34d0)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap1_coeff	R/W	TXFIR tap 1 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 17: PAM TX FIR TAP CONTROL2 (0x5800_34d4)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap2_coeff	R/W	TXFIR tap 2 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0xa8.

Table 18: PAM TX FIR TAP CONTROL3 (0x5800_34d8)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap3_coeff	R/W	TXFIR tap 3 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 19: PAM TX FIR TAP CONTROL4 (0x5800_34dc)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap4_coeff	R/W	TXFIR tap 4 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 20: PAM TX FIR TAP CONTROL5 (0x5800_34e0)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap5_coeff	R/W	TXFIR tap 5 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 21: PAM TX FIR TAP CONTROL6 (0x5800_34e4)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	txfir_level_shift_mode_en	R/W	Level shifting enable. Level shifting is achieved by repurposing the last 6 taps such that taps 6 through 8 provide level adjustment for level = 3, and taps 9 through 11 for level = –3. 1 = Enabled 0 = Disabled Reset value is 0.
14:8	txfir_dc_adjust	R/W	This field specifies the amount of DC offset added to TXFIR output. The range is –64 to +63. Reset value is 0.
7	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
6:0	txfir_tap6_coeff	R/W	TXFIR tap 6 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 22: PAM TX FIR TAP CONTROL7 (0x5800_34e8)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap7_coeff	R/W	TXFIR tap 7 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 23: PAM TX FIR TAP CONTROL8 (0x5800_34ec)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap8_coeff	R/W	TXFIR tap 8 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 24: PAM TX FIR TAP CONTROL9 (0x5800_34f0)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap9_coeff	R/W	TXFIR tap 9 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 25: PAM TX FIR TAP CONTROL10 (0x5800_34f4)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap10_coeff	R/W	TXFIR tap 10 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 26: PAM TX FIR TAP CONTROL11 (0x5800_34f8)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap11_coeff	R/W	TXFIR tap 11 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 27: PAM PAT GEN CONFIG (0x5800_35c0)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:12	patt_gen_start_pos	R/W	Valid values are 11 to 0. Defines the start position of the pattern in 20-bit chunks. 11 means start at bit 239. 10 means start at bit 219. 0 means start at bit 19. So start bit is (rg_patt_gen_start_pos × 20 + 19). Reset value is 0xb.

Table 27: PAM PAT GEN CONFIG (0x5800_35c0) (Continued)

Field	Field Name	Access	Description
11:8	patt_gen_stop_pos	R/W	Valid values are 11 to 0. Defines the stop position of the pattern in 20-bit chunks. This register value should be less than or equal to rg_patt_gen_start_pos. 11 means stop at bit 220. 10 means stop at bit 200. 0 means stop at bit 0. So stop bit is (rg_patt_gen_stop_pos × 20). Reset value is 0x0.
7	pam4_tx_jp03b_patt_en	R/W	JP03B fixed pattern Enable. Higher priority than pam4_tx_linearity_patt_en if both bits are enabled simultaneously. Make sure gray encoder and PAM-4 precoder is disabled for this fixed pattern mode. 1 = Enable the fixed pattern for JP03B pattern of 124 bits (that is, 62 symbols) long repeating pattern of {15{00,11}} + {16{11,00}}. Program reg field patt_gen_seq_1[15:8] bits = 8'b_0011_1100 = 8'h3C before enabling this pattern. Transmission order is MSB first. If this bit is enabled then make sure that other lane fixed pattern do not use fixed pattern 20-bit chunk of bits 39:20. 0 = Disable the JP03B fixed pattern generation Reset value is 0x0.
6	pam4_tx_linearity_patt_en	R/W	PAM-4 transmitter linearity pattern enable. Lower priority than pam4_tx_jp03b_patt_en if both bits are enabled simultaneously. Make sure gray encoder and PAM-4 precoder is disabled for this fixed pattern mode. 1 = Enable the fixed pattern for PAM-4 transmitter linearity pattern of 320 bits (that is, 160 symbols) long repeating pattern of 10 PAM-4 levels of {–1, –1/3, +1/3, +1, –1, +1, -1, +1, +1/3, –1/3}, where each level is 16UI in duration. Program reg field {patt_gen_seq_1[3:0], patt_gen_seq_0[15:0]} bits = 20'b_0001_1011_0011_0011_1001 = 20'h1B339 before enabling this pattern. Transmission order is MSB first. If this bit is enabled then make sure that other lane fixed pattern do not use fixed pattern 20-bit chunk of bits 19:0. 0 = Disable the PAM-4 transmitter linearity pattern generation Reset value is 0x0.
5:1	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
0	patt_gen_en	R/W	Fixed pattern generator enable. 1 = Enable the fixed pattern generator 0 = Disable the fixed pattern generator Reset value is 0x0.

Table 28: PAM PRBS GEN CONFIG (0x5800_35c4)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	prbs_gen_pause_ strobe	SC	PRBS Generator Pause Strobe (debug register). It is a self-clearing register bit. Writing to 1 pauses the PRBS generator for 1 clock cycle, which means same 40 bits of data is replicated in the paused clock cycle. This results in loss of PRBS checker lock on the link partner. Reset value is 0x0.
14:13	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
12	prbs_gen_mode_sel_ msb	R/W	Extending PRBS polynomial select by using this bit as bit[3] along with prbs_gen_mode_sel[2:0]. 1'b0 will select old PRBS polynomials for PRBS 7, 9, 11, 15, 23, 31, 49, and 58 based on prbs_gen_mode_sel[2:0]. 1'b1 will select new PRBS polynomials for PRBS 10, 20, 13 for PAM-4 based on prbs_gen_mode_sel[2:0]. 1'b1 and prbs_gen_mode_sel[2:0] == 0 will select PRBS 10. 1'b1 and prbs_gen_mode_sel[2:0] == 1 will select PRBS 20. 1'b1 and prbs_gen_mode_sel[2:0] == 2 will select PRBS 13 with polynomial (1 + x^1 + x^2 + x^12 + x^13). This pattern is also used for PAM-4 link training lane 0 pattern. 1'b1 and prbs_gen_mode_sel[2:0] == 3 is reserved for future use. 1'b1 and prbs_gen_mode_sel[2:0] == 4 will select PAM-4 link training lane 1 PRBS 13 polynomial (1 + x2 + x3 + x7 + x13). Debug modes so auto-detect and self-sync mode is not supported. 1'b1 and prbs_gen_mode_sel[2:0] == 5 will select PAM-4 link training lane 2 PRBS 13 polynomial (1 + x2 + x4 + x8 + x13). Debug modes so auto-detect and self-sync mode is not supported. 1'b1 and prbs_gen_mode_sel[2:0] == 6 will select PAM-4 link training lane 3 PRBS 13 polynomial (1 + x2 + x5 + x9 + x13). Debug modes so auto-detect and self-sync mode is not supported. 1'b1 and prbs_gen_mode_sel[2:0] == 7 is reserved for future use. Reset value is 0x0.
11:6	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
5	prbs_gen_err_ins	R/W	PRBS error insert. 0 to 1 transition on this signal will insert single bit error in the MSB bit of the data bus. Reset value is 0x0.
4	prbs_gen_inv	R/W	PRBS invert enable. 1 = Inverts all the data bits from the PRBS generator 0 = Sends normal data from the PRBS generator Reset value is 0x0.

Table 28: PAM PRBS GEN CONFIG (0x5800_35c4) (Continued)

Field	Field Name	Access	Description
3:1	prbs_gen_mode_sel	R/W	PRBS generator mode select. Selects the PRBS polynomial as shown here: 3'd0: PRBS 7 3'd1: PRBS 9 3'd2: PRBS 11 3'd3: PRBS 15 3'd4: PRBS 23 3'd5: PRBS 31 3'd6: PRBS 58 (1 + x^39 + x^58) 3'd7: PRBS 49 (1 + x^40 + x^49) Reset value is 0x5.
0	prbs_gen_en	R/W	PRBS generator enable. 1 = Enable the PRBS generator 0 = Disable the PRBS generator Reset value is 0x0.

Table 29: PAM RMT LPBK CONFIG (0x5800_35c8)

Field	Field Name	Access	Description
31:3	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
2	rmt_lpbk_pd_frc_on	R/W	Remote loopback PD enable by force irrespective of rg_rmt_lpbk_en. 1'b1 = enable the phase detector without the remote loopback enable. Can be used to lock RX and TX clock phases when there is a remote loopback outside PMD Reset value is 0x0.
1	rmt_lpbk_pd_mode	R/W	Remote loopback phase detector mode. For normal operating conditions keep it at the default value of 1'b1. 1'b0 = Swap increase/decrease 1'b1 = Normal mode Reset value is 0x1.
0	rmt_lpbk_en	R/W	RX to TX parallel loopback (remote loopback) enable. 1 = Loopback is enabled 0 = Loopback is disabled Reset value is 0x0.

Table 30: PAM TLB TX MISC CONFIG (0x5800_35cc)

Field	Field Name	Access	Description
31:5	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
4	tx_trn_active_auto_ mode_en	R/W	1'b1 will forcefully disable the below described TX datapath functions automatically while TX link training is enabled and active irrespective of these register bit settings: ■ PAM-4 Gray Encoder (enabled by field pam4_gray_enc_en) ■ PAM-4 Precoder (enabled by field pam4_precoder_en) ■ PAM-4 Symbol bit-swap (enabled by field pam4_tx_symbol_bit_swap) ■ NRZ Differential Encoder (enabled by field tlb_tx_diff_enc_en) In addition to these functions, back-channel encoder and scrambler are always disabled while TX link training is enabled and active irrespective of this register value. 1'b0 will ignore the control signal from TX link training and the above TX datapath functions will be enabled based on their individual enable bits irrespective of the TX training status being enabled or disabled. Reset value is 0x1.
3	tlb_tx_diff_enc_en	R/W	1'b1 will enable the differential encoder for pmd_tx_data. Only applicable to PCS TX data in OS1, 2, and 4 modes. Write it to 1'b0 for 1G OSR modes 16P5 and 20P625. Reset value is 0x0.
2	tx_mux_sel_order	R/W	TX data MUX select priority order. When 1'b1 then priority of Pattern and PRBS generators are swapped w.r.t. CL72. 0 = TX data mux select order from higher to lower priority is {rmt_lpbk, patt_gen, cl72_tx, prbs_gen, tx_pcs}. 1 = TX data mux select order from higher to lower priority is {rmt_lpbk, prbs_gen, cl72_tx, patt_gen, tx_pcs}. Reset value is 0x0.
1	tx_pcs_native_ana_ frmt_en	R/W	TX PCS interface native analog format enable. 1 = TX PCS interface is enabled in the native analog format mode. TX PCS sends the over-sampled data in this mode which is sent directly to AFE. 0 = Raw data mode, where for every data request TX PCS will send 20 bits of valid data. Reset value is 0x0.
0	tx_pmd_dp_invert	R/W	TX PMD datapath invert control. When enabled by writing to 1'b1, it will invert all the datapath bits of the logical lane. Recommended for use in case P and N pads are swapped on the PCB board. Reset value is 0x0.

Table 31: PAM TLB TX PAM-4 CONFIG 0 (0x5800_35d4)

Field	Field Name	Access	Description
31:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
3	pam4_tx_symbol_bit_swap	R/W	PAM-4 symbol bits {A,B} swap enable. Enable it only for the PAM-4 modes. Bit swapping is done just before the PAM-4 gray encoder. 1 = 2-bit PAM-4 symbol bits will be swapped, where PAM-4 symbol bits {A,B} maps to the datastream bits {[n+1], [n]}, where n is the first bit in transmission order. 0 = No swapping, default mode. PAM-4 symbol bits {A,B} maps to the datastream bits {[n], [n+1]}, where n is the first bit in transmission order. Reset value is 0x0.
2	tx_scrambler_en	R/W	PAM-4 TX datapath scrambler enable. Applicable only for the PAM-4 modes with PRBS or PCS data. 1 = PAM-4 TX datapath scrambler is enabled. If tx_scrambler_en is enabled then 40 bits of the transmitted data will be XORed with the 40 LSB bits of the fixed pattern sequence register {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]}. Make sure {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]} bits are only re-programmed or changed when both tx_scrambler_en and bc_enc_err_ins_en reg fields are 1'b0. 0 = PAM-4 TX datapath scrambler is disabled Reset value is 0x0.
1	pam4_precoder_en	R/W	PAM-4 precoder enable. Enable it only for the PAM-4 modes. 1 = PAM-4 precoder is enabled 0 = PAM-4 precoder is disabled Reset value is 0x0.
0	pam4_gray_enc_en	R/W	PAM-4 gray encoder enable. Enable it only for the PAM-4 modes. 1 = PAM-4 gray encoder is enabled 0 = PAM-4 gray encoder is disabled Reset value is 0x0.

Table 32: PAM RMT LPBK PD STATUS (0x5800_35e0)

Field	Field Name	Access	Description
31:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	rmt_lpbk_pd_early_ind	RO	1 means dp_tclk20 is sampling data earlier so delay the dp_tclk20 clock phase. This will result in TX PI phase step increment. Reset value is 0x1.
0	rmt_lpbk_pd_late_ind	RO	1 means dp_tclk20 is sampling data late so reduce the delay of the dp_tclk20 clock phase. This will result in TX PI phase step decrement. Reset value is 0x0.

Table 33: PAM TLB TX BC ENC CONFIG 0 (0x5800_35e4)

Field	Field Name	Access	Description
31:11	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
10:8	bc_enc_frm_len_sel	R/W	Back-channel encoder frame length select control. Determines the distance between two adjacent back-channel frames. The following table explains the value of this register and BC frame length in multiples of 128 tclk20 cycles or 128 × 20 PAM-4 symbols. bc_enc_frm_len_sel[2:0] — BC frame length in multiples of 128 × 20 PAM-4 symbols. 0 — 1 1 — 16 × 2^0 2 — 16 × 2^1 3 — 16 × 2^2 4 — 16 × 2^3 5 — 16 × 2^4 6 — 16 × 2^5 7 — 16 × 2^6 Reset value is 0x0.
7:3	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
2	bc_enc_err_ins_en	R/W	Back-channel encoder error insert enable. Applicable only for the modes when BC encoder is enabled. tx_scrambler_en reg field should be disabled for BC encoder error insertion to work; otherwise, all the TX data will be XORed instead and not only the BC encoder frame. 1 = Back-channel encoder error insert is enabled. If BC encoder error insertion is enabled and tx_scrambler_en is disabled then 40 bits of the transmitted BC frame will be XORed with the 40 LSB bits of the fixed pattern sequence register {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]}. Make sure {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]} bits are only re-programmed or changed when both tx_scrambler_en and bc_enc_err_ins_en reg fields are 1'b0. 0 = Back-channel encoder error insert is disabled Reset value is 0x0.
1	bc_enc_update	SC	Back-channel encoder update control. Self-clearing control register. Write this register to 1'b1 after updating the bc_enc_data and/or bc_enc_frm_len_sel fields. Updated information will be sent transmitted in the next back-channel encoder word/frame. Reset value is 0x0.
0	bc_enc_en	R/W	Back-channel encoder enable. Applicable only to PAM-4 modes along with PRBS or PCS TX data sources. 1 = Back-channel encoder is enabled 0 = Back-channel encoder is disabled Reset value is 0x0.

Table 34: PAM TLB TX BC ENC CONFIG 1 (0x5800_35e8)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	bc_enc_data_lsb	R/W	Back-channel encoder data LSB bits [15:0]. Reset value is 0xf628.

Table 35: PAM TLB TX BC ENC CONFIG 2 (0x5800_35eC)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	bc_enc_data_msb	R/W	Back-channel encoder data LSB bits [15:0]. Reset value is 0x0.

Table 36: PAM TLB TX BC ENC STATUS 0 (0x5800_35f8)

Field	Field Name	Access	Description
31:1	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
0	bc_enc_data_sent	RO	Status bit (when set to 1) indicating that the first back-channel frame/word with the updated BC data and/or frame length have been transmitted. Reset value is 0x0.

Table 37: pam_linktrn_base_r_pmd_control_register_150 (0x5800_0258)

Field	Field Name	Access	Description
31:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	linktrn_ieee_training_enable	R/W	1 = Enable the 10GBASE-KR start-up protocol 0 = Disable the 10GBASE-KR start-up protocol Reset value is 0.
0	linktrn_ieee_restart_training	SC	1 = Restart 10GBASE-KR linktrn training 0 = Normal operation Self-clearing. Reset value is 0.

Table 38: pam_linktrn_base_r_pmd_status_register_151 (0x5800_025c)

Field	Field Name	Access	Description
31:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
3	linktrn_ieee_training_failure	RO	1 = Training failure has been detected 0 = Training failure has not been detected Reset value is 0.

Table 38: pam_linktrn_base_r_pmd_status_register_151 (0x5800_025c) (Continued)

Field	Field Name	Access	Description
2	linktrn_ieee_training_status	RO	1 = Start-up protocol in progress 0 = Start-up protocol complete Reset value is 0.
1	linktrn_ieee_frame_lock	RO	1 = Training frame delineation detected 0 = Training frame delineation not detected Reset value is 0.
0	linktrn_ieee_receiver_status	RO	1 = Receiver trained and ready to receive data 0 = Receiver training Reset value is 0.

Table 39: pam_linktrn_base_r_ld_coeff_update_register_154 (0x5800_0268)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	linktrn_ieee_ld_coeff_update	RO	This register reflects the first 16-bit word of the outgoing training frame sent by the local device. This register is not writeable. linktrn supports link training for IEEE/OIF/FC standards. Refer to the appropriate standards for register bit definitions. Reset value is 0x0.

Table 40: pam_linktrn_base_r_ld_status_report_register_155 (0x5800_026c)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	linktrn_ieee_ld_status_report	RO	This register reflects the second 16-bit word of the outgoing training frame sent by the local device. linktrn supports link training for IEEE/OIF/FC standards. Refer to the appropriate standards for register bit definitions. Reset value is 0x0.

Table 41: pam_linktrn_base_r_lp_coeff_update_register_152 (0x5800_0260)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	linktrn_ieee_lp_coeff_update	RO	This register reflects the first 16-bit word of the training frame most recently received from the link partner. This register is not writeable when linktrn training is disabled as indicated in the IEEE standard. linktrn supports link training for IEEE/OIF/FC standards. Refer to the appropriate standards for register bit definitions. Reset value is 0x0.

Table 42: pam_linktrn_base_r_lp_status_report_register_153 (0x5800_0264)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	linktrn_ieee_lp_status_report	RO	This register reflects the second 16-bit word of the training frame most recently received from the link partner. linktrn supports link training for IEEE/OIF/FC standards. Refer to the appropriate standards for register bit definitions. Reset value is 0x0.

Table 43: PAM RX PMON CSR0 (0x5800_12c0)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	pmon_md_lock_f	RO	PMON lock flag status (1 = PMON is locked). Reset value is 0.
14	pmon_md_enable	RO	PMON enabled status (1 = PMON is enabled). Reset value is 0.
13:5	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
4	md_pmon_stat_updt	R/W	PMON status update (pulse high to update PMON status). Reset value is 0.
3	md_pmon_cfg_wstb	R/W	PMON configuration write strobe (pulse high to write config to PMON). Reset value is 0.
2	md_pmon_enable	R/W	Enable (1 = Enable PMON, 0 = Disable PMON). Reset value is 0.
1	md_pmon_sw_rstn	R/W	PMON software reset not (0 = Reset active, 1 = Reset inactive). Reset value is 0.
0	md_pmon_clk_dis	R/W	PMON Clock Disable (1 = Clock off, 0 = Clock on). Reset value is 1.

Table 44: PAM RX PMON CSR1 (0x5800_12c4)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	md_pmon_os_mode	R/W	0 = Select normal mode 1 = Select oversample mode Reset value is 0.
14	md_pmon_even_oddn	R/W	0 = Use odd bits when In NRZ mode 1 = Use even bits when in NRZ mode Reset value is 0.
13	md_pmon_din_inv	R/W	0 = Don't invert PMON Din 1 = Invert PMON Din Reset value is 0.

Table 44: PAM RX PMON CSR1 (0x5800_12c4) (Continued)

Field	Field Name	Access	Description
12	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
11:8	md_pmon_lock_thr	R/W	PMON lock threshold. Reset value is 2.
7:4	md_pmon_poly_sel	R/W	PMON polynomial select status: 0: PRBS58, 1: PRBS31 2: PRBS7, 3: PRBS9 4: PRBS10, 5: PRBS11 6: PRBS13, 7: PRBS15 8: PRBS20, 9: PRBS23 10: PRBS49, 11 to 15: RSVSD Reset value is 0.
3:0	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.

Table 45: PAM RX PMON CSR2 (0x5800_12c8)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	pmon_lol_irq	RO	0 = PMON loss of lock IRQ is not active 1 = PMON loss of lock IRQ is active Type WOC. Reset value is 0.
14	md_pmon_lol_irq_clr	R/W	PMON loss of lock interrupt request clear. (pulse high to clear rx_pmon_lol_irq.) Reset value is 0.
13	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
12	md_pmon_relock_ena	R/W	0 = PMON does not relock when an LOL occurs 1 = PMON attempts to relock when an LOL occurs Reset value is 0.
11:8	md_pmon_unlock_thr	R/W	PMON unlock threshold = number of consecutive clock cycles required, where md_rx_pmon_unlock_tol is exceeded to cause a loss of lock (LOL). 0 = LOL is disabled (PMON never drops lock) Reset value is 0.
7	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
6:0	md_pmon_unlock_tol	R/W	Unlock bit error tolerance = number of bit errors allowed (tolerated) per clock cycle to remain locked. Reset value is 16.

Table 46: PAM RX PMON CSR3 (0x5800_12cc)

Field	Field Name	Access	Description
31:14	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
13	pmon_md_din_inv	RO	0 = PMON Din not inverted 1 = PMON Din Inverted Reset value is 0.
12:11	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
10:8	pmon_md_fsm_state	RO	PMON current FSM state. Reset value is 0.
7:4	pmon_md_poly_select	RO	PMON polynomial select status: 0: PRBS58, 1: PRBS31 2: PRBS7, 3: PRBS9 4: PRBS10, 5: PRBS11 6: PRBS13, 7: PRBS15 8: PRBS20, 9: PRBS23 10: PRBS49, 11-15: RSVSD Reset value is 0.
3	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
2	md_pmon_err_mode	R/W	PMON error mode. 0 = Create one LSB/MSB bit error when lsb_err/msb_err are set 1 = Create one LSB/MSB bit error per clock cycle when lsb_err/msb_err are set Reset value is 0.
1	md_pmon_msb_err	R/W	PMON MSB error debug control (pulse high to create MSB bit error(s). Reset value is 0.
0	md_pmon_lsb_err	R/W	PMON LSB error debug control (pulse high to create LSB bit error(s). Reset value is 0.

Table 47: PAM RX PMON CHK CSR0 (0x5800_12d0)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	pmon_timer_irq	RO	PMON checker, interval timer interrupt request status flag. 1 = Current Interval timer period has expired Use md_pmon_timer_irq_clr to clear this flag/ **NOTE:** This flag will set each time the timer period expires when md_pmon_timer_mode = 1. Reset value is 0.
14	pmon_md_timer_done	RO	PMON checker, interval timer done status flag. 1 = Interval timer period has expired Reset value is 0.

Table 47: PAM RX PMON CHK CSR0 (0x5800_12d0) (Continued)

Field	Field Name	Access	Description
13	pmon_md_timer_run	RO	PMON checker, interval timer running status flag. Reset value is 0.
12	pmon_md_berr_oflow_odd	RO	PMON checker, odd/MSB bit error accumulator overflow flag status. 1 = Odd/MSB BER ACC has overflowed Reset value is 0.
11	pmon_md_berr_oflow_even	RO	PMON checker, even/LSB bit error accumulator overflow flag status. 1 = Even/LSB BER ACC has overflowed Reset value is 0.
10:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8	md_pmon_timer_irq_clr	R/W	PMON checker, interval timer interrupt request clear. Pulse high to clear pmon_timer_irq. Reset value is 0.
7	md_pmon_berr_oflow_clr	R/W	PMON checker, bit error accumulator overflow flags clear. Pulse high to clear BER ACC overflow flags Reset value is 0.
6	md_pmon_berr_clr	R/W	PMON checker, bit error accumulator clear. Pulse high to clear BER ACCs and BER ACC overflow flags Reset value is 0.
5:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
3	md_pmon_timer_restart	R/W	PMON checker, interval timer restart. Pulse high to clear ACCs, IRQ, and restart timer. Reset value is 0.
2	md_pmon_timer_ena	R/W	PMON checker, interval timer enable. 1 = BER ACCs will only accumulate while timer is running 0 = BER ACCs will run as long as the checker is enabled Reset value is 0.
1	md_pmon_chk_sw_ena	R/W	PMON checker, software enable. See md_pmon_chk_sw_sel Reset value is 0.
0	md_pmon_chk_sw_sel	R/W	PMON checker, software control select. 0 = Hardware controls enabling of checker 1 = md_pmon_chk_sw_ena is used to enable checker Reset value is 0.

Table 48: PAM RX PMON CHK CSR1 (0x5800_12d4)

Field	Field Name	Access	Description
31:15	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
14	md_pmon_berr_acc_mode	R/W	PMON checker, bit/burst error accumulator mode. 0 = Even: Even bit errors, Odd: Odd bit errors 1 = Even: Total bit errors, Odd: Burst errors Reset value is 0.
13	md_pmon_timer_read	R/W	PMON checker, interval timer value read select. 0 = pmon_md_berr_value_odd: Odd bit/burst error accumulator value 1 = pmon_md_berr_value_odd: Interval timer value Reset value is 0.
12	md_pmon_timer_mode	R/W	PMON checker, interval timer mode select. 0 = Interval Timer runs for one interval and then stops 1 = Interval Timer runs continuously (never stops) Reset value is 0.
11:10	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
9:8	md_pmon_burst_err_wdw	R/W	PMON checker, burst error window: 1. Defines the number of clock cycles (1 through 4) the burst error threshold must persist for a burst error to exist. Reset value is 0.
7	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
6:0	md_pmon_burst_err_thr	R/W	PMON checker, burst error threshold: 1. Defines the number of bit errors per clock cycle (1 through 128) that must be present for a burst error to exist. Reset value is 0.

Table 49: PAM RX PMON CHK CSR2 (0x5800_12d8)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	md_pmon_timer_per	R/W	PMON checker, interval timer period. These bits define the MS 16 bits of the 32-bit interval timer period. Note that the LS 16 bits of the timer period are always 16'hffff. Default = 042Ch = 100.0 ms at 700 MHz, 119.5 ms at 586 MHz. Reset value is 0x42c.

Table 50: PAM RX PMON CHK CSR3 (0x5800_12dc)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	pmon_md_berr_value_odd_lo	RO	PMON checker, odd/MSB BER ACC value low. LS 16 bits of the 32-bit Odd/MSB BER accumulator. Reset value is 0.

Table 51: PAM RX PMON CHK CSR4 (0x5800_12e0)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	pmon_md_berr_value_odd_hi	RO	PMON checker, odd/MSB BER ACC value high. MS 16 bits of the 32-bit Odd/MSB BER accumulator. Reset value is 0.

Table 52: PAM RX PMON CHK CSR5 (0x5800_12e4)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	pmon_md_berr_value_even_lo	RO	PMON checker, even/LSB BER ACC value low. LS 16 bits of the 32-bit Even/LSB BER accumulator. Reset value is 0.

Table 53: PAM RX PMON CHK CSR6 (0x5800_12e8)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	pmon_md_berr_value_even_hi	RO	PMON checker, even/LSB BER ACC value high. MS 16 bits of the 32-bit Even/LSB BER accumulator. Reset value is 0.

Table 54: PAM RX PMON CHK CSR7 (0x5800_12ec)

Field	Field Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	pmon_md_timer_hi	RO	PMON checker, interval timer high. MS 16 bits of the 32-bit interval timer. Reset value is 0.

4.3 Line-Side Registers

Table 55: TXFIR MICRO CONTROL0 (0x5003_44c0)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	tx_eee_alert_en	R/W	TX EEE alert mode control. 1 = Enable EEE alert mode when pmd_tx_mode (input pins) == 2'b10 0 = Disable EEE alert mode Reset value is 1.
14	tx_eee_quiet_en	R/W	TX EEE quiet mode control. 1 = Enable EEE quiet mode when pmd_tx_mode (input pins) == 2'b01 0 = Disable EEE quiet mode Reset value is 1.
13:10	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.

Table 55: TXFIR MICRO CONTROL0 (0x5003_44c0) (Continued)

Bits	Name	Type	Description
9:4	tx_disable_timer_ctrl	R/W	tx_disable timer value controls. tx_disable_timer_ctrl[5] (MSB) selects the timer units. 0 = 2 µs units 1 = 1 ms units tx_disable_timer_ctrl[4:0] (LSB[4:0]) = controls the number of units per this list: 0 = 0 units 1 = 1 units 2 = 2 units 3 = 3 units 4 = 4 units 5 = 5 units 6 = 6 units 7 = 7 units 8 = 8 units 9 = 10 units 10 = 12 units 11 = 14 units 12 = 16 units 13 = 20 units 14 = 24 units 15 = 28 units 16 = 32 units 17 = 40 units 18 = 48 units 19 = 56 units 20 = 64 units 21 = 80 units 22 = 96 units 23 = 112 units 24 = 128 units 25 = 160 units 26 = 192 units 27 = 224 units 28 = 256 units 29 = 320 units 30 = 384 units 31 = 448 units Reset value is 0x16.
3	pmd_tx_disable_pkill	R/W	TX disable using the pmd_tx_disable pin disable control. 0 = Enable TX disable from pmd_tx_disable pin 1 = Disable TX disable from pmd_tx_disable pin Reset value is 0.

Table 55: TXFIR MICRO CONTROL0 (0x5003_44c0) (Continued)

Bits	Name	Type	Description
2	dp_reset_tx_disable_dis	R/W	TX disable based on data path reset. 0 = Enable TX disable based on data path reset 1 = Disable TX disable based on data path reset Must set this bit to 1 if tx_disable_output_sel = 2'b01 (send TX power-down). Reset value is 0.
1	tx_disable_trigger	SC	TX disable trigger. When this bit is set to 1, it triggers a TX disable with timer starting at 0. No matter where the TX disable state is, it starts a new timer and applies TX disable. This bit is self-clearing. Reset value is 0.
0	micro_tx_disable	R/W	Micro TX disable. This field is used by the microcontroller for TX disable control during CL93N72 forced mode. Reset value is 0.

Table 56: TXFIR MISC CONTROL0 (0x5003_44c4)

Bits	Name	Type	Description
31:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
3:2	tx_disable_output_sel	R/W	These bits select TX disable output function: 2'b00 = Send electrical idles 2'b01 = Send power-down 2'b10 = Send ones 2'b11 = Send zeroes Reset value is 0.
1	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
0	sdk_tx_disable	R/W	SDK TX disable. This TX disable control field is for SDK use during TX programming. Reset value is 0.

Table 57: TXFIR MISC STATUS0 (0x5003_44c8)

Bits	Name	Type	Description
31:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	tx_elec_idle_status	RO	TX electrical idle status. When this bit is set, it indicates the TX electrical idle active due to: ■ TX disable being programmed to send electrical idles or ■ An internal logic signal derived from PMD interface pins for EEE TX MODE Reset value is 1.
0	tx_disable_status	RO	TX disable status. When this bit is set, it indicates the tx_disable is active due to: ■ Pin at AN/PCS to PMD interface OR ■ dp_reset being asserted ■ Register bit dedicated to micro use ■ Register bit dedicated to SDK use ■ TX disable timer that guarantees minimum assertion time has not expired Reset value is 1.

Table 58: TXFIR TAP CONTROL0 (0x5003_44cc)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	txfir_test_data_en	R/W	TXFIR DAC test data enable. 1 = Test mode. Enables test data path from the DAC memory to the DAC for characterization. 0 = Normal modes. TXFIR DAC driver is used to drive the DAC. Reset value is 0.
14	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
13:12	txfir_tap_en	R/W	TXFIR taps enable: 2'd0 = tap2:tap0 2'd1 = tap5:tap0 2'd2 = tap8:tap0 2'd3 = tap11:tap0 Reset value is 3.
11	txfir_tap_load	SC	Load TXFIR tap values. The sequence to load the taps is: 1. Set taps values in the txfir_tap*_coeff fields as needed. 2. Set txfir_tap_load field to 1'b1. This field is self-clearing; always reads back 0. Reset value is 0.
10	txfir_nrz_tap_range_sel	R/W	TXFIR NRZ tap range select. 0 = PAM-4 tap range –170 to +170 1 = NRZ tap range –127 to +127 Reset value is 0.

Table 58: TXFIR TAP CONTROL0 (0x5003_44cc) (Continued)

Bits	Name	Type	Description
9	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
8:0	txfir_tap0_coeff	R/W	TXFIR tap 0 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 59: TXFIR TAP CONTROL1 (0x5003_44d0)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap1_coeff	R/W	TXFIR tap 1 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 60: TX FIR TAP CONTROL2 (0x5003_44d4)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap2_coeff	R/W	TXFIR tap 2 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0xa8.

Table 61: TXFIR TAP CONTROL3 (0x5003_44d8)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap3_coeff	R/W	TXFIR tap 3 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 62: TXFIR TAP CONTROL4 (0x5003_44dc)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap4_coeff	R/W	TXFIR tap 4 coefficient values in signed 2's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 63: TXFIR TAP CONTROL5 (0x5003_44e0)

Bits	Name	Type	Description
31:9	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
8:0	txfir_tap5_coeff	R/W	TXFIR tap 5 coefficient values in signed two's complement format. Tap range: –170 to +170 in PAM-4 mode, –127 to +127 in NRZ mode. Reset value is 0x0.

Table 64: TXFIR TAP CONTROL6 (0x5003_44e4)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	txfir_level_shift_mode_en	R/W	Level shifting enable. Level shifting is achieved by repurposing the last 6 taps such that taps 6 through 8 provide level adjustment for level = 3, and taps 9 through 11 for level = –3. 1 = Enabled 0 = Disabled Reset value is 0.
14:8	txfir_dc_adjust	R/W	This field specifies the amount of DC offset added to TXFIR output. The range is –64 to +63. Reset value is 0.
7	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
6:0	txfir_tap6_coeff	R/W	TXFIR tap 6 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 65: TXFIR TAP CONTROL7 (0x5003_44e8)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap7_coeff	R/W	TXFIR tap 7 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 66: TXFIR TAP CONTROL8 (0x5003_44ec)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap8_coeff	R/W	TXFIR tap 8 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 67: TXFIR TAP CONTROL9 (0x5003_44f0)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap9_coeff	R/W	TXFIR tap 9 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 68: TX FIR TAP CONTROL10 (0x5003_44f4)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap10_coeff	R/W	TXFIR tap 10 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 69: TXFIR TAP CONTROL11 (0x5003_44f8)

Bits	Name	Type	Description
31:7	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
6:0	txfir_tap11_coeff	R/W	TXFIR tap 11 coefficient values in signed two's complement format. Tap range: –64 to +63 in PAM-4 mode, –24 to +23 in NRZ mode. Reset value is 0x0.

Table 70: PRBS CHK CNT CONFIG (0x5003_4580)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	rx_trn_active_auto_mode_en	R/W	1'b1 forcefully disables the below described RX datapath functions automatically while RX link training is enabled and active irrespective of these register bit settings: ■ PAM-4 Gray Decoder (enabled by field pam4_gray_dec_en) ■ PAM-4 Decoder (enabled by field pam4_decoder_en) ■ PAM-4 Symbol bit-swap (enabled by field pam4_rx_symbol_bit_swap) ■ PAM-4 back-channel decoder (enabled by field bc_dec_en) ■ PAM-4 descrambler (enabled by field rx_descrambler_en) ■ NRZ differential decoder (enabled by field tlb_rx_diff_dec_en) 1'b0 ignores the control signal from RX link training and the above RX datapath functions are enabled based on their individual enable bits irrespective of the RX training status being enabled or disabled. Reset value is 0x1.
14:13	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
12:8	prbs_chk_ool_cnt	R/W	Specifies the number of consecutive valid clock cycles with 1 or more bit errors for PRBS checker to go out of PRBS lock state. Valid values are 0 to 31, where 0 indicate that PRBS will go out of lock as soon as it gets the first clock cycle with 1 or more bit errors. Likewise, 31 indicates that PRBS goes out of lock as soon as it gets the 32 consecutive clocks with 1 or more errors. Reset value is 0x6.
7:5	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
4:0	prbs_chk_lock_cnt	R/W	Specifies the number of consecutive valid clock cycles without any bit error for PRBS checker to go into PRBS lock state. Valid values are 0 to 31, where 0 indicate that PRBS will lock as soon as it gets the first clock cycle with no bit error. Likewise, 31 indicates that PRBS locks as soon as it gets the 32 consecutive clocks with no error. Reset value is 0x2.

Table 71: PRBS CHK CONFIG (0x5003_4584)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	prbs_chk_burst_err_cnt_en	R/W	PRBS checker burst error count mode enable. 1'b1 will enable the PRBS checker burst error count mode. It should be enabled for prbs_chk_burst_err_cnt counter. Make sure that only one of the 2 register settings ((prbs_chk_en_timer_mode ≥2 and prbs_chk_en_timeout > 0) and prbs_chk_burst_err_cnt_en) are TRUE at any given time and not simultaneously TRUE. Reset value is 0x0.
14:13	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
12	prbs_chk_mode_sel_msb	R/W	Extending PRBS polynomial select by using this bit as bit[3] along with prbs_chk_mode_sel[2:0]. 1'b0 will select old PRBS polynomials for PRBS 7, 9, 11, 15, 23, 31, 49, and 58 based on prbs_chk_mode_sel[2:0]. 1'b1 will select new PRBS polynomials for PRBS 10, 20, 13 for PAM-4 based on prbs_chk_mode_sel[2:0]. 1'b1 and prbs_chk_mode_sel[2:0] == 0 will select PRBS 10. 1'b1 and prbs_chk_mode_sel[2:0] == 1 will select PRBS 20. 1'b1 and prbs_chk_mode_sel[2:0] == 2 will select PRBS 13. 1'b1 and prbs_chk_mode_sel[2:0] == 2 will select PRBS 13 with polynomial (1 + x^1 + x^2 + x^12 + x^13). This pattern is also used for PAM-4 link training lane 0 pattern. 1'b1 and prbs_chk_mode_sel[2:0] == 3 is reserved for future use. 1'b1 and prbs_chk_mode_sel[2:0] == 4 will select PAM-4 link training lane 1 PRBS 13 polynomial (1 + x2 + x3 + x7 + x13). Debug modes. 1'b1 and prbs_chk_mode_sel[2:0] == 5 will select PAM-4 link training lane 2 PRBS 13 polynomial (1 + x2 + x4 + x8 + x13). Debug modes. 1'b1 and prbs_chk_mode_sel[2:0] == 6 will select PAM-4 link training lane 3 PRBS 13 polynomial (1 + x2 + x5 + x9 + x13). Debug modes. 1'b1 and prbs_chk_mode_sel[2:0] == 7 is reserved for future use. Reset value is 0x0.
11	prbs_chk_clk_en_frc_on	R/W	PRBS checker clock enable. 1'b1 enables the PRBS checker clock. Recommended to be enabled before enabling the prbs_chk_en. Reset value is 0x0.
10	trnsum_error_count_en	R/W	Training sum error counter mode enable. 1 = Makes the PRBS error counter used as trnsum_error counter. PRBS checker cannot be used during this mode. 0 = PRBS checker mode Reset value is 0x0.

Table 71: PRBS CHK CONFIG (0x5003_4584) (Continued)

Bits	Name	Type	Description
9	prbs_chk_err_cnt_ burst_mode	R/W	PRBS error counter mode. 1 = Each burst of error is counted as 1 error in the error counter. Each error burst must be separated by 1 error-free cycle of data which in worst case should be 39 bits. 0 = Each bit error is counted Reset value is 0x0.
8	prbs_burst_len_chk_ en	R/W	0 = Disable 1 = Enable (default) Reset value is 0x1.
7	prbs_chk_en_auto_ mode	R/W	PRBS checker enable mode control. 1 = Select (rx_dsc_lock and prbs_chk_en) as PRBS checker enable control 0 = Select prbs_chk_en as PRBS checker enable control Reset value is 0x0.
6:5	prbs_chk_mode	R/W	PRBS LOCK state machine select. 2'd0 = Self-sync mode w/ hysteresis. PRBS seed register is continuously seeded with previous received bits. This mode results in faster locking, but bit errors are counted multiple times (often by 3x). 2'd1 = Initial seed mode w/ hysteresis. PRBS seed registers is seeded with previous received bits only till PRBS lock is acquired and then they run locally independently from the received data until the checker goes out of PRBS lock. 2'd2 = Initial seed mode w/o hysteresis. Similar to mode 1 above except once locked it stays locked until PRBS is disabled. 2'd3 = Reserved for future use. Reset value is 0x1.
4	prbs_chk_inv	R/W	PRBS invert enable. 1 = Inverts all the data bits to the PRBS checker 0 = Sends normal data to the PRBS checker Reset value is 0x0.
3:1	prbs_chk_mode_sel	R/W	PRBS checker mode select. Selects the PRBS polynomial as shown here: 3'd0 = PRBS 7 3'd1 = PRBS 9 3'd2 = PRBS 11 3'd3 = PRBS 15 3'd4 = PRBS 23 3'd5 = PRBS 31 3'd6 = PRBS 58 (1 + x^39 + x^58) 3'd7 = PRBS 49 (1 + x^40 + x^49) Reset value is 0x5.
0	prbs_chk_en	R/W	PRBS checker enable. 1 = Enable the PRBS checker 0 = Disable the PRBS checker Reset value is 0x0.

Table 72: DIG LPBK CONFIG (0x5003_4588)

Bits	Name	Type	Description
31:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
3	dig_lpbk_pd_bias_en	R/W	1'b1 enables PD increment bias mode where there is increment generated every 16th clock cycle. 1'b0 disables the PD bias mode so increase/decrease is generated based on the PD output. Reset value is 0x1.
2	dig_lpbk_pd_flt_ bypass	R/W	Digital loopback phase detector filter bypass. For repeater applications, it should be 1'b1. For other applications filter can be enabled for better jitter tolerance performance for the digital loopback. Reset value is 0x1.
1	dig_lpbk_pd_mode	R/W	Digital loopback phase detector mode. For normal operating conditions keep it at the default value of 1'b1. 1'b0 = Swap increase/decrease 1'b1 = Normal mode Reset value is 0x1.
0	dig_lpbk_en	R/W	TX to RX parallel loopback (digital loopback) enable. 1 = Loopback is enabled 0 = Loopback is disabled Reset value is 0x0.

Table 73: TLB RX MISC CONFIG (0x5003_458c)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	prbs_chk_auto_detect _relock_en	R/W	PRBS checker auto-detect relock enable. If enabled, then it will go and start the auto-detect upon loss of signal once it already found a valid auto-detect lock. Reset value is 0x0.
14	prbs_chk_auto_detect _en	R/W	PRBS checker auto-detect mode enable. If enabled then it will go through all the supported PRBS polynomials in round-robin fashion and search for prbs_chk_lock = 1 until AUTO-DETECT SEARCH timer is expired. Reset value is 0x0.
13	Reserved	RSVD	Reserved bit must be written with 0. A read returns an unknown value.
12:8	prbs_chk_auto_detect _cnt	R/W	Specifies the timer for the auto-detect search in each polynomial setting. Reset value is 0x7.

Table 73: TLB RX MISC CONFIG (0x5003_458c) (Continued)

Bits	Name	Type	Description
7	pam4_rx_symbol_bit_swap	R/W	PAM-4 Symbol bits {A,B} swap enable. Enable it only for the PAM-4 modes. Bit swapping is done just after the PAM-4 gray decoder. 1 = 2-bit PAM-4 symbol bits are swapped, where PAM-4 symbol bits {A,B} maps to the datastream bits {[n+1], [n]}, where n is the first bit in receive order. 0 = No swapping, default mode. PAM-4 symbol bits {A,B} maps to the datastream bits {[n], [n+1]}, where n is the first bit in receive order. Reset value is 0x0.
6	pam4_decoder_en	R/W	PAM-4 decoder enable. Enable it only for the PAM-4 NS mode. 1 = PAM-4 decoder is enabled 0 = PAM-4 decoder is disabled Reset value is 0x0.
5	pam4_gray_dec_en	R/W	PAM-4 gray decoder enable. Enable it only for the PAM-4 modes. 1 = PAM-4 Gray decoder is enabled 0 = PAM-4 Gray decoder is disabled Reset value is 0x0.
4	tlb_rx_nrz_ll_mode_en	R/W	RX low-latency mode enable for the NRZ OSR modes. It is not applicable to the PAM-4 modes. When enabled by writing to 1'b1 for NRZ OS modes, following will be the data format on the 40 bit RX data bus. RX data_valid will be forced to 1'b1 in this case. PCS RX data can be fed directly to the PCS TX data (with TX native analog format mode bit enabled) on the other end for Repeater Applications. OS1/2/4 modes: 20 bits of RX data will be replicated in 2 consecutive odd/even bits to form the 40-bit data bus going out to PCS. OS8/16/32 modes: 20 bits of over-sampled RX data will be replicated in 2 consecutive odd/even bits to form the 40-bit data bus going out to PCS. OS16.5/OS20.25 modes: 20 bits of over-sampled RX data is replicated in two consecutive odd/even bits to form the 40-bit data bus going out to PCS. Reset value is 0x0.
3	tlb_rx_diff_dec_en	R/W	1'b1 enables the Differential Decoder for pmd_rx_data. Only applicable to PCS RX data in OS1, 2, and 4 modes. Write it to 1'b0 for 1G OSR modes 16P5 and 20P625. Reset value is 0x0.
2	dbg_mask_dig_lpbk_en	R/W	Mask bit for dig_lpbk_en in the pmd_rx_lock equation. This is a debug register. 1 = pmd_rx_lock is forced to 1'b0 during digital loopback 0 = pmd_rx_lock is forced to 1'b1 during digital loopback Reset value is 0x0.

Table 73: TLB RX MISC CONFIG (0x5003_458c) (Continued)

Bits	Name	Type	Description
1	rx_descrambler_en	R/W	PAM-4 RX datapath descrambler enable. Applicable only for the PAM-4 modes with PRBS or PCS data. Not applicable when external FEC feedback is used. 1 = PAM-4 RX datapath descrambler is enabled. If rx_descrambler_en is enabled then 40 bits of the transmitted data will be XORed with the 40 MSB bits of the fixed pattern sequence register {patt_gen_seq_14[15:0], patt_gen_seq_13[15:0], patt_gen_seq_12[15:8]}. Make sure {patt_gen_seq_14[15:0], patt_gen_seq_13[15:0], patt_gen_seq_12[15:8]} bits are only re-programmed or changed when rx_descrambler_en reg field is 1'b0. 0 = PAM-4 RX datapath descrambler is disabled Reset value is 0x0.
0	rx_pmd_dp_invert	R/W	RX PMD datapath invert control. When enabled by writing to 1'b1, it inverts all the datapath bits of the logical lane. Recommended for use in case P and N pads are swapped on the PCB board. Reset value is 0x0.

Table 74: PRBS CHK EN TIMER CONTROL (0x5003_4590)

Bits	Name	Type	Description
31:13	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
12:8	prbs_chk_en_timeout	R/W	PRBS timer timeout value. Valid range 0 to 31 which maps to 0 to 448. Should be programmed before enabling the PRBS checker in timer mode. Reset value is 0x0.
7:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1:0	prbs_chk_en_timer_mode	R/W	prbs_chk_en timer mode. 2'b0x = prbs_chk_en timer is disabled and PRBS checker mode is enabled as per prbs_chk_en register. 2'b10 = Use heartbeat_toggle_1us for the timer. 2'b11 = Use heartbeat_toggle_1ms for the timer. Make sure that only one of the two register settings ((prbs_chk_en_timer_mode ≥2 and prbs_chk_en_timeout > 0) and prbs_chk_burst_err_cnt_en) are TRUE at any given time and not simultaneously TRUE. Reset value is 0x0.

Table 75: PRBS CHK BURST ERR CNT STATUS (0x5003_4594)

Bits	Name	Type	Description
31:10	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
9:0	prbs_chk_burst_err_cnt	RO	TYPE CR. PRBS Checker Burst Error Counter Status register. It is a clear-on-read register. This register counts the number of bursts in errors separated by at least 1 clock cycle worth of data without any bit in error. prbs_chk_burst_err_cnt_en should be set to 1'b1 for this counter to work. Reset value is 0x0.

Table 76: DBG PMD LOCK STATUS (0x5003_4598)

Bits	Name	Type	Description
31:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	dbg_pmd_rx_lock_change	RO	Type CR. Set to 1'b1 when change/transition on PMD RX LOCK. This is a sticky bit and cleared upon read. This is a debug register. Reset value is 0x0.
0	dbg_pmd_rx_lock	RO	Debug PMD RX lock indication. This is a live indication of the status of the pmd_rx_lock output port. 1 = PMD is in LOCKED state and RX PCS data should have acceptable BER 0 = PMD is not locked yet Reset value is 0x0.

Table 77: UC PMD LOCK STATUS (0x5003_459c)

Bits	Name	Type	Description
31:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	uc_pmd_rx_lock_change	RO	Type CR. Set to 1'b1 when change/transition on PMD RX lock. This is a sticky bit and cleared upon read. This is a debug register. Reset value is 0x0.
0	uc_pmd_rx_lock	RO	Debug PMD RX LOCK Indication. This is a live indication of the status of the pmd_rx_lock output port. 1 = PMD is in locked state and RX PCS data should have acceptable BER 0 = PMD is not locked yet Reset value is 0x0.

Table 78: DIG LPBK PD STATUS (0x5003_45a0)

Bits	Name	Type	Description
31:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
13	prbs_chk_mode_sel_msb_auto_detect	RO	Valid only when prbs_chk_auto_detect_lock = 1. Equivalent to prbs_chk_mode_sel_msb register in auto-detect mode. Reset value is 0x0.
12:10	prbs_chk_mode_sel_auto_detect	RO	Valid only when prbs_chk_auto_detect_lock = 1. Equivalent to prbs_chk_mode_sel register in auto-detect mode. Reset value is 0x0.
9	prbs_chk_inv_auto_detect	RO	Valid only when prbs_chk_auto_detect_lock = 1. Indicates the PRBS polynomial invert bit. Reset value is 0x0.
8	prbs_chk_auto_detect_lock	RO	Live indication of auto-detect Lock. Set to 1'b1 once auto-detect finds the PRBS lock. Reset value is 0x0.
7:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	dig_lpbk_pd_early_ind	RO	1 means dp_rclk20 is sampling data earlier so delay the dp_rclk20 clock phase. This results in RX PI phase step increment. Reset value is 0x1.
0	dig_lpbk_pd_late_ind	RO	1 means dp_rclk20 is sampling data late so reduce the delay of the dp_rclk20 clock phase. This will result in RX PI phase step decrement. Reset value is 0x0.

Table 79: PRBS CHK LOCK STATUS (0x5003_45a4)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:1	prbs_chk_err_cnt_no_clr	RO	PRBS checker error counter, which does not get cleared upon read. MSB bit 14 is OR of the MSB bits [30:14] of the internal error counter. LSB bits [13:0] are assigned to LSB bits [13:0] of the internal error counter. It can be cleared by reading the status register prbs_chk_err_cnt_msb. Reset value is 0x0.
0	prbs_chk_lock	RO	PRBS Checker LOCK Indication. This is a live indication of the status of the PRBS Checker state machine. 1 = PRBS checker is in locked state 0 = PRBS checker is out-of-lock state and state machine is searching for a lock Reset value is 0x0.

Table 80: PRBS CHK ERR CNT MSB STATUS (0x5003_45a8)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	prbs_chk_lock_lost_lh	RO	Type CR. PRBS checker LOCK_LOST latch high indication. This register captures the 1 to 0 transition on the prbs_chk_lock live status register and keep it latched until read. This is a clear-on-read status register. prbs_chk_lock_lost_lh status bit also indicate other PRBS checker states as shown here: ■ PRBS checker is currently not enabled || ■ PRBS checker is currently not locked || ■ PRBS_LOCK was lost when checker was enabled since the last read Reset value is 0x1.
14:0	prbs_chk_err_cnt_ msb	RO	Type CR. 15 bits MSB portion of PRBS Checker Error Counter Status register. It is a clear-on-read register. Once MSB bits [30:16] of the counter are read, then LSB bits [15:0] of the error counter are loaded into a holding register and all internal PRBS error counter's bits are cleared to 0s (or if there are any error in that particular clock cycle then that will be loaded). MSB portion must be read first before reading the LSB portion of the error counter Reset value is 0x0.

Table 81: PRBS CHK ERR CNT LSB STATUS (0x5003_45ac)

Bits	Name	Type	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	prbs_chk_err_cnt_lsb	RO	16 bits LSB portion of PRBS Checker Error Counter Status register. This register indicates the value in the holding register when MSB portion [30:16] of the error counter are read. MSB portion must be read first before reading the LSB portion of the error counter. Reset value is 0x0.

Table 82: PMD RX LOCK STATUS (0x5003_45b0)

Bits	Name	Type	Description
31:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	pmd_rx_lock_change	RO	Type CR. Set to 1'b1 when change/transition on PMD RX LOCK. This is a sticky bit and cleared upon read. Reset value is 0x0.
0	pmd_rx_lock	RO	PMD RX lock indication. This is a live indication of the status of the pmd_rx_lock output port. 1 = PMD is in locked state and RX PCS data should have acceptable BER 0 = PMD is not locked yet Reset value is 0x0.

Table 83: PRBS BURST ERR LENGTH STATUS (0x5003_45b4)

Bits	Name	Type	Description
31:6	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
5:0	prbs_burst_err_length_status	RO	Type CR. PRBS burst error length count. This is a live indication of the status of the PRBS burst error length and max at 6'd63. This register is cleared upon read. This register is supported for all the data traffic modes but only required for NRZ OSR modes OS1, OS2, and OS4 and PAM-4 NR/PAM-4 ER modes with and without back channel enabled. Reset value is 0x0.

Table 84: MAX PRBS BURST ERR LENGTH (0x5003_45b8)

Bits	Name	Type	Description
31:6	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
5:0	max_prbs_burst_err_length_status	RO	Type CR. PRBS burst error max length count. This is the status of the PRBS burst error max length and max at 6'd63. This register is cleared upon read. This register is supported for all the data traffic modes but only required for NRZ OSR modes OS1, OS2, and OS4 and PAM-4 NR/PAM-4 ER modes with and without back channel enabled. Reset value is 0x0.

Table 85: MAX PRBS BURST ERR LENGTH (0x5003_45c0)

Bits	Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:12	patt_gen_start_pos	R/W	Valid values are 11 to 0. Defines the start position of the pattern in 20-bit chunks. 11 means start at bit 239. 10 means start at bit 219. 0 means start at bit 19. so start bit is (rg_patt_gen_start_pos × 20 + 19). Reset value is 0xb.
11:8	patt_gen_stop_pos	R/W	Valid values are 11 to 0. Defines the stop position of the pattern in 20-bit chunks. This register value should be less than or equal to rg_patt_gen_start_pos. 11 means stop at bit 220. 10 means stop at bit 200. 0 means stop at bit 0. So stop bit is (rg_patt_gen_stop_pos × 20). Reset value is 0x0.
7	pam4_tx_jp03b_patt_en	R/W	JP03B fixed pattern enable. Higher priority than pam4_tx_linearity_patt_en if both bits are enabled simultaneously. Make sure gray encoder and PAM-4 precoder is disabled for this fixed pattern mode. 1 = Enable the fixed pattern for JP03B pattern of 124 bits (that is, 62 symbols) long repeating pattern of {15{00,11}} + {16{11,00}}. Program reg field patt_gen_seq_1[15:8] bits = 8'b_0011_1100 = 8'h3C before enabling this pattern. Transmission order is MSB first. If this bit is enabled then make sure that other lane fixed pattern do not use fixed pattern 20-bit chunk of bits 39:20. 0 = Disable the JP03B fixed pattern generation Reset value is 0x0.
6	pam4_tx_linearity_patt_en	R/W	PAM-4 transmitter linearity pattern enable. Lower priority than pam4_tx_jp03b_patt_en if both bits are enabled simultaneously. Make sure gray encoder and PAM-4 precoder is disabled for this fixed pattern mode. 1 = Enable the fixed pattern for PAM-4 transmitter linearity pattern of 320 bits (that is, 160 symbols) long repeating pattern of 10 PAM-4 levels of {–1, –1/3, +1/3, +1, –1, +1, –1, +1, +1/3, –1/3}, where each level is 16UI in duration. Program reg field {patt_gen_seq_1[3:0], patt_gen_seq_0[15:0]} bits = 20'b_0001_1011_0011_0011_1001 = 20'h1B339 before enabling this pattern. Transmission order is MSB first. If this bit is enabled then make sure that other lane fixed pattern do not use fixed pattern 20-bit chunk of bits 19:0. 0 = Disable the PAM-4 transmitter linearity pattern generation Reset value is 0x0.
5:1	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.

Table 85: MAX PRBS BURST ERR LENGTH (0x5003_45c0) (Continued)

Bits	Name	Access	Description
0	patt_gen_en	R/W	Fixed pattern generator enable. 1 = Enable the fixed pattern generator 0 = Disable the fixed pattern generator Reset value is 0x0.

Table 86: PRBS GEN CONFIG (0x5003_45c4)

Field	Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15	prbs_gen_pause_ strobe	SC	PRBS generator pause strobe (debug register). It is a self-clearing register bit. Writing to 1 pauses the PRBS generator for 1 clock cycle, which means same 40 bits of data are replicated in the paused clock cycle. This results in loss of PRBS checker lock on the link partner. Reset value is 0x0.
14:13	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
12	prbs_gen_mode_sel_ msb	R/W	Extending PRBS polynomial select by using this bit as bit[3] along with prbs_gen_mode_sel[2:0]. 1'b0 selects old PRBS polynomials for PRBS 7, 9, 11, 15, 23, 31, 49, and 58 based on prbs_gen_mode_sel[2:0]. 1'b1 selects new PRBS polynomials for PRBS 10, 20, 13 for PAM-4 based on prbs_gen_mode_sel[2:0]. 1'b1 and prbs_gen_mode_sel[2:0] == 0 will select PRBS 10. 1'b1 and prbs_gen_mode_sel[2:0] == 1 will select PRBS 20. 1'b1 and prbs_gen_mode_sel[2:0] == 2 will select PRBS 13 with polynomial (1 + x^1 + x^2 + x^12 + x^13). This pattern is also used for PAM-4 link training lane 0 pattern. 1'b1 and prbs_gen_mode_sel[2:0] == 3 is reserved for future use. 1'b1 and prbs_gen_mode_sel[2:0] == 4 will select PAM-4 link training lane 1 PRBS 13 polynomial (1 + x2 + x3 + x7 + x13). Debug modes so auto-detect and self-sync mode is not supported. 1'b1 and prbs_gen_mode_sel[2:0] == 5 will select PAM-4 link training lane 2 PRBS 13 polynomial (1 + x2 + x4 + x8 + x13). Debug modes so auto-detect and self-sync mode is not supported. 1'b1 and prbs_gen_mode_sel[2:0] == 6 will select PAM-4 link training lane 3 PRBS 13 polynomial (1 + x2 + x5 + x9 + x13). Debug modes so auto-detect and self-sync mode is not supported. 1'b1 and prbs_gen_mode_sel[2:0] == 7 is reserved for future use. Reset value is 0x0.
11:6	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.

Table 86: PRBS GEN CONFIG (0x5003_45c4) (Continued)

Field	Name	Access	Description
5	prbs_gen_err_ins	R/W	PRBS error insert. 0 to 1 transition on this signal will insert single bit error in the MSB bit of the data bus. Reset value is 0x0.
4	prbs_gen_inv	R/W	PRBS invert enable. 1 = Inverts all the data bits from the PRBS generator 0 = Sends normal data from the PRBS generator Reset value is 0x0.
3:1	prbs_gen_mode_sel	R/W	PRBS generator mode select. Selects the PRBS polynomial as shown here: 3'd0 = PRBS 7 3'd1 = PRBS 9 3'd2 = PRBS 11 3'd3 = PRBS 15 3'd4 = PRBS 23 3'd5 = PRBS 31 3'd6 = PRBS 58 (1 + x^39 + x^58) 3'd7 = PRBS 49 (1 + x^40 + x^49) Reset value is 0x5.
0	prbs_gen_en	R/W	PRBS generator enable. 1 = Enable the PRBS generator 0 = Disable the PRBS generator Reset value is 0x0.

Table 87: RMT LPBK CONFIG (0x5003_45c8)

Field	Name	Access	Description
31:3	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
2	rmt_lpbk_pd_frc_on	R/W	Remote loopback PD enable by force irrespective of rg_rmt_lpbk_en. 1'b1 = enable the phase detector without the remote loopback enable. Can be used to lock RX and TX clock phases when there is a remote loopback outside PMD Reset value is 0x0.
1	rmt_lpbk_pd_mode	R/W	Remote loopback phase detector mode. For normal operating conditions keep it at the default value of 1'b1. 1'b0 = Swap increase/decrease 1'b1 = Normal mode Reset value is 0x1.
0	rmt_lpbk_en	R/W	RX to TX parallel loopback (remote loopback) enable. 1 = Loopback is enabled 0 = Loopback is disabled Reset value is 0x0.

Table 88: TLB TX MISC CONFIG (0x5003_45cc)

Field	Name	Access	Description
31:5	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
4	tx_trn_active_auto_mode_en	R/W	1'b1 forcefully disables the below described TX datapath functions automatically while TX link training is enabled and active irrespective of these register bit settings: ■ PAM-4 gray encoder (enabled by field pam4_gray_enc_en) ■ PAM-4 precoder (enabled by field pam4_precoder_en) ■ PAM-4 symbol bit-swap (enabled by field pam4_tx_symbol_bit_swap) ■ NRZ differential encoder (enabled by field tlb_tx_diff_enc_en) In addition to these functions, back-channel encoder and scrambler are always disabled while TX link training is enabled and active irrespective of this register value. 1'b0 ignores the control signal from TX link training and the above TX datapath functions are enabled based on their individual enable bits irrespective of the TX training status being enabled or disabled. Reset value is 0x1.
3	tlb_tx_diff_enc_en	R/W	1'b1 will enable the differential encoder for pmd_tx_data. Only applicable to PCS TX data in OS1, 2, and 4 modes. Write it to 1'b0 for 1G OSR modes 16P5 and 20P625. Reset value is 0x0.
2	tx_mux_sel_order	R/W	TX data mux select priority order. When 1'b1 then priority of Pattern and PRBS generators are swapped w.r.t. CL72. 0 = TX data mux select order from higher to lower priority is {rmt_lpbk, patt_gen, cl72_tx, prbs_gen, tx_pcs} 1 = TX data mux select order from higher to lower priority is {rmt_lpbk, prbs_gen, cl72_tx, patt_gen, tx_pcs} Reset value is 0x0.
1	tx_pcs_native_ana_frmt_en	R/W	TX PCS Interface Native Analog Format Enable. 1 = TX PCS interface is enabled in the native analog format mode. TX PCS sends the over-sampled data in this mode which is sent directly to AFE. 0 = Raw data mode, where for every data request TX PCS sends 20 bits of valid data Reset value is 0x0.
0	tx_pmd_dp_invert	R/W	TX PMD datapath invert control. When enabled by writing to 1'b1, it will invert all the datapath bits of the logical lane. Recommended for use in case P and N pads are swapped on the PCB board. Reset value is 0x0.

Table 89: TLB TX PAM-4 CONFIG 0 (0x5003_45d4)

Field	Name	Access	Description
31:4	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
3	pam4_tx_symbol_bit_swap	R/W	PAM-4 symbol bits {A,B} swap enable. Enable it only for the PAM-4 modes. Bit swapping is done just before the PAM-4 gray encoder. 1 = 2-bit PAM-4 symbol bits are swapped, where PAM-4 symbol bits {A,B} maps to the datastream bits {[n+1], [n]}, where n is the first bit in transmission order. 0 = No swapping, default mode. PAM-4 symbol bits {A,B} maps to the datastream bits {[n], [n+1]}, where n is the first bit in transmission order. Reset value is 0x0.
2	tx_scrambler_en	R/W	PAM-4 TX datapath scrambler enable. Applicable only for the PAM-4 modes with PRBS or PCS data. 1 = PAM-4 TX datapath scrambler is enabled. If tx_scrambler_en is enabled then 40 bits of the transmitted data will be XORed with the 40 LSB bits of the fixed pattern sequence register {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]}. Make sure {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]} bits are only re-programmed or changed when both tx_scrambler_en and bc_enc_err_ins_en reg fields are 1'b0. 0 = PAM-4 TX datapath scrambler is disabled Reset value is 0x0.
1	pam4_precoder_en	R/W	PAM-4 precoder enable. Enable it only for the PAM-4 modes. 1 = PAM-4 precoder is enabled 0 = PAM-4 precoder is disabled Reset value is 0x0.
0	pam4_gray_enc_en	R/W	PAM-4 gray encoder enable. Enable it only for the PAM-4 modes. 1 = PAM-4 gray encoder is enabled 0 = PAM-4 gray encoder is disabled Reset value is 0x0.

Table 90: RMT LPBK PD STATUS (0x5003_45e0)

Field	Name	Access	Description
31:2	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
1	rmt_lpbk_pd_early_ind	RO	1 means dp_tclk20 is sampling data earlier so delay the dp_tclk20 clock phase. This results in TX PI phase step increment. Reset value is 0x1.
0	rmt_lpbk_pd_late_ind	RO	1 means dp_tclk20 is sampling data late so reduce the delay of the dp_tclk20 clock phase. This results in TX PI phase step decrement. Reset value is 0x0.

Table 91: TLB TX BC ENC CONFIG 0 (0x5003_45e4)

Field	Name	Access	Description
31:11	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
10:8	bc_enc_frm_len_sel	R/W	Back-channel encoder frame length select control. Determines the distance between two adjacent back-channel frames. The following table explains the value of this register and BC frame length in multiples of 128 tclk20 cycles or 128 × 20 PAM-4 symbols. bc_enc_frm_len_sel[2:0] — BC frame length in multiples of 128 × 20 PAM-4 symbols. 0 — 1 1 — 16 × 2^0 2 — 16 × 2^1 3 — 16 × 2^2 4 — 16 × 2^3 5 — 16 × 2^4 6 — 16 × 2^5 7 — 16 × 2^6 Reset value is 0x0.
7:3	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
2	bc_enc_err_ins_en	R/W	Back-channel encoder error insert enable. Applicable only for the modes when BC encoder is enabled. tx_scrambler_en reg field should be disabled for BC encoder error insertion to work; otherwise, all the TX data is XORed instead and not only the BC encoder frame. 1 = Back-channel encoder error insert is enabled. If BC encoder error insertion is enabled and tx_scrambler_en is disabled then 40 bits of the transmitted BC frame is XORed with the 40 LSB bits of the fixed pattern sequence register {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]}. Make sure {patt_gen_seq_2[7:0], patt_gen_seq_1[15:0], patt_gen_seq_0[15:0]} bits are only re-programmed or changed when both tx_scrambler_en and bc_enc_err_ins_en reg fields are 1'b0. 0 = Back-channel encoder error insert is disabled Reset value is 0x0.
1	bc_enc_update	SC	Type SC. Back-channel encoder update control. Self-clearing control register. Write this register to 1'b1 after updating the bc_enc_data and/or bc_enc_frm_len_sel fields. Updated information will be sent transmitted in the next back-channel encoder word/frame. Reset value is 0x0.

Table 91: TLB TX BC ENC CONFIG 0 (0x5003_45e4) (Continued)

Field	Name	Access	Description
0	bc_enc_en	R/W	Back-channel encoder enable. Applicable only to PAM-4 modes along with PRBS or PCS TX data sources. 1 = Back-channel encoder is enabled 0 = Back-channel encoder is disabled Reset value is 0x0.

Table 92: TLB TX BC ENC CONFIG 1 (0x5003_45e8)

Field	Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	bc_enc_data_lsb	R/W	Back-channel encoder data LSB bits [15:0]. Reset value is 0xf628.

Table 93: TLB TX BC ENC CONFIG 1 (0x5003_45ec)

Field	Name	Access	Description
31:16	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
15:0	bc_enc_data_msb	R/W	Back-channel encoder data LSB bits [15:0]. Reset value is 0x0.

Table 94: TLB TX BC ENC STATUS 0 (0x5003_45f8)

Field	Name	Access	Description
31:1	Reserved	RSVD	Reserved bits must be written with 0. A read returns an unknown value.
0	bc_enc_data_sent	RO	Type CR. Status bit (when set to 1) indicating that the first back-channel frame/word with the updated BC data and/or frame length has been transmitted. Reset value is 0x0.

Chapter 5: Electrical Characteristics

These tables detail the BCM81724 electrical characteristics.

Table 95: Power Consumption with AVS

Parameter	Condition	Min.	Typ.	Max.	Unit
8 × 56G PAM-4 to 16 × 25 G NRZ Forward and Reverse Gearbox modes	No FEC	—	7.2	—	W
8 × 56G PAM-4 to 16 × 25G NRZ Forward and Reverse Gearbox modes	KP4 FEC to KR4 FEC	—	8.1	—	W
8 × 56G PAM-4 to 16 × 25G NRZ Forward and Reverse Gearbox modes	KP4 FEC to PCS FEC	—	8	—	W
8 × 56G PAM-4 Retimer mode	No FEC	—	5.6	—	W
8 × 56G PAM-4 Retimer mode	KP4 FEC to KP4 FEC	—	6.5	—	W

Table 96: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Storage temperature	–45	—	+150	°C
Supply voltage on VDDIO	–0.3	—	2.1	V
Supply voltage on VDD_MDIO	–0.3V	—	2.1	V
Supply voltage on PVDD0P8, TVDD0P8, RVDD0P8, H_PVDD0P8, H_TVDD0P8, H_RVDD0P8, AVS, and VDDM	–0.3	—	1	V
Voltage on any CML, CMOS, or LVPECL input pin with respect to VSS	–0.3	—	VDDIO + 0.3	V
Supply voltage on TVDDDRV and H_TVDDDRV	–0.3	—	1.3	V
Supply voltage on PVDD1P8 and H_PVDD1P8	–0.3	—	2.1	V

CAUTION! Permanent damage may result if the device is stressed beyond the absolute maximum ratings. The device specifications are guaranteed only under the recommended operating conditions.

Table 97: Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Ambient temperature under bias	—	—	0	25	70	°C
Operating junction temperature	—	—	0	—	110	°C
Supply voltage on PVDD0P8_0, PVDD0P8_1, TVDD0P8, RVDD0P8_A, H_PVDD0P8_A, H_PVDD0P8_B, H_TVDD0P8_A, H_TVDD0P8_B, H_RVDD0P8_A, H_RVDD0P8_B, and VDDM	—	—	0.776	0.8	0.824	V
Supply voltage VDD	—	When AVS is disabled	0.684	0.72	0.756	V
Supply voltage on TVDDDRV, H_TVDDDRV_A, and H_TVDDDRV_B	—	0.8V mode	0.776	0.8	0.824	V
Supply voltage on TVDDDRV, H_TVDDDRV_A, and H_TVDDDRV_B	—	1.0V mode	0.97	1.0	1.03	V

Table 97: Recommended Operating Conditions (Continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage on PVDD1P8 and H_PVDD1P8	—	—	1.71	1.8	1.85	V
Supply voltage on VDD_MDIO	—	1.2V mode	1.14	1.2	1.26	V
	—	1.8V mode	1.71	1.8	1.85	V
Supply voltage on VDDIO	—	—	1.71	1.8	1.85	V
AVS voltage limits	—	0.72V mode	0.5	—	0.72	V
Ground voltage (VSS)	—	—	—	0	—	V
Reference clock frequency (typical)	—	—	—	156.25	—	MHz
Reference clock frequency tolerance asynchronous	—	—	–100	—	+100	ppm
Reference clock input voltage swing differential	Differential V_{DPP}	—	600	800	1200	mV
Reference clock duty cycle	—	—	40	—	60	%
Reference clock rise and fall times	—	20% to 80% of amplitude	—	—	600	ps
Reference clock jitter (phase jitter)	—	12 kHz to 20 MHz	—	—	0.25	psRMS

Table 98: Recovered Clock Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Recovered clock differential output amplitude	CLK_OUT_DIFF_P CLK_OUT_DIFF_N	—	—	400	—	mV
Recovered clock single-ended output amplitude	RCLK0 RCLK1	—	—	—	1.8	V

Table 99: Line-Side (Module) Output Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential peak-to-peak output swing	V_{DPP}	PAM-4 output	—	—	900	mV
Differential peak-to-peak output swing	V_{DPP}	NRZ output	—	—	1200	mV

Table 100: Line-Side Receiver (Module) Input Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential peak-to-peak input voltage	V_{DPP}	—	—	—	800	mV

Table 101: System-Side (ASIC) Output Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential peak-to-peak swing	V_{DPP}	—	—	900	mV

Table 102: System-Side (ASIC) Input Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential peak-to-peak input voltage	V_{DPP}	—	—	800	mV

Table 103: 1.8V CMOS DC Characteristics

Parameter	Condition	Specification			Unit
		Min.	Typ.	Max.	
CMOS output low voltage V_{OL}	—	—	—	0.4	V
CMOS output high voltage V_{OH}	8 mA*	1.4	—	—	V
CMOS input low voltage V_{IL}	—	—	—	0.63	V
CMOS input high voltage V_{IH}	—	1.17	—	—	V
Input low current I_{IL}	—	—	—	–5	µA
Input high current I_{IH}	—	—	—	5	µA

NOTE:

- Digital I/O power supply = 1.8V.
- * Drive strength: 16 mA for MDIO and 12 mA for INT0. Open-drain driver output high voltage depends on external pull-up voltage level.
- The specifications of the BSC interface (SCLAM and SDAAM) are I^2C compliant.

Table 104: 1.2V MDC/MDIO Power Supply CMOS DC Characteristics

Parameter	Condition	Specification			Unit
		Min.	Typ.	Max.	
CMOS output low voltage V_{OL}	4 mA	—	—	0.4	V
CMOS output high voltage V_{OH}	4 mA	0.8	—	—	V
CMOS input low voltage V_{IL}	—	—	—	0.42	V
CMOS input high voltage V_{IH}	—	0.78	—	—	V
Input low current I_{IL}	—	—	—	–5	µA
Input high current I_{IH}	—	—	—	5	µA

Table 105: MDC and MDIO AC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
MDIO output propagation delay after rising edge of MDC	t_{C2D}	—	—	—	25	ns
MDIO output from driven to high impedance after rising edge of MDC	t_{D2Z}	—	—	—	20	ns
MDC frequency	$MDC_{frequency}$	—	—	9	—	MHz
MDC duty cycle	t_{CKH}/t_{CK}	—	30	—	70	%
MDIO input setup time to rising edge of MDC	t_{DIS}	—	5	—	—	ns
MDIO input hold time after rising edge of MDC	t_{DIH}	—	5	—	—	ns

Figure 10: MDC and MDIO Timing Waveforms

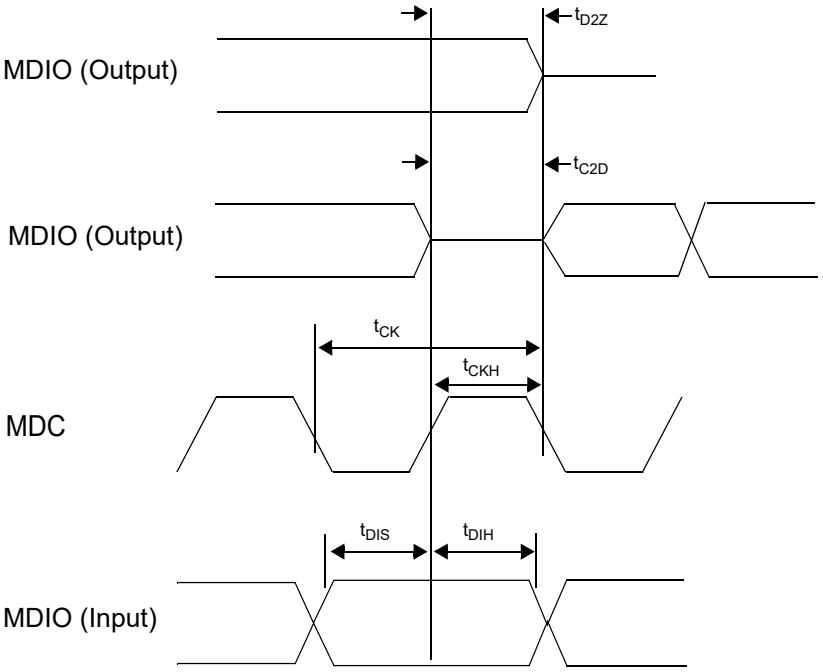
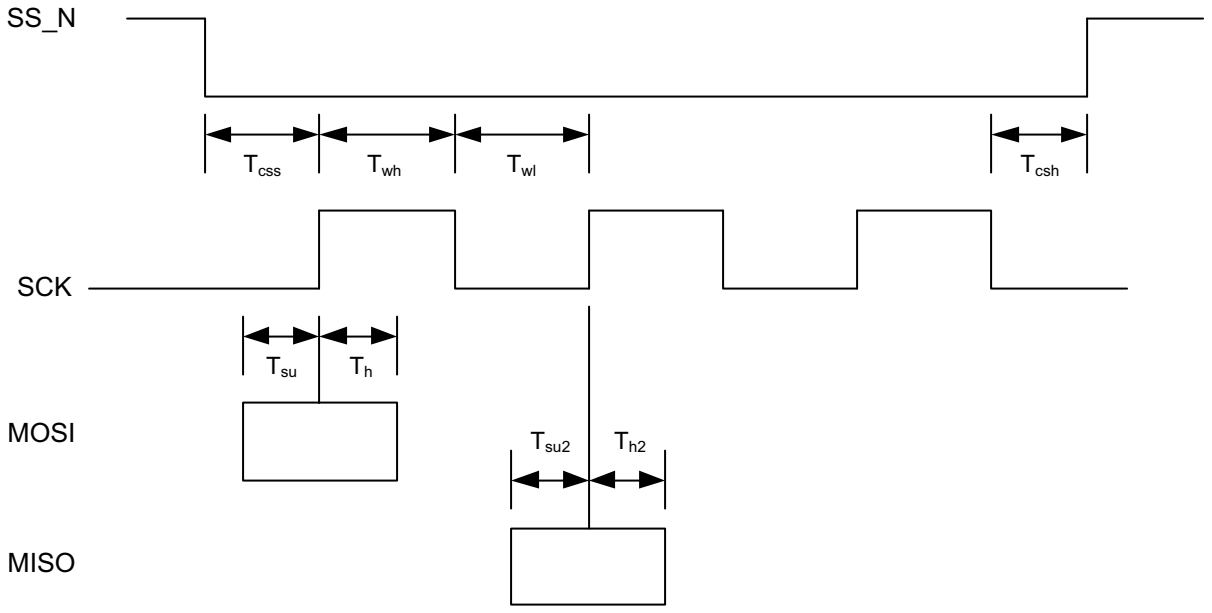


Table 106: SPI Interface AC Characteristics

Parameter	Symbol	Min.	Typ.	Unit
Operating frequency	F_{sck}	2.44	4	MHz
SPI CS setup time	T_{css}	250	—	ns
SPI CS hold time	T_{ch}	250	—	ns
SPI CK high-pulse width	T_{wh}	—	200	ns
SPI CK low-pulse width	T_{wl}	—	200	ns
Data output setup time	T_{su}	80	—	ns
Data output hold time	T_{h}	80	—	ns
Input data setup time	T_{su2}	—	15	ns
Input data hold time	T_{h2}	—	15	ns

Figure 11: SPI Interface Timing Waveforms



Chapter 6: Reference Clock

6.1 Reference Clock Pins

Table 107 and Table 108 list the reference clock pins. Figure 12 shows the reference clock input receiver.

Table 107: H1 and J1 Reference Clock Input Pins

Ball Number	Ball Name	Ball Type	Level
H1	REF_CLK_P	I	Differential Input. 100Ω differential. External AC-coupling required.
J1	REF_CLK_N		

Pins H1 and J1 are reference clock input pins. They are biased with internal differential 100Ω termination. They require external AC-coupling. The default reference clock frequency is 156.25 MHz.

Table 108: G6 and G12 Reference Clock Select Pins

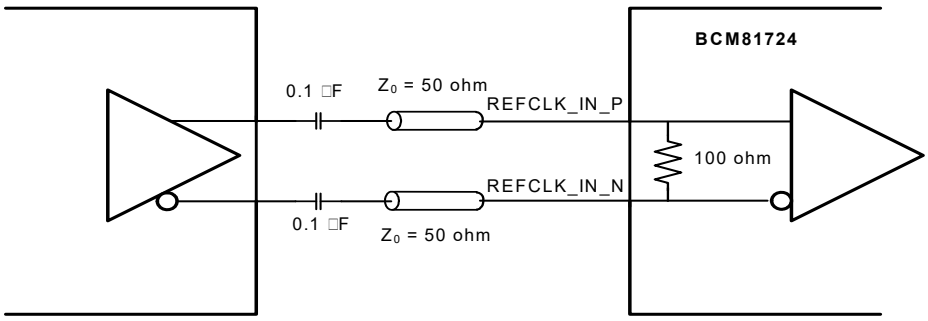
Ball Number	Ball Name	Ball Type	Level
G12	REF_SEL1	I	1.8V internal pull-down.
G6	REF_SEL0		

Pins G6 and G12 are reference clock select pins. These pins go through a clock divider and are meant for reference clock frequency of 2x or 4x the standard rate.

Here is the reference clock frequency range selection:

- If REF_SEL1 = 0 and REF_SEL0 = 0, frequency range = 100 to 170 MHz
- If REF_SEL1 = 0 and REF_SEL0 = 1, frequency range = 200 to 340 MHz

Figure 12: Reference Clock Input Receiver



6.2 Reference Clock PCB Design Guidelines

Here are the reference clock PCB design guidelines for the BCM81724:

- Always use a designated 100Ω differential transmission line (no split) from the reference clock source to the BCM81724 package reference clock input with minimal P and N skew (preferably under 10 mils) using the best design practice.
- Route the reference clock on external layers to avoid a via stub. Route on the top or bottom layers.
- Minimize routing layer changes to reduce the number of vias in the signal path. Less than two routing layer changes are recommended.
- Long routing (>10 in.) is acceptable provided:
  - Signal amplitude meets the Broadcom reference clock specifications at the input of the package after being attenuated by long routing traces.
  - No more impedance discontinuity than discussed above to create the reflection point.

Chapter 7: Recovered Clock

Table 107 lists the recovered clock pins.

Table 109: Recovered Clock Select Pins

Ball Number	Ball Name
J21	CLK_OUT_DIFF_P
J22	CLK_OUT_DIFF_N
J4	RCLK0
K4	RCLK1

Pins J21 and J22 are the differential recovered clock output pins. Pins J4 and K4 are individual single-ended recovered clock output pins.

The differential recovered clock pins are for the higher-speed recovered clock outputs (which are 50 MHz and above), whereas the single-ended recovered clock pins are for the lower-speed recovered clock outputs (which are below 50 MHz). The recovered clock outputs are a divided version of the CDR recovered clock from any of the line-side or system-side lanes. The source of the recovered clock (for example, which one of the 16 line lanes) and clock divider can be selected independently for each lane.

The recovered clock outputs can be selectively squelched (turned off) based on the loss of CDR lock or loss of signal detect for the selected lane used for the generation of the recovered clock. You can also squelch the recovered clock outputs that are not used. Under loss-of-signal or loss-of-lock conditions, the recovered clocks are squelched.

Table 110 and Table 111 show the available recovered clock divider rates and the approximate recovered clock frequencies for a few example data rates.

All the divider rates are defined in terms of the bit rate in NRZ mode and the baud rate in PAM-4 mode.

Table 110: Bit Rate in NRZ Mode

Example NRZ Data Rate (Gb/s)	Single-Ended Recovered Clock Divider Rates	Approximate RCLK 0 or RCLK 1 Output Frequency (MHz)
25	8192	6
	4096	12
	2048	24
	1024	48

Table 111: Baud Rate in PAM-4 Mode

Example PAM-4 Data Rate (Gb/s)	Differential Recovered Clock Divider Rates	Approximate CLK_OUT_DIFF_P/ CLK_OUT_DIFF_N Output Frequency (MHz)
56	8192	6
	4096	13
	2048	27
	1024	54
	512	109
	256	218
	128	436

The differential recovered clock outputs require external AC-coupling capacitors. Both the single-ended and the differential recovered clock outputs need external clock cleanup circuitry for Synchronous Ethernet applications.

Chapter 8: Decoupling Recommendations

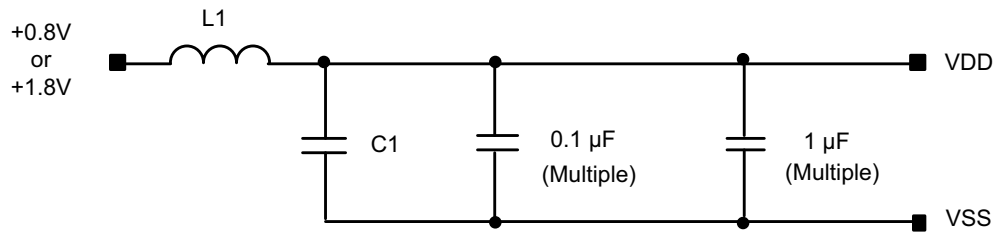
Table 112 and Figure 13 show the decoupling groups and decoupling circuit.

Table 112: Decoupling Groups

Ball Name	Recommended Max. Noise Ripple for Wide-Band Frequency from 50 kHz to Baud Rate (mVpp)	Power Supply Filter Bandwidth (kHz)	Filter Values	
			Inductance L (µH)	Capacitance C (µF)
PVDD0P8_0	8	13	4.7	33
PVDD0P8_1	8	13	4.7	33
H_PVDD0P8_A	8	13	4.7	33
H_PVDD0P8_B	8	13	4.7	33
PVDD1P8	8	50	1	10
TVDD0P8	8	50	1	10
TVDDDRV	8	50	1	10
RVDD0P8_A	8	50	1	10
H_PVDD1P8	8	50	1	10
H_TVDD0P8_A	8	50	1	10
H_TVDD0P8_B	8	50	1	10
H_TVDDDRV_A	8	50	1	10
H_TVDDDRV_B	8	50	1	10
H_RVDD0P8_A	8	50	1	10
H_RVDD0P8_B	8	50	1	10
VDDM	15	50	Ferrite bead	10
VDD_MDIO	30	50	Ferrite bead	10
VDDIO	30	50	Ferrite bead	10
VDD	15	50	Ferrite bead	4 × 330

Each group of supply pins must have its own independent decoupling circuits. All decoupling circuits must use the same discrete components as shown in Figure 13. Higher than normal current supplies, such as VDD, must use multiple 0.1-µF and 1-µF capacitors placed close to the pins. (Use about one 0.1 µF and 1 µF per power pin. If there is space for only one capacitor, 1 µF is preferred over 0.1 µF.) Inductors with sufficient DC resistance must be chosen to keep DC loss at an acceptable level, given the supply tolerance of the various supply domains.

Figure 13: Decoupling Circuit



If there are board space limitations, consolidate the power groupings as shown in Table 113.

Table 113: Consolidated Power Groupings

Power Grouping Serial No.	Power Supply
1	PVDD0P8_0
	PVDD0P8_1
2	PVDD1P8
	H_PVDD1P8
	VDD_MDIO
	VDDIO
3	TVDD0P8
	TVDDDRV
4	RVDD0P8
5	H_PVDD0P8_A
	H_PVDD0P8_B
6	H_TVDD0P8_A
	H_TVDD0P8_B
	H_TVDDDRV_A[1]
	H_TVDDDRV_B[1]
7	H_RVDD0P8_A
	H_RVDD0P8_B
8	VDDM
9	VDD
NOTE: If VDD_MDIO is fixed to 1.8V, share it with VDDIO.	

Chapter 9: Power-Sequencing Requirements

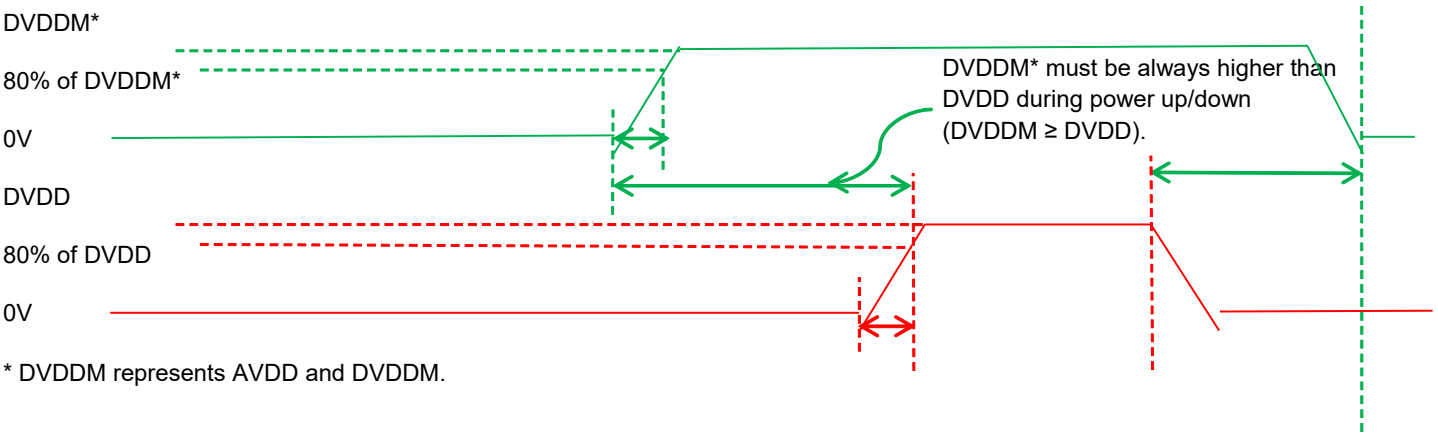
Here are the power-sequencing requirements for all power rails.

- The ramp-up and ramp-down times of all power rails must be less than 40 ms. The ramp-up time is defined as the time from 0V to 80% of each power rail's valid voltage level.
- Between the digital power rails DVDD and DVDDM, the DVDDM must be higher than the DVDD during power-up/down (DVDDM ≥ DVDD). In a steady state, if the DVDDM is higher than DVDD, then keep DVDDM ≤ DVDD + 350 mV. If the DVDD is higher than the DVDDM, then keep DVDD ≤ DVDDM + 250 mV. Figure 14 shows the DVDDM and DVDD power-sequence timing diagram.
- Analog AVDD (PVDD0P8, TVDD0P8, H_TVDDDRV, TVDDDRV, RVDD0P8, H_PVDD0P8, H_TVDD0P8, and H_RVDD0P8) and digital DVDDM can share the same power source.
- Digital DVDD1P8 and analog PVDD1P8 and H_PVDD1P8 should be powered up last. When powered down, digital DVDD1P8 and analog PVDD1P8 and H_PVDD1P8 should be powered down first.

In summary, the power sequence of the above power rails in power-up and power-down phases are as follows:

- When powered up: DVDDM/AVDD, DVDD, DVDD1P8
- When powered down: DVDD1P8, DVDD, DVDDM/AVDD

Figure 14: Power-Sequence Timing Diagram

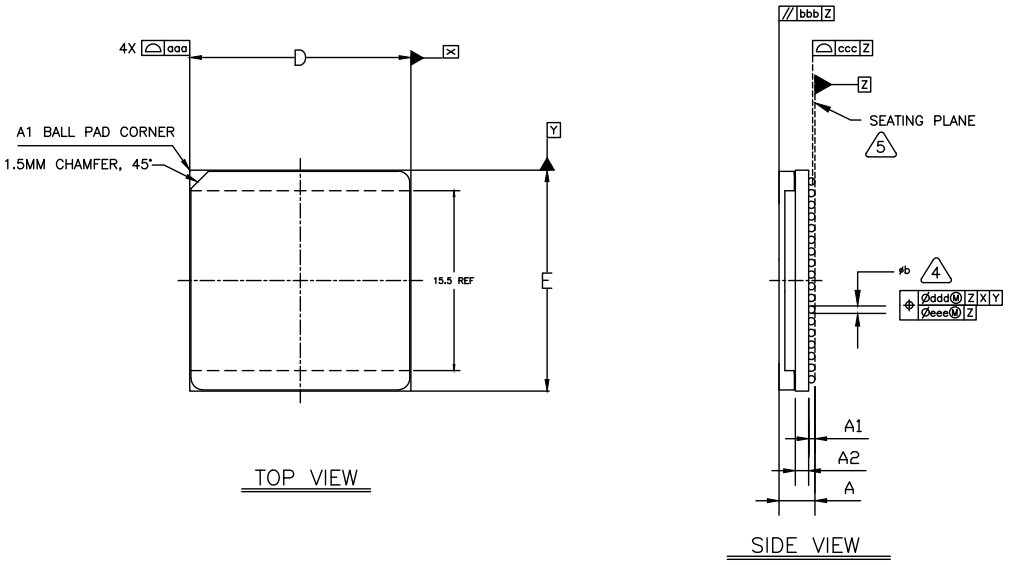


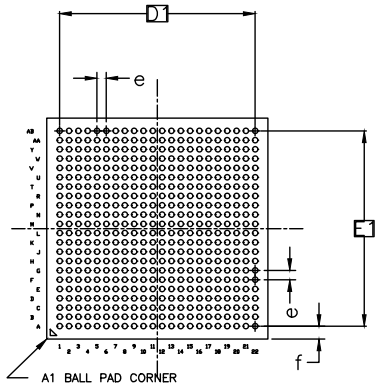
* DVDDM represents AVDD and DVDDM.

Chapter 10: Mechanical Information

10.1 Package Outline Drawing

Figure 15: 19 mm × 19 mm, 484-Ball BGA, RoHS-Compliant Package





DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	2.48	2.66	2.84
A1	0.350	0.400	0.450
A2	–	(0.844)	–
D	18.85	19.00	19.15
D1		16.80 BSC	
E	18.85	19.00	19.15
E1		16.80 BSC	
b	0.450	0.500	0.550
e		0.80 BSC	
f	–	1.10	–
aaa	–	–	0.15
bbb	–	–	0.35
ccc	–	–	0.20
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD81724 Rev. 001

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY D, REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.80 mm

2. THIS PACKAGE CONFORMS TO THE JEDEC PUBLICATION JEP95, DESIGN REGISTRATION 4.27.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
NOTES: UNLESS OTHERWISE SPECIFIED

10.2 Thermal Characteristics

The continuous maximum operating junction temperature must be ≤110°C (see Table 114).

Assumption: maximum ambient temperature = 70°C.

Table 114: Package Thermal Performance

θ_{JB} (°C/W)	4.05		
θ_{JC} (°C/W)	0.75		
Air Velocity	**With 60 mm × 60 mm × 30 mm Heat Sink**		
m/s	**θ_{JA} (°C/W)**	**Ψ_{JT} (°C/W)**	**Ψ_{JB} (°C/W)**
0.0	5.57	0.60	1.46
0.5	2.96	0.61	1.35
1.0	2.21	0.62	1.19
2.0	1.86	0.62	1.13
3.0	1.76	0.62	1.12

10.3 Electrostatic Discharge Handling Precautions

Devices that comply with Broadcom's design guidelines tolerate nominal electrostatic discharge (ESD) levels without damage. These high-speed, state-of-the-art devices undergo ESD susceptibility testing of input and output cells as part of a product qualification process before production.

Additionally, Broadcom employs personnel fully trained in proper ESD handling procedures. Devices are handled in static-controlled rooms with special workstations. All packaged devices are shipped in aluminum sealed bags inside boxes with Faraday cages designed to eliminate the risk of ESD damage.

CAUTION! Extreme caution must be exercised to prevent ESD damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store the unused material in its anti-static packaging.

Table 115: ESD Rating by Ball Type

Ball Type	ESD Rating	Unit
Any ball to any ball JEDEC JESD-A114-B (human body model)	1000	V

Chapter 11: Ordering Information

Table 116: Ordering Information

Part Number	Description
BCM81724A1KFSBG	A1 silicon, 19 mm × 19 mm, 0.8-mm ball pitch, 484-ball BGA, RoHS-compliant

Revision History

81724-DS200; September 10, 2020

Final release.