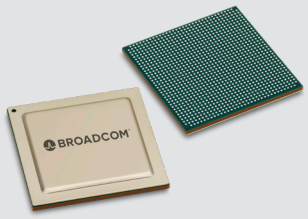
BROADCOM®

Product Brief

BCM81385

Dual 100G Retimer PHY with Class-C IEEE 1588 Timestamp Accuracy



Applications

- Supports 10G/25G/40G/50G/100G Ethernet applications
- Supports emerging 25G Ethernet with per-lane (or) lane-pair IEEE 802.3bj and IEEE 802.3by
- Optimizes switch I/O density by operating 40G over just two lanes into the switch ASIC
- Four 100GbE ports with CAUI4-to-CAUI4 port supports SR4/LR4/CR4 CFP2/CFP4/QSFP28 retimer and equalization

Overview

The Broadcom® BCM81385 is a low-power, high-density PHY that integrates IEEE 1588, retimer, and equalizer functions supporting 100-Gigabit Ethernet (GbE), 40GbE, 25GbE, and 10GbE applications.

In 100G mode, the BCM81385 supports two full-duplex 100G ports (CAUI4-to-CAUI4) for SR4, LR4, ER4, and copper CR4 CFP2/CFP4/QSFP28 line-card applications. In 40G mode, the BCM81385 supports two full-duplex 40GbE ports (XLPPI-to-XLAUI) for SR4, LR4, and copper CR4 QSFP+ line-card applications. In 10G mode, the BCM81385 supports eight full-duplex 10GbE ports (SFI-to-XFI) for SR, LR, and copper CR line-card applications.

The on-chip clock synthesis is performed by a single low-cost 156.25-MHz reference clock (for all IEEE standard 10G/25G/40G/100G rates) through high-frequency, low-jitter, phase-locked loops (PLLs). Individual clock recovery is performed on the device by synchronizing directly to the respective incoming data streams.

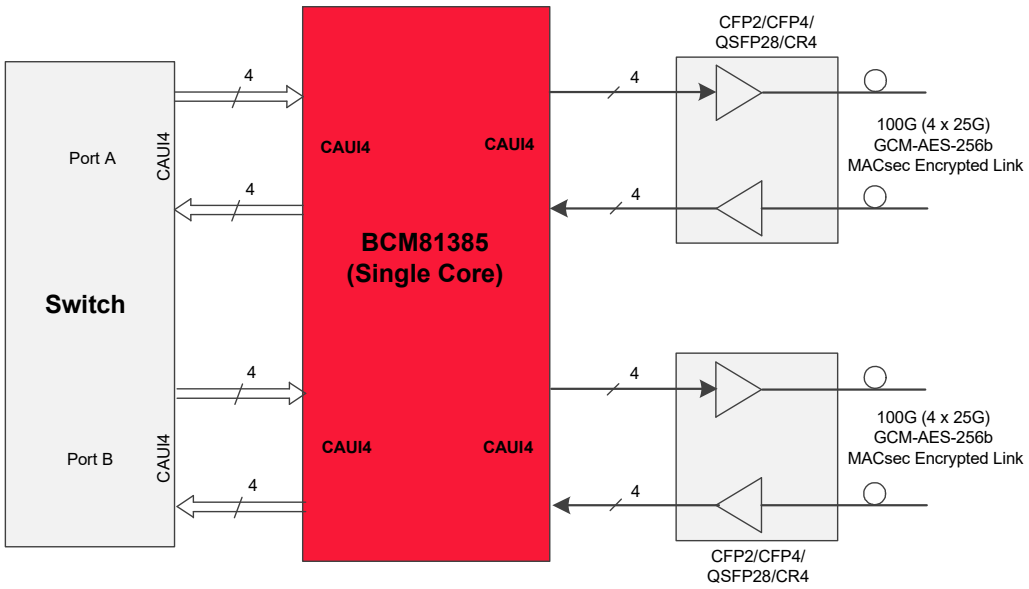
The BCM81385 is designed in 16-nm CMOS technology to provide a low-power solution with integrated AC-coupling capacitors.

The BCM81385 is available in a 23 mm × 23 mm, 729-ball BGA, RoHS-compliant package.

Features

- Dual 100GbE channels with two CAUI4-to-CAUI4 ports support SR4, LR4, and ER4 retimer
- Dual 40GbE channels with two XLPPI-to-XLAUI ports support SR4/LR4/CR4 QSFP+ retimer and equalization
- 10G mode with eight independent 10GbE SFI-to-XFI channels support SR/LR/CR retimer/equalization
- Supports IEEE 1588 timestamping with Class-C accuracy per G8273.2 spec and sync-E recovered clock outputs
- Supports IEEE 802.3bj 100GbE CR4 Clause 92 transmit training and IEEE 802.3ba 40GbE CR4 Clause 85 transmit training
- Supports 100G IEEE 802.3bj CL91 FEC and 25G IEEE 802.3by CL108
- Supports 25G/50G consortium specifications
- MDC and MDIO host interface
- Integrated AC-coupling capacitors on all high-speed receivers
- Hitless mux with no link flaps on both the line side and system side during switching:
  - In the ingress direction, the PHY transmits (broadcast) data received from the line side out to two links of muxed ports at the system side
  - In the egress direction, the PHY transmits data received from one selected switch mux port
- 23 mm × 23 mm BGA package, 0.8-mm ball pitch

Block Diagram



Ordering Information

Part Number	Package
BCM81385B0KFSBG	Commercial rated 23 mm × 23 mm, 729-ball BGA, RoHS-compliant
BCM81385B0IFSBG	Industrial rated 23 mm × 23 mm, 729-ball BGA, RoHS-compliant

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