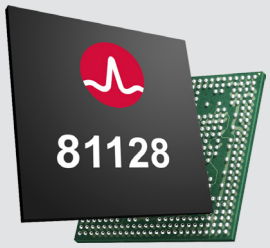
BROADCOM®

Product Brief

BCM81128

16-nm 100GbE PAM-4 PHY (4:2) or (2:2)



Key Features

- Single-chip 2× 50G PHY drives 100GbE over optics
  - Client side: 4× 25G NRZ or 2× 50G PAM-4
  - Line side: 2× 50G PAM-4
  - Single 100GbE mode: 4× 25G NRZ or 2× 50G PAM-4 to 2× 50G PAM-4
- Supports independent 100G PCS stream
- Client-side interface is compliant to the CEI-28G/56G MR specification supporting medium reach (MR) channels
- Supports various reach/media types:
  - MMF
  - SMF
- Low-power 16-nm CMOS design

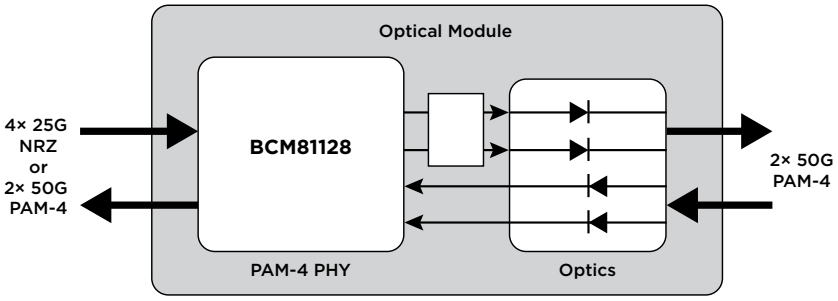
Description

The Broadcom® BCM81128 is a single-chip, low-power, low-latency PAM-4 PHY that integrates retimer and equalizer functions to support 100GbE applications. In 100GbE mode, the BCM81128 retimes, adds FEC (optional), and equalizes 4× 25G NRZ or 2× 50G PAM-4 host-side signals into 2× 50G PAM-4 line-side signals, which drive optical PAM-4 links inside next-generation modules, including QSFP28. The BCM81128 also provides 1× 100G applications with a single 100G PCS stream. The device also supports KP4 FEC, FEC bypass capability, and Broadcom's proprietary high-gain S-FEC for extended reach applications. The BCM81128 is compliant to IEEE standards with KP4 FEC and FEC bypass capability. On-chip clock synthesis is performed by a low-cost 156.25 MHz reference clock via high-frequency, low-jitter phase-locked loops (PLLs). The BCM81128 is fabricated in advanced low-power, 16-nm CMOS technology and is available in a RoHS-compliant package.

Applications

- 100GbE optical 2× 50G PAM-4 links for MMF/SMF
- 100GbE QSFP28 module form factors

Figure 1: BCM81128 Block Diagram



Ordering Information	
16-nm 100GbE PAM-4 PHY (4:2) or (2:2)	BCM81128A0KRFBG

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