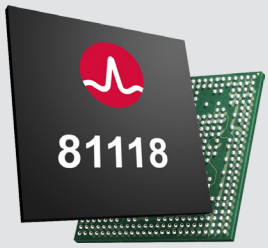
BROADCOM®

Product Brief

BCM81118

16-nm 50GbE PAM-4 PHY (1:1) or (2:1)



Key Features

- Single-chip 1× 50G PHY drives 50GbE over optics:
  - System side: 1× 50G PAM-4 or 2× 25G NRZ
  - Line side: 1× 50G PAM-4
  - Repeater and gearbox applications (no FEC termination)
  - Loopbacks (system side and line side)
- Client-side interface is compliant to the CEI-28G/56G MR specification supporting medium reach (MR) channels
- Supports various reach/media types:
  - MMF
  - SMF
- Low-power 16-nm CMOS design

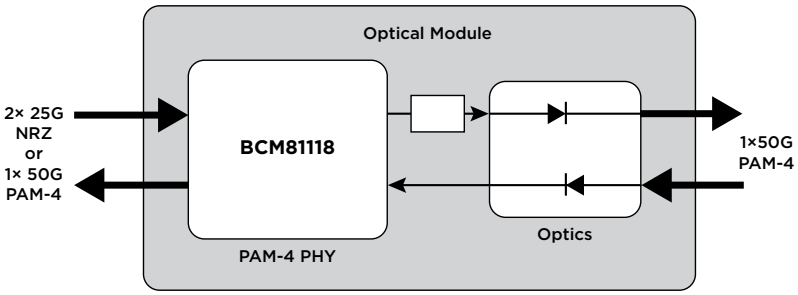
Description

The Broadcom® BCM81118 is a single-chip, low-power, low-latency PAM-4 PHY integrating retimer and equalizer functions supporting 50GbE applications. In 50GbE mode, the BCM81118 retimes and equalizes a 1× 50G PAM-4 or 2× 25G NRZ host-side signal lanes into a 1× 50G PAM-4 line-side signal to drive optical PAM-4 links inside next-generation modules, including SFP56. On-chip clock synthesis is performed by a low-cost 156.25 MHz reference clock via high-frequency, low-jitter phase-locked loops (PLLs). The BCM81118 is fabricated in advanced low-power, 16-nm CMOS technology and is available in a RoHS-compliant package.

Applications

- 50GbE optical 1× 50G PAM-4 links for MMF/SMF
- 50GbE SFP56 module form-factors

Figure 1: BCM81118 Block Diagram



Ordering Information	
16-nm 50GbE PAM-4 PHY (1:1) or (2:1)	BCM81118A0KRFBG

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