ACPM-7891

Tri-Band Power Amplifier Module
EGSM, DCS and PCS Multi-slot GPRS

Data Sheet and Application Note

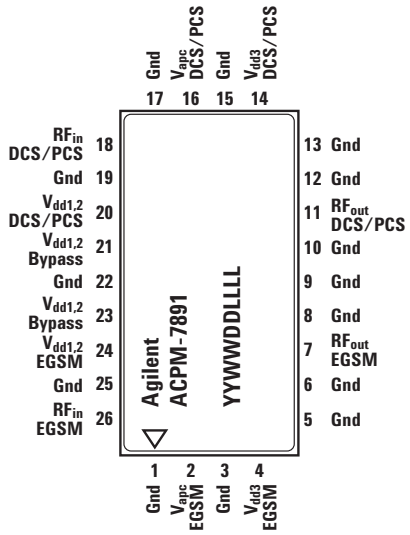
Description

The ACPM-7891 is a fully matched tri-band EGSM/DCS/PCS power amplifier module designed on Avago Technologies' leading edge Enhancement Mode PHEMT (E-pHEMT) process.

The ACPM-7891 has the highest Power-added Efficiency (PAE) for all three bands of operation in the industry, enabling customers to design handset, PDA and data card with up to 15% longer transmit or talk time.

The Avago ACPM-7891 provides a cost effective dual or tri-band GSM PA solution with the additional benefit of excellent efficiency enabling multi-slot GPRS operation and extended transmit time. The device is internally matched to 50Ω and therefore an effective design can be implemented quickly with a few additional capacitors for d.c. blocking of the output ports and bypassing of the supply pins.

Pin Connections and Package Marking



Notes:
Package marking provides orientation and identification.

"YYWWDDLLLL" = Year, Week, Day and Lot Code indicates the year, week, day and lot of manufacture.

Features

- Highest Power Added Efficiency in the industry
- Performance guaranteed for GPRS Class 10 (2-Slot) transmit operation
- Broadband DCS/PCS match for flat P_{out} and PAE
- Low harmonics
- Single 3.5 Volt supply (nominal)
- 50 Ohms input & output impedance
- Small SMT package 6 x 12 x 1.4 mm

Specifications

- 60% PAE at +35 dBm P_{out} for ESGM
- 56% PAE at +32.5 dBm P_{out} for DCS 1800
- 56% PAE at +32.5 dBm P_{out} for PCS 1900

Applications

- Cellular handsets
- Data modules for PDA
- Data cards for laptops

Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum
V_{dd}	Supply Voltage	V	6
P_{in} max	Input Power	dBm	+10
V_{apc}	Gain Control Voltage	V	4
I_{DS}	Operating Case Temperature	°C	-30 to 90
T_{STG}	Storage Temperature	°C	-40 to 125

Common Electrical Characteristics

Test conditions Vdd = +3.5V, a pulse width of 1154 µs and a duty cycle of 25% at a case temperature of +25°C unless otherwise stated.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Supply Voltage		V_{dd}	2.7	3.5	5.3	V
Leakage Current	V_{apc}= 0.06V	I_{dd}		20		µA
Control Voltage Range		V_{apc}	0		V_{dd}–0.3	V
Control Current		I_{apc}			3	mA
Nominal Input Impedance		Z_{in}		50		Ω
Nominal Output Impedance		Z_{out}		50		Ω
Rise And Fall Time	T_r to (P_{out1}– 0.5 dB) V_{apc} set to achieve P_{out1}	t_r,t_f		1	2	µs

EGSM Electrical Characteristics

Test conditions Vdd= +3.5V, a pulse width of 1154 µs and a duty cycle of 25% at a case temperature of +25°C unless otherwise stated.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Frequency Range		F_o	880	900	915	MHz
Output Power Nominal Conditions	P_{in} = +2 dBm V_{apc} = 2.2V	P_{out1}	34.5	35		dBm
Efficiency	$P_{out}=P_{out1}$	PAE	55	60		%
Output Power in off mode	V_{apc} = 0.2V, P_{in} = 4 dBm			-40	-36	dBm
Input Power		P_{in}	0	2	4	dBm
Input VSWR	P_{in} = 0 dBm			1.5	2.5	
Stability	V_{dd} = 3.0 to 5.3V, P_{in} = 0 – 4 dBm, $P_{out} \leq$ 34.5 dBm, $V_{apc} \leq$ 2.2V, VSWR ≤ 8:1, all phases		No parasitic oscillation > -36 dBm			
Load mismatch robustness	V_{dd} = 3.0 to 5.3V, P_{in} = 0 – 4 dBm, $P_{out} \leq$ 34.5 dBm, $V_{apc} \leq$ 2.2V, VSWR ≤ 10:1, all phases t = 20 sec		No module damage or permanent degradation			
Second Harmonic	V_{dd} = 3.5V P_{in} = 0 dBm P_{out} = 34.5 dBm V_{apc} = controlled for P_{out}	$2F_o$			-5	dBm
Third Harmonic	V_{dd} = 3.5V P_{in} = 0 dBm P_{out} = 34.5 dBm V_{apc} = controlled for P_{out}	$3F_o$			-5	dBm
Fourth to Eighth Harmonics	V_{dd} = 3.5V P_{in} = 0 dBm P_{out} = 34.5 dBm V_{apc} = controlled for P_{out}	$4F_o$-$8F_o$			-10	dBm
Noise Power	F=925 to 935 MHz, $P_{out} \leq$ 34.0 dBm, Pin = 0 dBm RBW = 100 kHz F = 925 to 960 MHz, $P_{out} \leq$ 34.0 dBm, Pin = 0 dBm RBW = 100 kHz	P_n P_n			-72 -82	dBm dBm
Band to Band Isolation	Measured at DCS freq EGSM signal: V_{dd} = 3.5V P_{in} = +2 dBm P_{out} = 34.5 dBm (fixed)				-25	dBm
Control Slope (Peak)	Pout = -5 dBm to P_{out}			400		dB/V
AM-AM	Pin = 0 – 4 dBm Pout = 6 dBm to P_{out}			5		dB/dB
AM-PM	Pin = 0 – 4 dBm Pout = 6 dBm to P_{out}			6		deg/dB

DCS & PCS Electrical Characteristics

Test conditions Vdd= +3.5V, a pulse width of 1154 µs and a duty cycle of 25% at a case temperature of +25°C unless otherwise stated.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Frequency Range	DCS PCS	F_o	1710 1850	1750 1880	1785 1910	MHz
Output Power Nominal Conditions	P_{in} = 2 dBm V_{apc} = 2.2V	P_{out1}	32.0	32.5		dBm
Efficiency	$P_{out} = P_{out1}$	DCS PAE PCS PAE	50 50	56 56		%
Output Power in off mode	V_{apc} = 0.2V, P_{in} = 4 dBm			-40	-36	dBm
Input Power		P_{in}	0	2	4	dBm
Input VSWR	P_{in} = 0 dBm			1.5	2.5	
Stability	V_{dd} = 3.0 to 5.3V, P_{in} = 0 – 4 dBm, $P_{out} \leq$ 32 dBm, $V_{apc} \leq$ 2.2V, VSWR ≤ 8:1, all phases		No parasitic oscillation > -36 dBm			
Load mismatch robustness	V_{dd} = 5.3V, P_{in} = 0 – 4 dBm, $P_{out} \leq$ 32 dBm, $V_{apc} \leq$ 2.2V, VSWR ≤ 10:1, all phases t = 20 sec		No module damage or permanent degradation			
Second Harmonic	V_{dd} = 3.5V P_{in} = 0 dBm P_{out} = 32 dBm V_{apc} = controlled for P_{out}	$2F_o$			-5	dBm
Third Harmonic	V_{dd} = 3.5V P_{in} = 0 dBm P_{out} = 32 dBm V_{apc} = controlled for P_{out}	$3F_o$			-5	dBm
Fourth to Eighth Harmonics	V_{dd} = 3.5V P_{in} = 0 dBm P_{out} = 32 dBm V_{apc} = controlled for P_{out}	$4F_o – 8F_o$			-10	dBm
Noise Power	F = 1805 to 1880 MHz, F = 1930 to 1990 MHz, $P_{out} \leq$ 31.5 dBm, Pin = 0 dBm RBW = 100 kHz	P_n			-77	dBm
Control Slope (Peak)	Pout = -5 dBm to P_{out1}			350		dB/V
AM-AM	Pin = 0 – 4 dBm Pout = 6 dBm to P_{out1}			5		dB/dB
AM-PM	Pin = 0 – 4 dBm Pout = 6 dBm to P_{out1}			6		deg/dB

GPRS Electrical Characteristics

Test conditions Vdd= +3.5V, a pulse width of 1154 µs and a duty cycle of 25% at a case temperature of +25°C unless otherwise stated.

P_{sat}: Pin = 0 dBm; V_{apc} = 2.2V

	P_{out} (dBm) 880 MHz	900 MHz	915 MHz	PAE (%) 880 MHz	900 MHz	915 MHz
Class 8 (1-slot)	35.18	35.40	35.40	60.23	60.47	59.55
Class 10 (2-slot)	35.15	35.45	35.43	60.07	61.02	59.77
Class 12 (4-slot)	35.16	35.32	35.36	60.09	59.62	59.35

P_{sat}: Pin = 0 dBm; V_{apc} = 2.2V

	P_{out} (dBm) 1710 MHz	1750 MHz	1785 MHz	PAE (%) 1710 MHz	1750 MHz	1785 MHz
Class 8 (1-slot)	33.00	33.08	33.12	59.00	59.19	59.62
Class 10 (2-slot)	33.00	33.08	33.10	59.35	59.42	59.40
Class 12 (4-slot)	33.00	33.08	33.10	59.35	59.42	59.40

P_{sat}: Pin = 0 dBm; V_{apc} = 2.2V

	P_{out} (dBm) 1850 MHz	1880 MHz	1910 MHz	PAE (%) 1850 MHz	1880 MHz	1910 MHz
Class 8 (1-slot)	33.10	33.10	33.02	59.14	58.93	58.66
Class 10 (2-slot)	33.10	33.10	33.02	59.14	58.93	58.66
Class 12 (4-slot)	33.10	33.04	32.96	58.75	58.50	58.25

Typical Performance

Test conditions: Vdd = +3.5V, case temperature of +25°C, and Zo=50 ohms unless otherwise stated.

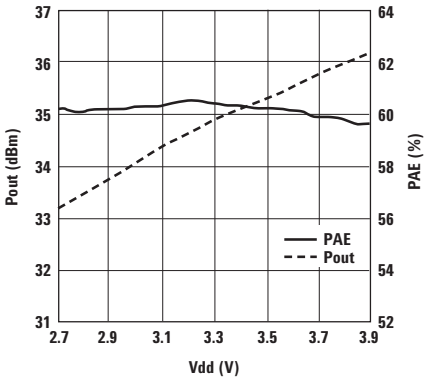


Figure 1. PAE and Pout vs Vdd (EGSM Band, Pin = 2 dBm, Vapc = 2.2V).

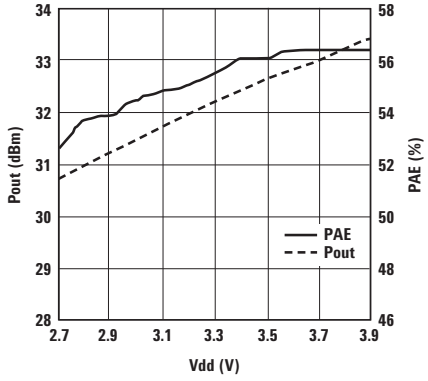


Figure 2. PAE and Pout vs Vdd (DCS 1750 MHz, Pin = 2 dBm, Vapc = 2.2V).

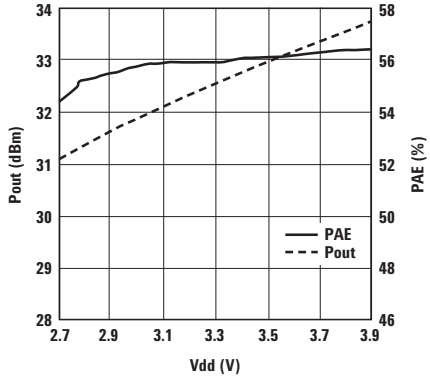


Figure 3. PAE and Pout vs Vdd (PCS 1880 MHz, Pin = 2 dBm, Vapc = 2.2V).

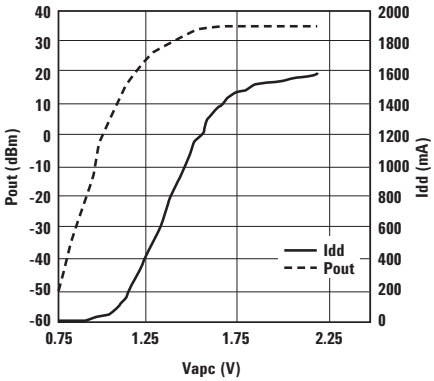


Figure 4. Pout and Idd vs Vapc (EGSM Band, Pin = 0 dBm, Vdd = 3.5V).

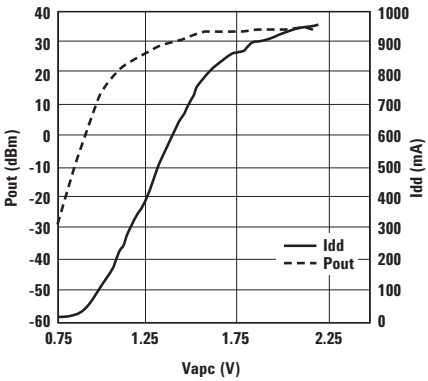


Figure 5. Pout and Idd vs Vapc (DCS 1750 MHz, Pin= 0 dBm, Vdd = 3.5V).

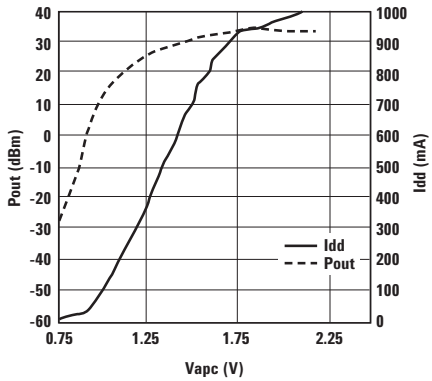


Figure 6. Pout and Idd vs Vapc (PCS 1880 MHz, Pin= 0 dBm, Vdd = 3.5V).

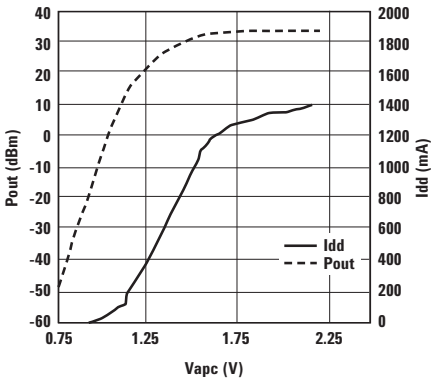


Figure 7. Pout and Idd vs Vapc (Vdd EGSM Band, Pin = 0 dBm, Vdd = 3.0V).

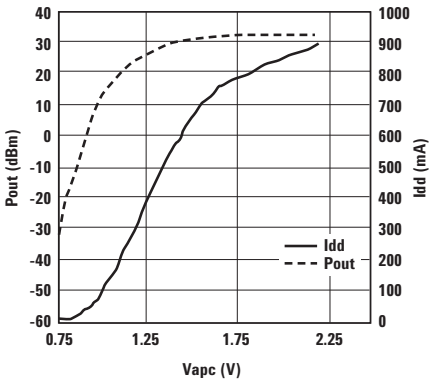


Figure 8. Pout and Idd vs Vapc (DCS 1750 MHz, Pin = 0 dBm, Vdd = 3.0V).

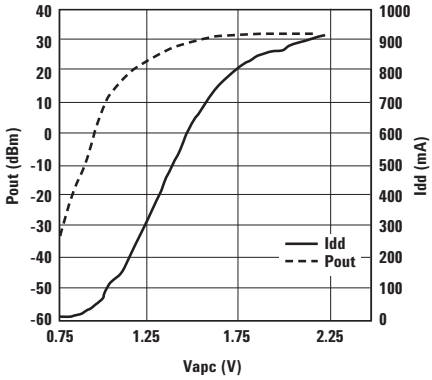


Figure 9. Pout and Idd vs Vapc (PCS 1880 MHz, Pin = 0 dBm, Vdd = 3.0V).

Typical Performance, continued

Test conditions: Vdd = +3.5V, case temperature of +25°C, and Zo=50 ohms unless otherwise stated.

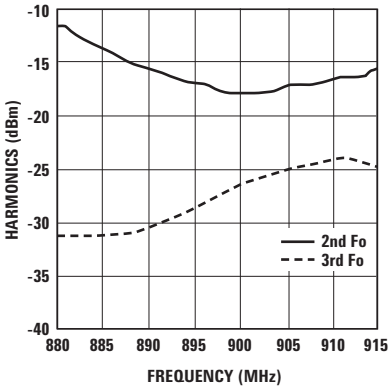


Figure 10. 2nd and 3rd Harmonic Performance (EGSM Band, Pin = 0 dBm, Pout = 34.5 dBm, Vdd = 3.5V).

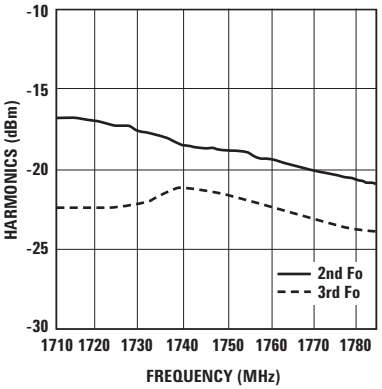


Figure 11. 2nd and 3rd Harmonic Performance (DCS Band, Pin = 0 dBm, Pout = 32 dBm, Vdd = 3.5V).

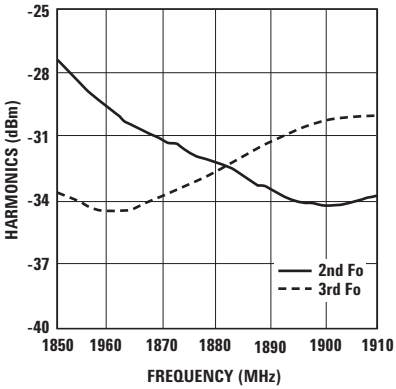


Figure 12. 2nd and 3rd Harmonic Performance (PCS Band, Pin = 0 dBm, Pout = 32 dBm, Vdd = 3.5V).

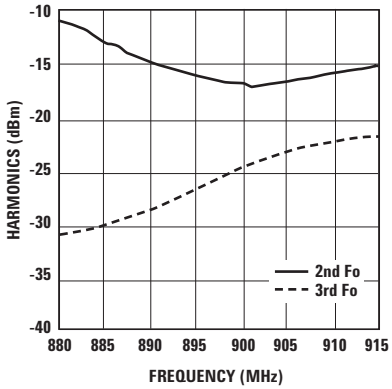


Figure 13. 2nd and 3rd Harmonic Performance (EGSM Band, Pin = 0 dBm, Pout = 34.5 dBm, Vdd = 3.0V).

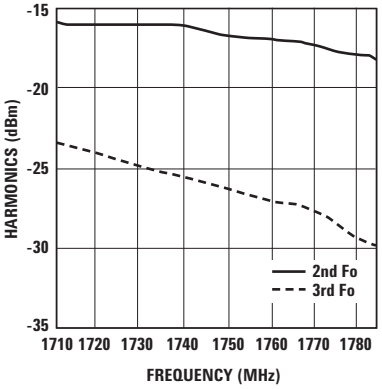


Figure 14. 2nd and 3rd Harmonic Performance (DCS Band, Pin = 0 dBm, Pout = 32 dBm, Vdd = 3.0V).

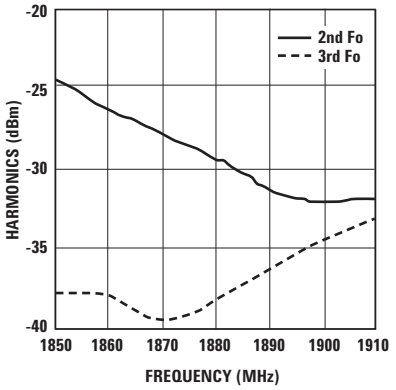


Figure 15. 2nd and 3rd Harmonic Performance (PCS Band, Pin = 0 dBm, Pout = 32 dBm, Vdd = 3.0V).

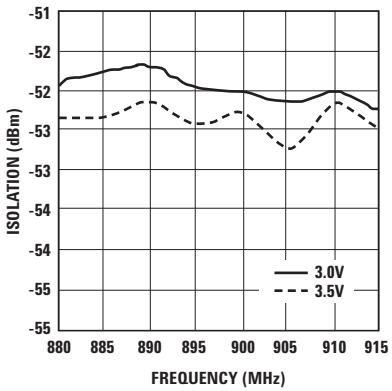


Figure 16. Isolation Performance (EGSM Band, Pin = 4 dBm, Vapc = 0.2V).

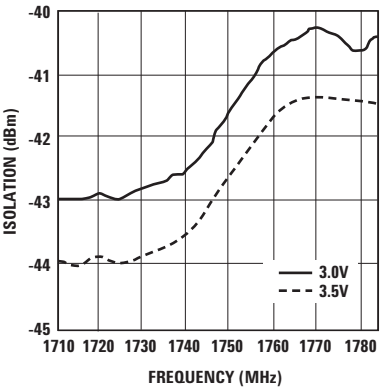


Figure 17. Isolation Performance (DCS Band, Pin = 4 dBm, Vapc = 0.2V).

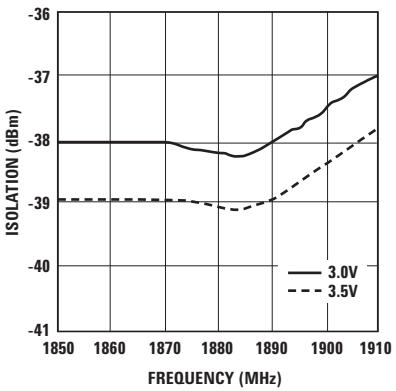


Figure 18. Isolation Performance (PCS Band, Pin=4 dBm, Vapc=0.2V).

Typical Performance, continued

Test conditions: Vdd = +3.5V, case temperature of +25°C, and Zo=50 ohms unless otherwise stated.

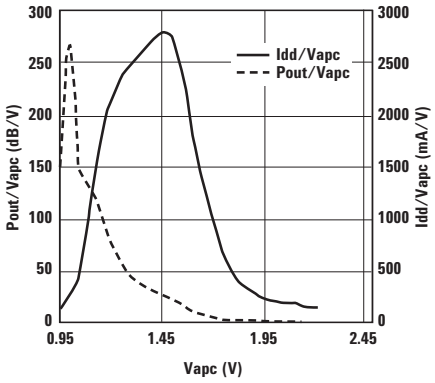


Figure 19. Pout/Vapc and Idd/Vapc vs. Vapc (EGSM band, Vdd = 3.5V).

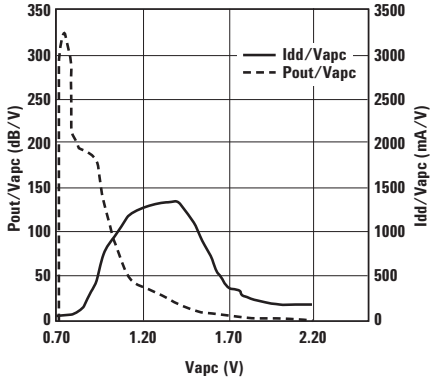


Figure 20. Pout/Vapc and Idd/Vapc vs. Vapc (DCS 1750 MHz, Vdd = 3.5V).

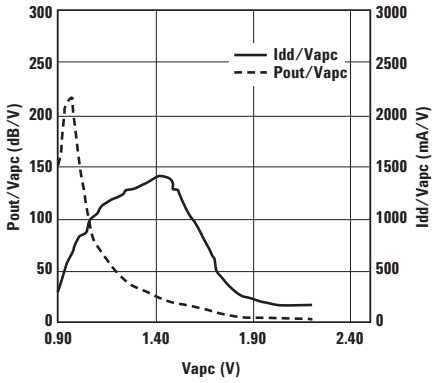


Figure 21. Pout/Vapc and Idd/Vapc vs. Vapc (PCS 1880 MHz, Vdd = 3.5V).

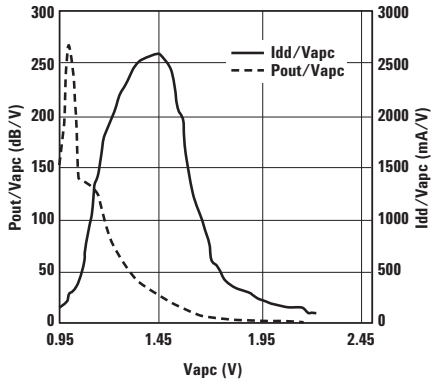


Figure 22. Pout/Vapc and Idd/Vapc vs. Vapc (EGSM band, Vdd = 3.0V).

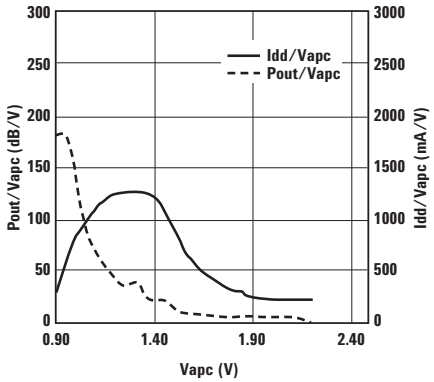


Figure 23. Pout/Vapc and Idd/Vapc vs. Vapc (DCS 1750 MHz, Vdd = 3.0V).

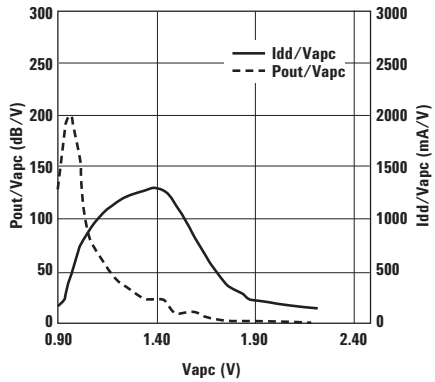
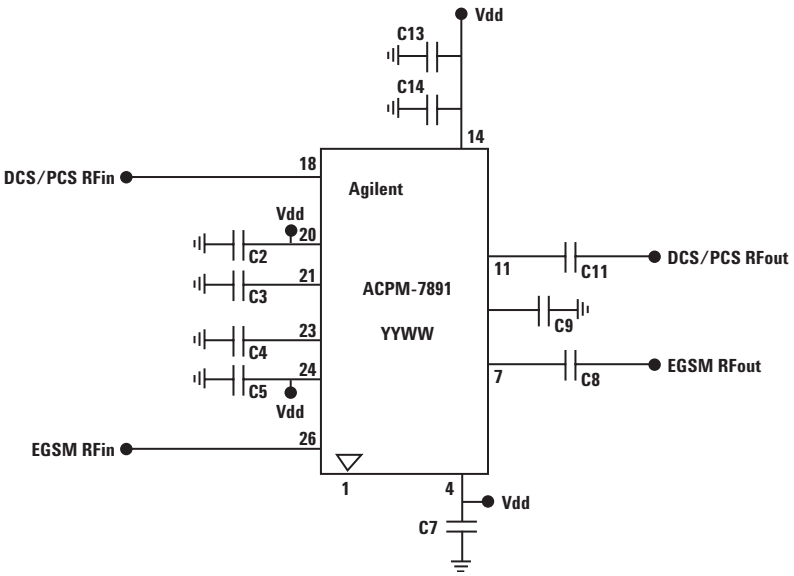


Figure 24. Pout/Vapc and Idd/Vapc vs. Vapc (PCS 1880 MHz, Vdd = 3.0V).

Demo Board Schematic for PA Only



Component Label	Component Value
C2	.033 µF
C3	12 pF
C4	220 pF
C5	.033 µF
C7	220 pF
C8	33 pF
C9	.033 µF
C11	33 pF
C13	.033 µF
C14	27 pF

Pin Description Table

No.	Function	Description	Notes
1	Gnd		
2	Vapc EGSM	EGSM Control Voltage	See datasheet Figure 4
3	Gnd		
4	Vdd3 EGSM	EGSM Supply 3rd stage	3.5V nominal – output stage, bypass with 0.033 µF//220 pF[1]
5	Gnd		
6	Gnd		
7	RFout EGSM	EGSM Output	50Ω nominal, external d.c. blocking required – 33 pF
8	Gnd		
9	Gnd		
10	Gnd		
11	RFout DCS/PCS	DCS/PCS Output	50Ω nominal, external d.c. blocking required – 33 pF
12	Gnd		
13	Gnd		
14	Vdd3 DCS/PCS	DCS/PCS Supply 3rd stage	3.5V nominal – output stage, bypass with 0.033 µF//27 pF[1]
15	Gnd		
16	Vapc DCS/PCS	DCS/PCS Control voltage	See datasheet Figure 5 (DCS) and Figure 6 (PCS)
17	Gnd		
18	RFin DCS/PCS	DCS/PCS Input	+2 dBm GMSK, 50Ω nominal, internally d.c. blocked
19	Gnd		
20	Vdd1,2 DCS/PCS	DCS/PCS Supply 1st and 2nd stages	3.5V nominal – driver stages, bypass with 0.033 µF
21	Vdd1,2 Bypass	DCS/PCS 1st and 2nd stage bypassing	bypass with 12 pF
22	Gnd		
23	Vdd1,2 Bypass	EGSM 1st and 2nd stage bypassing	bypass with 220 pF
24	Vdd1,2 EGSM	EGSM Supply 1st and 2nd stages	3.5V nominal – driver stages, bypass with 0.033 µF
25	Gnd		
26	RFin EGSM	EGSM Input	+2 dBm GMSK, 50Ω nominal, internally d.c. blocked

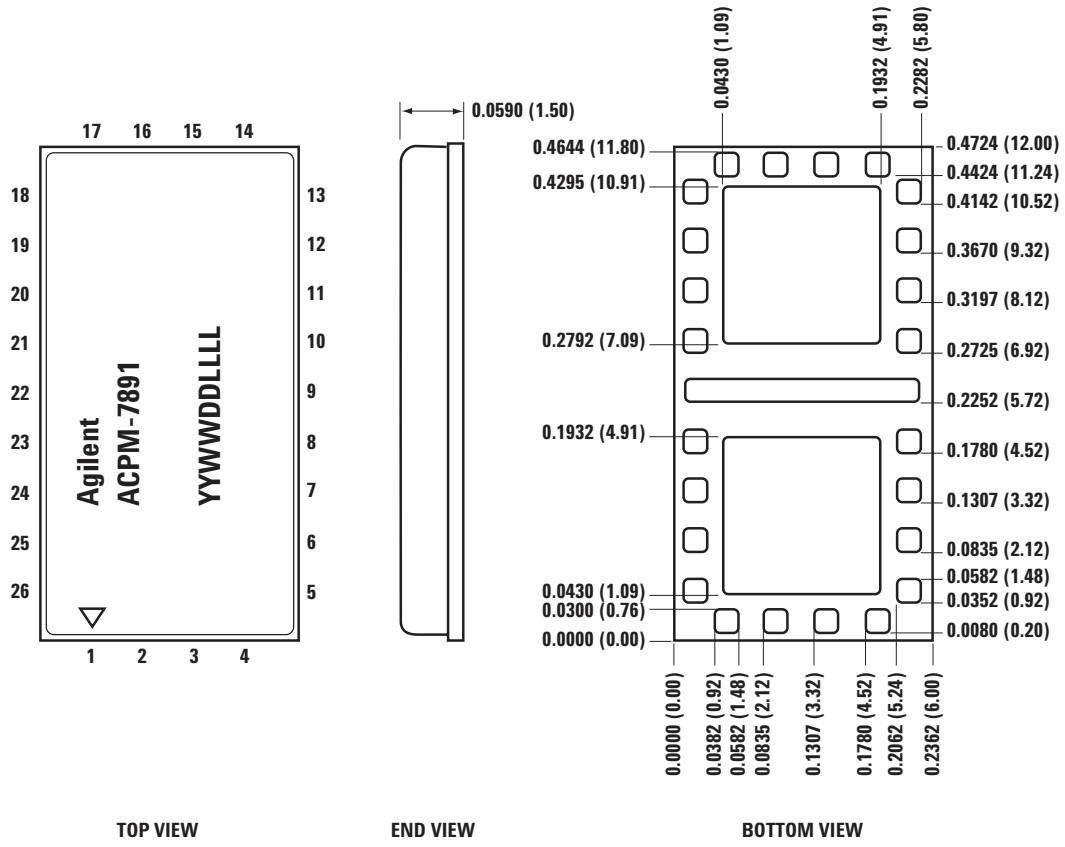
Note:

1. In addition a 2.2 µF capacitor should be connected to pins 4 and 14 or alternatively star connections can be made from a single 2.2 µF capacitor keeping the connection distances as short as possible.

Ordering Information

Part Number	No. of Devices	Container
ACPM-7891-BLK	10	Bulk
ACPM-7891-TR1	1000	13″ Tape and Reel

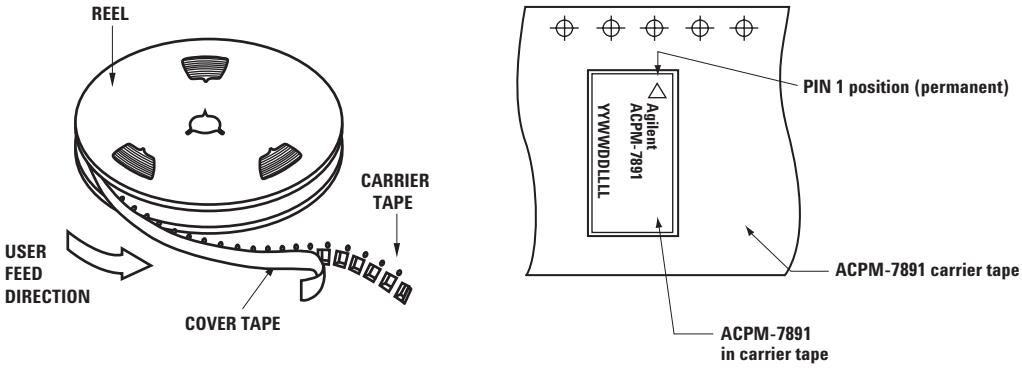
Package Dimensions



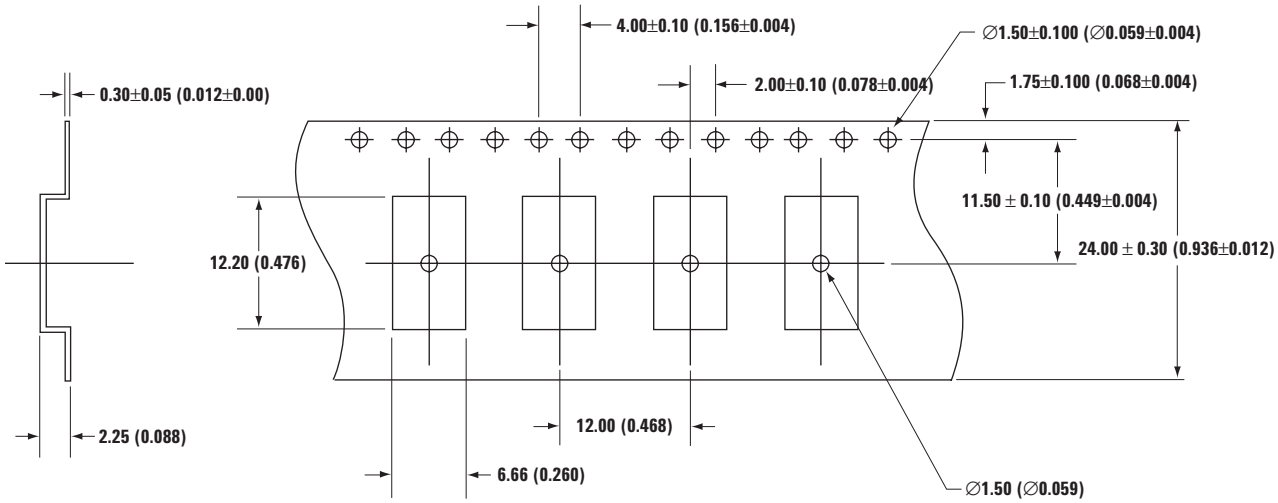
TOP VIEW **END VIEW** **BOTTOM VIEW**

Note:
Measurements are in inches (millimeters).

Tape Dimensions and Device Orientation



CARRIER TAPE



DEVICE IN CARRIER TAPE

Notes:
Drawing not to scale.
Measurements are in millimeters (inches).

Applications Information

Introduction

The Avago ACPM-7891 provides a cost effective dual or tri-band GSM Power Amplifier (PA) solution with the additional benefit of multi-slot GPRS operation, giving excellent efficiency and extended transmit time. Figure 1 illustrates how the ACPM-7891 fits into a typical dual-band or tri-band terminal design. The device is internally matched to 50Ω and therefore an effective design can be implemented quickly with a few additional capacitors for d.c. blocking of the output ports and bypassing of the supply pins.

The control loop can also be implemented quickly by using an integrated power controller such as the LT1758-2 from Linear Technology. An example using this controller is given later in this note. The required loop performance and stability can be achieved more easily in this way, without the need for complex and time consuming design work around an external error comparator or discrete Schottky diode detector.

Demoboards are available, and design engineers can evaluate the RF performance of the ACPM-7891 power amplifier to implement a solution quickly by using this application note in conjunction with the datasheet.

ACPM-7891 Performance

Figure 2 plots the actual output power of the ACPM-7891 PA for GSM900, DCS1800 and PCS1900 bands as a function of the control voltage, Vapc. The input power to the PA is a GMSK modulated RF carrier of a constant power level of 2 dBm. The PA's maximum output power is 35 dBm in the GSM900 band, and 33 dBm for the DCS1800/PCS1900 band at a control voltage of 2.2V. The input RF carrier and control voltage are both pulsed, following the GSM TDMA characteristic response with a period of 4.615ms and a duty cycle of 12.5~25% per the GSM standard.

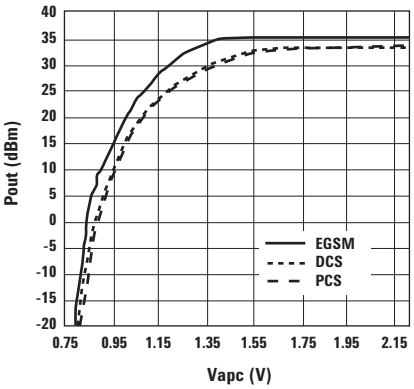


Figure 2. Output Power vs. Control Voltage for the ACPM-7891 Power Amplifier.

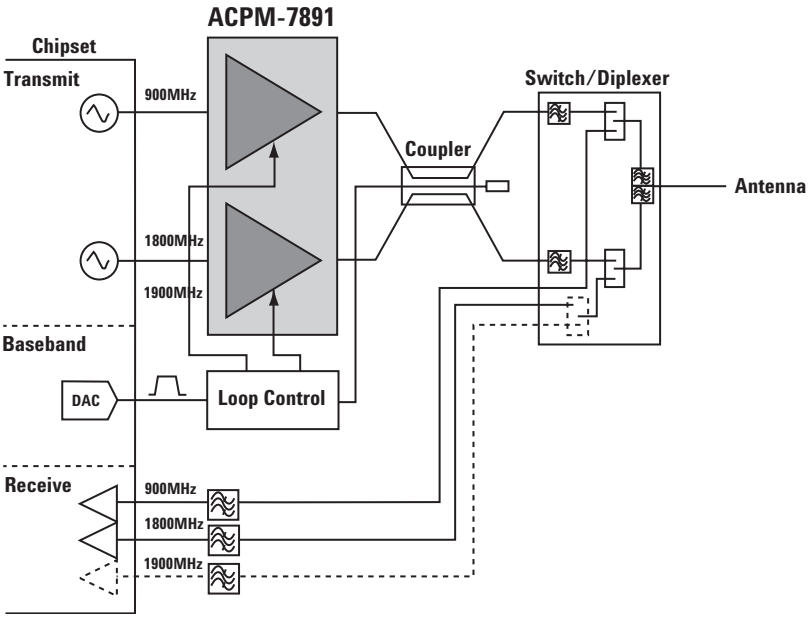


Figure 1. ACPM-7891 in a Typical Dual-band or Tri-band Terminal.

ACPM-7891 Evaluation

There are two options available when evaluating the ACPM-7891. Option A is to use the fully assembled and tested ACPM-7891 Test Board from Avago which includes the PA and associated passive components. This board can be used to evaluate the basic performance of the PA against the typical electrical characteristics provided in the datasheet. All maximum and minimum PA parameters are verified prior to sending out this board.

Option B allows the PA performance to be evaluated within a power control loop environment by using the ACPM-7891 PA Control Board from Avago which incorporates the commercially available control loop IC LT1758-2 from Linear Technologies. This device is used as an example; however, alternative off-the-shelf power control ICs are available from Linear Technologies, Analog Devices and other suppliers. The ACPM-7891 PA Control Board can be used in conjunction with an LT1758 Demoboard, available from Linear Technologies, which supplies the DAC and timing functions. Alternatively the DAC and timing functions can be supplied by a conventional two channel function generator.

Demo Board Test Conditions

For both types of demoboards, a common set of test conditions apply. Tables 1 and 2 detail the test conditions for EGSM, DCS and PCS at Vdd = +3.5V, pulse width of 1154 µs, and a duty cycle of 25% for a case temperature of +25°C.

Table 1. EGSM Test Conditions.

Parameter	Symbol	Test Condition
Operating Frequency	f (MHz)	Tx EGSM frequency range: 880 ~ 915 MHz
Supply Voltage	Vdd (V)	Nominal voltage 3.5V. Extreme voltage conditions of 2.7V and 5.3V
Input Power Level	Pin (dBm)	2 dBm ± 2 dBm
Control Voltage	Vapc (V)	Standard DAC output control level estimated at 0.1 to 2.6V. Maximum Vapc level: Vdd-0.3V
Temperature	To (C)	-30, +25, +85°C

Table 2. DCS/PCS Test Conditions.

Parameter	Symbol	Test Condition
Operating Frequency	f (MHz)	Tx DCS frequency range: 1710 ~ 1785 MHz Tx PCS frequency range: 1850 ~ 1910 MHz
Supply Voltage	Vdd (V)	Nominal voltage 3.5V. Extreme voltage conditions of 2.7V and 5.3V
Input Power Level	Pin (dBm)	2 dBm ± 2 dBm
Control Voltage	Vapc (V)	Standard DAC output control level estimated at 0.1 to 2.6V. Maximum Vapc level: Vdd-0.3V
Temperature	To (C)	-30, +25, +85°C

Option A

ACPM-7891 Test Board

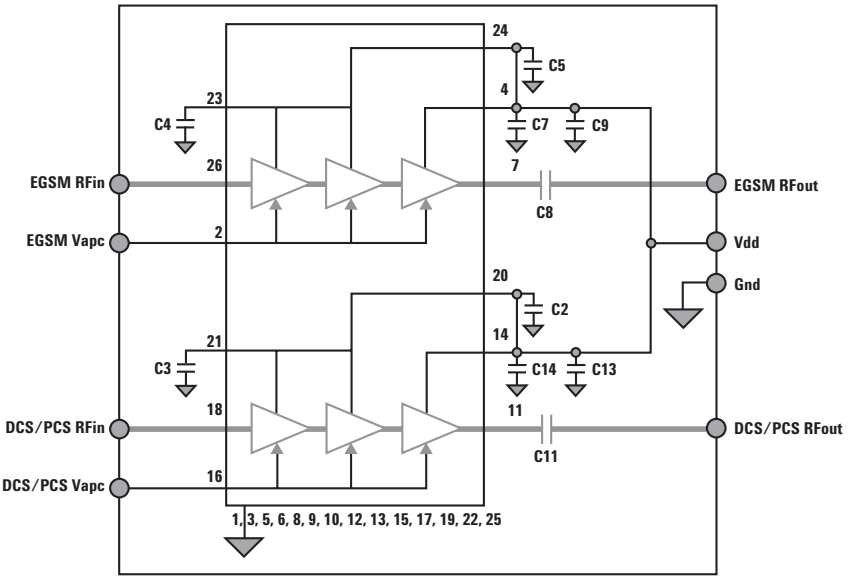
Figure 3 shows the schematic for the ACPM-7891 Test Board which provides a straightforward method of testing and evaluating the ACPM-7891. External RF sources, power and Vapc supplies are used.

Option B

Power Control Loop Design

The implementation of a transmitter power control is one of the most engineering-intensive and time-consuming aspects of GSM handset design. It dictates the correct transmit power level and burst shaping in a GSM network. The use of an off-the-shelf power control IC helps simplify the engineering effort and shorten the design cycle time.

The ACPM-7891 PA Control Board includes the ACPM-7891 PA, Linear Technology LTC1758-2 power control IC, EGSM/DCS/PCS directional couplers, triband diplexer and a 20-pin interface socket designed to work with an LTC1758 demo board from Linear Technology.



Component Label	Component Value
C2	.033 µF
C3	12 pF
C4	220 pF
C5	.033 µF
C7	220 pF
C8	33 pF
C9	.033 µF
C11	33 pF
C13	.033 µF
C14	27 pF

Figure 3. Schematic of ACPM-7891 Test Board.

Figure 4 depicts the basic block diagram of the ACPM-7891 PA control board, Figure 5 shows the control board layout, and Table 3 details its bill of materials.

The supporting LTC1758 demoboard is available upon request from Linear Technology. It has a 900 MHz and an 1800 MHz RF channel controlled by the LTC1758. Timing signals for TXEN are generated on the board using a 13 MHz crystal reference. The PCTL power control pin is driven by a 10-bit DAC and the DAC profile can be loaded via a serial port. The serial port data is stored in flash memory which is capable of storing eight ramp profiles. The board is supplied preloaded with four GSM power profiles and four DCS power profiles, covering the entire power range. External timing signals can also be used in place of the internal crystal controlled timing.

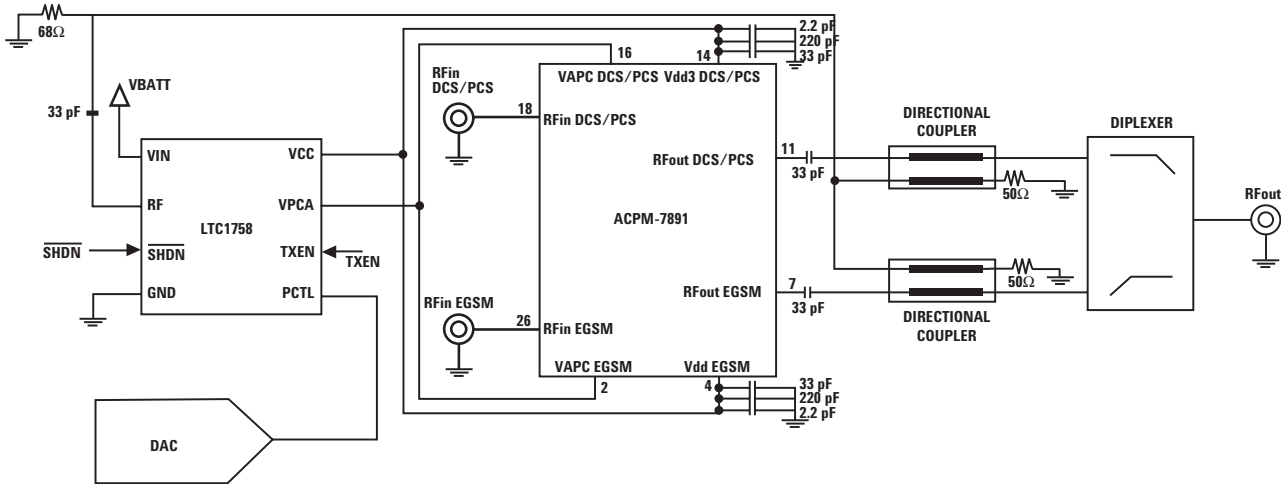


Figure 4. Block Diagram of the ACPM-7891 PA Control Board.

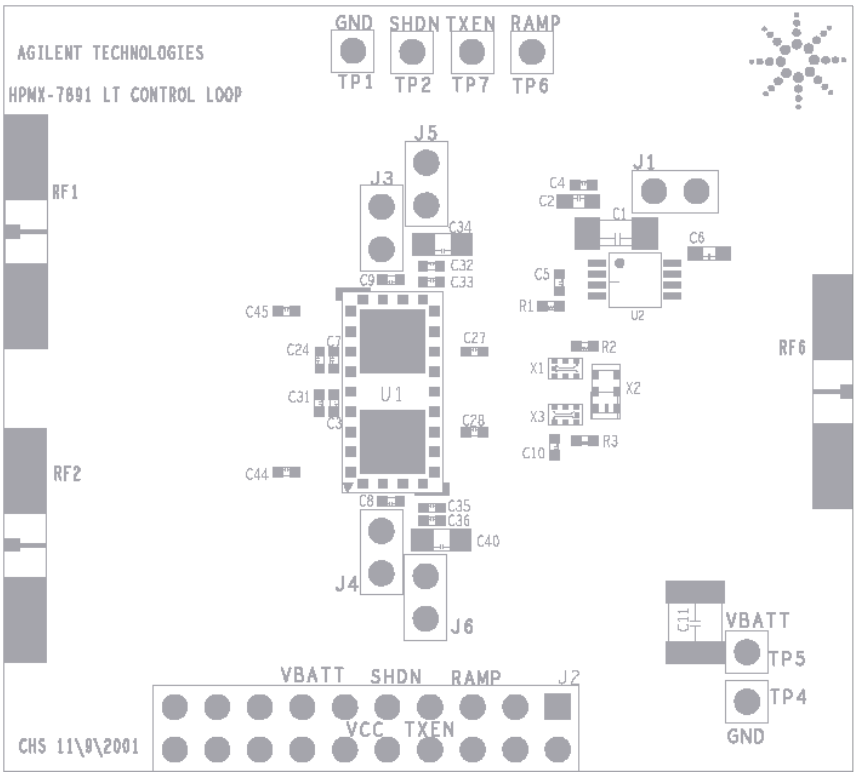


Figure 5. ACPM-7891 Control Board Layout.

Table 3. Bill of Materials for ACPM-7891 Control Board.

Qty	Device Type, Component Value & Tolerance	Reference
1	Avago ACPM-7891 Power Amplifier	U1
2	CAP_C0402-.033µF,+80,-20A .033µF +80	C24,C31
1	CAP_C0402- 15pF,5%, 50V, CEA 15pF 5%	C3
2	CAP_C0402- 220pF,10%, 50V, A 220pF10%	C33,C36
11	CAP_C0402- 33pF,5%, 50V, CEA 33pF 5%	C4, C5, C8, C9, C10, C27, C28, C32, C35, C44, C45
1	CAP_C0402- 47pF,5%, 50V, CEA 47pF 5%	C7
2	CAP_C0603- .1µF,5%, 20V, CEA .1µF 5%	C2, C6
1	CAP_TANT_C0805_T-ECST1AZ225R, CB 2.2µF +/-20%	C34
1	CAP_TANT_SMT6032-ECST1AZ225R, CB 2.2µF +/-20%	C4
1	CAP_C1206- .47µF,+80-20%, A .47µF +80-20%	C1
1	CONN20PIN_EDGE20-CONN20PIN,HEAB	J2
6	TP_FLAT-TP	TP1, TP2, TP4, TP5, TP6, TP7
5	JUMPER_2	J1, J3, J4, J5, J6
1	Murata LDC211G7420H-055, Directional Coupler	X1
1	Murata LDC21897M20H-056, Directional Coupler	X3
1	Murata LFD31897MDP1A010, Diplexer	X2
1	CAP_1812- 22µF, 10%, 10V, Taiyo Yuden LMK432	C11
1	Linear Technology LTC1758_LT_MSOP8, Control Loop IC	U2
1	MCR01J680, 68 5%	R1
2	RC-4-0402-50R0J, 50 5%	R2, R3
3	SMA_3	RF1, RF2, RF6

ACPM-7891 PA Control Board

We have designed the ACPM-7891 PA control board to interface with the LTC1758 demo board to simplify engineering efforts. Test Setup I, Figure 6, illustrates the equipment setup if the LTC1758 demo board is to be used with the ACPM-7891 PA Control Board.

However, the ACPM-7891 PA Control Board can also be tested without using the LTC1758 demo board. Test Setup II, Figure 7, illustrates the equipment setup under that scenario.

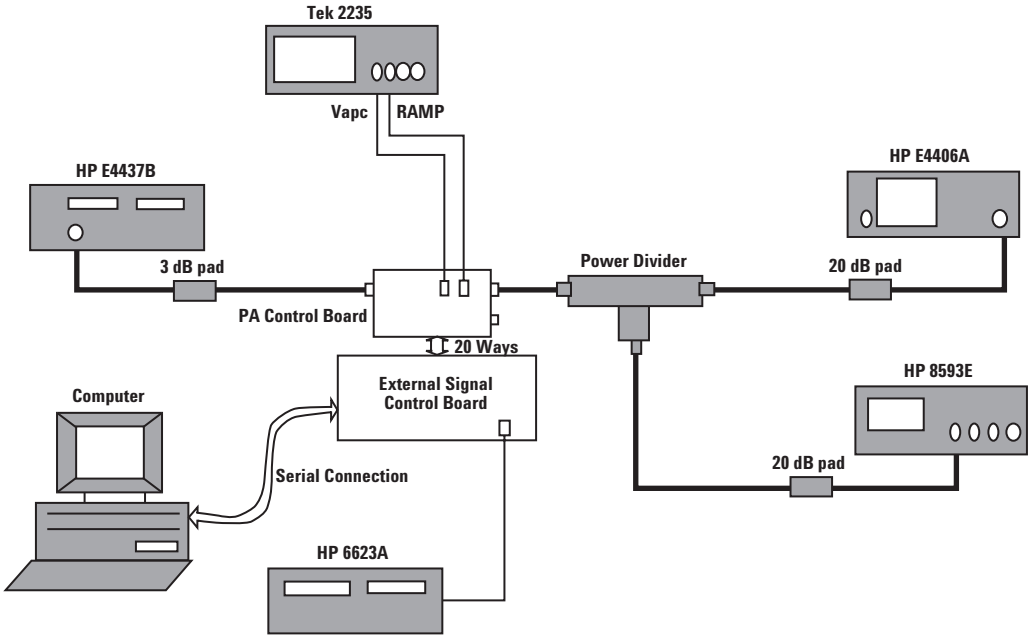


Figure 6. Test Setup with the LT1758 Demoboard.

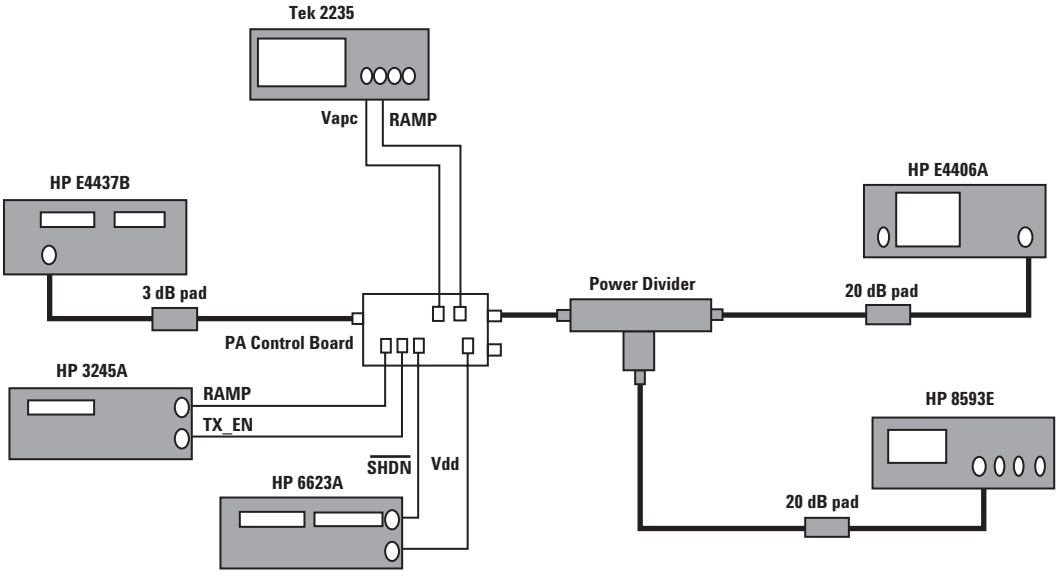


Figure 7. Test Setup without the LT1758 Demoboard.

Test Setup I
(With Linear Tech Board)

Connect an RF signal generator with GMSK modulated signal to RFin EGSM port (RF2) or RFin DCS/PCS (RF1) on the PA control board. The maximum input power at RF1 and RF2 is +10 dBm. Typically +2 dBm is applied for the EGSM, DCS/PCS channels. Connect two measurement instruments, one for spectrum analyzer and the other VSA, to RFout (RF6). The maximum output power should be limited to +35 dBm.

Connect the LTC-1758 demo board and the ACPM-7891 PA control board using 20 pin-connection socket. The external signal control board supplies bias voltage to PA control board and three timing signals — SHDN, TXEN and PCTL — to generate V_{PCA} signal of the LTC1758. The V_{PCA} signal is Power control voltage output and drives V_{APC} voltage of ACPM-7891 to define power ramp profile. Figure C2 in Appendix C details the LTC1758 timing diagram.

The RF power supply voltage of the PA control board is set by $V_{BATT\ ADJ}$ on the external signal control board. This voltage can be varied over a 2.7V to 5.3V range and is nominally set to 3.5V. The V_{BATT} voltage can be monitored on TP5 on the PA control board.

Linear Technologies supplies the application program associated with the .txt file to be downloaded to the FLASH memory. The program controls the code level of the DAC, whose data range is –1V to +1V. –1V corresponds to the zero code level and the actual 10-bit DAC range is 0V to +2.048V. The resolution is set about 2mV per step. The first sample of the data file is assigned the "default" value, which is included 1251 sample waveform of input data. This is a "code" value for the Lab View application program. The first sample being the default value and the other 1250 samples being the waveform data to be outputted to the DAC. The default value will then be loaded into all memory locations after the 1250 samples have been loaded. After programming the flash 16k segments the system can be set to run by setting the rotary switch to the programmed memory segment and resetting the external signal control board using the reset switch.

Test Setup II (Without Linear Tech Board)

Without LTC1758 demo board, we can get the same test result as above test. In this case, the Avago (HP) 3245A generates two relevant signals, TX_EN and RAMP with synchronized time.

Connect an RF signal generator with GMSK modulated signal to RFin EGSM port (RF2) or RFin DCS/PCS (RF1) on the PA control board. Typically +2 dBm is applied for the EGSM, DCS/PCS channels. Connect two measurement instruments, one for spectrum analyzer and the other VSA, to RFout (RF6). The maximum output power should be limited to +35 dBm.

Avago (HP) E4406A: The Avago E4406A, transmitter tester is used to measure power level in EGSM/DCS/PCS mode displaying the characteristic time mask.

Avago (HP) E4437B: The signal generator is used to provide GMSK GSM modulated input signal at a defined frequency.

Avago (HP)8593E: The Avago 8991A is a spectrum analyzer used to measure the output power of diplexer in the frequency and time domain.

Tek 2235: The Tek 2235 is an oscilloscope used to monitor RAMP signal and Vapc connected using the test points of PA control board.

Avago (HP) 6623A: The Avago 6623A, power supply is nominally set to voltage 3.5V for Vdd.

SHDN is set to 2.8V as high mode during TXEN and RAMP are enable.

Avago (HP) 3245A: The Avago 3245A, function generator with two channels is set to two relevant signals based on the GSM specification. One signal generates TX_EN with 2.7V that has a period of 4.615 ms with a duty cycle of 12.5% (577 µs) and 216 Hz frequency. This TX_EN connects to TX_EN (TP7) pin on the RF control board.

The other signal is RAMP signal that is same as PCTL of LTC1758. This RAMP connects to RAMP (TP6) pin on the RF control board.

Test Results

Using the demoboard with the Linear Technology IC, the results shown in Table 4 were obtained.

The LTC1758 RAMP signal is generated from a DAC and a simple single-pole filter is used to shape the power ramp. The input RF signal is based on the GSM GMSK modulated signal.

The results highlight the excellent power control functionality obtained by using the ACPM-7891 in conjunction with a power loop controller such as the LT1758. Results are given for all three bands, at four example power level settings, with the supply voltage at 3V, 3.6V and 4.3V. The figures show that excellent power output control is maintained over this supply voltage range, illustrating that the ACPM-7891 can enable designs that meet GSM transmitter specifications.

Table 4. Results with variable Vdd and three point frequency ranges

GSM900

Frequency	Vdd (V)	GSM5 (33 dBm) Vapc (V)	GSM5 (33 dBm) Pout (dBm)	GSM10 (23 dBm) Vapc (V)	GSM10 (23 dBm) Pout (dBm)	GSM15 (13 dBm) Vapc (V)	GSM15 (13 dBm) Pout (dBm)	GSM19 (5 dBm) Vapc (V)	GSM19 (5 dBm) Pout (dBm)
900 MHz	3.0	2.00	33.07	1.3	23.54	1.1	13.49	1.0	5.09
	3.6	1.60	33.04	1.3	23.55	1.1	13.51	1.0	5.12
	4.3	1.58	33.04	1.3	23.56	1.1	13.52	1.0	5.09

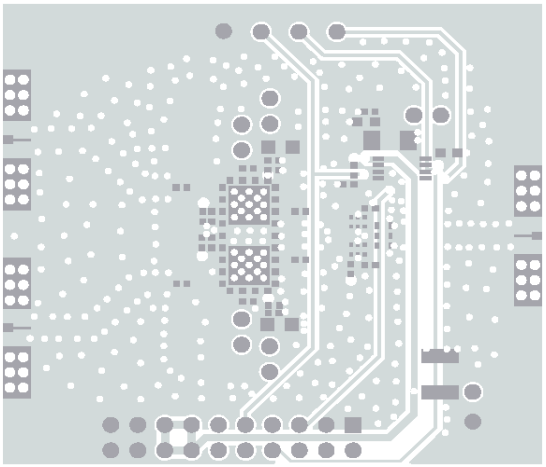
DCS1800

Frequency	Vdd (V)	DCS0 (30 dBm) Vapc (V)	DCS0 (30 dBm) Pout (dBm)	DCS5 (20 dBm) Vapc (V)	DCS5 (20 dBm) Pout (dBm)	DCS10 (10 dBm) Vapc (V)	DCS10 (10 dBm) Pout (dBm)	DCS15 (0 dBm) Vapc (V)	DCS15 (0 dBm) Pout (dBm)
1750 MHz	3.0	2.0	30.35	1.3	20.20	1.1	10.42	1.0	0.08
	3.6	1.7	30.32	1.3	20.17	1.1	10.40	1.0	0.06
	4.3	1.7	30.28	1.3	20.14	1.1	10.37	1.0	0.06

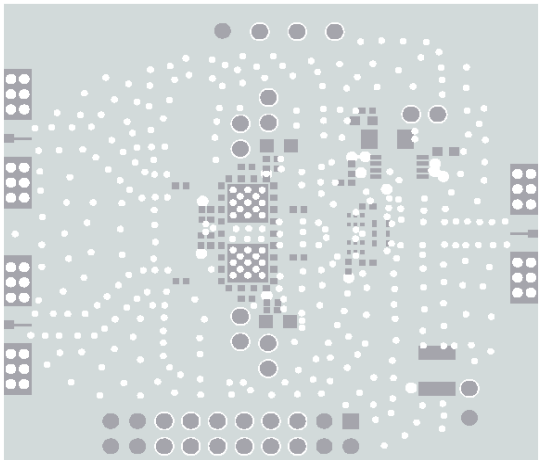
PCS1900

Frequency	Vdd (V)	PCS0 (30 dBm) Vapc (V)	PCS0 (30 dBm) Pout (dBm)	PCS5 (20 dBm) Vapc (V)	PCS5 (20 dBm) Pout (dBm)	PCS10 (10 dBm) Vapc (V)	PCS10 (10 dBm) Pout (dBm)	PCS15 (0 dBm) Vapc (V)	PCS15 (0 dBm) Pout (dBm)
1880 MHz	3.0	1.95	29.26	1.3	20.12	1.1	10.64	1.0	-0.04
	3.6	1.7	29.24	1.3	20.10	1.1	10.60	1.0	-0.05
	4.3	1.7	29.20	1.3	20.07	1.1	10.56	1.0	-0.09

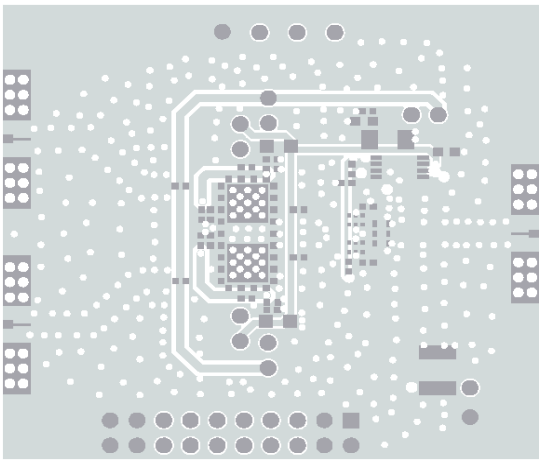
Appendix A
ACPM-7891 PA Control Board Layout



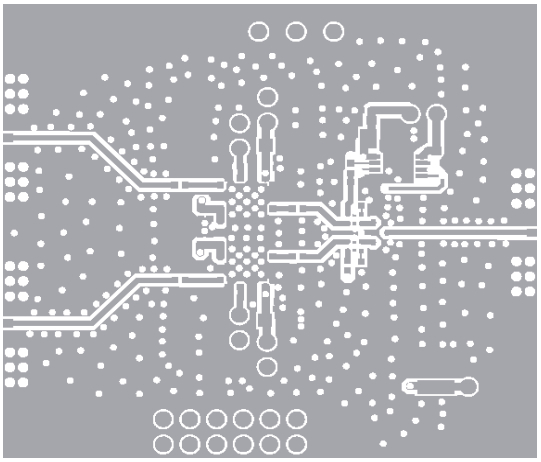
Bottom



GND



Power



Top

Appendix B
Stencil Design on PCB for ACPM-7891

In order to dissipate heat, additional via holes on the PCB are needed on the printed circuit board.

Solder mask should not be applied to thermal/ground plane underneath the vias in a way that will reduce heat transfer efficiency from conductive paddle to ambient. The stencil design enables solder paste to fill up the vias and form a solid conducting bar that further improves the thermal dissipation.

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure B1. The stencil has a solder paste deposition opening approximately 90% of the PCB pad. Reducing stencil opening of the conductive paddle potentially generate void underneath, on the other hand stencil opening larger than 100% will lead to excessive solder paste smear across the conductive paddle to adjacent I/O pads.

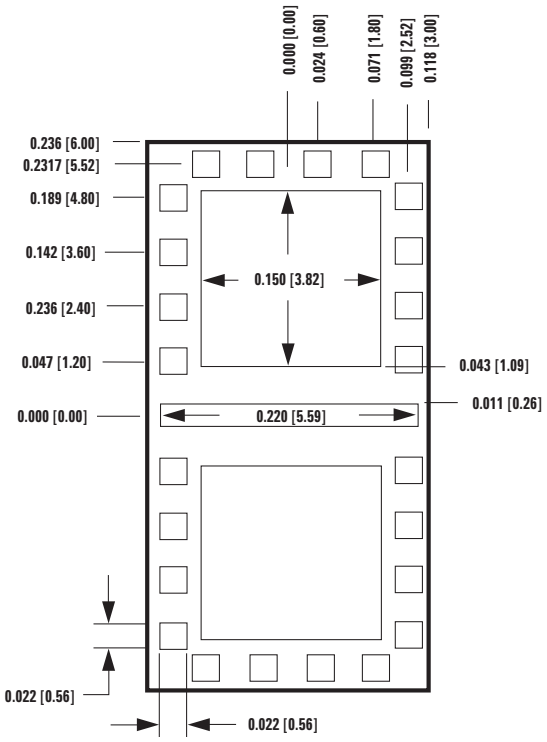


Figure B1. Recommended Stencil.

Appendix C
LTC1758 Theory of Operation

The LTC1758-2 is a dual band RF power controller for RF power amplifiers operating in the 850 MHz to 2 GHz range.

RF power is controlled by driving the RF amplifier power control pins and sensing the resultant RF output power via a directional coupler. The RF sense voltage is peak detected using an on-chip Schottky diode. This detected voltage is compared to the DAC voltage at the PCTL pin to control the output power. The RF power amplifier is protected against high supply current and high power control pin voltages. Internal and external offsets are cancelled over temperature by an autozero control loop, allowing accurate low power programming. The shutdown feature disables the part and reduces the supply current to <1_A.

Modes of Operation

The LTC1758-2 supports three operating modes: shutdown, autozero and enable.

In shutdown mode (SHDN = Low) the part is disabled and supply currents will be reduced to <1_A. VPCA and VPCB will be connected to ground via 100_ switches.

In autozero mode (SHDN = High, TXEN = Low) VPCA and VPCB will remain connected to ground and the part will be in the autozero mode. The part must remain in autozero for at least 50_s to allow for the autozero circuit to settle.

In enable mode (SHDN = High, TXEN = High) the control loop and protection functions will be operational. When TXEN is switched high, acquisition will begin. The control amplifier will start to ramp the control voltage to the RF power amplifier. The RF amplifier will then start to turn on. The feedback signal from the directional coupler and the output power will be detected by the LTC1758-2 at the RF pin. The loop closes and the amplifier output tracks the DAC voltage ramping at PCTL. The RF power output will then follow the programmed power profile from the DAC.

The LTC1758 datasheet provides more detailed description of the part's operation and can be downloaded from Linear Technology's website.

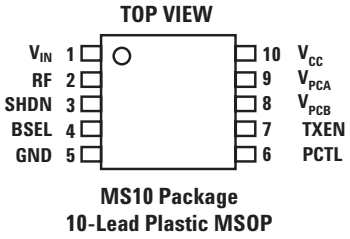
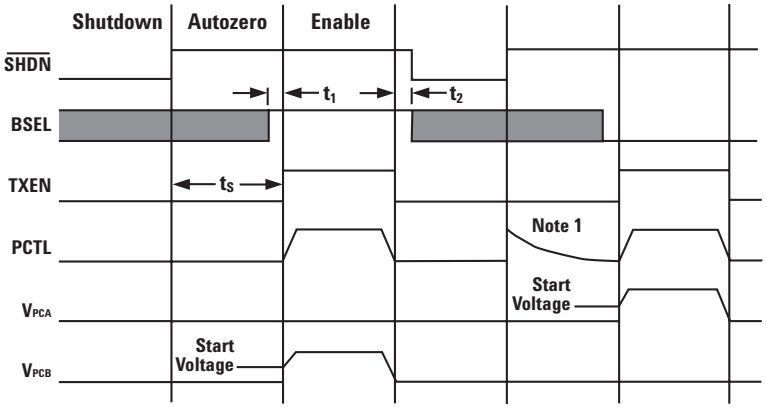


Figure C1. LTC-1758-2 Pinout.

MODE	$\overline{SHDN}$	TXEN	OPERATION
Shutdown	Low	Low	Disabled
Autozero	High	Low	Autozero
Enable	High	High	Power Control



tS: autozero settling time, 50μs minimum

t1: BSEL change prior to TXEN, 200ns typical

t2: BSEL change after TXEN, 200ns typical

Note 1: The external DAC driving the PCTL pin can be enabled during autozero. The autozero system will cancel the DAC transient. the DAC must be settled to an offset ≥ 400mv before TXEN is asserted high.

Figure C2. LTC1758-2 Timing Diagram.

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

Obsoletes 5988-8926EN
5988-9542EN May 22, 2006