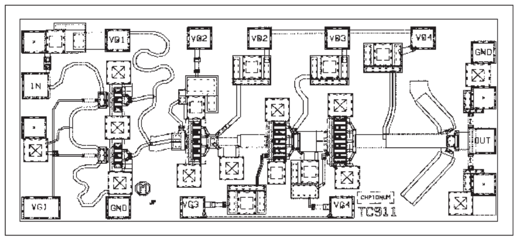
Avago HMMC-5038

38 GHz LNA

Data Sheet



Chip Size:	1630 x 760 µm (64.2 x 29.9 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions:	80 x 80 µm (3.1 x 3.1 mils)

Description

The HMMC-5038 MMIC is a high-gain low-noise amplifier (LNA) designed for communication receivers that operate from 37 GHz to 40 GHz. The gain of this four stage LNA can be adjusted by altering the gate bias of the output two, or three, stages while maintaining optimum noise figure bias for the input stage(s). Large FETs provide high power handling capability to avoid power compression. The backside of the chip is both RF and DC ground. This helps simplify the assembly process and reduce assembly related performance variations and costs. The HMMC-5038 is fabricated using a PHEMT integrated circuit structure that provides good noise and gain performance.

Features

- **Low noise figure:** 4.8 dB
- **Frequency range:** 37–40 GHz
- **High gain (adjustable):** 3 V, 120 mA @ 23 dB gain; 3 V, 80 mA @ 20 dB gain
- **50Ω input/output matching**

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
$V_{D1, 2\text{-}3\text{-}4}$	Drain Supply Voltages	V		5
$V_{G1, 2, 3\text{-}4}$	Gate Supply Voltages	V	-3.0	0
I_{DD}	Total Drain Current	mA		300
P_{in}	RF Input Power	dBm		15
T_{ch}	Channel Temperature[2]	°C		160
T_A	Backside Ambient Temp.	°C	-55	+125
T_{st}	Storage Temperature	°C	-65	+165
T_{max}	Maximum Assembly Temp.	°C		310

Notes:

1. Absolute maximum ratings for continuous operation unless otherwise noted.
2. Refer to DC Specifications/Physical Properties table for derating information.

HMMC-5038 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$V_{D1,2\text{-}3\text{-}4}$	Low Noise Drain Supply Operating Voltages	V	2	3	5
I_{D1}	First Stage Drain Supply Current (V_{DD} = 3 V, $V_{G1} \cong$ -0.8 V)	mA		22	
$I_{D2\text{-}3\text{-}4}$	Drain Supply Current for Stage 2, 3, and 4 Combined (V_{DD} = 3 V, $V_{GG} \cong$ -0.8 V)	mA		98	
$V_{G1,2\text{-}3\text{-}4}$	Gate Supply Operating Voltages ($I_{DD} \cong$ 120 mA)	V		-0.8	
V_P	Pinch-off Voltage (V_{DD} = 3 V, $I_{DD} \leq$ 10 mA)	V	-2	-1.2	-0.8
$\theta_{ch\text{-}bs}$	Thermal Resistance[2] (Channel-to-Backside at T_{ch} = 160°C)	°C/W		62	
T_{ch}	Channel Temperature[3] ($T_{backside}$ = 25°C)	°C		150	

Notes:
1. Backside ambient operating temperature T_A = 25°C unless otherwise noted.
2. Thermal resistance (°C/Watt) at a channel temperature T(°C) can be estimated using the equation: $\theta(T) \cong 62 \times [T(°C) + 273]/[160°C + 273]$.
3. De-rate MTTF by a factor of two for every 8°C above $T_{ch.}$

RF Specifications, T_A = 25°C, V_{DD} = 3V, I_{DD} = 120 mA, Z_o = 50Ω

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
BW	Operating Bandwidth	GHz	37		40
Gain	Small Signal Gain[1]	dB	20	23	
ΔGain	Small Signal Gain Flatness	dB		±0.5	
$\Delta S_{21}/\Delta T$	Temperature Coefficient of Gain	dB/°C		-0.4	
$(RL_{in})_{MIN}$	Minimum Input Return Loss w/o external capacitive matching[2]	dB	8	12	
$(RL_{out})_{MIN}$	Minimum Output Return Loss	dB	12	18	
Isolation	Reverse Isolation	dB		50	
P_{-1dB}	Output Power at 1dB Gain Compression	dBm		12	
NF	Noise Figure[3]	dB		4.8	5.5
ΔNF/ΔT	Temperature Coefficient of NF	dB/°C		+.02	

Notes:
1. Gain may be reduced by biasing for lower $I_{DD.}$ Increasing I_{DD} will increase gain.
2. Minimum input return may be improved by approximately 3 dB by including a small capactive (30 fF) stub on the input transmission line.
3. Noise figure may be further reduced by optimizing DC bias conditions.

Applications

The HMMC-5038 low noise amplifier (LNA) is designed for use in digital radio communication systems and point-to-multipoint links that operate within the 37 GHz to 40 GHz frequency band. High gain and low noise temperature make it ideally suited as a front-end gain stage in the receiver. The MMIC solution is a cost effective alternative to hybrid assemblies.

Biasing and Operation

The recommended DC bias condition is with all drains connected to single 3 volt supply and all gates connected to an adjustable negative voltage supply as shown in Figure 6. The gate voltage is adjusted for a total drain supply current of typically 120 mA.

Reducing the current in stages 3 and 4 will reduce the overall gain. The gain can be adjusted further by altering the current through stage 2 with little effect on noise figure. Optimum noise figure is realized with V_{D1} = 3 to 4 volts and I_{D1} = 20 to 25 mA.

The second, third, and fourth stage DC drain bias lines are connected internally and therefore require only a single bond wire. An additional bond wire is needed for the first stage DC drain bias, V_{D1}.

The third and fourth stage DC gate bias lines are connected internally. A total of three DC gate bond wires are required: one for V_{G1}, one for V_{G2}, and one for the V_{G3}-to-V_{G4} connection as shown in Figure 6(b).

A DC blocking capacitor is needed in the RF input transmission line only if there is DC voltage present. The RF output is AC-coupled.

Optimum input match is achieved when an optional capacitive (30 fF) stub is included on the input transmission line. This capacitance complements the bond wire inductance to complete the input matching network.

No ground wires are needed because ground connections are made with plated through-holes to the backside of the device.

Assembly Techniques

It is recommended that the RF input and RF output connections be made using either 500 line/inch (or equivalent) gold wire mesh, or dual 0.7 mil diameter gold wire. The RF wires should be kept as short as possible to minimize inductance. The bias supply wires can be a 0.7 mil diameter gold.

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Avago application note #54, “GaAs MMIC ESD, Die Attach and Bonding Guidelines” provides basic information on these subjects.

HMMC-5038 Typical Performance Characteristics

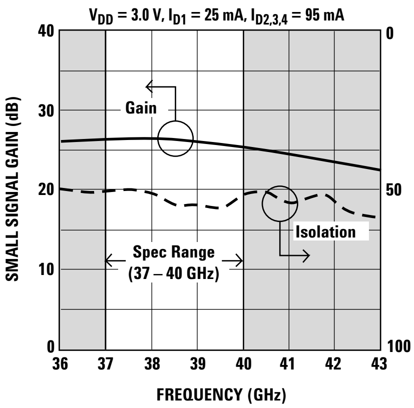


Figure 1. Gain and Isolation vs. Frequency.

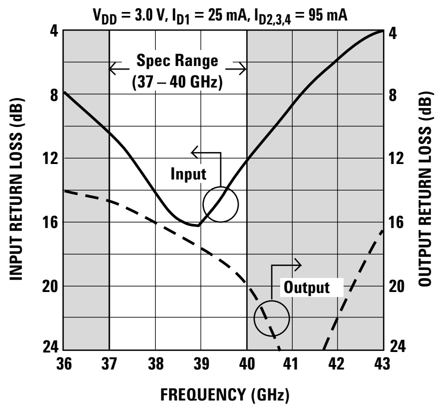


Figure 2. Input and Output Return Loss vs. Frequency.

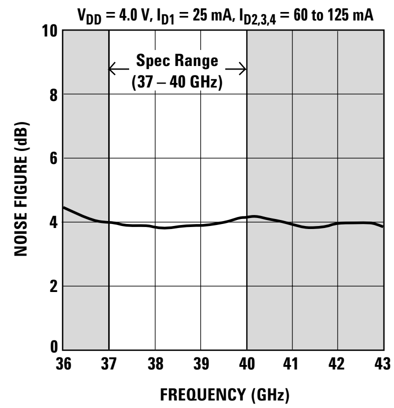


Figure 3. Noise Figure vs. Frequency.

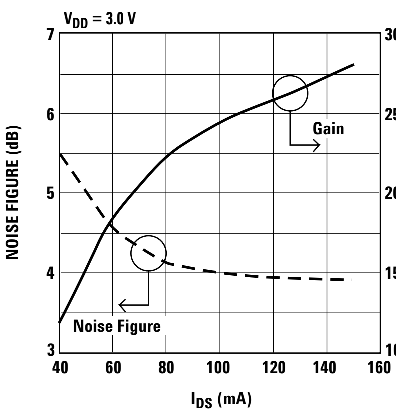


Figure 4. 38 GHz Noise Figure and Gain vs. I_{DD}.

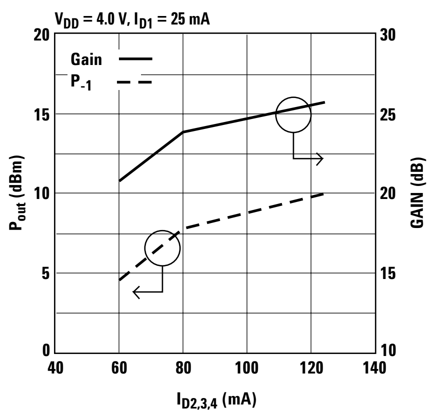


Figure 5. 38 GHz Gain and Power Performance vs. I_{DD}.

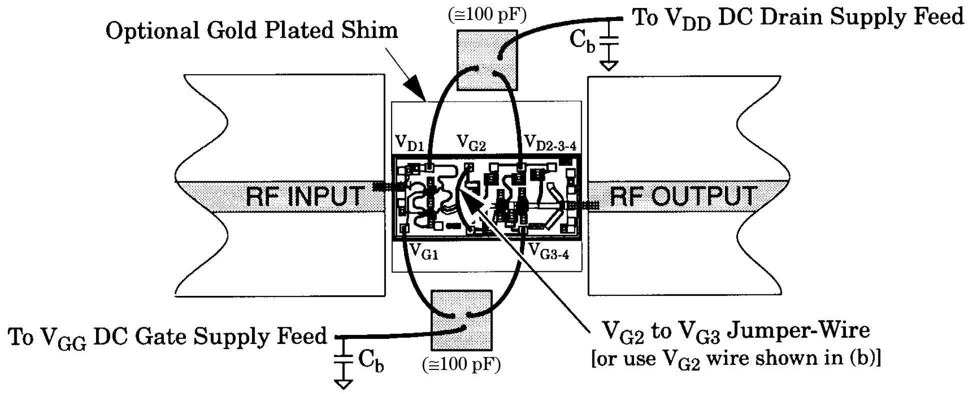


Figure 6a. Single drain-supply and single gate-supply assembly.

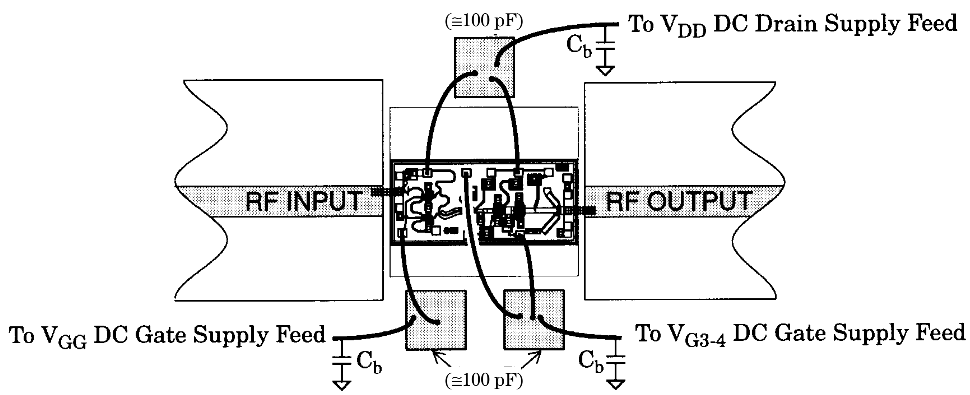


Figure 6b. Separate first-stage gate bias supply.

This diagram shows an optional variation to the V_{G2} jumper-wire bonding scheme presented in (a).

Figure 6. HMMC-5038 Common Assembly Diagrams.

(Note: To assure stable operation, bias supply feeds should be bypassed to ground with a capacitor, C_b > 100 nF typical.)

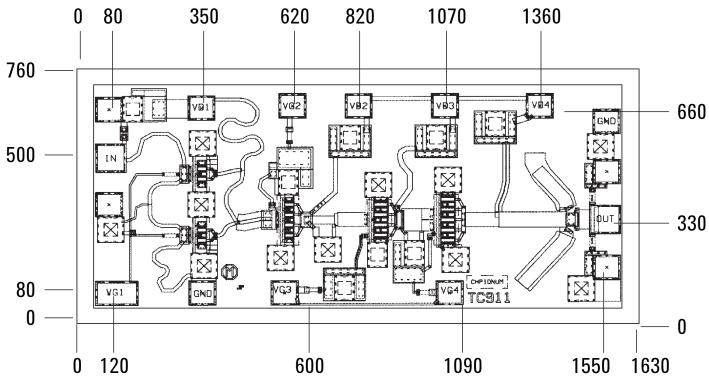


Figure 7. HMMC-5038 Bonding Pad Positions. (Dimensions are in micrometers)

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Avago Technologies' sales representative.

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

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