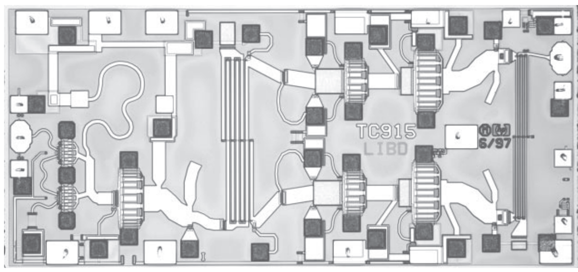
Avago HMMC-5033

17.7–32 GHz Power Amplifier

Data Sheet



Chip Size:	2.74 x 1.31 mm (108 x 51.6 mils)
Chip Size Tolerance:	±10 µm (±0.4 mils)
Chip Thickness:	127 ± 15 µm (5.0 ± 0.6 mils)

Description

The HMMC-5033 is a MMIC power amplifier designed for use in wireless transmitters that operate within the 17.7 GHz to 32 GHz range. At 28 GHz it provides 26 dBm of output power (P_{-1dB}) and 18 dB of small-signal gain from a small easy-to-use device. The HMMC-5033 was designed to be driven by the HMMC-5040 (20–40 GHz) or the HMMC-5618 (5.9–20 GHz) MMIC amplifier for linear transmit applications. This device has input and output matching circuitry for use in 50 ohm environments.

Features

- **26 dBm output $P_{(-1dB)}$ at 28 GHz**
- **High gain: 1.8 dB**
- **50Ω input/output matching**
- **Small size**
- **RF detector network**

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_{D1}, V_{D2}	Drain Supply Voltages	V		5.2
V_{G1}, V_{GG}	Gate Supply Voltages	V	-3.0	0.5
I_{D1}	First Stage Drain Current	mA		320
I_{D2}	Second Stage Drain Current	mA		640
P_{in}	RF Input Power	dBm		23
Det. Bias	Applied Detector Bias (Optional)	V		5.2
T_{ch}	Channel Temperature[2]	°C		170
T_A	Backside Ambient Temp.	°C	-55	+85
T_{st}	Storage Temperature	°C	-65	+170
T_{max}	Max. Assembly Temperature	°C		300

Notes:

1. Absolute maximum ratings for continuous operation unless otherwise noted.
2. Refer to DC Specifications/Physical Properties table for derating information.

HMMC-5033 DC Specifications/Physical Properties[1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
V_{D1}	Drain Supply Operating Voltage	V		3.5	5
V_{D2}	Drain Supply Operating Voltage	V		5	5
I_{D1}	First Stage Drain Supply Current (V_{D1} = 3.5 V, V_{G1} = Open, V_{GG} set for I_{D2} typical)	mA		240	320
I_{D2}	Second Stage Drain Supply Current (V_{D2} = 5 V, $V_{GG} \cong$ -0.8 V)	mA		460	640
V_{G1}, V_{GG}	Gate Supply Operating Voltages ($I_{D1} + I_{D2} \cong$ 700 mA)	V		-0.8	
V_P	Pinch-Off Voltage [V_{DD} = 2.5 V, (I_{D1}+ I_{D2}) $\leq$ 20 mA]	V	-2.5	-1.2	-0.8
Det. Bias	Detector Bias Voltage (Optional)	V		V_{D2}	5
$\theta_{1(ch\text{-}bs)}$	First Stage Thermal Resistance[2] (Channel-to-Backside at T_{ch} = 160°C)	°C/W		67	
$\theta_{2(ch\text{-}bs)}$	Second Stage Thermal Resistance[2] (Channel-to-Backside at T_{ch} = 160°C)	°C/W		37	
T_{ch}	Channel Temperature[3] (T_A= 75°C, MTTF $\geq 10^6$ hrs, V_{D2} = 5 V, I_{D2} = 460 mA)	°C		160	

Notes:
1. Backside ambient operating temperature T_A = 25°C unless otherwise noted.
2. Thermal resistance (in °C/Watt) at a channel temperature T(°C) can be estimated using the equation: $\theta(T) \cong \theta_{ch\text{-}bs}$ x [T(°C) + 273]/[160°C + 273].
3. Derate MTTF by a factor or two for every 8°C above $T_{ch.}$

HMMC-5033 RF Specifications, (T_A = 25°C, Z_0 = 50 Ω, V_{D1} = 3.5 V, V_{D2} = 5 V, I_{D2} = 460 mA, $I_{D1} \cong$ 240 mA)

			Lower Band Specifications			Mid Band Specifications			Upper Band Specifications		
Symbol	Parameters/Conditions	Units	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
BW	Operating Bandwidth	GHz	17.7		21	21		26.5	25		31.5
Gain	Small Signal Gain	dB	17	22		17	20		15	18	
P_{-1dB}	Output Power at 1 dB Gain Compression	dBm	22	23		24	25		25	26	
P_{sat}	Saturated Output Power[1]	dBm		25			27			28	
$RL_{in(min)}$	Minimum Input Return Loss	dB	8	10		9	12		10	12	
$RL_{out(min)}$	Minimum Output Return Loss	dB	15	20		15	20		15	20	
Isolation	Minimum Reverse Isolation	dB		50			50			50	

Note:
1. Devices operating continuously beyond 1 dB gain compression may experience power degradation.

Applications

The HMMC-5033 MMIC is a broadband power amplifier designed for use in transmitters that operate in various frequency bands between 17.7 GHz and 32 GHz. It can be attached to the output of the HMMC-5040 (20 – 40 GHz) or the HMMC-5618 (5.9 – 20 GHz) MMIC amplifier, increasing the power handling capability of transmitters requiring linear operation.

Biasing and Operation

The recommended DC bias condition for optimum efficiency, performance, and reliability is V_{D1} = 3.5 volts and V_{D2} = 5 volts with V_{GG} set for $I_{D1} + I_{D2}$ = 700 mA (no connection to V_{G1}). This bias arrangement results in default drain currents I_{D1} = 240 mA and I_{D2} = 460 mA.

A single DC gate supply connected to V_{GG} will bias all gain stages.

If operation with both V_{D1} and V_{D2} at 5 volts is desired, an additional wire bond connection from the V_{G1} pad to the V_{GG} external bypass chip-capacitor (shorting V_{G1} to V_{GG}) will balance the currents in each gain stage. V_{GG} (= V_{G1}) can be adjusted for $I_{D1} + I_{D2}$ = 700 mA.

Muting can be accomplished by setting V_{G1} and/or V_{GG} to the pinchoff voltage V_P.

An on chip RF output power detector network is provided. The differential voltage between the Det-Ref and Det-Out pads can be correlated with the RF power emerging from the RF Output port. Bias the diodes at ~200 mA.

The RF ports are AC-coupled at the RF input to the first stage and the RF output of the second stage.

If the output detector is biased using the on-chip optional Det-Bias network, an external AC-blocking capacitor may be required at the RF Output port.

No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

Assembly Techniques

It is recommended that the electrical connections to the bonding pads be made using 0.7–1.0 mil diameter gold wire. The microwave/millimeter-wave connections should be kept as short as possible to minimize inductance. For assemblies requiring long bond wires, multiple wires can be attached to the RF bonding pads.

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Avago application note #54, “GaAs MMIC ESD, Die Attach and Bonding Guidelines” provides basic information on these subjects.

Additional References:

AN# 52, “1 Watt 17.7 GHz – 32 GHz Linear Power Amplifier,” and PN#6, “HMMC-5033 Intermodulation Distortion.”

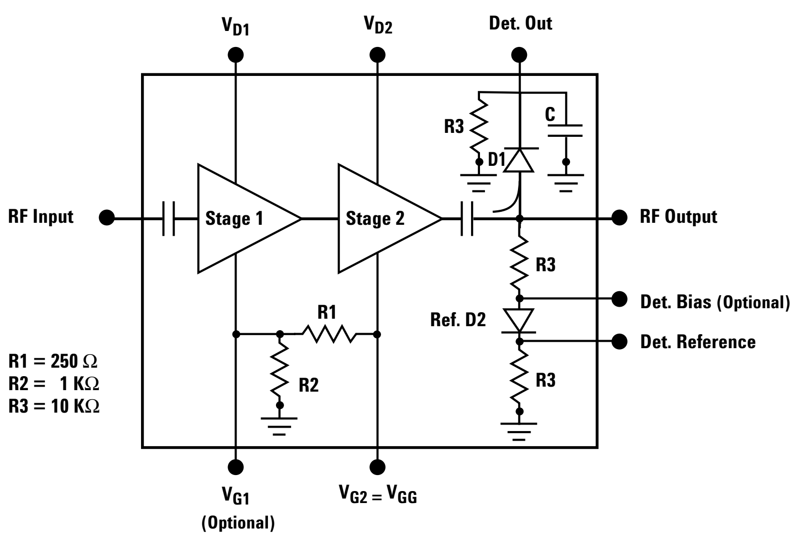


Figure 1. HMMC-5033 Simplified Schematic Diagram.

HMMC-5033 Typical Performance Characteristics

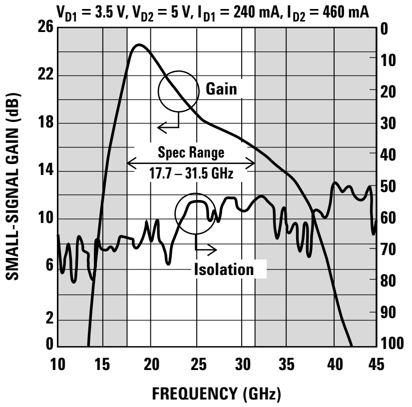


Figure 2. Gain and Isolation vs. Frequency.

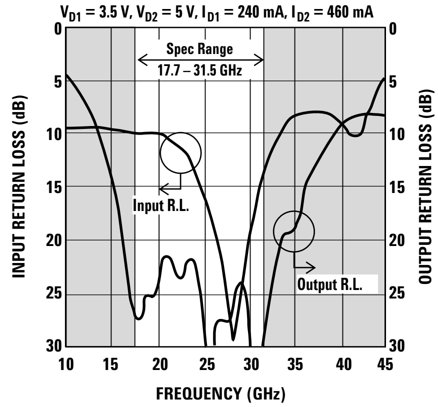


Figure 3. Input and Output Return Loss vs. Frequency.

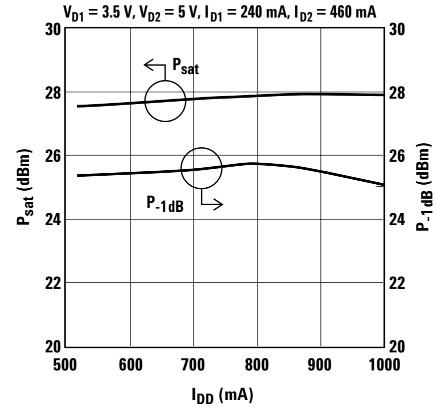


Figure 4. Output Power vs. Total Drain Current.

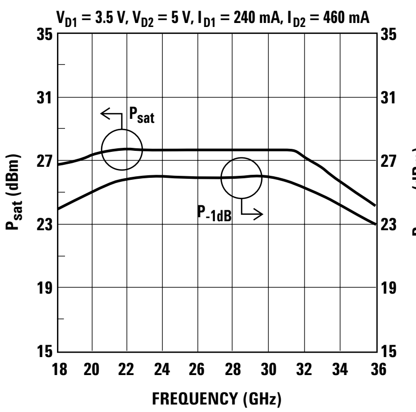


Figure 5. Output Power vs. Frequency.

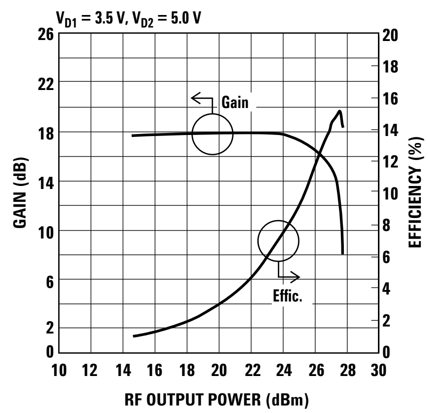


Figure 6. Gain Compression and Efficiency at 28 GHz.

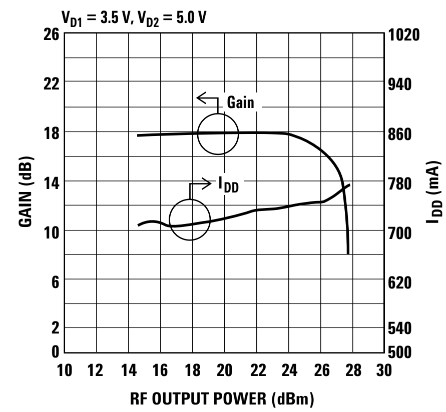


Figure 7. Gain and Total Drain Current vs. Output Power.

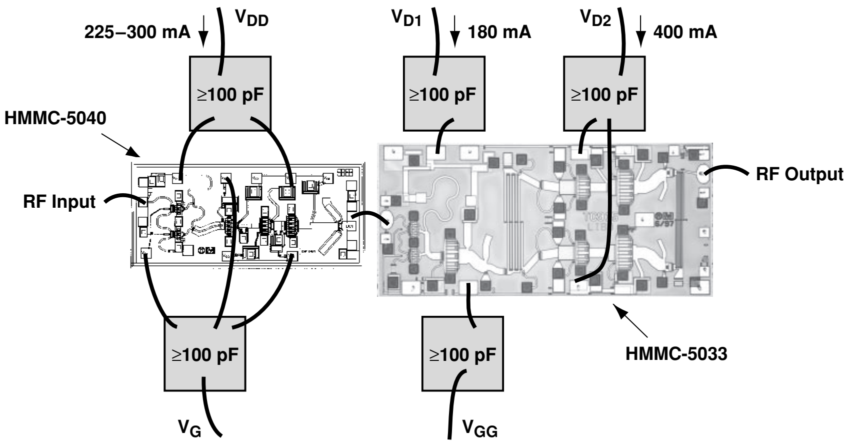


Figure 8. Assembly diagram illustrating the HMMC-5033 cascaded with the HMMC-5040 for 20–32 GHz applications.

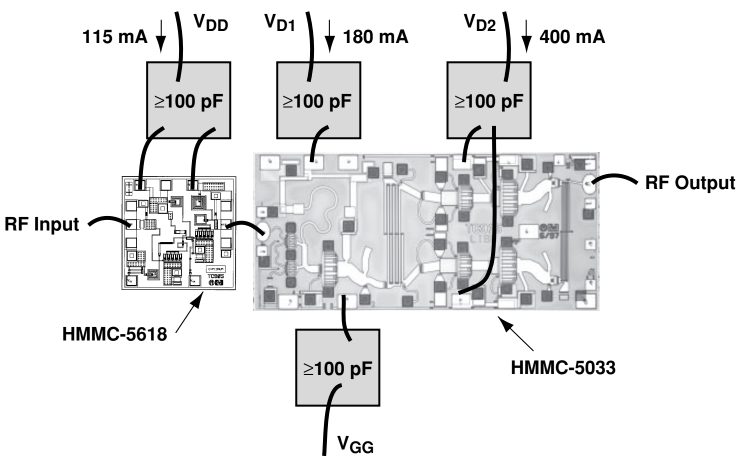


Figure 9. Assembly diagram illustrating the HMMC-5033 cascaded with the HMMC-5618 for 17.7–20 GHz applications.

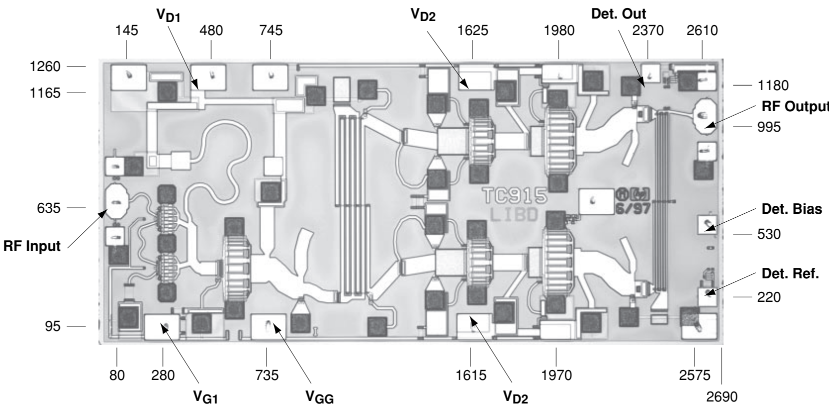


Figure 10. HMMC-5033 Bonding Pad Locations. (Dimensions are in micrometers)

This data sheet contains a variety of typical and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term *typical* refers to the 50th percentile performance. For additional information contact your local Avago Technologies' sales representative.

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

Obsoletes 5966-4573E
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