SMART Duplex Single Mode Transceivers

Application Note 1098

Introduction

This application note details the recommended circuit connections for Avago's duplex single mode transceiver products shown in Table 1.

Avago supplies an evaluation board, the HFCT-5000.

All products listed in Table 1 are 155 Mb/s SONET/SDH compliant SC receptacled transceivers, except the HFCT-5103, which is FDDI and Fast Ethernet power compliant and operates at 100-125 Mb/s.

Table 1 gives details of the options available for these products. Consult product marketing for availability and complete data sheets.

Functional Description

Transmitter Section

Design

The transmitter section, shown in Figure 1, uses a laser as its optical source which has been designed to be compliant with IEC 825 eye safety requirements under fault conditions. The optical output is controlled by a custom IC which detects the laser output via the monitor photodiode. This IC provides both DC and AC current drive to the laser to ensure correct modulation, eye diagram and extinction ratio over temperature, supply voltage and end of life. The IC provides laser shutdown, the modulation current and laser bias current is reduced to zero. Facilities are provided to monitor the laser bias and monitor diode status on the 2 x 9 products listed in Table 1.

Table 1. Avago Duplex Single Mode Transceiver Products

Part Number	+5 V	Intermediate Reach	Long Reach	1 x 9 Pinout	2 x 9 Pinout	-40° C to +85° C	0° C to +70° C	Black Case	Blue Case
HFCT-5205A	3	3		3		3		3	
HFCT-5205B	3	3		3			3	3	
HFCT-5205C	3	3		3		3			3
HFCT-5205D	3	3		3			3		3
HFCT-5103B	3			3			3	3	
HFCT-5103D	3			3			3		3
HFCT-5201A	3	3			3	3		3	
HFCT-5201B	3	3			3		3	3	
HFCT-5201C	3	3			3	3			3
HFCT-5201D	3	3			3		3		3
HFCT-5215B	3		3	3			3	3	
HFCT-5215D	3		3	3			3		3

Electrical Characteristics

Supply Voltage

The transceiver module operates with a positive supply voltage in the range +4.75 V to +5.25 V. Pins labeled N/C must not be connected.

Care should be taken to avoid power supply transients. These products are not recommended for 'hot plug' applications.

Noise Immunity

It is recommended that the power supply filter network illustrated in Figure 1 is used to further improve device performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Power Supply Filtering

Good power supply filtering is required for optimum transmitter performance. The results are shown in Figure 2 for DC supply +5.0 V @+25° C without power supply filtering present. When using the recommended filter arrangement, power supply noise >100 mV pk-pk, over a frequency range of 10 Hz to 1 MHz, can be tolerated before a receiver sensitivity penalty of 1.0 dB occurs.

Data Inputs

Figure 3 shows the recommended interface circuit for the transmitter data inputs.

Single-ended operation is not recommended as data sheet specifications can only be guaranteed when both differential inputs are used.

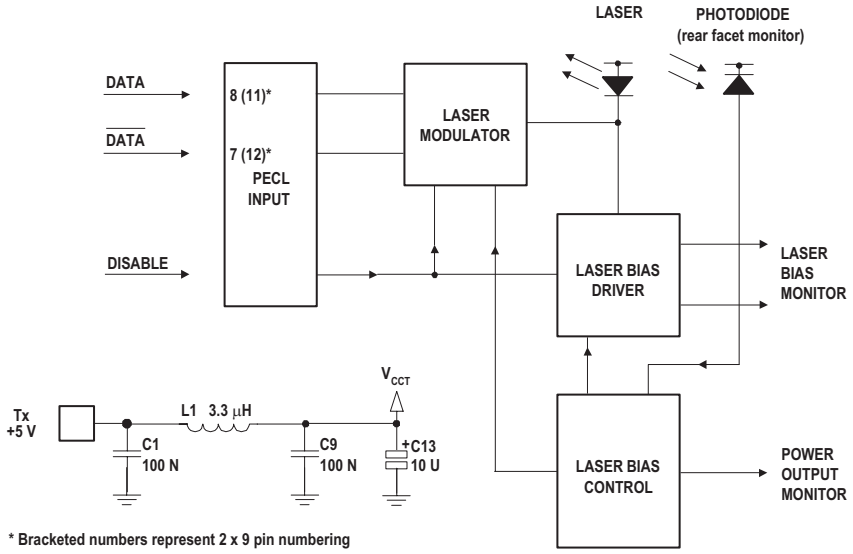


Figure 1. Simplified Transmitter Schematic and Recommended Transmitter Power Supply Filtering

Notes:
1. Pseudo-ECL Logic is ECL Logic operated from +5 V power supplies.
2. The electrical interface is PECL in both the transmitter and receiver. The optical interface is a duplex SC connector.

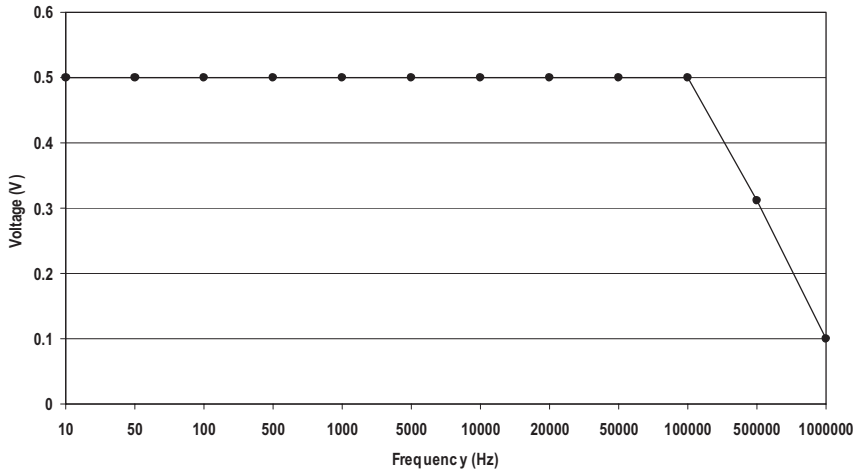


Figure 2. HFCT-5205/HFCT-5103/HFCT-5201/HFCT-5215 Tolerable Transmitter Injected Power Supply Noise Amplitude versus Frequency without Power Supply Filtering

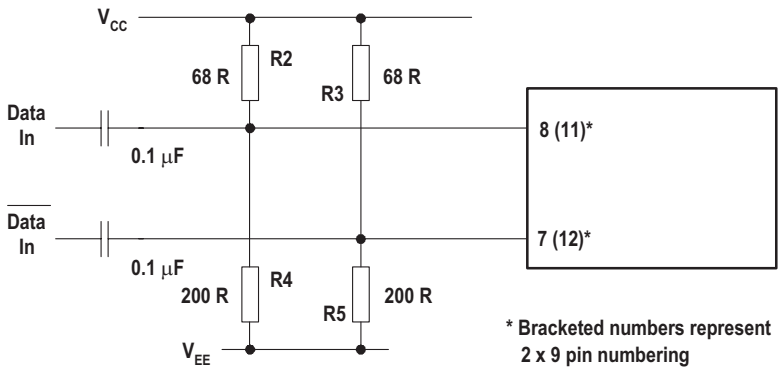


Figure 3. Recommended Interface Circuit for the Transmitter Data Inputs

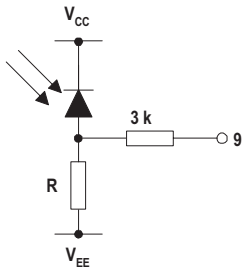


Figure 5. Laser Power Monitor External Connection for the HFCT-5201 listed in Table 1

The data and data inputs will accept standard PECL levels (10 KH). The use of standard logic levels is recommended although inputs will toggle with swings between 250 mV and 1 V peak-to-peak when driven differentially.

Both inputs are internally tied to V_{CC} -1.3 V. Adequate decoupling to the supply rails must be provided as close to the termination resistors as possible.

Care must be taken to choose a large enough capacitor to give the required low-frequency cutoff. The frequency is defined as ½ π RC(Hz) where R is the termination resistor. The low-frequency cutoff should be set to approximately a factor of 10 below the lowest frequency content of the transmitted signal. A 0.1 μF capacitor is recommended.

Transmitter Signal Input

The inputs to the transceiver module transmitter will require a 50% duty cycle or DC balanced signal for normal operation. Failure to provide this may cause the optical parameters to move out of specification. Extinction ratio and duty cycle distortion may be affected. The lower cutoff frequency of the transmitter mean power control loop is <20 kHz.

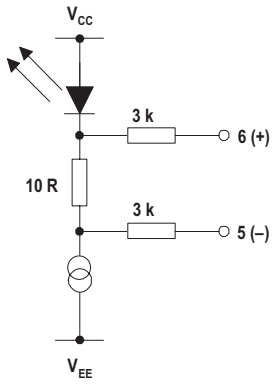


Figure 4. Bias Monitor External Connections for the HFCT-5201 listed in Table 1

The module will function with up to 72 consecutive 1's or 0's within the PRBS pattern as specified by CCITT G.957 (ITU) for STM-1/STM-4.

In the absence of data the transmitter will emit a mean optical power within the specified limit.

Analog Monitor Points

Bias Monitor

The external connections to the laser bias monitor for the HFCT-5201 product listed in Table 1 is implemented as in Figure 4.

During normal (modulated) operation the bias current will correspond approximately to laser threshold. In the absence of data the bias current will be equal to the laser forward current required to give the correct optical output power. This will equate to the laser bias current plus half of the current previously supplied by the data modulation current, Equation A.

$$\text{Equation A: } I_{bias} = I_{th} + \frac{I_{mod}}{2}$$

The differential voltage generated between pin 5 and pin 6 is 10 mV/mA with a common mode voltage of approximately V_{CC} -1.6 V (to Pin 6).

This monitor may be used to detect an end-of-life bias current. A typical example is to have an end-of-life current of 70 mA. This will give a differential voltage of 0.7 V at end-of-life and Tmax. It is important to note that if such an alarm is used the absence of data will increase the bias current and may cause a false alarm. Users should note that bias current is temperature dependent. For more accurate alarms a temperature compensated operational alarm point will need to be provided by the user. For most applications a 70 mA end-of-life alarm will be sufficient.

Power Monitor

For the HFCT-5201 product listed in Table 1, external connections are provided to the monitor photodiode that measures the rear facet power of the laser diode, as shown in Figure 5. This connection is part of the output power control loop.

Under normal operation, modulated or not, this voltage will remain constant ±10% (over life, over temperature). The DC voltage is measured at pin 9. The voltage on pin 9 is nominally 1.21 V with respect to V_{EE} (a bandgap voltage). Note this voltage should be measured into a high impedance.

This monitor may be used to detect a high or low optical power failure. Any such failure would be catastrophic and so the alarm should be set to ±50% of the initial value to detect gross movement.

An airflow of $\geq$ 2 m/s must be provided to ensure that the case temperature does not exceed the specified maximum operating ambient temperature.

Functional Description

Receiver Section

Design

The receiver section contains an InGaAs/InP PIN diode and a preamplifier within the receptacle. This couples to a single postamp and signal detect circuit on a separate circuit board. The postamplifier is AC coupled to the preamplifier as illustrated in Figure 6. The coupling capacitor is large enough to pass the SONET/SDH test pattern at the rated speed without significant distortion or performance penalty. If a lower signal rate, or a code which has significantly more low-frequency content is used, sensitivity, jitter and pulse distortion could be degraded.

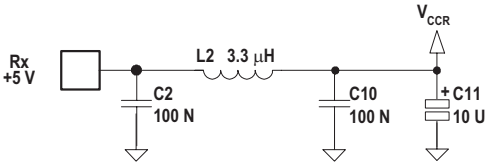


Figure 7. Recommended Receiver Power Supply Filtering

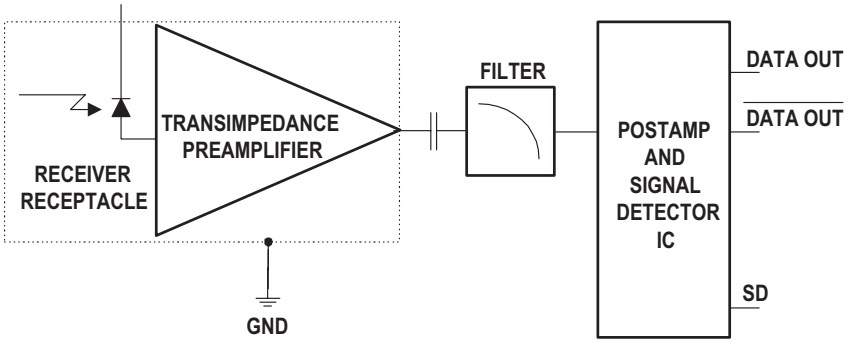


Figure 6. Simplified Receiver Schematic

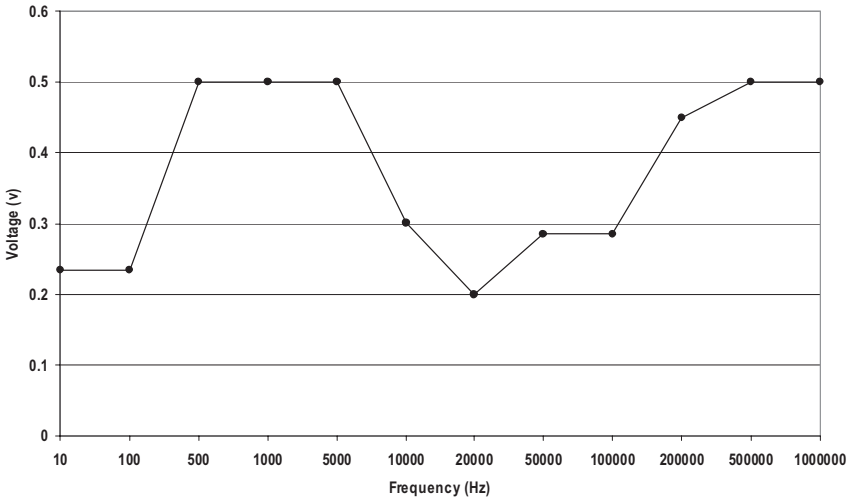


Figure 8. HFCT-5205/HFCT-5103/HFCT-5201/HFCT-5215 Tolerable Receiver Injected Power Supply Noise Amplitude versus Frequency without Power Supply Filtering

Figure 6 schematically shows a filter network that limits the bandwidth of the preamp output signal. The filter is designed to bandlimit the preamp output noise and thus improve the receiver sensitivity.

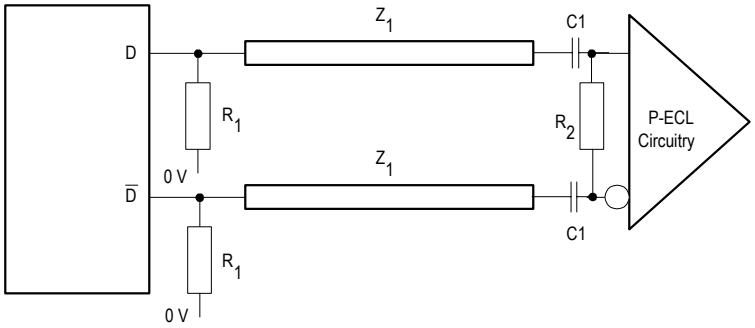
These components will also reduce the sensitivity of the receiver as the signal bit rate is increased above the rated speed.

Electrical Characteristics

Supply Voltage

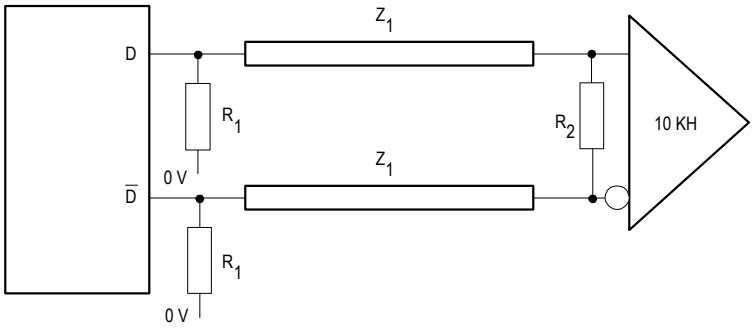
The receiver module operates from a positive supply in the range +4.75 V to +5.25 V.

Option 1. P-ECL Operation, Capacitively Coupled, as on HFCT-5000 evaluation board



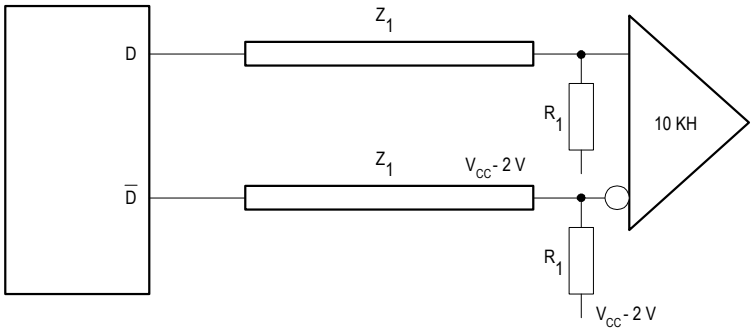
(1) C_1 = 100 nF
R_1 = 270 Ω
R_2 = 100 Ω
Z_1 = 50 Ω Interconnect
Z_1 = 50 Ω Interconnect
R_1 = 270 Ω
R_2 = 100 Ω

Option 2. P-ECL Operation, DC coupled



(2) Z_1 = 50 Ω Interconnect
R_1 = 50 Ω

Option 3. 50 Ω to V_{CC} – 2 V



Note:
1. Options 1 to 3 show termination configurations for data and data outputs.
2. 50 Ω to -2 V may be replaced by the Thevenin equivalent 82 Ω to V_{CC} and 130 Ω to V_{EE}.

Figure 9. Examples of ECL Terminations

Noise Immunity

The receiver includes internal circuit components to filter power supply noise. The results are shown in Figure 8 for a DC supply of +5.0 V without power supply filtering present. However, good power supply filtering is required for optimum receiver performance. It is recommended that the filter network illustrated in Figure 7 is used to further improve device performance. The values of the filter components are general recommendations and may be changed to suit a particular system environment. Shielded inductors are recommended.

Power Supply Filtering

The LC filtering technique illustrated in Figure 7 provides power supply noise immunity of >100 mV pk-pk, over a frequency range of 10 Hz to 1 MHz, before a receiver sensitivity penalty of 1.0 dB occurs.

Receiver Signal Input

The transceiver module receiver will function with up to 72 consecutive 1's or 0's within the PRBS pattern of the optical input signal as specified by CCITT G.957 (ITU) for STM-1/STM-4.

Receiver Data Output

Figure 9 shows one recommended electrical interface circuit configuration for the receiver data outputs. The data and data output voltage levels conform to PECL standard levels (10 kH). Single-ended operation is not recommended as data sheet specifications can only be guaranteed when both differential outputs are used.

Supply Transients

Care should be taken to avoid power supply transients. These products are not recommended for 'hot-plug' applications.

The Signal Detect Circuit

The signal detect circuit works by sensing the peak level of the received signal and comparing this level to a reference. The signal detect output of the receiver is PECL logic and must be terminated. The signal detect circuit is much slower than the data path, so the AC noise generated by an asymmetrical load is negligible. Power consumption may be reduced by using a higher than normal load impedance for the signal detect output as transmission line effects are not generally a problem with the switching rate being slow.

Layout

Due to the relatively high frequencies and low noise levels involved, it is important that good RF techniques are used for the PCB layout. The use of ground planes and 50 K transmission line interconnects is required for the PECL outputs.

Jitter Tolerance

SONET standards currently specify jitter tolerance as the jitter amplitude that increases by 1 dB the input signal level at which the network element will operate with a BER of 10^{-10}.

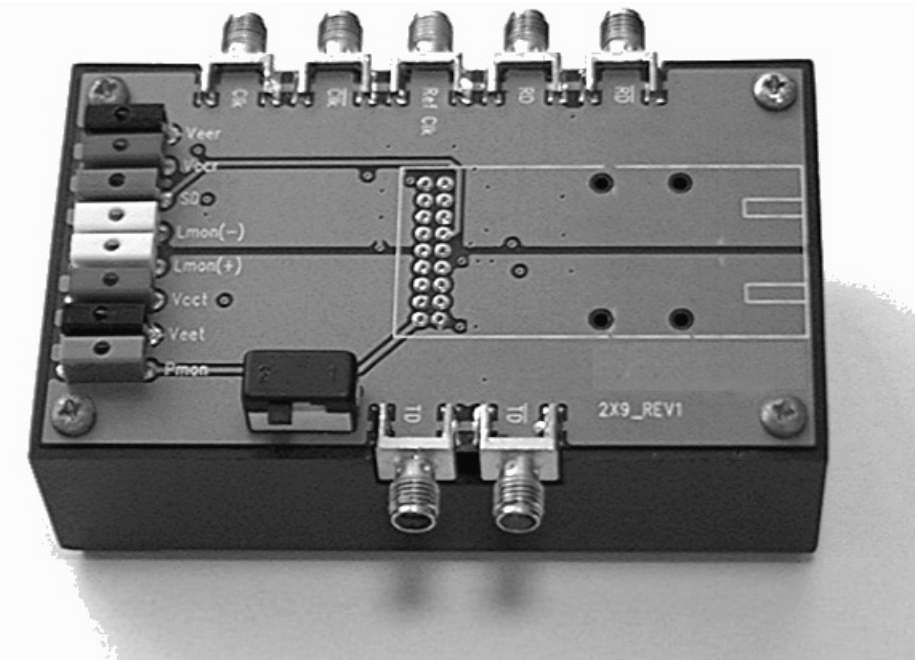


Figure 10. HFCT-5000 Evaluation Board

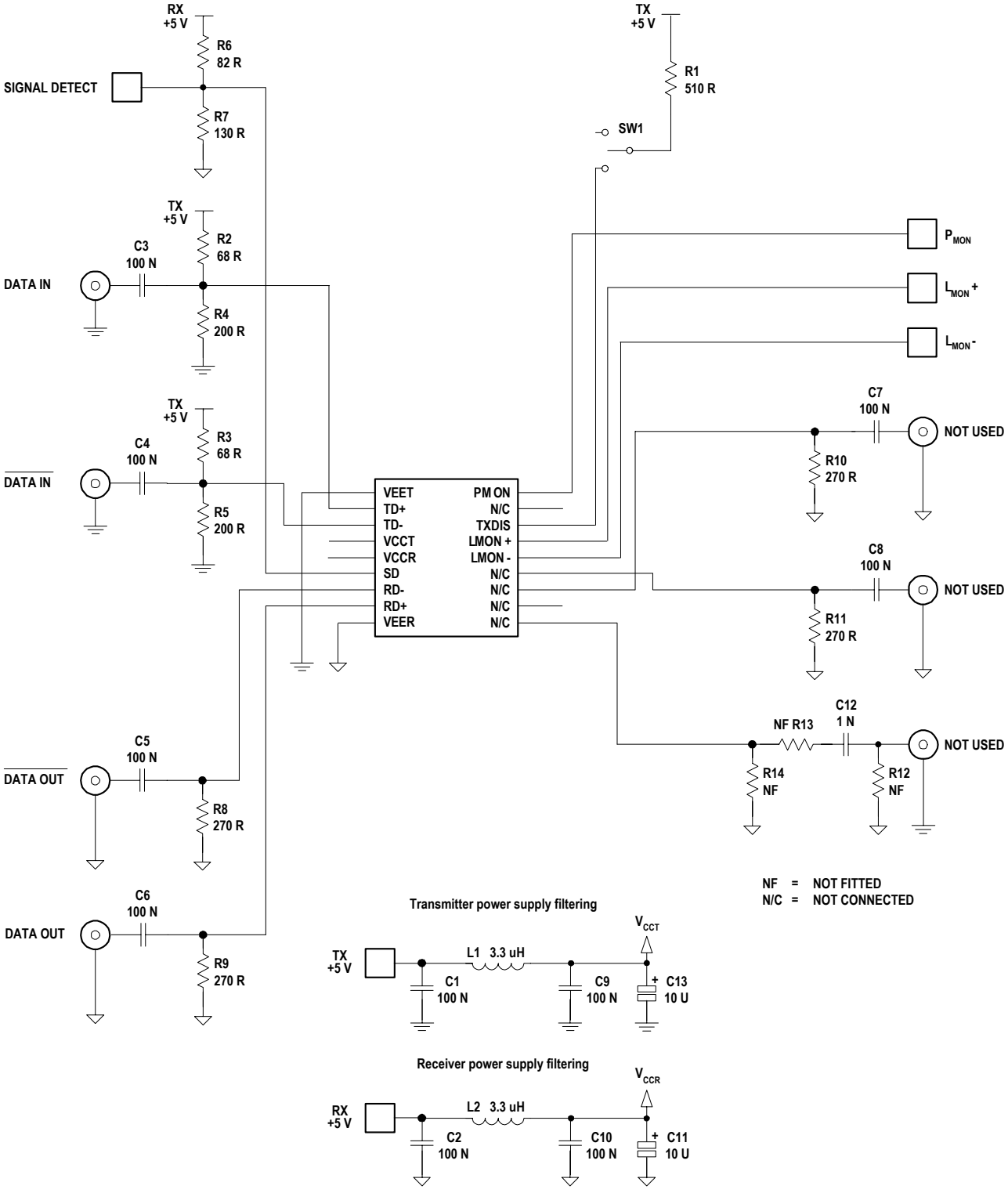


Figure 11. HFCT-5000 Evaluation Board Schematic

Table 2. Pinout Table (Refer to Figure 11)

Pin Out			
1 x 9	**2 x 9***	**Symbol**	**Functional Description**
NP	1	N/C	Not Connected
NP	2	N/C	Not Connected
NP	3	N/C	Not Connected
NP	4	N/C	Not Connected
NP	5	L_{MON}(-)	Laser Bias Monitor (-) This analog current is monitored by measuring the voltage drop across a 10 Ω resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
NP	6	L_{MON}(+)	Laser Bias Monitor (+) This analog current is monitored by measuring the voltage drop across a 10 Ω resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
NP	7	Tx_{DIS}	Transmitter Disable Transmitter Output Disabled : V_{CCT} - 1.5 V ≤ V_7 ≤ V_{CCT}. Transmitter Output Uncertain: V_{CCT} - 4.2 V ≤ V_7 ≤ V_{CCT} - 1.5 V. Transmitter Output Enabled: V_{EET} ≤ V_7 ≤ V_{CCT} - 4.2 V or open circuit.
NP	8	N/C	Not Connected
NP	9	P_{MON}	Power Monitor The analog voltage measured at this high impedance output provides an indication of whether the optical power output of the Laser Diode is operating within the normal specified power output range per the following relationships: High Light Indication: $V_9 \geq V_{EET}$ + 1.7 V. Normal Operation: $V_9 \cong V_{EET}$ + 1.2 V. Low Light Indication: $V_9 \leq V_{EET}$ + 0.7 V.
9	10	V_{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.
8	11	TD	Transmitter Data In Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin.
7	12	$\overline{TD}$	Transmitter Data In Bar Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin.
6	13	V_{CCT}	Transmitter Power Supply Provide +5 V DC via the recommended power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
5	14	V_{CCR}	Receiver Power Supply Provide +5 V DC via the recommended power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
4	15	SD	Signal Detect Normal input optical levels to the receiver result in a logic "1" output. Low input optical levels to the receiver result in a fault indication shown by a logic "0" output. SD is a single-ended, PECL output and may be terminated as in Figure 11. The SD output can be used to drive a PECL input on an upstream circuit, such as, SD input, Loss of Signal-bar input. SD can be used as a low-power PECL output by completing the interconnection of SD output with other PECL inputs. If SD output is not used, leave it open-circuit.

NP = Not present
* 2 x 9 = HFCT-5201A/B/C/D

Table 2. Pinout Table (continued)

Pin Out			
1 x 9	**2 x 9***	**Symbol**	**Functional Description**
2	16	$\overline{RD}$	Re-timed Receiver Data Out Bar Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
3	17	RD	Re-timed Receiver Data Out Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
1	18	V_{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.
Mounting Studs			The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the non-conductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.

NP = Not present
* 2 x 9 = HFCT-5201A/B/C/D

Evaluation Board and Pinout Designations

(Part No. HFCT-5000)

Avago can supply an evaluation board, as shown in Figure 10, to provide power and interface connections to the devices listed in Table 1.

The evaluation board operates at +5 V bias. On the evaluation board, SMA connections are provided for differential PECL interfacing. The required termination resistors are provided.

For products with a 2 x 9 pinout the transmitter is normally enabled if no connection is made to the disable pin 7. With no connection, the disable input is internally pulled to V_{EE} with a 16 kΩ resistor. The disable switch on the evaluation board will connect pin 7 to V_{CC} to disable the module when in position (1) indicated on the switch.

Figure 11 shows the HFCT-5000 Evaluation Board Schematic layout. Table 2 gives the modules pin out, functionality and connection information.

Cleaning of Optical Subassemblies

Solvents should not be used to clean the transmitter optical subassembly (TOSA) or receiver optical subassembly (ROSA).

The TOSA connector interface is a single-mode physical contact, the ROSA is a nonphysical contact and in both cases cleanliness is extremely important.

It is recommended that an NTT international 'Cletop Stick-Type' cleaner , or similar lint-free swab is used for quick cleaning of the ferrule endface and SC ports. Using a dry 'Cletop Stick' every time, insert into SC port and rotate and remove.

Regulatory Compliance

The transceiver products are intended to enable commercial system designers to develop equipment that complies with the various regulations governing Certification of Information Technology Equipment as specified in the product data sheet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

All transceiver products have been characterized without a chassis enclosure to demonstrate the robustness of the part's integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well- designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Table 3. Regulatory Compliance – Typical Performance

Feature	Test Method	Performance	
Electromagnetic Interference (EMI) HFCT-5103, HFCT-5205, HFCT-5215 and HFCT-5201	FCC Class B CENELEC EN55022 Class B (CISPR 22B) VCCI Class 2	Typically provide greater than 11 dB margin below 1 GHz to FCC Class B when tested in a GTEM with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz dependent on customer board and chassis designs.	
Immunity HFCT-5103, HFCT-5205, HFCT-5215 and HFCT-5201	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 27 MHz to 1 GHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.	
Eye Safety	IEC 825/CDRH Class 1	CDRH Accession Numbers:	HFCT-5205 9521220 - 08 (i) HFCT-5205 9521220 - 17 (ii) HFCT-5205 9521220 - 26 (iii) HFCT-5103 9521220 - 01 HFCT-5103 9521220 - 27 (ii) HFCT-5201 9521220 - 06 HFCT-5201 9521220 - 08 HFCT-5201 933/5108116/03 HFCT-5215 9521220 - 11
		TUV Bauart License:	HFCT-5205A/C 933/510018/02 HFCT-5205B/D 933/510018/02 HFCT-5205xx 933/510018/02 HFCT-5205xxx 933/510018/02 HFCT-5103 933/510018/02 HFCT-5201 933/510018/02 HFCT-5215 933/510918/01

(i) Product date coded up to and including 9835
(ii) Product date coded 9836 to 9950.
(iii) Product date coded 9951 and beyond.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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