HDMP-163K Evaluation Board User's Guide

Application Note 1204

Evaluation Board Description

The purpose of the HDMP-163K evaluation board is to make it easy to quickly evaluate the HDMP-1636A[1] transceiver IC for 1.25 GB Gigabit Ethernet and 1.0625 GB Fibre Channel. The HDMP-1636A is packaged in a 10x10 mm plastic QFP package. The transceiver is also available in a 14x14 mm package (HDMP-1646A). It is recommended that the user refer to the HDMP-1636A/46A data sheet for more details on the transceiver IC. The evaluation board brings out all pins from the chip to various connectors and jumper options. It can be used in a stand-alone configuration or connected to an external host. The parallel interface to the host is through a 2x10 ribbon header on the input and a 2x14 ribbon header on the output. SMA connectors are provided on all the high-speed serial coax lines and on the reference clock input (REFCLK). A socket for an onboard reference clock is also provided. The following discussion refers to the evaluation board operating at the Gigabit Ethernet rate of 1.25 GB, but it also applies if it is used at the Fibre Channel rate of 1.0625 GB.

Figure 1 shows the complete schematic for the evaluation board and Table 1 contains the material list. The evaluation board uses a 4-layer structure of FR4 material (refer to Figure 2). Table 2 summarizes the function of all connections and jumper options on the board. Notice that both the Dout and Din lines have series coupling capacitors (CC1–CC4) loaded on the evaluation board. This conveniently allows AC coupling to the test equipment on both I/O ports. The evaluation board is normally loaded with the high-speed series source termination resistors R3 = R4 = 0 Ω.

BER Test

The following section shows how to measure the bit error rate ratio (BER) of the HDMP-1636A using the evaluation board. The BER test procedure of Figure 3 tests one aspect of the transceiver's performance. It fully exercises the transmitter part of the transceiver. All functions of the transceiver's RX section are exercised except the byte alignment function and the TTL output clocks RBC0/RBC1 timing relation to the parallel output data bits (RX[0..9]). Most importantly, the test fully exercises the transmitter and receiver phase locked loops (PLL), which are the most complicated sections of the transceiver. It also tests the serializing and deserializing functions of the transceiver.

BER can be measured by applying the appropriate parallel 10-bit word pattern on the TX and then looking for bit errors on the parallel output of the RX. Unfortunately, a BER Tester (BERT) with a pattern generator that has a parallel output capable of operating at the 125 MHz rate (106.25 MHz for Fibre Channel) is not common. The pattern generator would also need to transmit a special start-up sequence using a comma character for byte alignment. Fortunately, serial BERTs are common and provide an easy means to test the HDMP-1636A.

For this test, the parallel receiver outputs (RX[0..9]) are simply fed back into the parallel transmitter inputs (TX[0..9]) using a standard parallel ribbon cable as shown in Figure 3. It would be convenient if one of the receiver output clocks (RBC0 or RBC1) could be fed back to the TX REFCLK. Parallel data is latched into the TX using the rising edge of the input clock REFCLK. RBC0 and RBC1 are phase aligned to the parallel data from the RX, but these clocks are not at the frequency that the TX clock input wants to see. The TX input clock (REFCLK) expects a frequency of 125 MHz, but the RX output clocks are dual polarity half speed clocks, running at 62.5 MHz. So the RX output clock cannot be applied to the TX clock input.

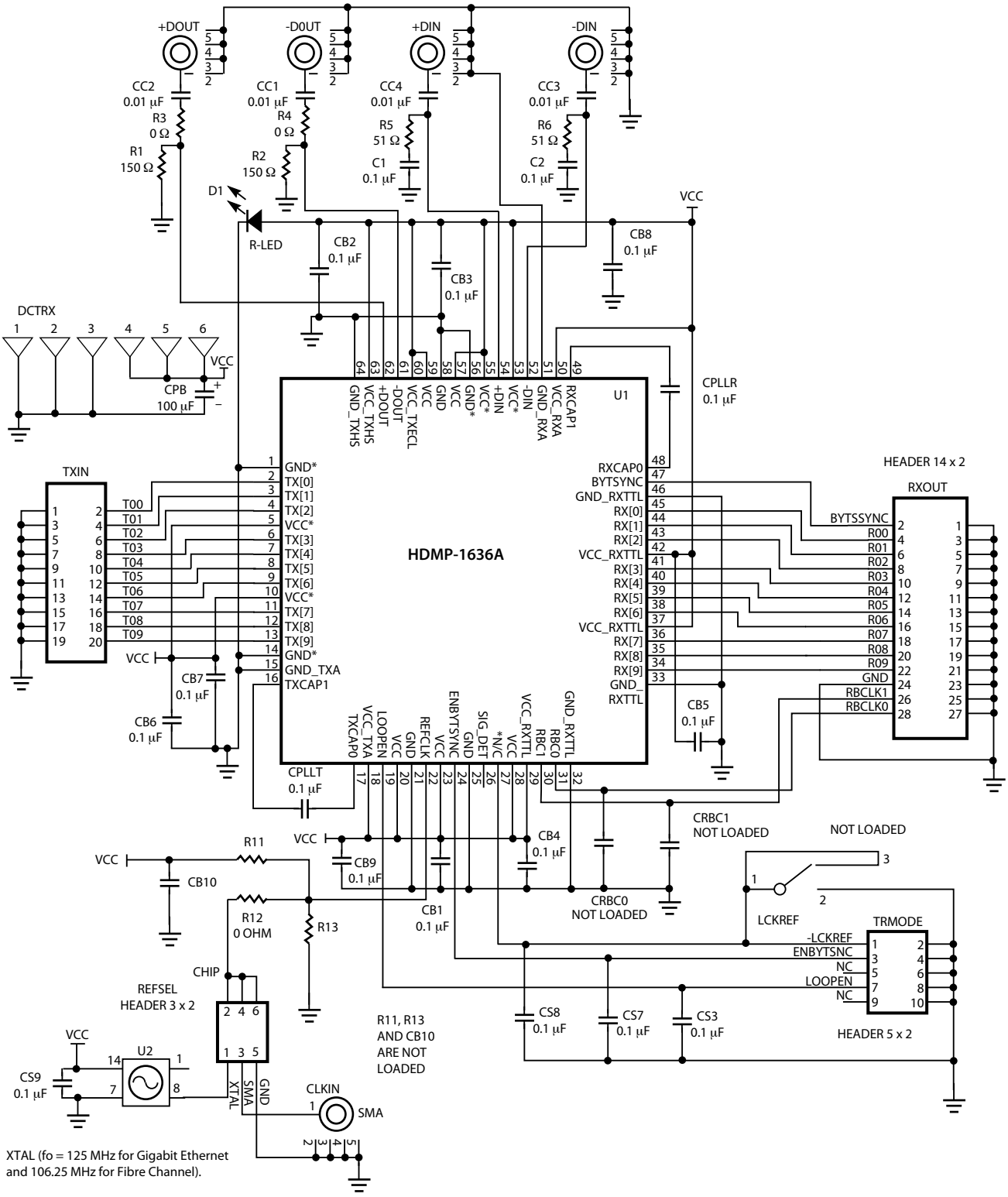
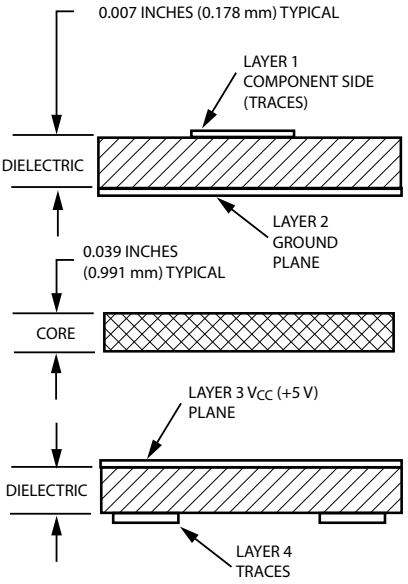


Figure 1. HDMP-1636A Evaluation Board Circuit Diagram.



LAYERS 1 AND 4: 1/2 OZ. COPPER FOIL = 0.0007 INCHES (0.0178 mm) THICK.

LAYERS 2 AND 3: 1 OZ. COPPER FOIL = 0.0014 INCHES (0.0356 mm) THICK.

$\varepsilon_r = 4.4$

Figure 2. Multilayer PC Board Structure.

The serial BERT also requires a high-speed clock at 1.25 GHz to drive the pattern generator and clock out the high-speed data. This 1.25 GHz signal is supplied by the Avago Technologies' 70311A generator as shown in Figure 3. The generator drives a power splitter with one path applied to the clock input of the BERT and the other path driving a divide by 10 circuit. Output of the divider circuit provides the 125 MHz reference clock for the evaluation board and is discussed later in this application note.

The 125 MHz reference clock is passed through a variable delay line before being supplied to the HDMP-1636A transceiver. This phase shift relative to the TX parallel data input makes sure that the rising edge is centered in the data valid window of the parallel data (TX[0..9]= RX[0..9]). Note that the HDMP-1636A reference clock input (REFCLK) serves two functions. An automatic locking feature allows the RX PLL to lock onto the input data stream without external PLL training controls. It does this by continually frequency locking onto the 125 MHz reference clock, and then phase locking onto the input data stream. For the transmitter section of the transceiver, REFCLK is always used by the internal multiplexer to clock in the parallel data input and is multiplied by 10 to generate the 1250 MHz clock necessary for clocking the high-speed serial outputs. The following is a step-by-step procedure to perform the BER test.

• Connect the evaluation board to a serial BERT as shown in Figure 3. In this case an Avago Technologies' serial BERT is used which includes the Avago Technologies' 70004A display CRT, Avago Technologies' 70841A pattern generator, and the Avago Technologies' 70842A error detector. This particular BERT operates up to 3 Gbits/sec. As shown in Figure 3, the parallel ports (TX[0..9] and RX [0..9] of the HDMP-1636A) are tied together using the short length of standard ribbon cable supplied with the evaluation board.

• Place a jumper across pins 3 and 4 of REFSEL header. REFCLK is now applied through the SMA connector (labeled CLKIN).

• Use the Avago Technologies' 70841A pattern generator to apply serial data at 1.25 Gb/s to the high-speed inputs of the HDMP-1636A (+Din and -Din). Set the generator to a PRBS pattern of 27-1. This is the closest instrument-supplied pattern to the 8B/10B code used in Gigabit Ethernet in terms of the longest run of zeros or ones.

• Activate the Dout and Din high-speed serial ports by setting LOOPEN = 0 on the TRMODE header.

• Disable comma detection (enbytsync = 0) because byte alignment at the parallel ports is not required for this test. Also, if enabled, some bits prior to any comma character located in the serial bit stream could be lost, resulting in faulty bit errors.

• The 125 MHz crystal oscillator on the evaluation board (not supplied) is not used in this test. Unplug it from the evaluation board if one has been inserted in the XTAL socket.

• The transceiver auto-locks to the incoming data from the BERT. Ignore the -LCKREF position on the TRMODE header by leaving it open (no jumper). The automatic locking feature allows the Rx PLL to lock onto the input data stream without external control. The variable delay line may require adjusting to get no errors on the serial BERT. Frequency lock occurs within 500 µs. After frequency lock, phase lock occurs within 2500 bit times.

Auto-lock works by continually frequency locking onto the 125 MHz clock and then phase locking onto the input data stream. An internal signal detection circuit monitors the presence of the input and invokes the phase detection as the data stream appears. Once bit locked, the receiver generates the high speed sampling clock at 1250 MHz for the input sampler and recovers the two 62.5 MHz receiver byte clocks (RBC1/RBC0).

A BER much better than 1 x 10-14 can be routinely measured using the HDMP-1636A evaluation board and equipment setup of Figure 3. This is over 24 hours of error free operation at 1.25 GB.

Table 1. Parts list for the HDMP-1636A Evaluation Board

Designator	Qty	Part Type	Footprint	Manufacturer Part Number
+DOUT	1	PC Mount	SMA	EF Johnson 142-0701-201
-DIN	1	PC Mount	SMA	EF Johnson 142-0701-201
-DOUT	1	PC Mount	SMA	EF Johnson 142-0701-201
+DIN	1	PC Mount	SMA	EF Johnson 142-0701-201
CLKIN	1	PC Mount	SMA	EF Johnson 142-0701-201
CPLLR	1	0.1 μF	0805	Venkel C0805Z5U-250-104-MNE
CPLLT	1	0.1 μF	0805	Venkel C0805Z5U-250-104-MNE
C1, C2	2	0.1 μF	0805	Venkel C0805Z5U-250-104-MNE
CB1-CB9	9	0.1 μF	0805	Venkel C0805Z5U-250-104-MNE
CC1-CC4	4	0.01 μF	0805	Venkel C0805Z5U-250-103-MNE
CS3-CS4	2	0.1 μF	0805	Venkel C0805Z5U-250-104-MNE
CS6-CS9	4	0.1 μF	0805	Venkel C0805Z5U-250-104-MNE
CPB	1	100 μF	0805	SPRAGUE 30D107G25DD2-DSN
R3, R4, R12	2	0 ohm	0805	Venkel CR080-10W-0R0-JT
R5, R6	2	51 ohm	0805	Venkel CR080-10W-510-JT
R1,R2	2	150 ohm	0805	Venkel CR080-10W-151-JT
XTAL		TTL 125 MHz for Gigabit Ethernet, 106.25 MHz for Fibre Channel		
	4	Mini-spring pin socket		
REFSEL	1	HEADER	HEADER 3X2	AMP 4-103186-0*
RXOUT	1	HEADER	HEADER 14X2	AMP 4-103186-0*
TRMODE	1	HEADER	HEADER 5X2	AMP 4-103186-0*
TXIN	1	HEADER	HEADER 10X2	AMP 4-103186-0*
U1	1	IC		Avago HDMP-1636A
D1	1	R-LED 5V		Avago HLMP-3600
	4	Standoff with Internal Thread	1", 6-32	
	4	Screw 4-40	6-32 x 0.5"	

* 2x40 header cut to size

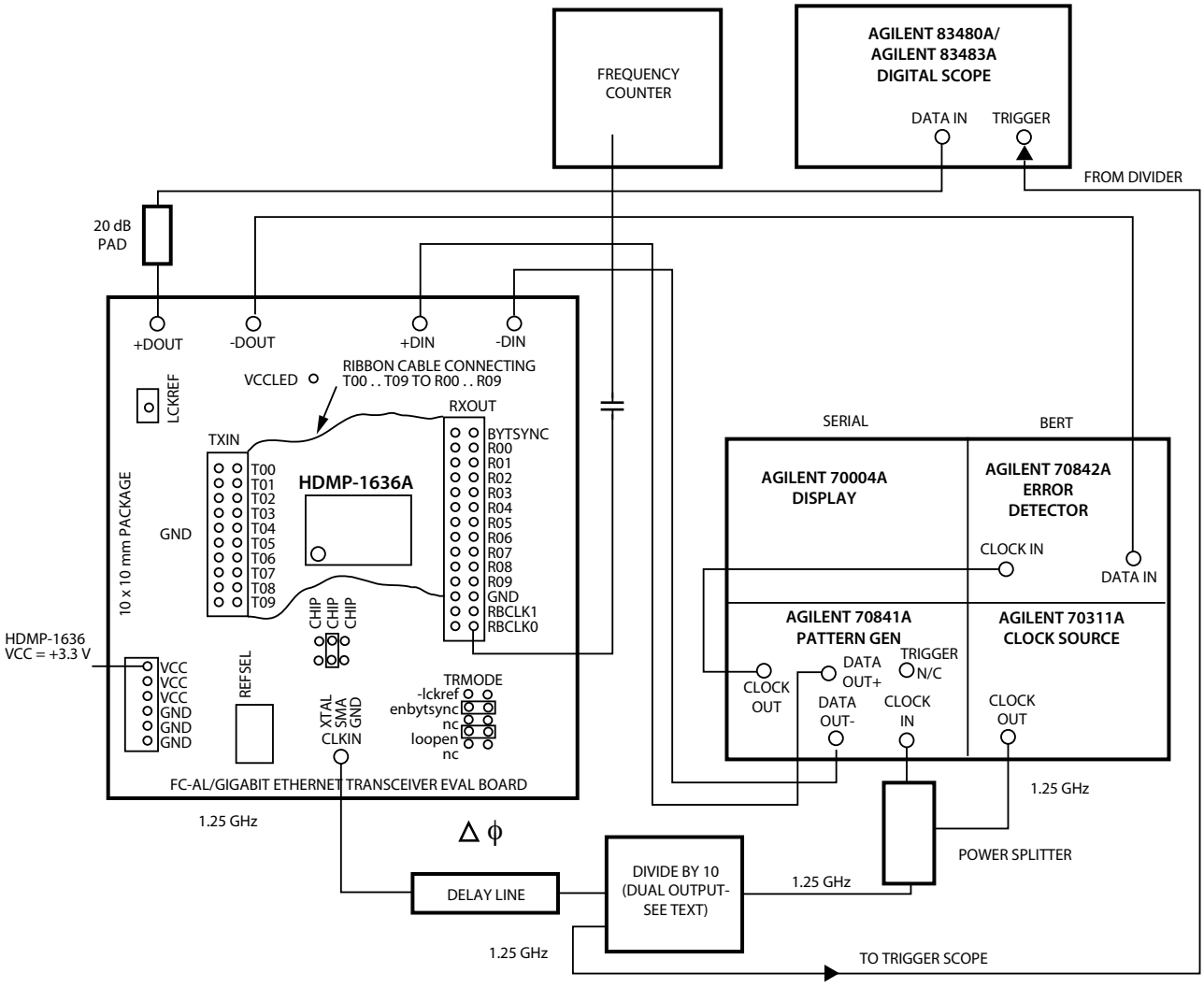
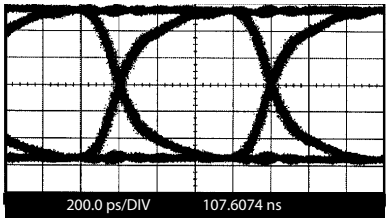


Figure 3. BER Test Setup using the HDMP-1636A Evaluation Board and Avago Technologies' Serial BERT.

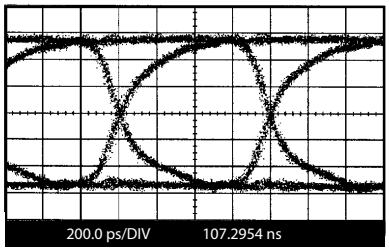
Table 2. List of all Headers/Connections and their functions on the Evaluation Board.

Header Name	Pin Name	Function	Jumper Position
REFSEL	XTAL	XTAL is the reference clock	XTAL to CHIP
	SMA	External reference clock is applied to SMA	SMA to CHIP
	GND	Common ground	
TRMODE	-lckref	Lock to Reference Not used since autolock is always enable.	NC
	enbytsync	Enable Byte Sync Input. When enbytsync = 1, clock syncs to a comma character	Enabled with no jumper Disabled with enbytsync to gnd
	loopen	Loopback Enable Input. When Loopen = 1, high speed serial data is internally wrapped from Tx to Rx	Dout to Din: Loopen to gnd Internally wrapped: no jumper
TXIN	T00-T09	Parallel data input to Tx	
RXOUT	BYTSYNC	Asserted when common character detected or K28.5 special character of positive disparity	
	R00-R09	Parallel data output from Rx	
	GND	Common ground	
	RBCLK1	Receiver Byte Clock 1	
	RBCLK0	Receiver Byte Clock 0	



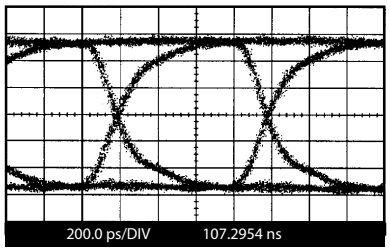
f1 300 mV/DIV

(a) DIFFERENTIAL OUTPUT (DOUTDOUT-).



f1 150 mV/DIV

(b) DOUT+



f1 150 mV/DIV

(c) DOUT-

Figure 4. Eye Diagrams of the High-Speed Serial Outputs from the HDMP-1636A as captured on the Avago Technologies' 83480A Digital Communications Analyzer. The equipment setup of Figure 3 was used with a PRBS = 2^7–1.

Figure 4 shows the eye diagram at 1.25 GB as measured on the Avago Technologies' 83480A Communications Analyzer connected to the Dout- coax port of the HDMP-1636A.

Divide by 10 Circuit

Figure 5 shows the schematic for the divide by 10 circuit used in the BER test and called out in the equipment setup of Figure 3. The divide by 10 circuit uses an MC12080D prescaler IC followed by two MC100ELT21D PECL to TTL converters. The MC12080D is manufactured by Motorola and the MC100ELT21D is manufactured by On Semiconductor. The two MC100ELT21D ICs can also be replaced with a single MC100ELT23D dual PECL to TTL converter.

Using An Optical Transceiver

The HDMP-163K evaluation board can be combined with the HFBR-0535 evaluation board to test Avago Technologies' multimode HFBR-53D5 or single-mode HFCT-53D5 optical transceivers. The HFBR-0535 evaluation board was designed for evaluating the multimode, 1-row-by-9-pins (1x9) HFBR-53D5 VCSEL fiber-optic transceiver and the single-mode 1x9 HFCT-53D5 F-P Laser fiber-optic transceiver for 1.25 Gb/s Ethernet applications. Figure 6 shows a recommended test configuration for evaluating the combination. More detailed information on testing this combination can be found in the HFBR-0535 application note [3] and respective data sheets [4,5]. The HDMP-163K evaluation board can also be combined with the HFBR-0553 evaluation board to test Avago Technologies' multimode HFBR-53D3 or single-mode HFCT-53D3 Fibre Channel optical transceivers. The test configuration of Figure 6 also applies when testing these transceivers. The PC board layout for the HDMP-163K evaluation board is shown in Figure 7.

References

[1] HDMP-1636A/1646 Gigabit Ethernet Transceiver Chip Data Sheet. Pub Number 5967-6245A (4/00)

[2] IEEE 802.3z Gigabit Ethernet Specification

[3] Avago Technologies' HFBR-0535 Gigabit/s Ethernet (1.25 GBd) 1x9 Fiber Optic Transceiver Evaluation Board, AN1218, pub. number 5988-1849EN

[4] HFBR-53D5, Gb/s (Gigabit) Ethernet: 1.25 GBd 850 nm VCSEL Transceiver in Low Cost 1x9 Package Style

[5] HFCT-53D5 Gigabit Ethernet: 1.25 GBd 1300 nm Laser Transceiver in Low Cost 1x9 Package Style

This evaluation board is intended for evaluation purposes only. Avago Technologies does not guarantee its performance in a production environment.

Information in this application note is subject to change without notice.

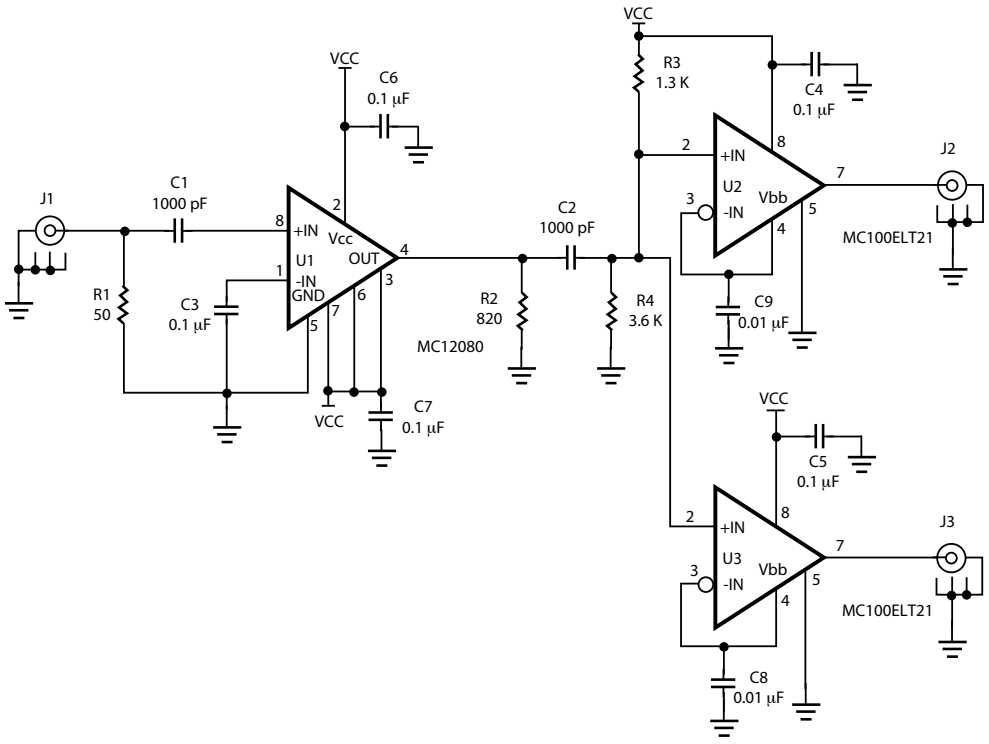


Figure 5. Divide by 10 Network used with the BER Test.

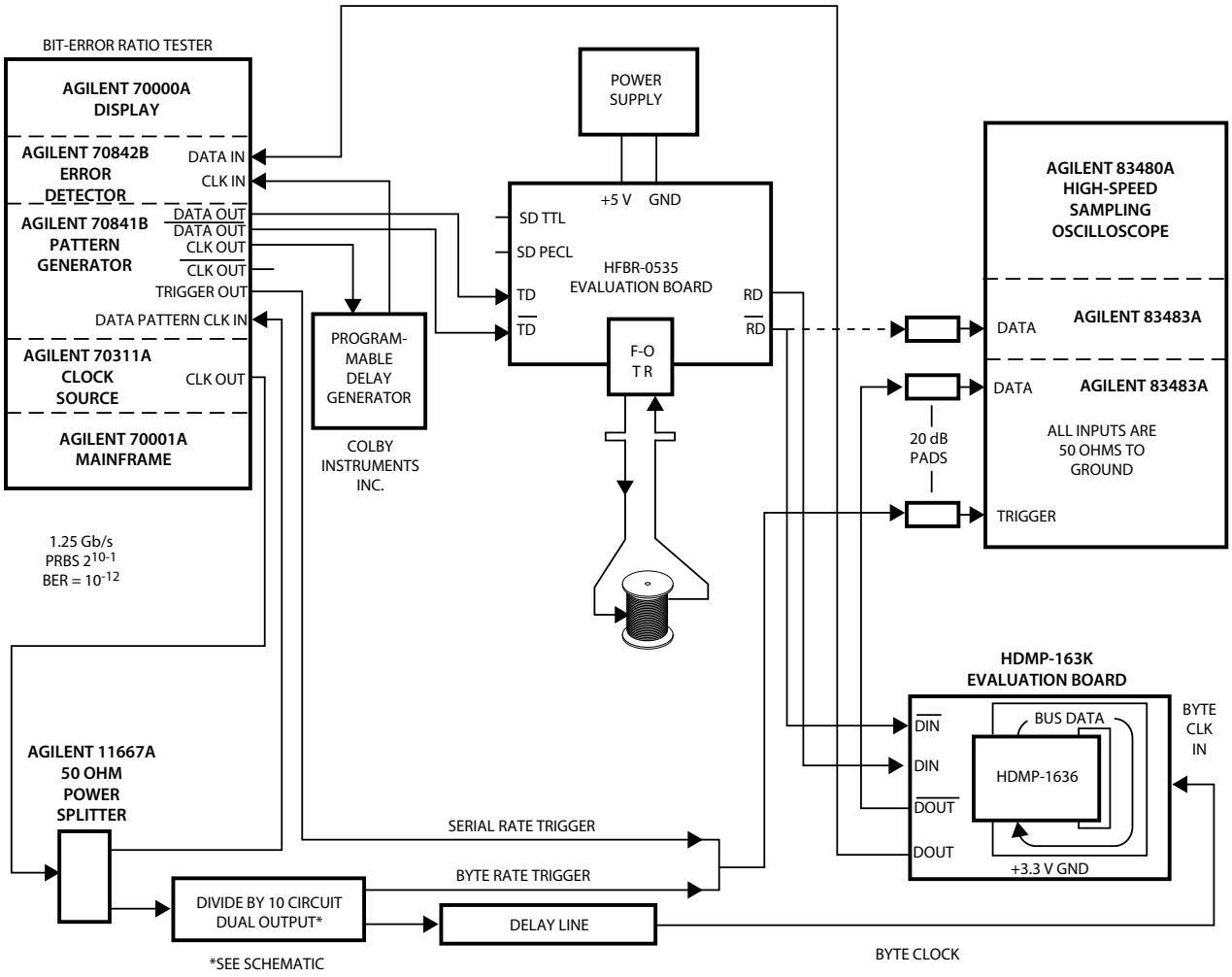


Figure 6. Recommended Test Configuration for One Looped-back HFBR-53D5 or HFCT-53D5 Fiber-optic Transceiver Link with a Looped-back Parallel Bus Gigabit/sec Ethernet HDMP-1636A Transceiver IC.

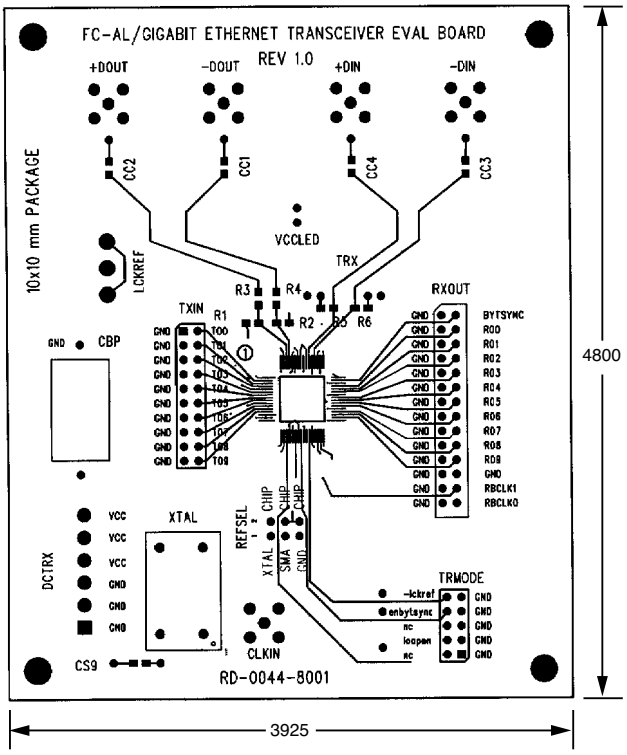


Figure 7a. Top

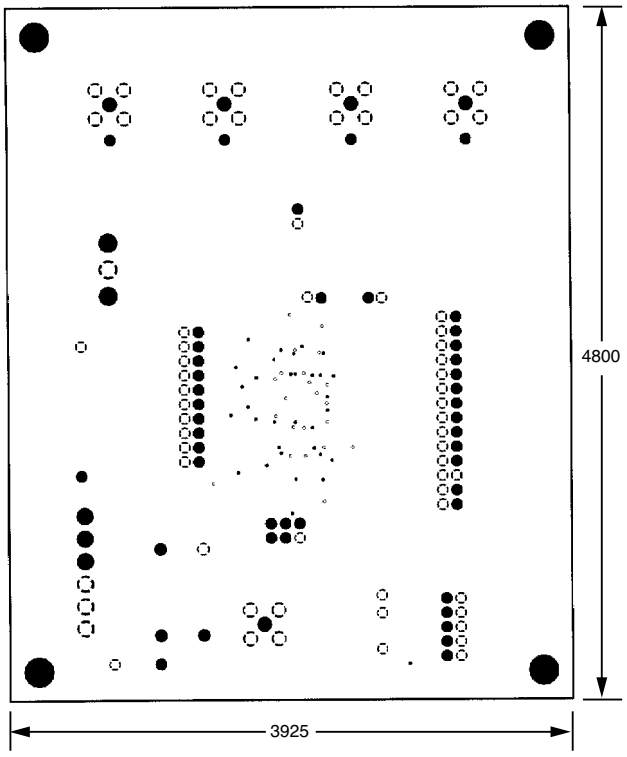


Figure 7b. Ground Plane

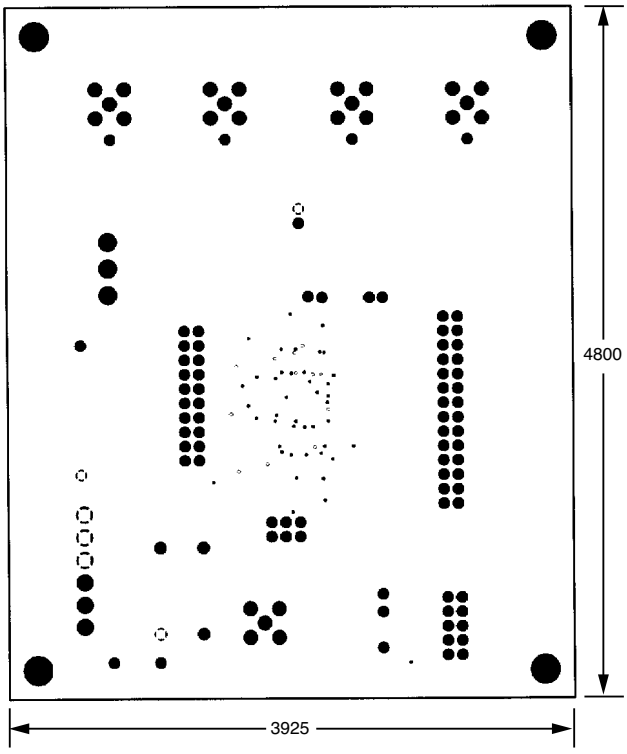


Figure 7c. V_{CC} Plane

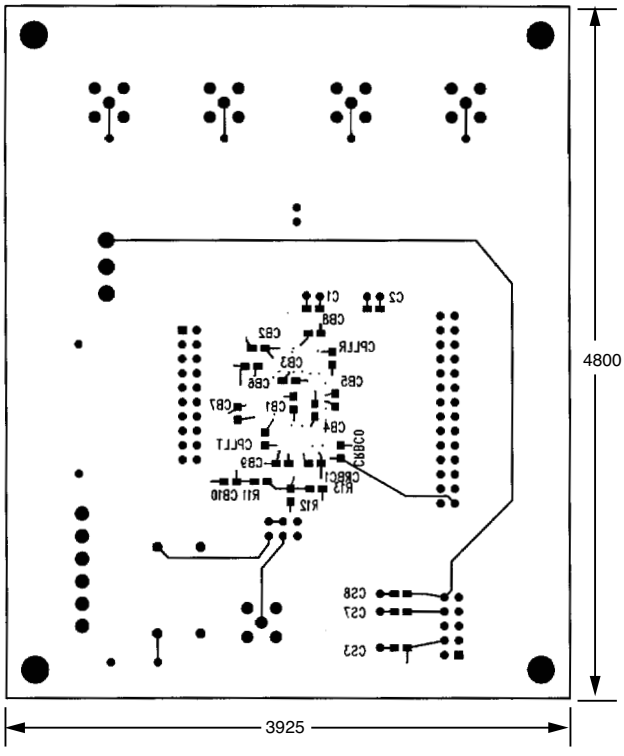


Figure 7d. Bottom

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