Design of an Input Matching Network for a DC biased 850 MHz Small Signal Detector

AVAGO TECHNOLOGIES

Application Note 1187

Introduction

This application note describes the use of the HSMS-2820 in small signal detector applications at 850 MHz. The single series diode (HSMS-2820) has a detection sensitivity[1] of about 30 mV /μW; i.e., it can produce an output of about 30 mV for an input power of -30 dBm (1 μW). This general-purpose single diode is housed in a miniature, inexpensive plastic surface mount SOT-23 package.

The input match circuit is the most critical item of the detector performance because it affects the sensitivity of the design. The detector is built on 0.031-inch thick FR-4 material circuit board, producing a low cost design.

Small Signal Detector Designs

Design considerations:

This is a small signal detector design so the main focus should be in the -50 dBm to -30 dBm input power range (square-law region)[2]. This is the region where the output DC voltage of the detector will be proportional to the square of the input RF voltage, or simply proportional to the input power. The optimum bias point for best sensitivity was empirically determined to be 3 μA but if the dynamic range needs to be increased to -20 dBm, the bias can be increased to 15 μA to compensate. Temperature and higher input power (-20 dBm and above) will affect the sensitivity of the detector, because they change the input impedance of the diode[2]. There is an optimal matching circuit that gives a good sensitivity given a certain bias current, temperature and power.

In this application note, a full description of the most pertinent steps of the DC biased small signal detector design will be described. The small signal detector was designed using Avago-EESOF's Advanced Design System (ADS) and then tested in the laboratory.

For a differential detector design, diode pairs (in a single package) should be used for the excellent match between the diodes. For instance, the HSMS-2825 (unconnected pair housed in SOT-143) or the HSMS-282K (high isolation pair in SOT-363) can be used for temperature compensation of the diode's bias-induced forward voltage. When Avago Technologies puts multiple diodes into one package, the diodes come from adjacent slots on the wafer and this means the best match possible. However, the main focus of this paper is not to describe the differential detector but the input matching network design.

Therefore, the single diode (HSMS-2820) board was built in the laboratory and other testing techniques were used to remove this forward voltage V_F due to the bias. In the simulations, two HSMS-2820 diodes in a differential detector topology were used to remove this bias induced forward voltage.

Getting started on Avago Advanced Design System – ADS

The first step in the design is to place two diodes on the design page from the ADS component library and filling the proper model parameter values for each HSMS-2820 (found in the Avago Technologies website-AvagoRFhelp design model section). See Figure 1. The package is modeled by the simple series 2 nH and parallel 80 fF[3].

The diode is then biased with a 3 μA current. A voltage source of 1 V and a resistor of 100 kΩ as shown in Figure 2 establish this bias point. The two identical diodes have the same forward voltage V_F. The detected voltage V_O is found by subtracting the second diode's voltage bias induced forward voltage, V_F, from the detector diode's (main diode) output $V_O + V_F$[4].

Input Impedance Match Design

The matching circuit at the input of the detector is one of the most critical elements in the design[1][5]. The input impedance is determined to help design the input matching circuit. A small signal S-parameter test of the biased diode including the bond pad capacitance is performed to determine the S11. As shown in Figure 3, the S11 is at the edge of the Smith Chart at 0.97| – 30°.

Then a simple two lumped elements match (inductors with Q = 30 at 800 MHz) was used to match it at the low power level of -50 dBm (see Figure 4). As the input RF power increases (using a large signal S-parameter simulation setup in Figure 5), the matching is degraded as shown in Figure 6 and Figure 8. The series and shunt inductors were placed as close as possible to the diode to minimize the loss of the matching network. To better model the bond pad capacitance, a microstrip structure was used with a width of 60 mils, length of 130 mils, thickness of 31 mils and a dielectric constant of 4.8 (FR-4 material).

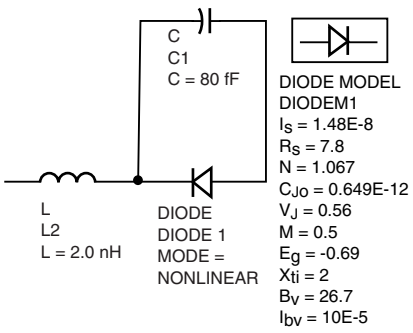


Figure 1. HSMS-2820 diode model found in AvagoRFhelp (includes package)

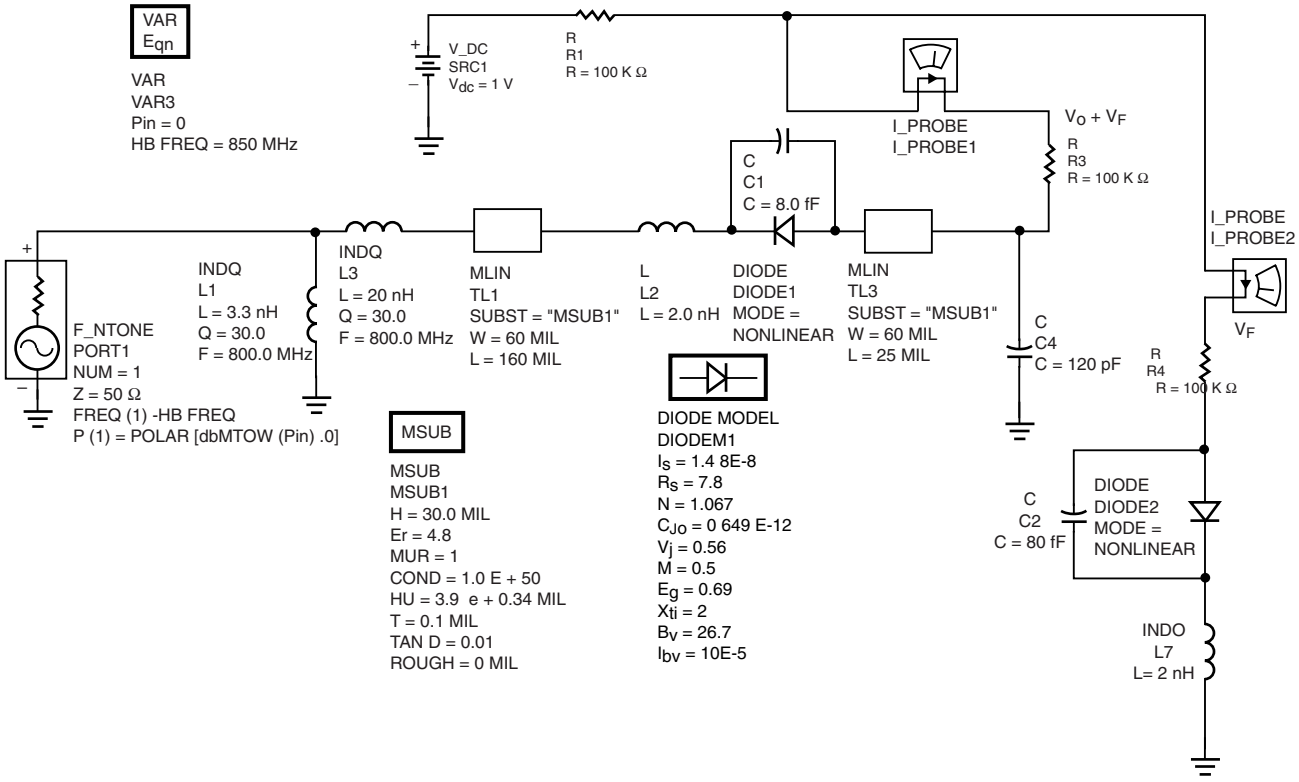


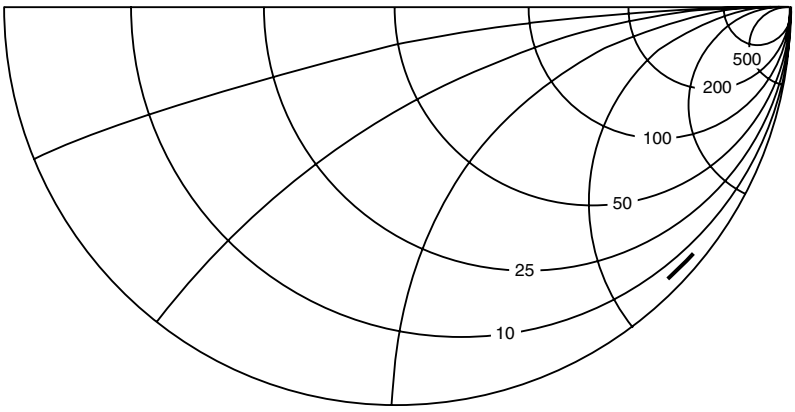
Figure 2. Simulated circuit

As can be seen from Figure 6 and Figure 8, the degradation of the matching from -50 dBm input power, (with S11 = -19.1 dB), to -30 dBm input power, (where S11 = -10.3 dB) is apparent but is still not significant. However, there is much more mismatch as the input power increases (e.g. at -20 dBm, S11 = -3.3 dB).

At this input power of -20 dBm where the mismatch increases drastically, the diode is no longer in the square-law region. It is in fact in the linear region where the voltage detected is no longer proportional to the input power but to the input voltage. As can be seen, the bias current starts being affected by the RF carrier because the rectified current is now comparable to the 3 μA original bias. (See Figure 7.)

In the simulation, the inductors used had the nearest manufacturer values. The series 20 nH inductor in the simulation was replaced by the actual 22 nH with a ±10% manufacturer tolerance. The self-resonance frequency (SRF) was 1700 MHz. For the shunt 3.3 nH inductor, the self-resonance frequency was greater than 6 GHz. In both cases, the self-resonance frequencies are far enough that it would not affect the design at 850 MHz.

A 100 kΩ resistor is used as a resistive load for the detector's output voltage. A few more microstrip models were used in the simulations to accurately describe the circuit board that was built.



FREQUENCY	MAG [m. . S(1.1)]	. . .e[m. . S(1.1)]
800 MHz	0.973	-39.349
825 MHz	0.973	-40.612
850 MHz	0.972	-41.878
875 MHz	0.971	-43.148
900 MHz	0.970	-44.421

Figure 3. S11 of Diode with the Bond Pad Capacitance

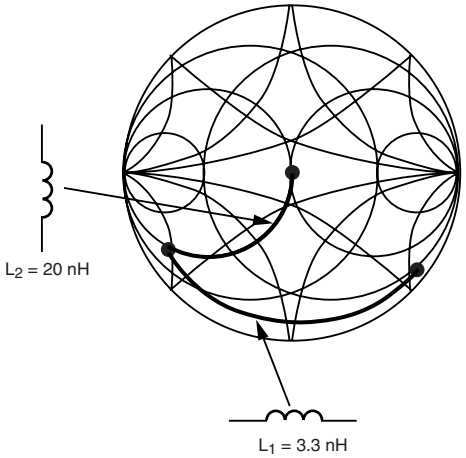


Figure 4. Matching with two inductors with Q = 30

LSSP

HB2
Freq(1) = HB freq.
Order(1) = 3
LSSP_FreqAtPort(1) = HBfreq Hz

Parameter Sweep

ParamSweep
Sweep1
SweepVar = "Pin"
Start =
Stop =
Step =

Harmonic Balance

Harmonic Balance
HB1
Freq (1) = HBfreq
Order(1) = 7
SweepVar = "Pin"
Start =
Stop =
Step =

Sweep Plan

SweepPlan
Plan1
Start = -50 Stop = 5 Step = 5 Lin =
UseSweepPlan
SweepPlan

Figure 5. Large signal S-parameter setup by sweeping pin

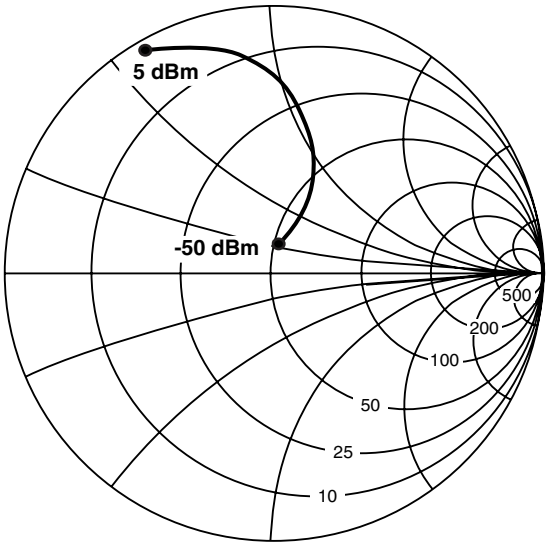


Figure 6. S11 as a function of input power (-50 to 5 dBm)

At 850 MHz Pin (dBm)	Peak Freq.	V_0 at Peak Freq.	I_C drawn (μA)
-40	840	0.0036	3.1
-35	845	0.0101	3.1
-30	850	0.0284	3.1
-25	860	0.0709	3.1
-20	**875**	**0.1597**	**3.2**
-15	895	0.3253	3.4
-10	920	0.6519	3.7
-5	945	1.2680	4.3
0	965	2.4110	5.4
5	980	4.4430	7.6

Figure 7. When Pin = -20 dBm, the bias starts being affected

A series of transfer curves with the voltage detected versus the input power are shown in Figure 10. The actual measurements and the simulated result are reasonably close.

Results

The ADS simulation results for the detected voltage V_O as a function of Pin are shown in Figure 9. The lab measurement of the built circuit board is compared with the simulation in Figure 10. As can be seen, the comparisons are closer when in the square law region (lowest input power) as would be expected because the matching was done for the low power and consequently there is great return loss in this low power range.

The shift of the peak frequency, similar to what is seen on the scope, was simulated using the setup in Figure 11. The resulting plot is shown in Figure 12. The comparison with the actual lab work is shown in Figure 13.

The peak frequency is slightly off due to the limitations of the model.

A temperature sweep was also performed using the temperature option in the simulation setup as shown in Figure 14.

The voltage sensitivity decreases with temperature as shown in Figure 15 and Figure 16. (Note: Pin is fixed at -30 dBm.) The sensitivity voltage V_O as a function of Pin was simulated at various temperatures shown in Figure 16 at 850 MHz.

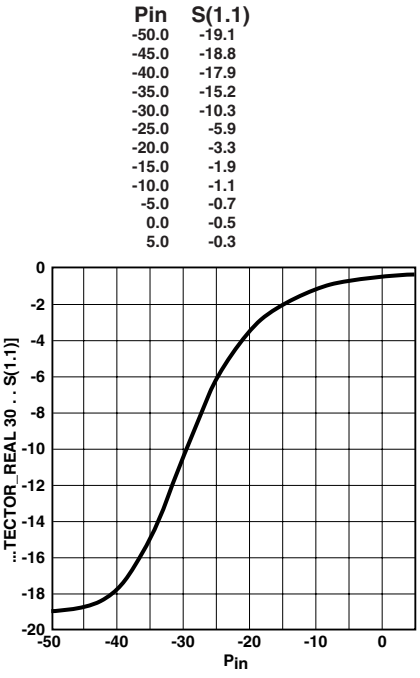


Figure 8. S11 as a function of input power in dB

The differences observed between the measurements and simulations are due to the limitation of the lossy matching network model. A slight variation in the matching circuit seems to greatly affect the sensitivity.

The manufacturer inductor values and Q have a tolerance of about 10%. The small distance between the matching and the diode must also be accurately modeled. A combination of these uncertainties resulting in non-perfect models explains the slight differences observed between the simulations and measurements.

Circuit Board

The layout for the detector is shown in Figure 17. The board material used is a 0.031-inch thick FR-4. A closer look of the simplified version of the board is shown in Figure 18.

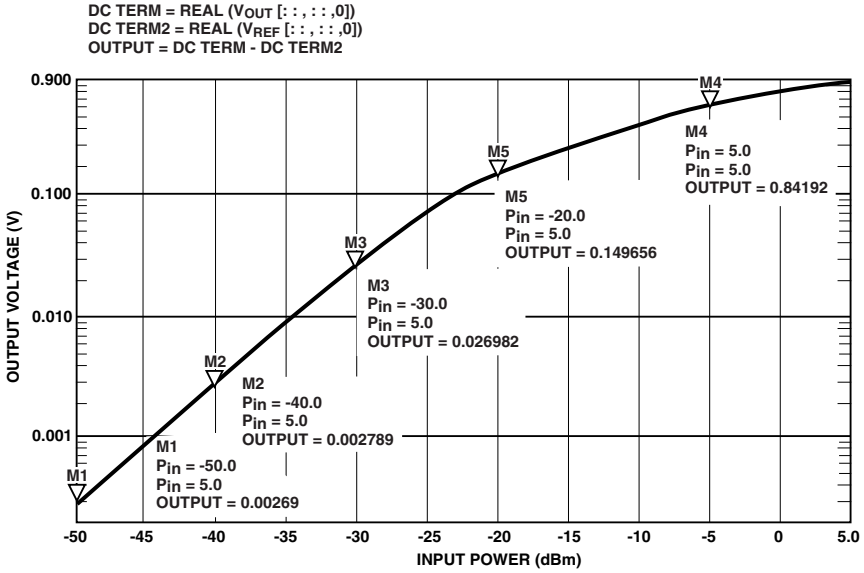


Figure 9. ADS Result of V_0 vs. Pin

At 850 MHz Pin (dBm)	Measured Vout	Simulated Vout
-40	0.00306	0.00279
-35	0.00900	0.00880
-30	0.02844	0.02698
-25	0.06650	0.07298
-20	0.12220	0.14966
-15	0.19410	0.24788
-10	0.30500	0.37675
-5	0.46750	0.55367
0	0.72370	0.74701
5	1.13000	0.84192

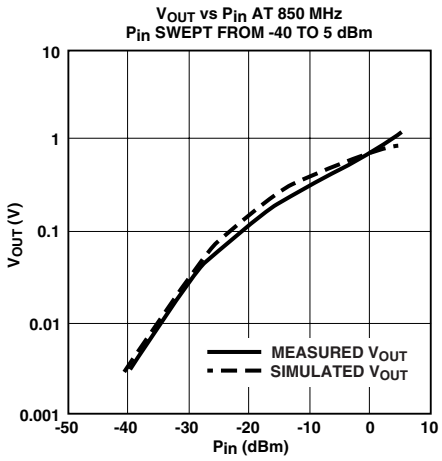


Figure 10. Measured and simulated Vout vs. Pin at 21° C

Summary

Using the non-linear Schottky diode model for the HSMS-2820, a DC biased small signal detector can be designed in AvagoEEsof ADS. A careful input match design is necessary to obtain optimal results.

When building the small signal detector (differential detector), the designer should use the HSMS-2825 (unconnected pair housed in SOT-143) or the HSMS-282K (high isolation pair in SOT-363).

References

[1] Application Note 923, "Schottky Barrier Diode Video Detectors" and Application Note 969, "The Zero Bias Schottky Detector Diode".

[2] Application Note 1156, "Diode Detector Simulation using Avago Technologies ADS Software" and Application Note 986, "Square Law and Linear Detection".

[3] Application Note 1124, "Linear Models for Diode Surface Mount Packages".

[4] Design Tip D003, "Notes on differential detector circuits".

[5] Application Note 1089, "Designing Detectors for RF/ID Tags".

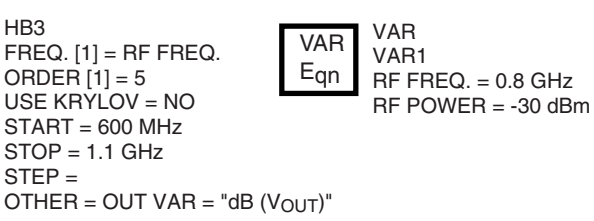


Figure 11. V_0 as a function of frequency simulation setup

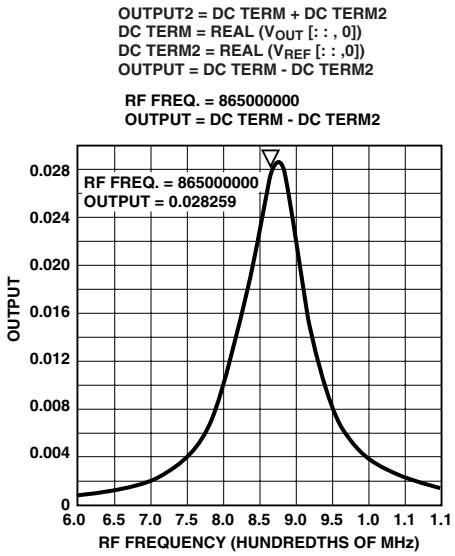


Figure 12. V_0 as a function of frequency

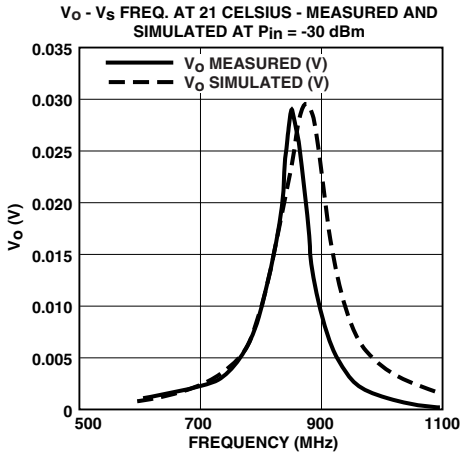


Figure 13. V_0 as a function of frequency comparison with measurement done on actual circuit board

LSSP

HB2
Freq(1) = HB freq.
Order(1) = 3
LSSP_FreqAtPort(1) = HBfreq Hz

Parameter Sweep

ParamSweep
Sweep1
SweepVar = "Pin"
Start =
Stop =
Step =

Options

Options
Options1
Temp = 75

Harmonic Balance

Harmonic Balance
HB1
Freq (1) = HBfreq
Order(1) = 7
SweepVar = "Pin"
Start =
Stop =
Step =

Sweep Plan

SweepPlan
Plan1
Start = -50 Stop = 5 Step = 5 Lin =
UseSweepPlan
SweepPlan

Figure 14. Temperature sweep setup

At 850 MHz Pin = -30 dBm)	Measured Vout	Simulated Vout
-25	0.0331	0.0334
0	0.0276	0.0304
21	0.0256	0.0275
25	0.0245	0.0270
50	0.0227	0.0239
75	0.0186	0.0212

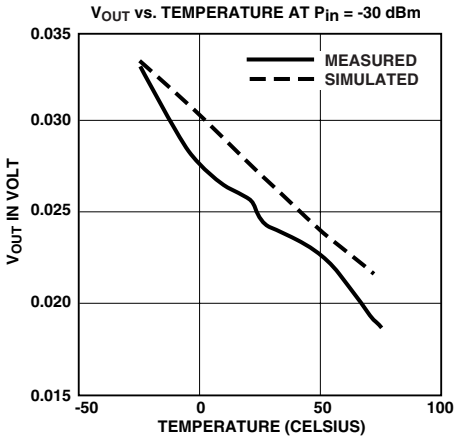


Figure 15. Vout as a function of temperature (Pin = -30 dBm)

At 850 MHz Pin (dBm)	V_0 at -25	V_0 at 25	V_0 at 75
-40	0.0039	0.0028	0.0021
-35	0.0119	0.0088	0.0066
-30	0.0334	0.0270	0.0212
-25	0.0772	0.0730	0.0644
-20	0.1439	0.1497	0.1476
-15	0.2347	0.2479	0.2507
-10	0.3599	0.3768	0.3818
-5	0.5359	0.5537	0.5631
0	0.7217	0.7470	0.8152
5	0.8138	0.8419	0.9888

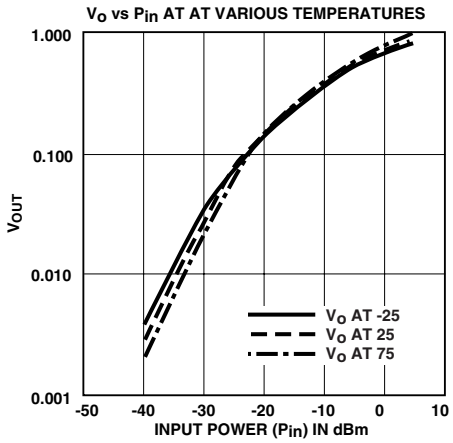


Figure 16. Vout as a function of pin at various temperatures (°C) (F = 850 MHz)

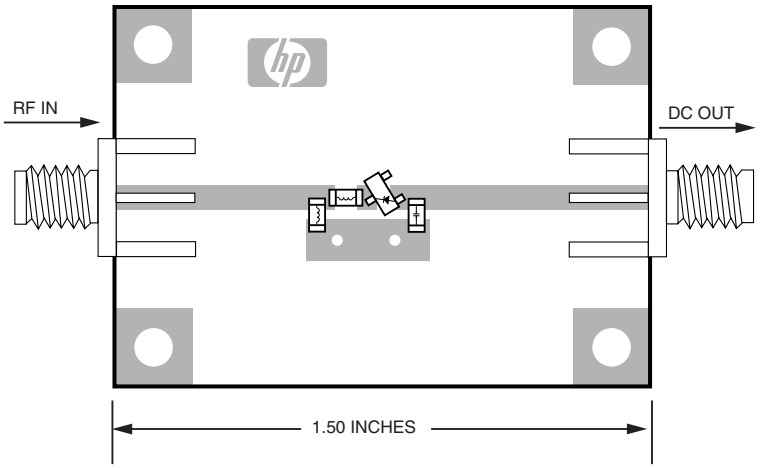


Figure 17. Circuit board

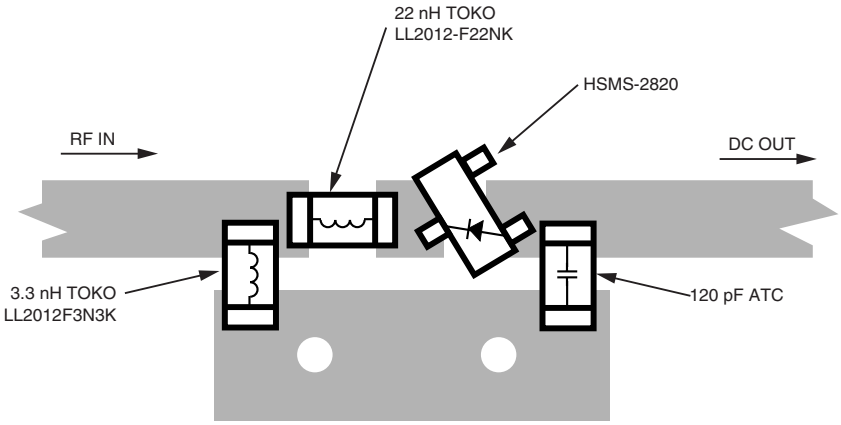


Figure 18. HSMS-2820 Detector demonstration board

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