A 400, 900, and 1800 MHz Buffer/Driver Amplifier using the HBFP-0450 Silicon Bipolar Transistor

Application Note 1206

Introduction

Avago Technologies' HBFP-0450 is a high performance isolated collector silicon bipolar transistor housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The HBFP-0450 is described in three amplifiers for use in the 400 MHz, 900 MHz, and 1800 MHz frequency bands. The amplifiers are designed for use with 0.032-inch thick FR-4 printed circuit board material. The HBFP-0450 amplifier is biased at a V_{CE} of 4 V and I_C of 50 mA. The three amplifiers use the same bias conditions. Typical performance of the 400 MHz amplifier is 17 dBm P-1dB, 19 dB gain, and an output intercept point of 29.5 dBm. The 900 MHz amplifier typically provides 17.0 dBm P-1dB, 17 dB gain, 3.2 dB noise figure, and an output IP3 of 33.5 dBm. The 1800 MHz amplifier typically provides 19.4 dBm P-1dB, 12 dB gain, 3.5 dB noise figure, and an output IP3 of 34 dBm.

Amplifier Design

The amplifiers were designed for a V_{CE} of 4 volts and I_C of 50 mA. Typical power supply voltage, V_{CC}, would be in the 5.0 to 5.5 volt range. Higher V_{CC} results in improved bias point stability over temperature. The amplifier schematic is shown in Figure 1. A component list is shown in Table 1 for the HBFP-0450 400MHz amplifier and Table 2 for the 900 MHz amplifier. The artwork and component placement drawing for the amplifier test board is shown in Figure 2.

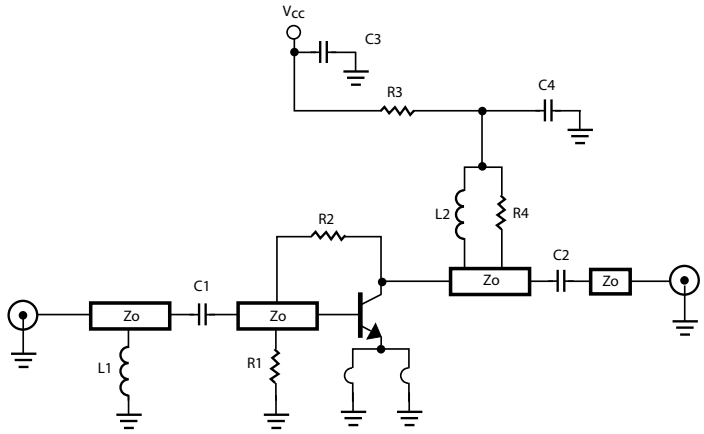

Figure 1. Amplifier Schematic.

Table 1. Component Parts List for the 400 MHz HBFP-0450 Amplifier.

C1	18 pF chip capacitor
C2	100 pF chip capacitor
C3	1000 pF chip capacitor
C4	100 pF chip capacitor
L1	10 nH TOKO LL1608-FH10N
L2	100 nH TOKO LL1608-FHR10
Q1	Avago Technologies' HBFP-0450 Silicon Bipolar Transistor
R1	150 Ω chip resistor
R2	470 Ω chip resistor
R3	18 Ω chip resistor
R4	350 Ω chip resistor (set for amplifier stability)
Zo	50 Ω Microstripline

Table 2. Component Parts List for the 900 MHz HBFP-0450 Amplifier.

C1	5.6 pF chip capacitor
C2	100 pF chip capacitor
C3	1000 pF chip capacitor
C4	100 pF chip capacitor
L1	6.8 nH TOKO LL1608-FH6N8
L2	47 nH TOKO LL1608-FH47N
Q1	Avago Technologies' HBFP-0450 Silicon Bipolar Transistor
R1	150 Ω chip resistor
R2	470 Ω chip resistor
R3	18 Ω chip resistor
R4	350 Ω chip resistor (set for amplifier stability)
Zo	50 Ω Microstripline

Table 3. Component Parts List for the 1800 MHz HBFP-0450 Amplifier.

C1	1.8 pF chip capacitor
C2	100 pF chip capacitor
C3	1000 pF chip capacitor
C4	100 pF chip capacitor
L1	2.7 nH TOKO LL1608-FH2N7S
L2	22 nH TOKO LL1608-FH22N
Q1	Avago Technologies' HBFP-0450 Silicon Bipolar Transistor
R1	150 Ω chip resistor
R2	470 Ω chip resistor
R3	18 Ω chip resistor
R4	680 Ω chip resistor (set for amplifier stability)
Zo	50 Ω Microstripline

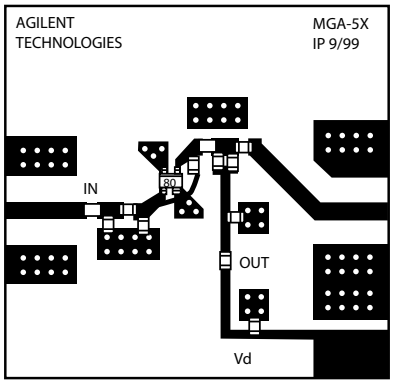

Figure 2. Board layout with component placement (TCW used to connect R2 to collector junction).

For other power supply voltages, resistor R3 can be used to help set the collector voltage for a given collector current. The input matching network uses a high pass network for best match. The high pass network consists of a series capacitor (C1) and a shunt inductor (L1). C1 also provides a dc blocking function. R1 sets the collector current (higher values for higher current). R2 has a dual purpose—a feedback resistor and providing base bias voltage. No output impedance matching network is required as the feedback and the input matching network provide a suitable solution. A shunt resistor (R4) is used in parallel with inductor (L2), with the collector to provide broadband stability by reducing amplifier gain slightly. C3, R3, and C4 provide bias decoupling and a low frequency resistive termination for the device.

HBFP-0450 400 MHz Amplifier Performance at V_{CE} = 4.0 V and I_C = 50 mA.

The P-1dB of the amplifier was measured at 17 dBm with an Output Third Order Intercept Point, IP3, of 29.5 dBm. The measured gain and noise figure of the completed amplifier is shown in Figure 3. Amplifier noise figure measured 3.3 dB at 400 MHz with an associated gain of 19 dB. Measured input and output return loss is shown in Figure 4. The input return loss at 400 MHz is 10.5 dB with a corresponding output return loss of 17.1 dB.

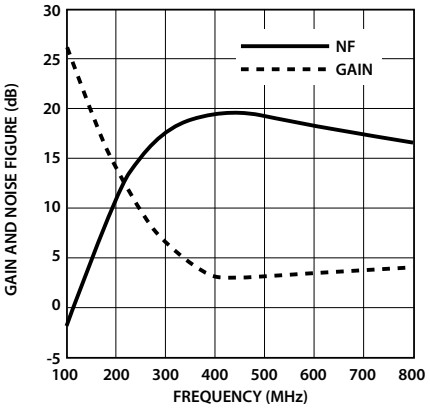

Figure 3. Gain and Noise Figure vs. Frequency.

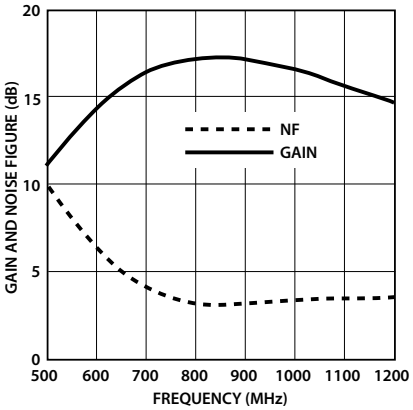

Figure 5. Gain and Noise Figure vs. Frequency.

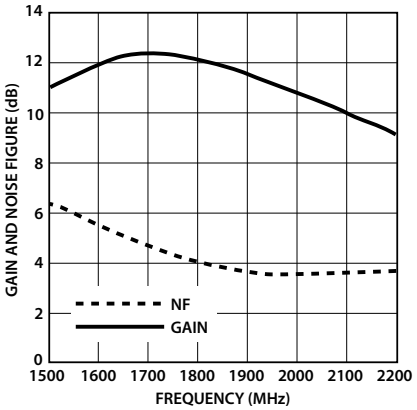

Figure 7. Gain and Noise Figure vs. Frequency.

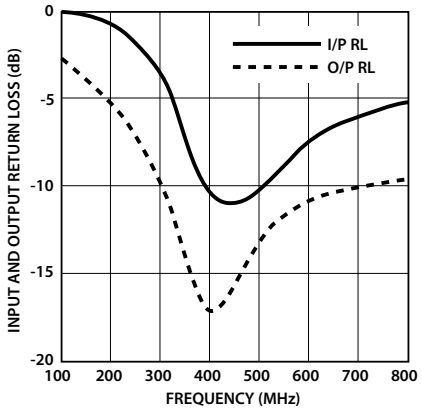

Figure 4. Input/Output Return Loss vs. Frequency.

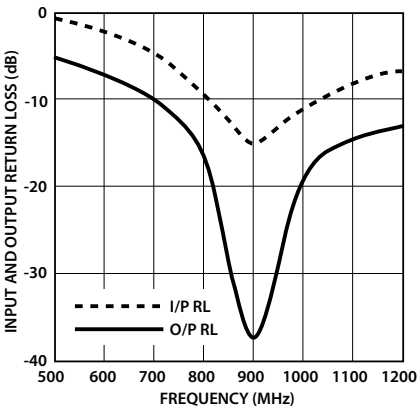

Figure 6. Input/Output Return Loss.

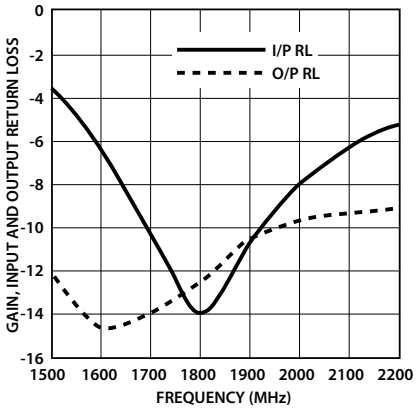

Figure 8. Input/Output Return Loss.

HBFP-0450 900 MHz Amplifier Performance at V_{CE} = 4 V and I_C = 50 mA

The P-1dB of the amplifier was measured at 17.3 dBm and Output Third Order Intercept Point, IP3, of 33.5 dBm. The measured gain and noise figure of the completed amplifier is shown in Figure 5. Amplifier noise figure measured 3.2 dB at 900 MHz with an associated gain of 17.3 dB. Measured input and output return loss is shown in Figure 6. The input return loss at 900 MHz is 14.5 dB with a corresponding output return loss of 37.0 dB.

HBFP-0450 1800 MHz Amplifier Performance at V_{CE} = 4 V and I_C = 50 mA

The P-1dB of the amplifier was measured at 19.4 dBm and Output Third Order Intercept Point, IP3, of 34 dBm. The measured gain and noise figure of the completed amplifier is shown in Figure 7. Amplifier noise figure measured 3.5 dB at 1800 MHz with an associated gain of 12.2 dB. Measured input and output return loss is shown in Figure 8. The input return loss at 1800 MHz is 13.7 dB with a corresponding output return loss of 12.4 dB.

Using the MGA-5X Demoboard

The MGA-5X demoboard was designed for use for a GaAs RFIC amplifier, MGA-52543. The addition of a single wire connection between R2 to the base of the HBFP-0450 is the only board modification required. A production layout could use a two layer board or the DC track covered with etch resist could be run under the HBFP-0450. Copper foil was used to bridge gaps in the board.

HBFP-0450 Buffer/Driver Amplifier Design

Using Avago Technologies' Eesof Advanced Design System Software, the amplifier circuit can be simulated in both linear and non-linear modes of operation. The original design draft was an amplifier with a P-1dB of 17 dBm with close to 20 dB of gain at 400 MHz. In order to achieve a compact design and at the same time reduce the total component board count, the bias resistor (R2) was used for DC bias and to provide RF feedback. The RF feedback provided a stable design and good third order intercept performance. Avago Technologies' AppCAD was used to determine the values of the bias resistors. The following equations may be used to calculate the resistor values. (Note: Choose I_{B2}, suggest a voltage divider current of 10% of IC to calculate R_{B2}.)

$$R_{B2} = \frac{V_{BE}}{I_{B2}}$$

$$R_{B1} = \frac{V_{CE} - (I_{B2} \times R_{B2})}{I_B + I_{B2}}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C + I_B + I_{B2}}$$

$$I_B = \frac{I_C}{h_{FE}}$$

V_{CC} = 5.0 V, V_{CE} = 4 V, I_C = 50 mA,
h_{FE} = 80 typ, 50 min, 150 max
V_{BE} = 0.78 V, I_{CBO} = 1x10^{-7} A @ 25°C
R_{B2} = 156 Ohms, R_{B1} = 572 Ohms
R_C = 18 Ohms

Non-Linear Analysis

The circuit used for the non-linear analysis is shown in Figure 14. The model was downloaded from the Avago Technologies Semiconductor web site, www.semiconductor.Avago.com. The ADS unarchive function was used to extract the model. See ADS for further details on unarchiving models.

To perform the non-linear analysis, the Hamonic Balanced controller or one of the other non-linear simulators must be inserted into the schematic window.

The current probe and the node point were inserted to check that the bias conditions were correct. The values of the current and voltages can be viewed with the data viewer along with the gain, noise figure, input and output return losses. The results of the simulation at 400 MHz are shown in Figures 9 and 10. The P-1dB and IP3out performance can be viewed as well.

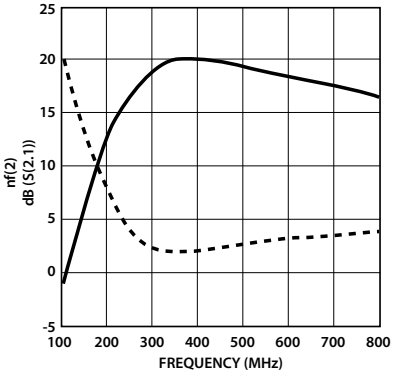

Figure 9. Non-Linear Simulated Gain and Noise Figure vs. Frequency.

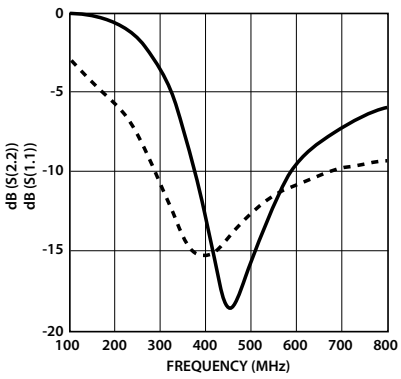

Figure 10. Non-Linear Simulated Input and Output Return Loss.

The non-linear simulated performance of the amplifier was very close to the measured results. It was noted that at higher frequencies the measured results for input and output return loss showed a slight frequency drift when compared to the measured results and linear S-parameter simulation results. A summary of the non-linear simulation results is shown in Table 4.

Linear Analysis

The circuit used for the linear analysis is identical to the non-linear analysis circuit. The HBFP-0450 model is replaced with the 2-Port S-parameter file icon available from the linear data file palette. The HBFP-0450.s2p file can be downloaded from the Avago Semiconductor web site, www.semiconductor.Avago.com.

The results of the simulation for gain, noise figure, input and output return loss are shown in Figures 11 and 12. The linear simulated performance of the amplifier was very close to the measured results. A summary of the linear simulation results is shown in Table 5.

Table 4. Summary of Non-Linear Analysis

Frequency	400 MHz	900 MHz	1.8 GHz
S21, dB	19.7	18.3	14.2
NF, dB	2.1	2.3	2.8
S11, dB	-12.1	-10.8	-6.3
S22, dB	-15.7	-23.0	-21.9
P-1dB, dBm	16.6	17.7	18.3
OIP3, dBm	30.7	32.3	33.3

Table 5. Summary of Linear Analysis

Frequency	400 MHz	900 MHz	1.8 GHz
S21, dB	20.1	17.5	12.9
NF, dB	2.1	2.1	3.1
S11, dB	-12.6	-15.7	-29.6
S22, dB	-15.2	-22.3	-11.8

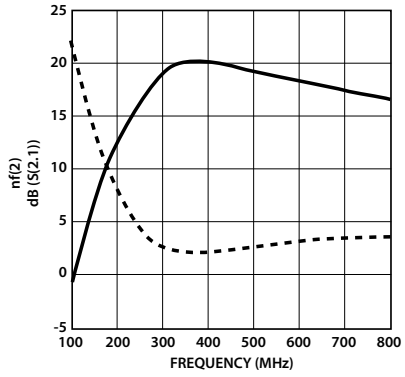

Figure 11. Linear Simulated Gain and Noise Figure vs. Frequency.

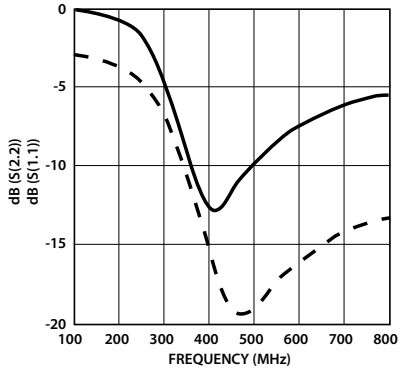

Figure 12. Linear Simulated Input and Output Return Loss.

Circuit Simulation

An accurate circuit simulation can certainly provide the appropriate first step to a successful amplifier design. Manufacturing tolerances in both the active and passive components often prohibit perfect correlation. Besides providing important information regarding gain, noise figure, input and output return loss, the computer simulation provides very important information regarding circuit stability. Unless a circuit is oscillating on the bench, it may be difficult to predict instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett stability factor K and generating stability circles are two methods made considerably easier with computer simulations.

Additional lead length is used to supply increased emitter inductance for design stability. The increase in emitter inductance helped improve stability and input return loss at the expense of amplifier gain performance. The gain was degraded by a few tenths of a dB. The MGA-5X board was modified by using a scalpel blade to remove the via holes closest to the HBFP-0450 on the underside of the board. The inductance associated with the chip capacitors and resistors was included in the simulation.

The simulated gain, noise figure, and input/output return loss of an HBFP-0450 amplifier is shown in Figures 9, 10, 11, and 12. These plots only address the performance near the actual desired operating frequency. It is still important to analyze out-of-band performance in regards to abnormal gain peaks, positive return loss, and stability.

A plot of Rollett stability factor K as calculated from 0.1 GHz to 10 GHz is shown in Figure 13 for the 400 MHz amplifier. The feedback resistor R2 is the dominant factor in stability. Emitter inductance can be used to help stability. It should be noted, however, that excessive inductance causes high frequency stability to worsen (i.e., decreased value of K). The resistive loading consisting of R4 is the main contributor to low frequency stability. Decreasing the value of R4 will make the stability factor K higher. As stability is improved, certain amplifier parameters such as gain and power output may have to be sacrificed.

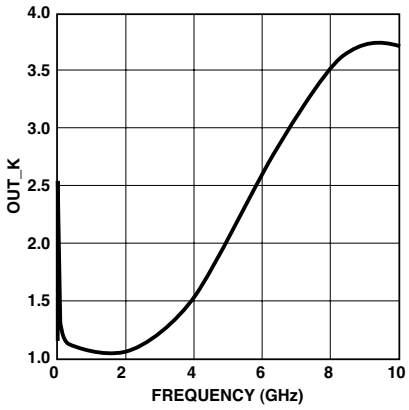

Figure 13. Simulated Rollett Stability Factor K.

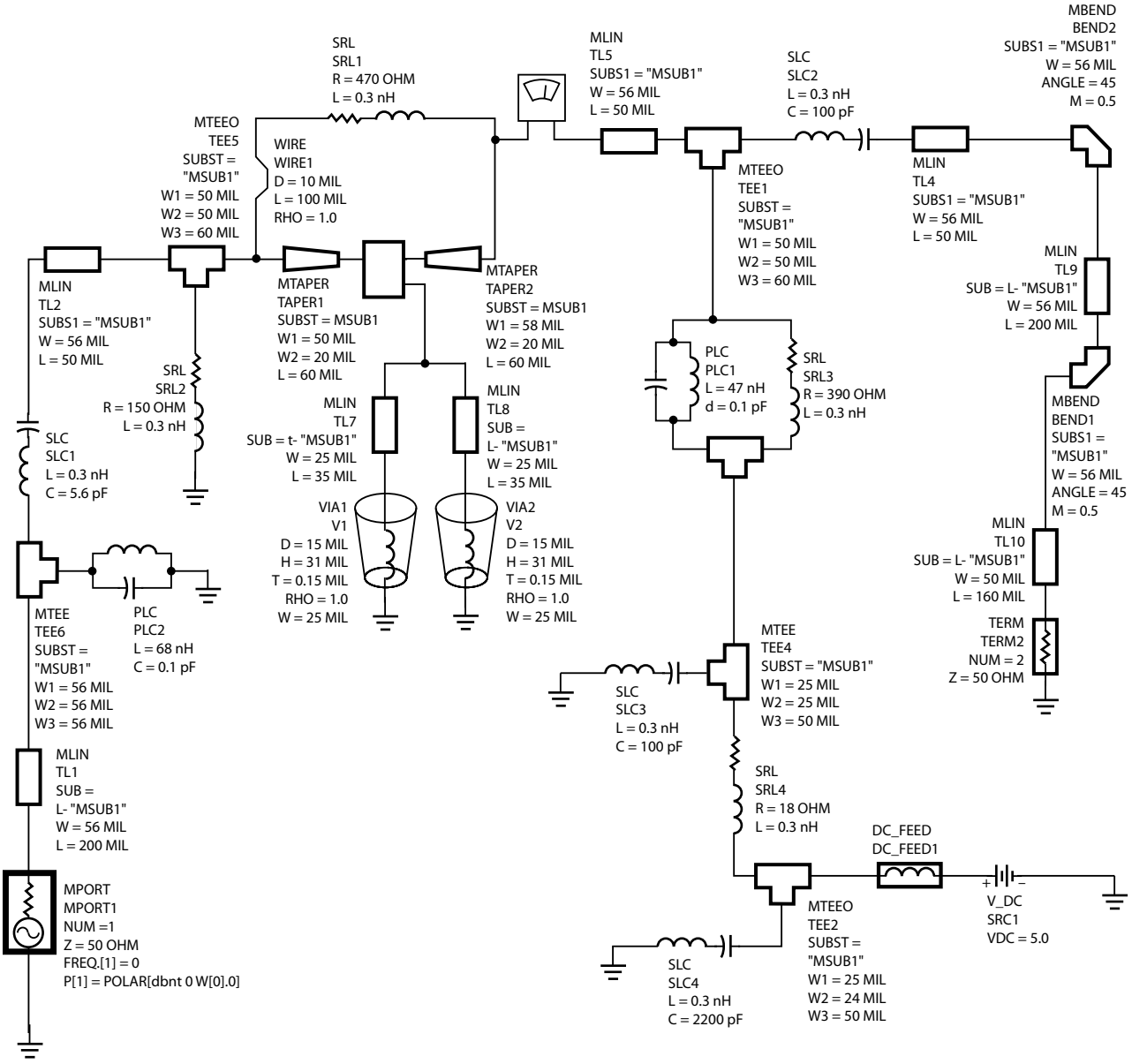

Figure 14. Schematic Layout from ADS (Non-Linear Simulation).

Conclusion

The HBFP-0450 can provide medium power, high gain, and high IP3 solutions for various commercial applications in the 400 MHz through 2500 MHz frequency range. The non-linear model showed that by changing the bias to V_{CE} of 3.4 volts and I_C of 60 mA, the gain performance of the amplifier was slightly improved without any degradation to the P-1dB or OIP3 performance. Variations in H_{FE} and ambient temperature have been considered in the amplifier design. The new bias conditions improved the worse case junction temperature of the amplifier. Successful amplifier design is a careful balance between various parameters including power, stability, noise figure, gain, return loss, intercept point, and dc power availability.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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