1800 to 1900 MHz Amplifiers using the HBFP-0405 and HBFP-0420 Low Noise Silicon Bipolar Transistors

Application Note 1160

Introduction

Avago Technologies' HBFP-0405 and HBFP-0420 are high performance isolated collector silicon bipolar transistors housed in 4-lead SC-70 (SOT-343) surface mount plastic packages. Both the HBFP-0405 and HBFP-0420 are described in three low noise amplifiers for use in the 1800 to 1900 MHz frequency range. The amplifiers are designed for use with 0.032-inch thick FR-4 printed circuit board material. The HBFP-0405 amplifier is biased at a V_{ce} of 2 V and I_c of 5 mA. The amplifier provides a 1.7 dB noise figure, 18 dB gain, and an input intercept point of -2.4 dBm. The HBFP-0420 amplifier operates at a V_{ce} of 2 V and I_c of 5 mA and provides a 1.3 dB noise figure, 13.7 dB gain, and an input intercept point of +2 dBm. The second HBFP-0420 amplifier is designed to be a high dynamic range LNA with a V_{ce} of 2 V and I_c of 15 mA. The amplifier has 14 dB gain, 2 dB noise figure, and an input IP3 of +5 dBm at 1.9 GHz.

LNA Design

The amplifiers are designed for a V_{ce} of 2 volts and I_c of 5 mA (15 mA for the high IP3 model). Typical power supply voltage, V_{cc}, is in the 2.7 to 3 volt range. Higher V_{cc} results in better bias point stability over temperature. The amplifier schematic is shown in Figure 1.

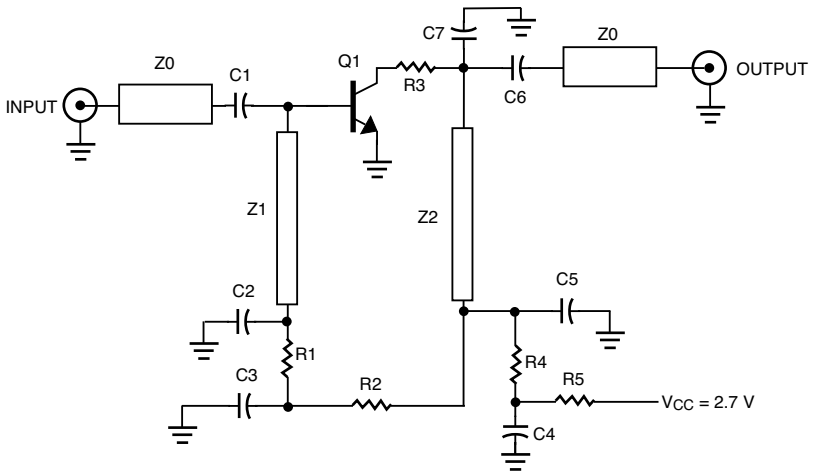

Figure 1. Schematic Diagram

A component list is shown in Table 1 for the HBFP-0405 and Table 2 for the HBFP-0420. The artwork and component placement drawing for the HBFP test board are shown in Figure 2.

For other power supply voltages, resistor R5 can be used to help set the collector voltage for a given collector current.

Table 1. Component Parts List for the HBFP-0405 Amplifier.

C1	2.7 pF chip capacitor
C2, C5	10 pF chip capacitor
C3, C4	1000 pF chip capacitor
C6	0.8 pF chip capacitor
C7	0.3 pF (can be used to tune VSWR/IP3, see text)
Q1	Avago Technologies' HBFP-0405 Silicon Bipolar Transistor
R1, R4	50 Ω chip resistor
R2	22 KΩ chip resistor (adjust for rated I_C)
R3	13 Ω chip resistor
R5	Set for desired supply voltage, R5 = 75 Ω for V_{CC} = 2.7 V
Zo	50 Ω Microstripline
Z1, Z2	Microstrip matching network

Table 2. Component Parts List for the HBFP-0420 Amplifier.

C1	5 pF chip capacitor
C2, C5	10 pF chip capacitor
C3, C4	1000 pF chip capacitor
C6	2 pF chip capacitor
C7	0.3 pF, Used at higher Ic
Q1	Avago Technologies' HBFP-0420 Silicon Bipolar Transistor
R1, R4	50 Ω chip resistor
R2	22 KΩ chip resistor, 6.7 KΩ for high IP3 amplifier (adjust for rated I_C)
R3	13 Ω chip resistor
R5	Set for desired supply voltage, R5 = 75 Ω for V_{CC} = 2.7 V
Zo	50 Ω Microstripline
Z1, Z2	Microstrip matching network

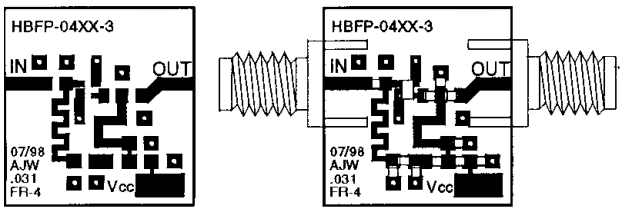

Figure 2. 1X Artwork and Component Placement Drawing for the 1800 MHz Amplifier

The input matching network uses a high pass network for the noise match. The high pass network consists of a series capacitor (C1) and a shunt microstripline (Z1). The shunt microstripline also doubles as a means of inserting base current for the transistor. C1 provides a dc block and also provides some low frequency gain roll-off. C2, R1 and C3 provide bias decoupling and a good low frequency termination for the device. The output impedance matching network is also a high pass structure consisting of a series capacitor (C6), and a shunt microstripline (Z2). A resistor (R3) is used in series with the collector to provide broadband stability by reducing amplifier gain slightly. C4, R4, and C5 provide bias decoupling and a low frequency resistive termination for the device.

HBFP-0405 Amplifier Performance at $V_{ce} = 2$ V and $I_c = 5$ mA

The measured gain and noise figure of the completed amplifier is shown in Figures 3 and 4. Amplifier noise figure measured 1.7 dB between 1800 to 1900 MHz with an associated gain of 18 dB. Measured input and output return loss is shown in Figure 5. The input return loss at 1900 MHz is 8.7 dB with a corresponding output return loss of 15.2 dB, improving to 26.3 dB at 1950 MHz.

Output intercept point, IP3, was measured at several frequencies from 1800 MHz through 2000 MHz. IP3 was then compared to output return loss as shown in Figure 6. At 1950 MHz where the best output return loss of 26.3 dB occurred, the output IP3 measured +16.1 dBm with a corresponding input IP3 of -1.3 dBm.

At 1900 MHz where the output return loss is 15 dB, the IP3 measured +15.4 dBm with a corresponding input IP3 of -2.4 dBm. At 2000 MHz where the return loss is 17.5 dB, the IP3 increased to +16.8 dBm. For best output IP3, it appears that best output return loss should be achieved slightly lower in frequency than where best IP3 is desired. Capacitor C7 can be used to fine-tune output VSWR versus IP3. Capacitor C7 can also be eliminated if the length of the shunt microstrip transmission line Z2 can be made variable in length. Removing resistor R3 will also improve IP3 at the expense of stability.

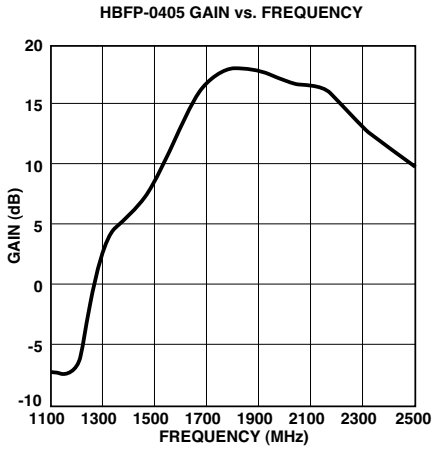

Figure 3. Gain vs. Frequency

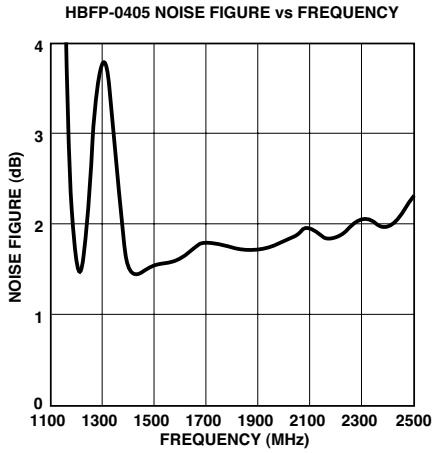

Figure 4. Noise Figure vs. Frequency

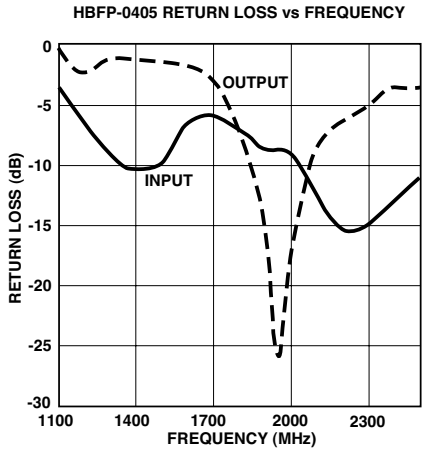

Figure 5. Input/Output Return Loss

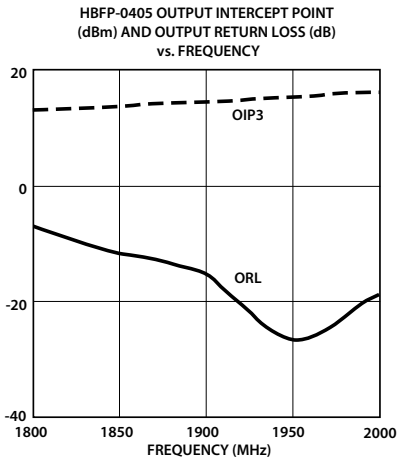

Figure 6. Output Intercept Point and turn Loss vs. Frequency

HBFP-0420 Amplifier Performance at V_{ce} = 2 V and I_c = 5 mA

The measured gain and noise figure of the completed amplifier is shown in Figures 7 and 8. Optimum amplifier noise figure is 1.3 dB and occurs at 1900 MHz. The associated gain at 1900 MHz is 13.7 dB. The amplifier exhibits very good bandwidth with less than a 1.4 dB noise figure from 1600 MHz through 2200 MHz. Gain varies from 12 dB to 15.5 dB over the same frequency range.

Measured input and output return loss is shown in Figure 9. The input return loss at 1800 MHz is 8 dB with a corresponding output return loss of 14.6 dB, improving to 23.6 dB at 2000 MHz.

Output intercept point, IP3, was measured at several frequencies from 1600 MHz through 2100 MHz. IP3 was then compared to output return loss as shown in Figure 10. At 1900 MHz, where the output return loss was measured at 18 dB, the output IP3 measured +15.8 dBm. At higher frequencies where the output return loss actually improved to 23.6 dB, the output IP3 measured +17 dBm. Input IP3 calculates to be +2.1 dBm at 1900 MHz and +4.1 dBm at 2000 MHz. Output IP3 could be improved slightly by removing resistor R3; however, return loss and stability may be sacrificed.

High IP3 HBFP-0420 Amplifier Performance at V_{ce} = 2 V and I_c = 15 mA

The high intercept point HBFP-0420 amplifier is biased at a V_{ce} of 2 V and I_c of 15 mA. This is accomplished by changing the value of resistor R2 from 22 KΩ to 6.7 KΩ. Capacitor C7 is used to rematch the output for best return loss and IP3. C7 could be eliminated if microstripline Z2 were made variable and increased in length for the higher power level.

The measured gain and noise figure of the completed amplifier is shown in Figures 11 and 12. Optimum amplifier noise figure is 1.95 dB between 1750 MHz and 2050 MHz. The associated gain between 1800 MHz and 1900 MHz is greater than 15 dB.

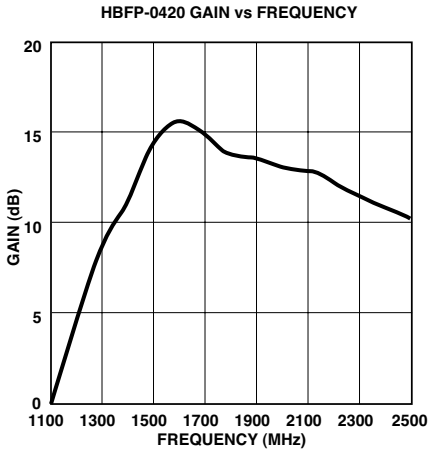

Figure 7. Gain vs. Frequency

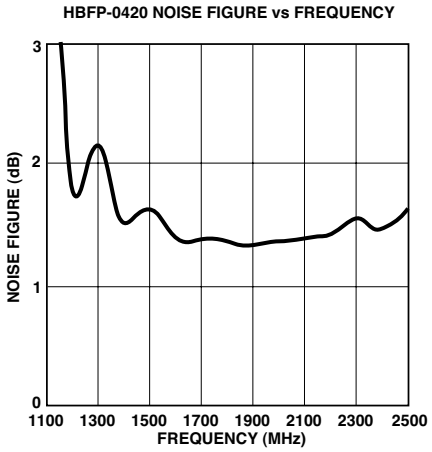

Figure 8. Noise Figure vs. Frequency

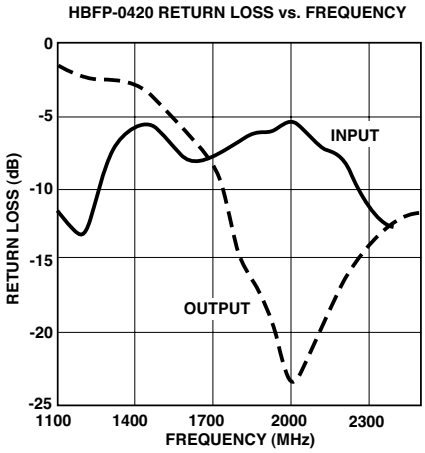

Figure 9. Input/Output Return Loss

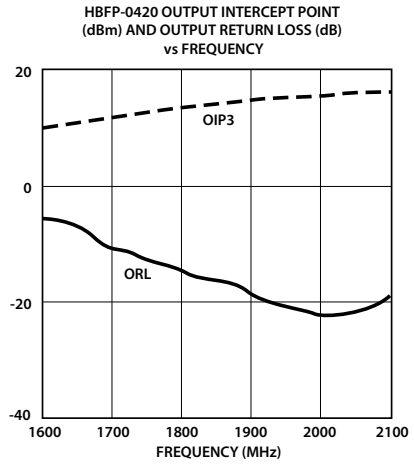

Figure 10. Output ntercept Point and Return Loss vs. Frequency

Measured input and output return loss is shown in Figure 13. The input return loss varies from 9 to 10 dB from 1800 MHz through 1900 MHz. Output return loss is 15 to 20 dB over the same frequency range.

Output intercept point, IP3, was measured at several frequencies from 1800 MHz through 2000 MHz. IP3 was then compared to output return loss as shown in Figure 14. At 1800 MHz, where the output return loss was measured at 20 dB, the output IP3 measured +19 dBm. Between 1900 MHz and 2000 MHz where the output return loss is a nominal 15 dB, IP3 improved to +20 dBm. Input IP3 calculates to be +5 dBm at 1900 MHz. IP3 could be improved slightly by removing resistor R3; however, return loss and stability may be sacrificed. IP3 increases by a dB if I_C is increased from 15 mA to 20 mA.

Using the HBFP-04XX-3 demo board at other frequencies

The demo board and design techniques presented here can be used to build low noise amplifiers for other frequencies in the 1500 through 2500 MHz frequency range. The input and output matching networks, Z1 and Z2, can be scaled for small frequency excursions with good success.

Conclusion

Both the HBFP-0405 and HBFP-0420 can provide economical low noise, high gain and moderate IP3 LNA solutions for various commercial applications in the 1500 MHz through 2500 MHz frequency range. Successful amplifier design is a careful balance between various parameters including noise figure, gain, return loss, intercept point, and dc power availability.

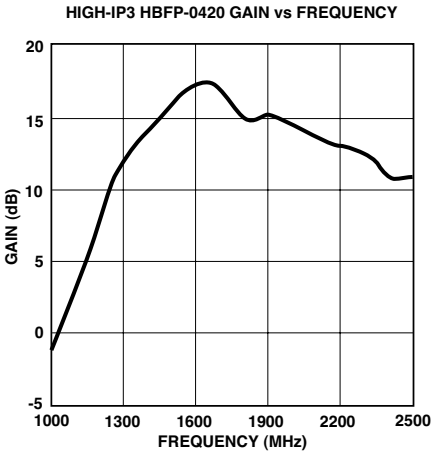

Figure 11. Gain vs. Frequency

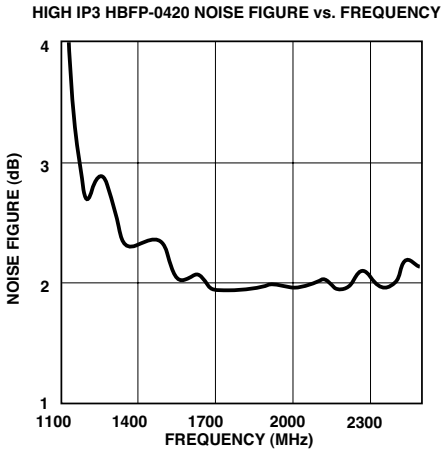

Figure 12. Noise Figure vs. Frequency

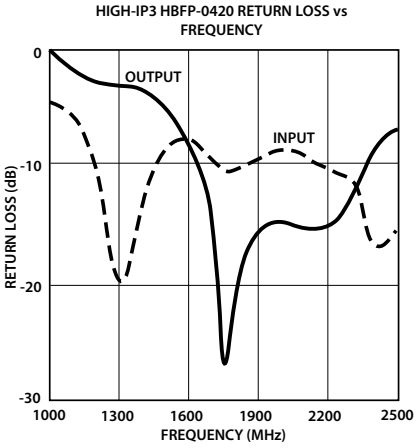

Figure 13. Input/Output Return Loss

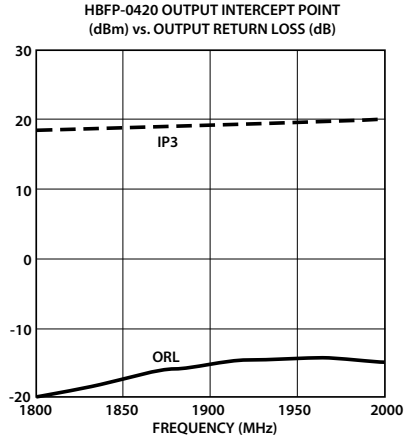

Figure 14. Output Intercept Point and Return Loss vs. Frequency

Low Noise Amplifier Design Primer

Introduction

Successful low noise amplifier design requires careful circuit modeling and may involve some performance tradeoffs. As an example, designing an amplifier to achieve the best noise figure that the device is capable of, along with its rated associated gain, does not necessarily guarantee a very good input return loss or a very stable amplifier. Gain may have to be sacrificed to enhance stability. Gain and/or noise figure may also have to be traded off for improved input return loss. These and other tradeoffs must be carefully evaluated.

Evaluation of S Parameters

The first step to successful amplifier design is to evaluate the S Parameters of the device. In a common emitter configuration, a 50 Ω source is connected to the base of the transistor and a 50 Ω load is connected to the collector of the transistor. The common lead or emitter(s) is connected to ground. This is equivalent to evaluating the device without external matching networks. Calculating the Rollett Stability Factor K from the four S Parameters at each frequency gives some insight into the device's stability. At frequencies where K is greater than or equal to 1, the device is unconditionally stable regardless of input or output terminations. When $K < 1$, the device is conditionally stable indicating that certain input or output terminations may cause the device to be unstable. An amplifier that is not unconditionally stable may still be a useful amplifier provided that stability circles for both the input and output planes are calculated. It is then a simple matter of ensuring that certain undesired impedances are not presented to the device.

As with most discrete transistors, the device will not be unconditionally stable at all frequencies. Making a device unconditionally stable, or as nearly unconditionally stable as possible, over a wide frequency range is the challenge left to the circuit designer. Certain techniques such as emitter degeneration and resistive loading can be used to enhance stability. These topics are discussed in the following sections.

Device Grounding

The entire stability picture changes when the device is mounted on a microstrip circuit board. The device is elevated above electrical ground by placing the device on the top side of the microstrip board and using plated through-holes to attach each emitter lead to ground. However short the 0.031 inch or 0.062 inch long plated through-holes may appear, they can add significant inductance in series with the device. The old "school of thought" that the device common leads need to be "hard grounded" to get performance out of a discrete transistor does not apply to all transistors. High frequency PHEMT devices generally require very good grounding because of their very small geometry and very high frequency gain. Most bipolar devices are more tolerant of greater inductance in series with the emitter grounding. Actually, some degree of equivalent inductance in series with the emitter leads can actually improve overall amplifier performance. The effect of the emitter inductance is best analyzed with the help of a good microwave circuit simulator such as those created by Avago Technologies' EEsof.

In order to remedy the modeling difficulty associated with adding the model for the plated through-holes and modeling the complex union between the device leads and the plated through-hole grounds, the device S and Noise Parameters can on occasion include the effect of device grounding. Such is the case with the Avago Technologies' HBFP series of low noise silicon bipolar transistors. The S and Noise Parameters for the HBFP series of transistors are measured on a microstripline made on a 0.025-inch thick alumina carrier. The input reference plane is at the end of the base lead. The output reference plane is at the end of the collector lead. The S and Noise parameters include the effect of four plated through-holes connecting the emitter leads on the top side of the board to the microstrip groundplane on the bottom side of the carrier. Two 0.020 inch diameter holes are placed within 0.010 inch from each emitter lead contact point with one via on either side of that point.

Effect of Emitter Inductance

The cross sectional view of a transistor with two emitter leads connected to the bottom side groundplane with the use of plated through-holes is shown in Figure 15. The distance LL is 0.0 when the device S and Noise Parameters are measured. Adding additional inductance in the form of top-side etch, shown as additional distance LL, can be used to improve in-band stability and input return loss.

The graph in Figure 16 shows the effect of emitter lead length (LL) on stability factor versus frequency for the Avago Technologies' HBFP-0420. The HBFP-0420 is biased at a Vce of 2 volts and and Ic of 5 mA. The additional microstrip etch has a width of 0.040" and is varied from zero to 0.12" in length. Length LL is measured from the edge of the plated through-hole to the edge of the emitter lead.

With a minimal value of LL, the device exhibits very good high frequency (near 10 GHz) stability as evidenced by K being greater than 1. As LL is increased in 0.040" increments, K improves at lower frequencies and becomes worse at higher frequencies. At the lower frequencies below 2 GHz where K is less than 1, the additional emitter inductance is used

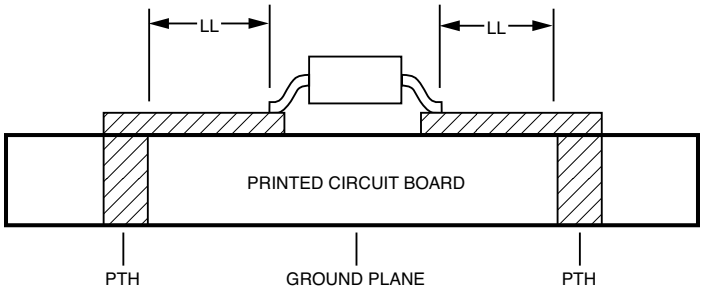

Figure 15. Cross-sectional View Showing Emitter Connections to Groundplane

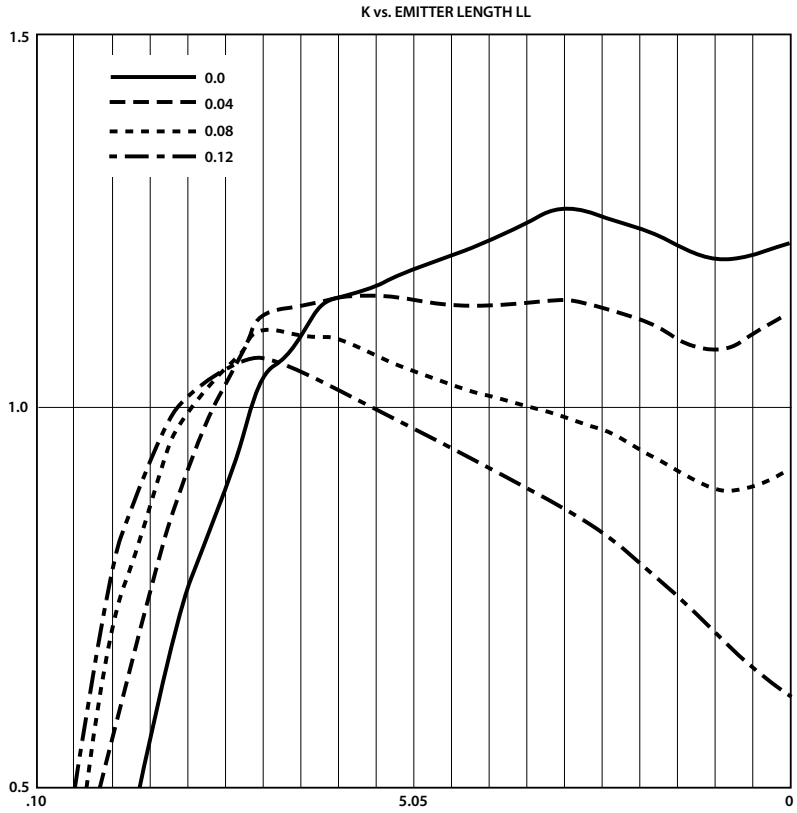

Figure 16. Stability Factor vs. Emitter Lead Length LL

to increase K above 1 if possible. The limitation on how much additional emitter inductance can be used depends on what effect the additional inductance has on stability at higher frequencies. As can be seen from Figure 16, excessive values of LL can produce greater potential for high frequency oscillations.

For the HBFP-0420, a value of 0.080" was used as a starting value for LL. Once the matching networks are attached to the device, some fine-tuning of this value may be in order. Using emitter inductance to improve stability at lower frequencies where the device is going to be operated is a fairly lossless method of stabilization. Lossless means that noise figure and power output are minimally affected. Generally some in-band gain is sacrificed to enhance stability, but this also improves input intercept point. Another very important aspect of emitter inductance is its ability to improve input return loss without sacrificing noise figure. The addition of inductance in series with the emitter has the effect of forcing S11* and Γo (reflection coefficient required for best noise figure) closer in value. Therefore, the best input return loss and lowest noise figure have a better chance of occurring simultaneously.

When modeling the additional emitter lead length, keep in mind that the circuit simulators generally assume that the emitter is a single node. Therefore, when adding additional emitter lead length in the form of LL, it should be simulated as two microstriplines in parallel of width W and length LL in series with the transistor common lead and ground. In the case of the HBFP transistors, adding additional emitter lead length LL appears to be in series with the bottom of the plated through-hole and ground. Its effect is the same as placing it between the emitter and the top side of the plated through-hole.

Impedance Matching Networks

Impedance matching networks can take on any of several different configurations based on frequency and space allocations. A low loss matching network with good bandwidth at 900 MHz would be a low pass topology consisting of a series inductor. Shunt capacitance on either side of the series inductor could be used for fine tuning. A shunt inductor which would be used for bias decoupling also acts as a high pass filter for low frequency rejection. Choosing a small value dc blocking capacitor also aids in reducing low frequency gain. A simple output matching network could consist of a shunt inductor/series capacitor in a high pass topology. Again, the shunt inductor also provides a means of injecting collector voltage. A small value dc blocking capacitor also provides low frequency gain reduction.

At 1900 MHz, the lumped inductors may not appear to be inductive due to their associated parasitic capacitance. The inductors can be replaced by transmission lines etched on the microstripline material. The loss and variability of the dielectric material can affect the performance of the microstriplines, but the cost of one inductor has been eliminated. High pass networks consisting of a shunt microstripline and a series capacitor offer a simple approach for a suitable matching network. High pass networks can be quite advantageous in reducing the level of low frequency signals incident on the amplifier. The shunt microstriplines when suitably bypassed provide a convenient method of bias insertion.

Once a rough check is performed to determine the optimum circuit configuration for both the noise matching circuit on the input and the gain matching circuit on the output, the computer can be used to optimize performance. With the input optimized for best noise figure and output optimized for best associated gain (G_a), other amplifier parameters start to unfold. Most notable may be that the circuit is not unconditionally stable and the input return loss is not very good.

Designing an amplifier to produce G_a (associated gain at minimum noise figure) may not necessarily guarantee unconditional stability. One may find that a dB or two of gain may have to be sacrificed to enhance stability. There are several ways to accomplish this gain reduction. Designing the output circuit for an intentional mismatch is one way to lower gain which enhances stability. Unfortunately, the intentional mismatch results in a high output VSWR which could add passband ripple, especially if a filter is to be cascaded with the amplifier.

Lossless feedback in the form of emitter inductance is quite often the first item to optimize. Take a second look at the effect that emitter inductance has on overall stability from 100 MHz to 10 GHz. Consider a readjustment from the earlier value that was picked based on just the S Parameters. As discussed in an earlier section, a small amount of emitter inductance can be used to reduce gain, enhance stability, and even improve input return loss. The use of emitter inductance is a powerful tool if used properly. Be cautious about adding an excessive amount of emitter inductance. Make sure that the amplifier circuit is analyzed for stability from as low as 100 MHz to as high a frequency as the device has S Parameters. Although it might appear from the computer simulation that adding considerable emitter inductance will make the amplifier circuit unconditionally stable in-band (i.e., at 900 or 1900 MHz), excessive inductance may have actually created a potential instability at a much higher frequency. The emitter inductance has a degenerative effect at lower frequencies and a regenerative effect at higher frequencies.

After determining the appropriate amount of emitter inductance, the task of stabilization can be best accomplished with the use of resistive terminations. Theoretically, resistive loading can be used in series with the emitter, base, or collector port, or in shunt with any 2 ports. In a typical low noise amplifier in a common emitter configuration, it is generally desirable to minimize the use of resistive loading in the emitter and base ports of the device. Any shunt resistive loading that includes the base port also adds to the noise figure unless some reactive components are used in series with the resistive loading to minimize its effect at a particular frequency. The best place to use resistive loading would then be the collector. The resistive loading can be in series with the collector or in shunt between the collector and ground. Ground is defined as the common return point for all three device terminals. This is generally the bottom groundplane in a typical microstrip layout and not the emitter pad(s). Remember that the emitter is elevated above the groundplane by virtue of the plated through-hole(s) and any associated lead length.

The use of a resistor in series with the collector does provide a convenient broadband de-Qing element which does enhance stability. Shunt resistive loading is a convenient way to provide a broadband termination for an otherwise high impedance device. Lowering the resistor value tends to swamp out the loading effect of the transistor making the device very stable over a very wide frequency range. A simple two element matching network can then provide a very good output VSWR. The undesirable side effect is some loss of gain, but most notable output P1dB and IP3. P1dB and IP3 may have to be traded off for stability and output return loss. Other techniques such as lossless feedback and feedforward techniques can be used to improve IP3. They require an increase in component count and real estate and are beyond the scope of this application note.

It is important to note that even though some transistors may have higher G_a and higher S21, the key parameter is how much stable gain can be achieved from a particular amplifier design. High amplifier gain is useless if the amplifier is sensitive to terminations. Most good VHF through L band amplifier designs incorporate some resistive loading to limit gain and improve stability.

Passive Component Modeling

Passive components such as chip capacitors and inductors can exhibit unusually high frequency characteristics due to package parasitics. As a first order approximation, a chip capacitor has some associated lead inductance which can be modeled as a single inductor in series with the capacitor. This is shown schematically in Figure 17.

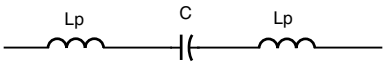

Figure 17. Capacitor Modeled with Lead Inductance

Tests conducted on a sample of high quality microwave chip capacitors suggest a combined lead inductance between 0.7 and 0.8 nH for capacitors in the 1 to 27 pF range. A high quality 1000 pF capacitor had 1.2 nH of associated lead inductance.

A wirewound chip inductor can also have a small amount of shunt capacitance distributed across the turns of the coil. Figure 18 shows schematically the parasitic capacitance in parallel with the inductor.

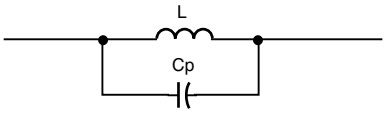

Figure 18. Inductor Modeled with Shunt Capacitance

Tests indicate the equivalent shunt capacitance can vary from 0.05 to 0.17 pF for chip inductors in the 4 to 27 nH range. If the series resistance, E.S.R., is known, it can also be added into the model for each device. Circuit simulation accuracy is improved immensely if the component parasitics are included in the simulation. Most component manufacturers have developed models for their products.

Sample Computer Simulation

An accurate circuit simulation can certainly provide the appropriate first step to a successful amplifier design. Manufacturing tolerances in both the active and passive components often prohibit perfect correlation. Besides providing important information regarding gain, noise figure, input and output return loss, the computer simulation provides very important information regarding circuit stability. Unless a circuit is actually oscillating on the bench, it may be difficult to predict instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett Stability factor K and generating stability circles are two methods made considerably easier with computer simulations.

The HBFP-0420 is analyzed in a 1900 MHz circuit with the use of Libra for Windows. The input was optimized for lowest noise figure coincident with good input return loss. The output network was optimized for stability and return loss. The circuit simulation is shown in Appendix A. Initially, the transmission lines at Z1 and Z2 were simulated as straight microstriplines (i.e., no bends). The out-of-band gain performance of the simulation did not compare very well to the bench tests. Once the actual bends were incorporated in both Z1 and Z2, the gain versus frequency plot compared very well to the bench tests. See Figure 19.

The emitter grounds are modeled as discussed earlier in this application note. Additional lead length is used to supply increased emitter inductance for stability. The transition from the transistor base and collector leads is modeled as a series of microstriplines with varying line widths.

The inductance associated with the chip capacitors was included in the simulation. The chip resistors were assumed to be ideal. In reality, there is some shunt capacitance which could influence the effect of R3 at high frequencies. At low frequencies where R1 and R4 offer a resistive termination to the Q1, the capacitance across these resistors is probably insignificant.

The simulated gain, noise figure, and input/output return loss of an HBFP-0420 amplifier is shown in Figures 19, 20, and 21. These plots only address the performance near the actual desired operating frequency. It is still important to analyze out-of-band performance in regards to abnormal gain peaks, positive return loss, and stability.

A plot of Rollett Stability factor K as calculated from 0.1 GHz to 10 GHz is shown in Figure 22. The emitter inductance is the dominant factor in high frequency stability. Increasing emitter inductance causes high frequency stability to worsen (i.e., decreased value of K). The resistive loading consisting of R3 is the main contributor to low frequency stability. Increasing the value of R3 makes the stability factor K higher. As stability is improved, certain amplifier parameters such as gain and power output may have to be sacrificed.

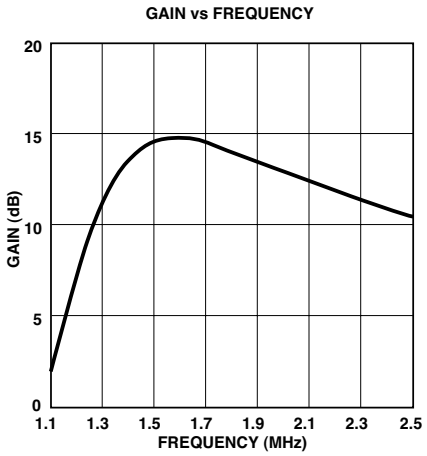

Figure 19. Gain vs. Frequency

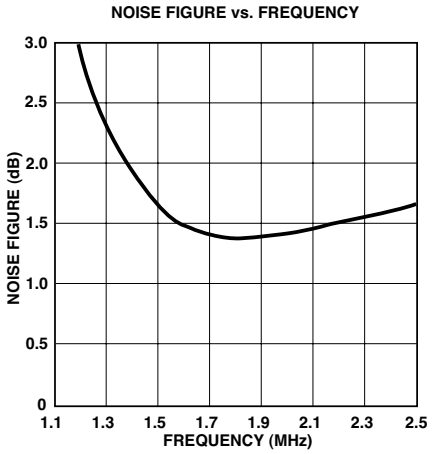

Figure 20. Noise Figure vs. Frequency

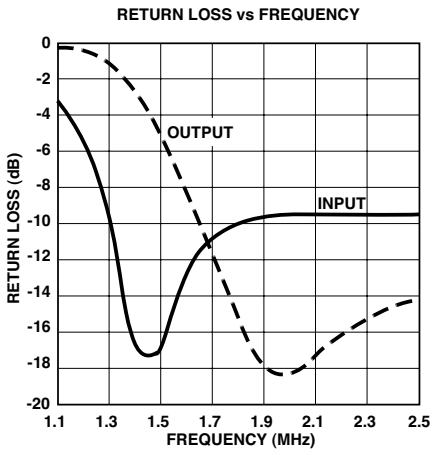

Figure 21. Input and Output Return Loss vs. Frequency

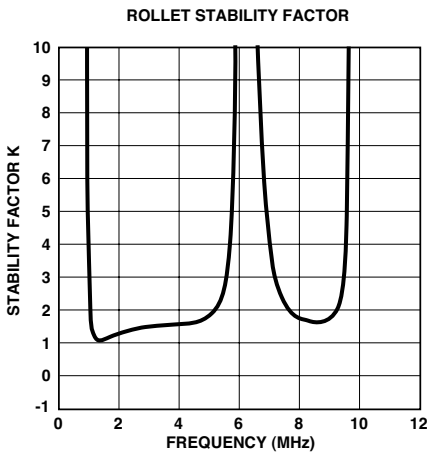

Figure 22. Rollett Stability Factor vs. Frequency

Appendix A

HBPF-0420 1900 MHz LOW NOISE AMPLIFIER
SINGLE STAGE AMPLIFIER DESIGN
A.J.WARD 8-18-98
BIAS CONDITIONS Vce = 2V, I = 5 mA

```
DIM
    FREQ GHZ
    IND  NH
    CAP  PF
    LNG  IN

VAR

LL1#.001 0.04  .04  !EMITTER LEAD LENGTH, NEED TO DOUBLE FOR USING TWO
!EMITTER LEADS

CKT
        MSUB    ER=4.8    H=.031    T=.0014        RHO=1          RGH=0
        TAND    TAND=.004
        !INPUT MATCHING NETWORK
        MLIN    1         2         W=.05          L=.2
        SLC     2         3         L=.7  C#1      5  10          !C1
        MLIN    3         4         W=.05  L=.015
        MTEE    4         5         6  W1=.05  W2=.05  W3=.02
        MLIN    5         7         W=.05  L=.015
        MSTEP   7         8         W1=.05  W2=.02
        MLIN    8         13        W=.02  L=.02
        MSTEP   13        14        W1=.02  W2=.012
        MLIN    14        15        W=.012  L=.001
        MLIN    6         120       W=.02  L=.04      NODES 6 THROUGH 20 MAKE UP Z1
        MCORN   120       121       W=.02
        MLIN    121       122       W=.02  L=.03
        MCORN   123       122       W=.02
        MLIN    123       124       W=.02  L=.03
        MCORN   125       124       W=.02
        MLIN    125       126       W=.02  L=.03
        MCORN   126       127       W=.02
        MLIN    127       128       W=.02  L=.03
        MCORN   128       129       W=.02
        MLIN    129       130       W=.02  L=.03
        MCORN   131       130       W=.02
        MLIN    131       132       W=.02  L=.03
        MCORN   133       132       W=.02
        MLIN    133       134       W=.02  L=.03
        MCORN   134       135       W=.02
        MLIN    135       136       W=.02  L=.03
        MCORN   136       137       W=.02
        MLIN    137       138       W=.02  L=.03
        MCORN   139       138       W=.02
        MLIN    139       140       W=.02  L=.03
```

```
MCORN   141     140     W=.02
MLIN    141     20      W=.02  L=.04
MTEE    20      21      22              W1=.02  W2=.1  W3=.1
SLC     22      23      L=.8            C=10                    !C2
VIA     23      0       D1=.03  D2=.03  H=.031  T=.0014
RES     21      25      R=50                                    !R1
MLIN    25      26      W=.06  L=.06
SLC     26      27      L=1.2  C=1000                  !C3
VIA     27      0       D1=.03  D2=.03  H=.031  T=.0014

S2PA    15      50      40              C:\S_DATA\BJT\hbfp420a.s2p
MLIN    40      0       W=.04  L^LL1
S AND NOISE PARAMETER FILES ALREADY INCLUDE VIAS,
LL1 REPRESENTS ADDITIONAL LEAD LENGTH/INDUCTANCE
ADDED IN SERIES WITH DEVICE EMITTER LEADS, LL1
SHOULD BE DOUBLED AND USED IN BOTH EMITTER LEADS
THEREFORE IF LL1 = .040 INCHES, THEN .080 INCHES
 OF MLIN IS ADDED TO EACH EMITTER LEAD.

MLIN    50      51      W=.012  L=.001
MSTEP   51      53      W1=.012  W2=.02
MLIN    53      54      W=.02  L=.01
MSTEP   54      55      W1=.02  W2=.06
MLIN    55      56      W=.06  L=.05
RES     56      57      R=13                                    !R3
MLIN    57      58      W=.06  L=.01
SLC     58      0       L=.7  C=.3  C7 FINE TUNING POWER/OUTPUT RETURN LOSS
MTEE    58      59      60              W1=.06  W2=.05  W3=.037
MLIN    59      61      W=.05  L=.01
SLC     61      62      L=.75  C#.1 2  5                        !C6
MLIN    62      63      W=.05  L=.2
MLIN    60      170     W=.037  L=.07    NODES 60 THROUGH 70 MAKE UP Z2
MCORN   170     171     W=.037
MLIN    171     172     W=.037  L=.07
MCORN   173     172     W=.037
MLIN    173     174     W=.037  L=.065
MCORN   175     174     W=.037
MLIN    175     70      W=.037  L=.075
MTEE    70      71      72              W1=.037  W2=.15  W3=.1
SLC     72      80      L=.8  C=10                              !C5
VIA     80      0       D1=.03  D2=.03  H=.031  T=.001
RES     71      90      R=50                                    !R4
SLC     90      91      L=1.2  C=1000                  !C4
VIA     91      0       D1=.03  D2=.03  H=.031  T=.0014

DEF2P 1   63 AMP
```

```
FREQ
        SWEEP   0.1     10      .1
        STEP    1.9
        SWEEP   1.1     2.5     .05

OUT
        AMP     DB[S11]
        AMP     DB[S21]  GR1
        AMP     DB[S12]
        AMP     DB[S22]
        AMP     NF
        AMP     K        GR2
        AMP     B1
        AMP     NPAR
        AMP     GA
!GRID
        FREQ    .1      2       .1
        GR1     1       20      1
        GR2     0.5     1.5     0.5

OPT
        FREQ    1.9     1.9
        AMP     DB[S21]>14
        AMP     DB[S11]<-13
        AMP     DB[S22]<-13
        AMP     NF<1.3 50
        AMP     K>1
```

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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