BROADCOM®

Data Sheet

BCM56980

12.8 Tb/s Multilayer Switch

Overview

The Broadcom® BCM56980 family is a class of high-performance, high-connectivity network switching devices supporting up to 32x 400GbE, 64x 200GbE, or 128x 100GbE switch ports. The device family features a maximum of 32 integrated BlackhawkCores, each with eight integrated 50G PAM4 SerDes transceivers and associated PCS for native support of XFI, 10GBASE-KR/CR/SR/ER/LR, 40GBASE-KR4/CR4/SR4/ER4/LR4, 50GbE, and 100GBASE-KR4/CR4/SR4/ER4/LR4. The BCM56980 delivers high-bandwidth, glueless network connectivity up to 12.8 Tb/s on a single chip.

The BCM56980 is a family of Ethernet switches designed to address performance, capacity, and service requirements for next-generation data center and cloud computing environments. The BCM56980 architecture delivers complete Layer 2 (L2) and Layer 3 (L3) switching and routing capabilities with maximum port density, while consuming minimum power, latency, and board footprint. Software compatibility is maintained across the StrataXGS® product portfolio to simplify customer designs and reduce customer time-to-market.

As server interfaces transition to higher Ethernet speeds and virtualization continues to increase link utilization, data center networks are demanding switches with dense 100GbE and 400GbE connectivity at the edge and aggregation layers. With up to 256 50G PAM4 SerDes that conform to IEEE 802.3bs and 802.3cd specifications, and full flexibility in configuring 10/25/40/50/100/200/400GbE ports, a single BCM56980 switching chip can be used to build scalable, cost-effective Top of Rack (ToR) switch, blade switch, and aggregation equipment across the entire data center. The BCM56980 has extensive features to address the rapidly increasing scale of data center network deployments and distributed computing applications: large L2 and L3 forwarding capacity supporting numerous multi-pathing technologies; enhanced instrumentation; switching, migration, and robust buffer performance including many-to-one burst absorption capabilities that assist in TCP incast scenarios.

With the BCM56980 device, customers can build data centers with much higher server node counts while simultaneously improving per-port power efficiency. The BCM56980 is built using state-of-the-art silicon process technology and incorporates advanced power management features to minimize power based on the features in use.

Features

General features:

- 256x 50G PAM4 SerDes configuration.
- Flexible port configurations: 10GbE to 400GbE support with run-time reconfigurability (Flexport™).
- Oversubscription to maximize I/O throughput.
- Low pin-to-pin latency in cut-through and store-and-forward modes.
- Supports IEEE 802.3bj Clause 91 Forward Error Correction (FEC), IEEE 802.3bj Clause 93 100GbE-KR4 transmit training, and IEEE 802.3ap Clause 72 10G-KR transmit training.

Data center features:

- Hardware-based encapsulation.
- DCBX congestion management: priority-based flow control (PFC), enhanced transmission selection (ETS).
- Per virtual machine traffic shaping.

StrataXGS scalable architecture supports high-performance switch designs for L2/L3 packet processing:

- Full IPv4 and IPv6 routing support.
- Hardware-based encapsulations, including MPLS, GRE, and ISATAP.
- Three-stage ContentAware™ processing with ICAP stage supports exact match feature.
- Dedicated hash table for L2 MAC and L3 host.
- Flexible ingress/egress counter pools.

Features (continued)

Buffering and traffic management:

- Integrated high-performance SmartBuffer memory for maximum burst absorption and service guarantees.
- Full Quality of Service (QoS) support:
- Weighted random early discard (WRED).
- srTCM and trTCM color marking and metering.
- Congestion management capabilities including ECN.
- Dynamic load balancing (DLB) for ECMP groups.
- Packetized MMU statistics.
- Network monitoring.
- Elephant trap monitors.
- DLB monitors.
- Latency distribution histogram.
- Network congestion detection.
- sFlow redirect.
- Visibility and packet tracing.
- Enhanced load balancing.
- Enhanced trunk hashing capabilities: RTAG7, symmetric hash, flex hash, and resilient hash.
- Support for jumbo frames up to 9416 bytes.
- High-speed vector-based scheduler with 12 queues per port and scheduling algorithms: SP, RR, WRR, and WDRR.

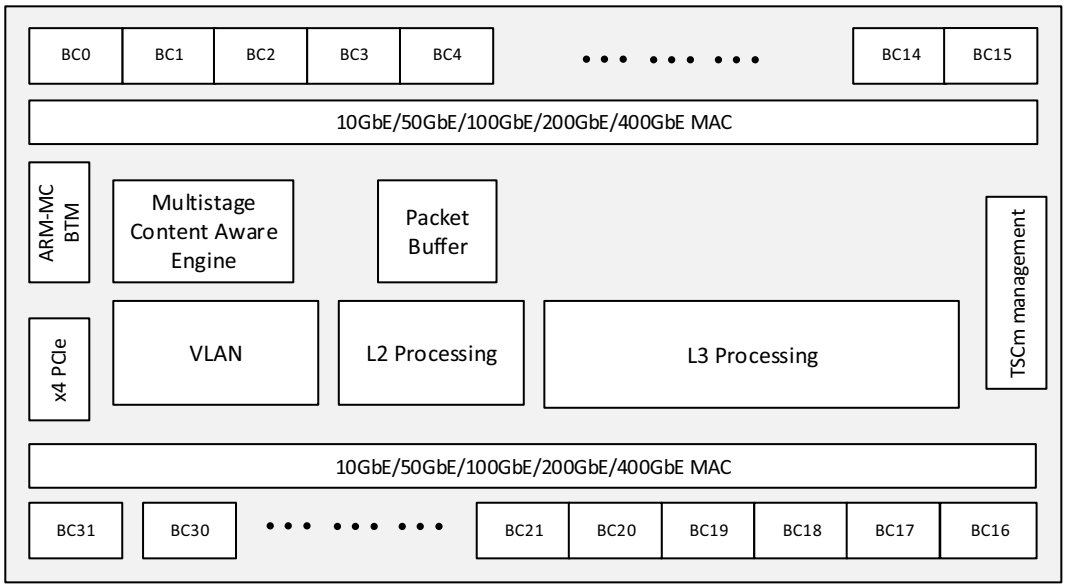
Additional features:

- In-band telemetry.
- Elephant trap.
- Comprehensive time synchronization support:
  - Integrated IEEE 1588v2 processor.
  - IEEE 802.1AS support.
  - Synchronous Ethernet.
  - Ingress and egress per packet time stamping.
- sFlow support includes ingress, egress, and flex sampler. Option to forward truncated sFlow packets to remote agent.
- Packet sampling (PSAMP) ingress-based mirroring with option to truncate as well as zero out the payload at different offset.
- Two dedicated 1G/10G auxiliary Ethernet ports
- x4 PCI Express (PCIe) Gen 3.0 interface to support a local CPU.
- Adjustable voltage scaling (AVS) for reduced average and peak power.

Applications

- Data center ToR, blade, and aggregation switching.
- Mobile core switches.
- Cloud computing.
- Large-scale enterprise campus backbone.
- Service provider core switching.

Figure 1: 12.8 Tb/s Multilayer Switch



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Chapter 1: Introduction

The Broadcom BCM56980 family consists of several devices with flexible port configurations. All switching features and table sizes are identical within each device, except as noted in the following tables.

NOTE: The BCM56980 supports PAM4-based SerDes controller cores, BlackhawkCore (BC), and MerlinCore (TSCm).

Table 1: BCM56980 Family I/O Bandwidth and Throughput

Device	I/O Bandwidth (Tb/s)	BC (#)	Dedicated Mgmt. TSCm (#)	Typical Configuration
BCM56980	12.8	32	2	32 × 400G, 128 × 100G
BCM56982	8.0	20	2	20 × 400G, 48 × 100G + 8 × 400G
BCM56983	6.4	16	1	16 × 400G
BCM56984	6.4	32	2	64 × 100G (NRZ only)

The BCM56980 family includes the configurations described in the following table.

Table 2: BCM56980 Device Family Port Configurations

Device	400 Gb/s	200 Gb/s	100 Gb/s	50 Gb/s	10 Gb/s
BCM56980	32 maximum	64 maximum	128 maximum	144 maximum	144 maximum
BCM56982	20 maximum	40 maximum	80 maximum	144 maximum	144 maximum
BCM56983	16 maximum	32 maximum	64 maximum	72 maximum	72 maximum
BCM56984	—	—	64 maximum	128 maximum	144 maximum

The BCM56980 supports a maximum of 144 front-panel ports by using 32 BlackhawkCores in the eight pipelines. Ports can be configured only as Ethernet ports.

NOTE: The BCM56983 uses only four of the eight pipelines, which reduces the supported number of front-panel ports to 72.

In addition to the BlackhawkCores, the device contains one MerlinCore that can be used to support a maximum of two auxiliary ports. The MerlinCore consists of four SerDes lanes. If an auxiliary port is configured in single SerDes lane mode, lane 0 or lane 2 should be used. If the port is configured as RXAUI mode, either lanes 0 and 1, or lanes 2 and 3 should be used. If a single auxiliary port is used, the four-lane XAUI port mode should be used.

The device also supports a four-lane PCIe interface that can be operated at Gen1, Gen2, and Gen3 speed. The PCIe interface is typically connected to the root complex of the host CPU as an x1, x2, or x4 PCIe Gen1, Gen2, or Gen3 interface.

Chapter 2: Device Overview

The BCM56980 has a modular, high-performance packet-switching architecture and provides the following benefits:

- Flexible port configurations
- Scalable throughput
- Scalable packet processing features
- Low pin-to-pin latency

2.1 Feature List

The BCM56980 features are listed in the following table.

Table 3: BCM56980 Features

Feature	Description
Configuration	■ 10/25/40/50/100/200/400GbE multilayer Ethernet switch. ■ All ports operate in oversubscription mode. ■ Flexible SerDes contains eight SerDes lanes per BlackhawkCore, configured to operate in any of the following configurations: – 25GbE (1-lane) – 40GbE (2-lane) – 40GbE (4-lane) – 50GbE (1-lane) – 50GbE (2-lane) – 100GbE (2-lane) – 100GbE (4-lane) – 200GbE (4-lane) – 400GbE (8-lane)
L2 Switching	■ L2 learn cache for software based learning. ■ Software-based MAC address aging. ■ Supports Ethernet/IEEE 802.3 packet sizes (64 bytes to 1522 bytes) and jumbo packets up to 9416 bytes. ■ Reserved MAC address table for CPU control packets, bridge protocol data units (BPDUs), and the ability to perform shared VLAN switching.
Switching	■ Supports Ethernet/IEEE 802.3 packet sizes (64 bytes to 1522 bytes) and jumbo packets up to 9416 bytes.
L2 Multicast	■ Three port filtering modes (PFM) to control multicast packet behavior.
VLAN	■ Supports 4K VLANs. ■ Supports up to 128 VLAN profiles on a per VLAN basis.
VLAN	■ Assign VLAN for untagged and priority tagged packets based on the following: – Port-based VLANs. ■ Supports up to 128 VLAN profiles on a per VLAN basis. ■ Ingress filtering for IEEE 802.1Q VLAN security.
Spanning Tree Group Table	Indicates spanning tree state of each port for each spanning tree group.

Table 3: BCM56980 Features (Continued)

Feature	Description
Mirroring	■ Ingress/egress mirroring support. ■ Total of four mirror-to-port (MTP) ports are supported. They are shared by ingress and egress mirroring logic. The device can support any combination of four mirroring port types. ■ A separate packet is created for each MTP port. ■ Mirror-to-port receives unmodified packet for ingress mirroring. ■ Mirror-to-port receives modified packet for egress mirroring. ■ Remote switched port analyzer (RSPAN) mirroring, VLAN mirroring, flow mirroring ■ Encapsulated remote switched port analyzer (ERSPAN) mirroring into a GRE tunnel. ■ Multiple packets can be generated in the StrataXGS architecture: one packet for the switched copy, and four mirror copies which can be of any type. ■ Payload zeroing and truncation for mirrored copies.
DSCP	■ Per port DSCP remarking. ■ DSCP remarking based on a FP filter match. ■ DSCP to IEEE 802.1p mapping. ■ Remap incoming DSCP to new outgoing DSCP.
Layer 3 Routing (IPv4, IPv6)	■ Native support for IPv4 and IPv6 unicast and multicast routing. ■ Direct-attached hosts in the L3 table. ■ Longest prefix match (LPM) based routing. ■ ECMP/WCMP routing: ECMP path resolution based on source/source IP address, Protocol, IPv6 flow label, and TCP/UDP port. ■ Software-based aging support. ■ Routing of IPv6 packets. ■ True 128-bit IPv6 support as well as /64 support for LPM.
Virtual Routing and Forwarding (VRF)	■ Segmentation of L3 routing tables. ■ VPN ID assigned based on ingress port, VLAN, or flow.
IP Multicast	■ Simultaneous L2 bridging and L3 routing. ■ Flexible multicast packet replication. ■ Optional source port checks. ■ Dual lookup: {S, G, V} and {*, G, V}. ■ Ability to fall back to L2 multicast lookup on IPMC miss. ■ Port filter mode (PFM) per VLAN for L2 multicast, IPv4 multicast, and IPv6 multicast packets. ■ Control trapping of unknown IPMC packets to CPU on a per VLAN, per IP-type basis. ■ IP multicast address consistency check with destination MAC address.
IPv6 Tunneling	■ IPv6-in-IPv6: The outer header is IPv6, and the payload is IPv6. ■ IP-in-IPv6 Tunnel: The outer header is IPv6, and the payload is IPv4.
GRE Tunneling	■ Supports IPv4 as payload. ■ Supports IPv6 as payload.
Preclassification ContentAware™ processor (VCAP)	■ 512 entries. ■ Rules for assignment of VLAN based on flexible criteria, block packets, bind MAC address with IP address, and assign VRF ID. ■ Support for single-wide and double-wide modes. ■ Field selectors on per port, per slice, and per packet type basis. ■ Ability to add or replace VLAN tag, change priority, assign classification ID, drop.
Protection Switching	Dedicated hardware support for the following: ■ MPLS fast reroute (FRR). ■ Per next HOP (Layer 3).

Table 3: BCM56980 Features (Continued)

Feature	Description
ContentAware Processing (ICAP)	Rules for L2–L7 packet classification on ingress, ACLs, metering, statistics: ■ 3K entries per pipe: 160-bits per entry. ■ 9 logical slices allowing 9 parallel lookups and matches. ■ Supports 16 logical tables. ■ Layer 2 through Layer 7 packet classification. ■ Parses 128 bytes deep into packet. ■ ACL-based policing. ■ Ingress port based filtering with maximum 18 ICAP ports per pipeline. ■ Multiple look-ups, matches and actions per packet. ■ MAC destination address remarking. ■ Class-based marking for SLAs. ■ Traffic class definition based on the filter. ■ Classification of different packet formats (IPv6, IPv4, HTLS, IEEE 802.1Q, Ether II, IEEE 802.3). ■ Support for single-wide and double-wide mode for IPv6 filtering. ■ TCP/UDP source and destination port number range checking. ■ Filtering IP packets with options. ■ Metering support on ingress ports and CPU queues. ■ Programmable meters allow policing of flows. ■ Dual leaky bucket meters support srTCM, trTCM, and modified trTCM (RFC2697, RFC2698, and RFC4115). ■ Metering granularity from 8 Kb/s to 1 Mb/s. ■ Per port, per slice, and per packet type field selection. ■ Filter on multistage classifier classification ID, source MAC classification ID, or VRF ID.
ContentAware Processing (ECAP)	Rules for packet classification on egress: ACLs, and statistics: ■ 512 entries. ■ Filter on fully modified packets allowing egress ACLs. ■ Filter on modified L3 routed and IPMC replicated packets. ■ Keys based on L2–L4 fields for IPv4 and IPv6 packets: ■ Actions: drop, change DSCP, change inner/outer priority, change inner/outer VLAN ID, change outer, TPID. ■ Byte-based and packet-based statistics.
Port Security	■ Supports IEEE 802.1X. ■ Blocking of egress ports on per-MAC address basis. ■ Blocking of egress ports, on a per-VLAN basis, for broadcast, unknown unicast, and multicast packets.
BroadShield™: Denial-of-Service Attack Prevention	■ Built-in illegal address check (IPv4, IPv6). ■ Land packets (SIP = DIP). ■ Null scan (TCP sequence number = 0, control bits = 0). ■ Ping flood (flood of ICMP packets). ■ SYN/SYN-ACK flooding. ■ SYN with sPort < 1024. ■ Smurf attack. ■ Individual control over handling of DoS packet.
BroadShield HPAE	■ Limit access based on source/destination MAC address, source/destination IP address. ■ Detection Dynamic Host Configuration Protocol (DHCP) snooping, IP address snooping. ■ Classification of groups based on L2–L4 field.
CPU Protocol Packet Processing	■ Ability to control CPU protocol packet handling individually, including BPDU, Address Resolution Protocol (ARP), Internet Group Management Protocol (IGMP), Multicast Listener Discovery (MLD), and DHCP. ■ Individual control of trapping protocol packets and setting internal priority. ■ Extensive control of handling of IGMP and MLD packet types.

Table 3: BCM56980 Features (Continued)

Feature	Description
QoS	■ Shared UC and MC queues (12 per port). ■ VLAN shaping support. ■ 48 CoS queues for CPU. ■ Three drop precedence colors. ■ Per port, per CoS drop profiles. ■ Minimum/maximum bandwidth guarantee (shaping) per CoS, per port. ■ Traffic shaping available on CPU queues: bandwidth based and packet-per-second based. ■ Programmable priority to CoS queue mapping. ■ Provides two levels of drop precedence per queue. ■ Explicit Congestion Notification (ECN) support. ■ Strict priority (SP), weighted round-robin (WRR), and weighted deficit round-robin (WDRR) mechanism for shaped queue selection. ■ Priority-based flow control (PFC). ■ Linear programming of bucket size of egress port shaping and CoS shaping. ■ Supports ingress port rate-based policing and pause flow control. ■ Mapping of incoming priority, CFI to outgoing priority and drop precedence.
Memory Management Unit	■ Integrated SmartBuffer. See Table 4 for size information. ■ Transition cut-through switching for low latency. ■ Static and dynamic memory allocation. ■ Programmable transmit queue thresholds. ■ Ingress cell triggers for back pressure. ■ Cell and packet thresholds for triggering HOL prevention. ■ WRED congestion control.
Port Table	Per port configuration settings and attributes (for example, L2 learning, port discards, VLAN handling, and priority assignment).
IEEE 802.1bb PFC	Enables per-priority flow control, so that a low-priority application that is causing congestion can be throttled without impacting higher priority or loss sensitive applications.
IEEE 802.1az Enhanced Transmission Selection (ETS)	Enables per priority group minimum bandwidth guarantees.
Flexible Counters	■ Programmable packet/byte RX/TX counters for forwarding addresses (such as MAC, IP, and MPLS). ■ Programmable packet/byte RX/TX counters for service instances (VLAN, VRF, and so on).
Management Information Base	■ sFlow support, RFC 3176. ■ SMON MIB, IETF RFC 2613. ■ RMON statistics group, IETF RFC 2819. ■ SNMP interface group, IETF RFC 1213, 2836. ■ Ethernet-like MIB, IETF RFC 1643. ■ Ethernet MIB, IEEE 802.3u. ■ Bridge MIB, IETF RFC 1493.
Oversubscription	■ Clock frequency is set to match the aggregated port bandwidth assumed under application-worst-case loading conditions. ■ Reduces peak power based on system traffic loading and packet length mix assumptions.
Low-Latency Mode	This is the default mode of operation and uses the maximum allowable internal clock rates, resulting in the highest power. It is possible to reduce the internal clock rates, trading off higher latency versus lower power.
EFP Bypass	This mode allows lower latency by bypassing the EFP stage of the pipeline. In this mode, no EFP processing is possible.

Table 3: BCM56980 Features (Continued)

Feature	Description
IP Multicast	■ Simultaneous L2 bridging and L3 routing. ■ Flexible multicast packet replication. ■ Optional source port checks. ■ Dual lookup: {S, G, V} and {*,G, V}. ■ PIM-SM, PIM-DM, and PIM-SSM (encapsulation). ■ DVMRP on a per-VLAN basis. ■ Reverse path forwarding checks. ■ Ability to fall back to L2 multicast lookup on IPMC miss. ■ Port filtering mode (PFM) per VLAN for L2 multicast, IPv4 multicast, and IPv6 multicast packets. ■ Control trapping of unknown IPMC packets to CPU on a per VLAN, per IP-type basis. ■ IP multicast address consistency check with destination MAC address.
Tunnel Encapsulation and Deencapsulation	Supports the following: ■ IPv6 to IPv4. ■ ISATAP. ■ Configured tunnels. ■ IP-IP (mobile-IP) tunnels. ■ MPLS.
Network Time Sync	Packet-based time synchronization (IEEE 1588 and IEEE 802.1AS): ■ Integrated IEEE 1588 v2 processor for running PTP stack and clock recovery servo. ■ One-step and two-step time stamping. ■ High-precision frequency synthesizer. ■ Synchronous Ethernet layer-one clock recovery. Precision Time Protocol (PTP): ■ Transparent clock. ■ Boundary clock.
Resilient Hashing	■ Provide the same Resource Isolation attributes of consistent hashing. ■ Minimize the imbalance among resources within the same resource group when adding/deleting load balancing resources.
Overtemperature Protection	■ Supports real time temperature monitoring, and ability to set temperature for interrupt.
Elephant Trap	■ Identify and trap flows that transfer large amount of data based on user specified criteria.
In-band Network Telemetry	■ Supports insertion of meta-data in packets for identifying network faults and isolating their location, transient failures, congestion information and latency.
PSAMP	■ Samples of packets from a network device, and the transmission of samples to a collector device, with the appropriate meta-data.
ECMP Group Dynamic Load Balancing with Flow Monitoring	■ Randomly sample packets undergoing DLB and Copy to CPU. ■ Sample the packet to mirror or the CPU when macroflow assignment or re-assignment occurs.
Stacking/Chassis	■ Supports HiGig3™ in transit mode only.

The following table lists BCM56980 device scalability.

Table 4: BCM56980 Family Device Scalability

<table>
<tr><th>Feature</th><th>All BCM56980 Devices</th></tr>
<tr><td>I/O bandwidth</td><td>12,800 G</td></tr>
<tr><td>Number of SerDes</td><td>256 × 50G (128 x 50G for the BCM56983)</td></tr>
<tr><td>Integrated Packet Buffer Memory</td><td>64 MB (32 MB for the BCM56983)</td></tr>
<tr><td>MAC Entries</td><td>8K</td></tr>
<tr><td>L2MC</td><td>512
NOTE: Can be increased to 1K if L3MC not used and IFP rules are added.</td></tr>
<tr><td>BlackhawkCore</td><td>32</td></tr>
<tr><td>VLAN</td><td>4K</td></tr>
<tr><td>VRF</td><td>2048</td></tr>
<tr><td>L3 Hosts – Combined</td><td>IPv4 UC: 16K
IPv4 MC: 8K
IPV6 UC: 8K
IPV6 MC: 4K</td></tr>
<tr><td>L3 LPM</td><td>
<table>
<tr><th>LPM Mode</th><th>Packet Type</th><th>Total Raw Entries (TCAM/SRAM)</th></tr>
<tr><td rowspan="3">LPM TCAM</td><td>IPv4 (32b)</td><td>4K</td></tr>
<tr><td>IPv6 (64b)</td><td>2K</td></tr>
<tr><td>IPv6 (128b)</td><td>1K</td></tr>
<tr><td>ALPM</td><td>IPv4/IPv6</td><td>Up to 960K[a]</td></tr>
</table>
a. Refer to Theory of Operations (56980-PG1xx)
</td></tr>
<tr><td>L3 Multicast groups</td><td>512</td></tr>
<tr><td colspan="2">ContentAware Processor Total Rules/Slices</td></tr>
<tr><td>■ Preingress</td><td>512/4 (512 per pipe)</td></tr>
<tr><td>■ Ingress</td><td>3K/9 (3K per pipe)</td></tr>
<tr><td>■ Egress</td><td>512/4 (512 per pipe)</td></tr>
<tr><td>ECMP groups</td><td>4096 maximum</td></tr>
<tr><td>ECMP members per group</td><td>4K maximum</td></tr>
<tr><td>Total ECMP group members</td><td>64K</td></tr>
<tr><td>Ports per modules</td><td>144 front panel ports</td></tr>
</table>

Table 5: Device Table Lookup Size

Table	Depth	Description
DSCP_TABLE	4096	Differential service code point table.
EFP_COUNTER_TABLE	1024	Counter table for the EFP.
EFP_POLICY_TABLE	512	Policy table for determining actions in the EFP.
EGR_DSCP_TABLE	10240	Egress DSCP table to select the new DSCP for outer tunnel header packets (64 entries for each of the 128 profiles).
EGR_GPP_ATTRIBUTE	160	Egress GPP attribute table, feature-specific Ethernet.
EGR_IP_TUNNEL	4096	Egress IP tunnel table. Used to make new tunnel header.

Table 5: Device Table Lookup Size (Continued)

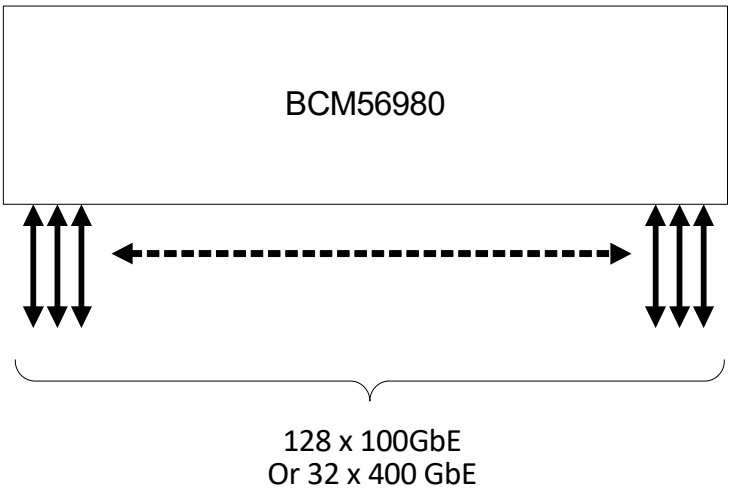
Table	Depth	Description
EGR_IPMC	512	Per IPMC group attributes needed in EP.
EGR_L3_INTF	8192	L3 interface table.
EGR_L3_NEXT_HOP	32768	Egress L3 next hop table.
EGR_VLAN	4096	VLAN membership table for egress.
EGR_VLAN_STG	64	Egress spanning tree state table.
IFP_METER_TABLE	512	Per pipe meter table structures for the IFP.
IFP_POLICY_TABLE	3072	Per pipe policy table for determining actions in the IFP.
ING_L3_NEXT_HOP	32768	L3_NEXT_HOP table.
IPROT_NHI_TABLE	256	Protection switching next hop table.
L2X	8192	L2_ENTRY table. Includes L2_ENTRY_TILE, L2_HITDA and L2_HITSA.
L2_USER_ENTRY	256	Combined L2_ENTRY TCAM/data RAM for guaranteed L2 entries and BPDUs.
L2MC	512	L2 multicast table.
L3_ECMP	65536	L3 equal cost multipath table.
L3_IIF	8192	L3 input interface properties.
L3_IPMC	512	L3 IPMC table.
L3_TUNNEL_SINGLE	16384	Single L3 tunnel table TCAM.
L3_TUNNEL_DOUBLE	8192	Double L3 tunnel table TCAM.
L3_TUNNEL_QUAD	4096	Quad L3 tunnel table TCAM.
MPLS_ENTRY_SINGLE	16384	MPLS label single lookup. Dual-hash table with keys and data.
SOURCE_TRUNK_MAP_TABLE	160	Source trunk map table.
VFP_POLICY_TABLE	512	Policy table for determining actions in the VCAP.
VLAN_MPLS	4096	Contains MPLS controls associated with the 4K VLANs.
VLAN	4096	Contains controls associated with the 4K VLANs.
VRF	2048	VRF properties – address is VRF value.

2.2 Target Applications

2.2.1 100GbE/200GbE/400GbE Aggregation Switch

Data center switching represents a fast growing segment of the Ethernet switching market and is the primary driver behind 100GbE, 200GbE, and 400GbE port growth. Data centers are where computer resources (servers or blade chassis) are centralized and managed in a structured way utilizing high-efficiency Ethernet connectivity. A single 32x 400GbE, 64x 200GbE, or 128x 100GbE aggregation switch (as shown in the following figure), can be built using a single BCM56980 device.

Figure 2: 32x 400GbE Aggregation Switch



Chapter 3: System Interfaces

This section provides a brief functional description of BCM56980 interfaces. The signal descriptions and AC and DC timing sections provide the electrical description of each interface in more detail.

NOTE: For more information on interfaces supporting Broadcom proprietary logical protocols, refer to the BCM56980 *Theory of Operations* (56980-PG1xx).

The BCM56980 external interfaces are described in the following table.

Table 6: BCM56980 External Interfaces

Interface	Description
50G BlackhawkCore Octal SerDes	■ Integrated octal 50G PAM4/NRZ SerDes core for front-panel ports. ■ 400GbE ■ 200GbE ■ 100GbE ■ 50GbE ■ 40GbE ■ 10GbE **NOTE:** Does not support 1G. ■ Supports full-duplex operation (half-duplex is not supported at any speed).
10G Merlin Quad SerDes	■ Integrated SerDes core for management ports. Supports up to two ports, lanes 0 and 2 only. ■ 10GbE: XFI, SFI, KR, CR, XAUI, and RXAUI. ■ 2.5GbE: 2500BASE-X. ■ 1GbE: 10/100/1000 Mb/s SGMII, and 1000BASE-X ■ Supports full-duplex operation (half-duplex is not supported at any speed).
CPU (PCIe)	■ x4 PCIe v3.0-compliant interface. ■ Scatter-gather DMA for packet transfer to CPU. ■ Table DMA: For copying any switch table into system memory. ■ Statistics DMA: For gathering on-chip statistics counters. ■ Packet DMA: For transferring packets from and to the CPU.
LED	■ Integrated on chip controller for up to 512 system LEDs at a 30 Hz refresh rate. ■ Simple micro-controller implementation with instructions optimized for LED control. ■ Low-cost two-wire interface to system LEDs. ■ 512 bytes of program RAM. ■ 512 bytes of data RAM. ■ LED micro controller has direct hardware access to per-port speed, duplex state, flow control state, link state, transmit and receive activity.
MIIM	■ IEEE 802.3u-compliant MIIM interface for communication with external PHY devices. ■ 2.5-MHz operation. ■ Compliant to CL22 and CL45.
BSC	■ CPU-controlled master mode to communicate with other NXP I^2C-compatible devices.
JTAG	■ JTAG-compliant interface used to support boundary scan operations. ■ 12.5-MHz operation.

Table 6: BCM56980 External Interfaces (Continued)

Interface	Description
BroadSync®	■ Packet-based time synchronization support: IEEE 802.1AS, IEEE 1588. ■ Provides time-of-day synchronization to grand master clock source. ■ Master mode to accept time-of-day information from a grand master clock source. ■ Slave mode to externalize the time-of-day information to an external device.
Adjustable Voltage Scaling (AVS)/ROV	■ AVS or ROV pins. This interface is designed to connect to system power supply control pins to scale core input voltage to the device at the appropriate level to optimize device's power consumption.

3.1 BlackhawkCore SerDes

The BlackhawkCore (BC or TSCbc) SerDes is the versatile physical layer interface for the BCM56980, and is specifically designed to support up to 400 Gb/s. This serial interface supports the following features:

- Octal SerDes block supporting eight serial links.
- Support for data rates of 10.3125 Gb/s up to 53.125 Gb/s per serial link.

The BCM56980 device family incorporates PAM4-based SerDes Core (BC). This macro allows the device to support low-latency throughput, oversubscription capability, and Flexport configuration. The BC macro consists of the digital control logic and a BlackhawkCore analog block. The terms BC, TSCbc, and BlackhawkCore are used interchangeably in this document.

The BCM56980 device has 32 BlackhawkCores. Each BlackhawkCore contains eight SerDes lanes. Each BlackhawkCore lane can be configured as a single individual port, or multiple lanes can be aggregated into an single port.

The 32 BlackhawkCores in the device are separated into the following eight pipes:

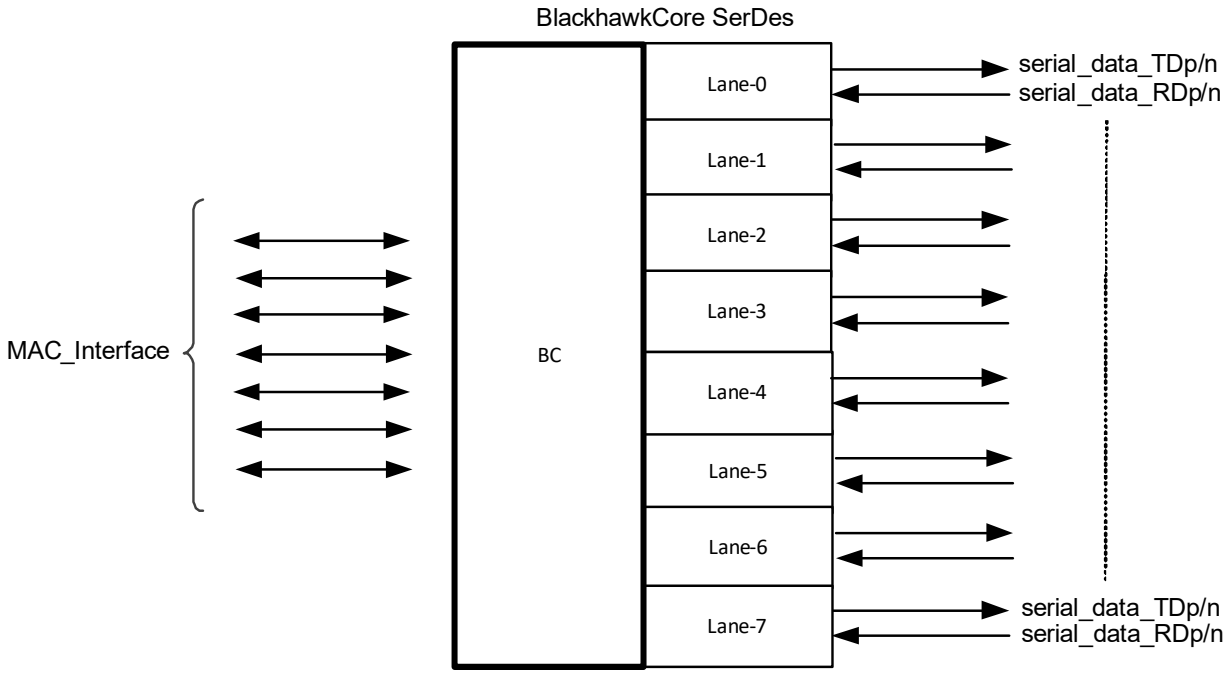
- Pipe-0: BlackhawkCore [31:0]
- Pipe-1: BlackhawkCore [63:32]
- Pipe-2: BlackhawkCore [95:64]
- Pipe-3: BlackhawkCore [127:96]
- Pipe-4: BlackhawkCore [159:128]
- Pipe-5: BlackhawkCore [191:160]
- Pipe-6: BlackhawkCore [223:192]
- Pipe-7: BlackhawkCore [255:224]

The device contains 32 BlackhawkCores divided into 8 pipes of 4 BlackhawkCores, which enables up to 12800G of I/O bandwidth. See Figure 3 for the BlackhawkCore configuration within each pipe.

Figure 3: BlackhawkCore (BC) Configuration

The following figure is a conceptual view of the relation of the BlackhawkCore block within the device. The number of BlackhawkCores supported depends on the device part number.

Figure 4: Conceptual View for BlackhawkCore 8 SerDes Lanes



Each SerDes lane operates in a range from 10.3125 Gb/s to 53.125 Gb/s.

50GBASE-KR is supported in a single lane, and each BlackhawkCore instance can support 8 × 50GBASE-KR ports.

The following table shows the different BlackhawkCore configurations.

Table 7: BlackhawkCore Configurations

Port Speed	Interface Type	Logical Lane Type	Physical Lanes	FEC	Signaling Mode
400G	400GAUI-8 (C2C, C2M) 400GBASE-KR8 400GBASE-CR8	FEC	8	RS544	26.5625G PAM4
400G/350G/300G	Reduced Lane Mode (RLM)	FEC	8/7/6	RS544	26.5625G PAM4
200G	200GAUI-4 (C2C, C2M) 200GBASE-KR4 200GBASE-CR4	FEC	4	RS544	26.5625G PAM4
		FEC	4	RS272	26.5625G PAM4
		PCS/VIRTUAL	4	NONE	25.78125G PAM4
200G/150G	Reduced Lane Mode (RLM)	FEC	4/3	RS544	26.5625G PAM4

Table 7: BlackhawkCore Configurations (Continued)

Port Speed	Interface Type	Logical Lane Type	Physical Lanes	FEC	Signaling Mode
100G	100GAUI-2 (C2C, C2M) 100GBASE-KR2 100GBASE-CR2	FEC	2	RS544	26.5625G PAM4
		FEC	2	RS272	26.5625G PAM4
		PCS/Virtual	2	NONE	25.78125G PAM4
		FEC	2	RS528	25.78125G PAM4
	100GAUI-4 (C2C, C2M) 100GBASE-KR4 100GBASE-CR4	FEC	4	RS544	26.5625G NRZ
		FEC	4	RS528	25.78125G NRZ
		PCS/VIRTUAL	4	NONE	25.78125G NRZ
50G	50GAUI-1 (C2C, C2M) 50GBASE-CR 50GBASE-KR	FEC	1	RS544	26.5625G PAM4
		FEC	1	RS272	26.5625G PAM4
		FEC	1	RS528	25.78125G PAM4
	LAUI-2 (C2C, C2M) 50GAUI-2 (C2C, C2M) 50GBASE-KR2 50GBASE-CR2	FEC	2	RS544	26.5625G NRZ
		FEC	2	RS528	25.78125G NRZ
		PCS/VIRTUAL	2	NONE	25.78125G NRZ
40G	XLAUI XLPPI 40GBASE-CR4 40GBASE-KR4	PCS/VIRTUAL	4	BASE-R	10.3125G NRZ
		PCS/VIRTUAL	4	NONE	10.3125G NRZ
	XLAUI2	PCS/VIRTUAL	2	NONE	20.625G NRZ
25G	25GAUI (C2C, C2M) 25GBASE-C 25GBASE-CR-S 25GBASE-CR 25GBASE-KR	FEC	1	RS528	25.78125G NRZ
		PCS/VIRTUAL	1	BASE-R	25.78125G NRZ
		PCS/VIRTUAL	1	NONE	25.78125G NRZ
10G	10G-KR SFI XFI	PCS/VIRTUAL	1	BASE-R	10.3125G NRZ
		PCS/VIRTUAL	1	NONE	10.3125G NRZ

NOTE: The lane-swapping mode is configurable.
For PAM4 modes without FEC (single lane 50G, dual lane 100G, 200G) or using RS528 FEC (single lane 50G, dual lane 100G), the lane speed is 51.5625G.
RS272 FEC is a Broadcom proprietary protocol to achieve lower latency. When operating in RS272, all ports within the upper- or lower-half four lanes of a BlackhawkCore must operate at the same FEC (RS272). For example, in a 2 × 100G configuration (each 100G port is 2 × 50G), one 100G port cannot operate at RS544 FEC while the other operates at RS272 FEC.

NOTE: The BCM56980 supports simultaneous operation of all seven port speeds (also called speed modes) listed in this table across various ports of the chip. However, within a single BlackhawkCore, there are restrictions on which port modes can coexist. For more information, refer to the *BCM56980 Hardware Design Guide* (56980-DG1xx).

3.2 BlackhawkCore Octal SerDes Configuration Guidelines

Each device has up to 32 BlackhawkCores, depending on the device part number. The BlackhawkCores are organized into eight pipes. None of the eight pipes can exceed 1/8 of the total switching throughput. In configurations where not all ports are active, bandwidth should be balanced across all eight pipelines.

A physical port consists of one or more SerDes lane in the device. There are up to 32 BlackhawkCores, each with eight physical SerDes lanes. A logical port is defined as a front-panel, CPU, or loopback port. The total number of logical ports per device is 160. Out of 160, up to 144 ports, excluding the management port, can be assigned as front-panel ports. The rest are used as CPU and internal loopback ports.

NOTE: The BCM56983 device supports 72 front-panel ports because only four pipes are active. Each pipe supports up to 18 general ports.

Physical-port to logical-port numbering limitations exist across pipes that are integrated into the SDK software.

3.2.1 Flexport Configuration

The BlackhawkCore supports the ability to change a port configuration (speed and number of lanes per port) at runtime without affecting the operation of the other ports or requiring the device to be reset. If the SerDes continue to be associated with the same logical ports, then the Flexport configuration amounts to a speed change and can be handled automatically by the BlackhawkCore driver. Logical ports can be added, removed, or associated with a different number of SerDes through user API calls. The configuration of two SerDes within a BlackhawkCore can be changed without affecting the ports) using the remaining SerDes.

Two PLLs are in a BlackhawkCore: PLL0 (secondary) and PLL1 (primary). Each of the two PLLs can generate one of the three basic port frequencies: 10G-NRZ (20.625 GHz), 25G-NRZ (25.78125 GHz), or 50G-PAM4 (26.5625 GHz). The SDK software sets the primary PLL frequency after collecting all available port speeds allocated within a BlackhawkCore. Changing the secondary VCO without a reset is allowed if no other port in the BlackhawkCore is using the secondary VCO. However, changing the primary VCO requires a BlackhawkCore reset.

3.3 10G Quad MerlinCore SerDes

The MerlinCore SerDes is the management-port physical-layer interface for the BCM56980 specifically designed to support up to two 10 Gb/s management ports on the single MerlinCore. This serial interface supports the following features:

- The MerlinCore SerDes has four serial links and can support the following:
  - Two ports in single-lane mode.
  - Two ports in RXAUI mode.
  - One port in XAUI mode.
- Single-lane mode supports 1000BASE-x, SGMII, 2500BASE-X, SFI, XFI, or 10GBASE-KR.
- Two-lane mode supports RXAUI.
- Four-lane mode supports XAUI.
- There is no support for mixing a two-lane and a four-lane port with any other port type.
- All single-lane port types can be mixed.

NOTE: When a 2500BASE-X port is mixed with a SFI, XFI, or 10GBASE-KR port, the transmit jitter on the 2500BASE-X port violates the IEEE specification.

3.4 PCIe

The PCIe interface provided by the BCM56980 switch conforms to the PCIe Gen3 specification and supports Gen1 and Gen2. The BCM56980 PCIe interface supports x1, x2, or x4 wide connections (8.0G link speed or 7.88 Gb/s data rate in each direction). No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

The device provides strap signals to limit the maximum link speed and link width of the PCIe interface. The internal pulls on the strap signals cause the device to default to allowing a maximum link width of x4 and PCIe Gen3 link speeds.

For all PCIe speeds, the design requires QSPI flash memory programmed with Broadcom-provided firmware to be connected to the IP_QSPI interface on the device, and the device must be strapped to perform a download from this memory. This is required because the firmware configures the PCIe interface into a mode that is functional and compliant to the Gen3 specification. The exact strap settings and design requirements are as follows:

- BOOT_DEV[2:0] = 3'b000
- MHOST0_BOOT_DEV = 1'b1
- PCIE_FORCE_GENTYPE[1:0] = 2'b00
- QSPI flash memory is programmed with Broadcom provided firmware
- QSPI flash memory is connected to IP_QSPI interface

NOTE: Design requirements include a QSPI flash memory that contains the Broadcom-provided PCIe firmware for all PCIe operating modes.The device must also be strapped to download and execute the code from this flash memory for the PCIe interface to be functional.

3.5 LED

There are three LED processors in the BCM56980 device that support up to 256 physical ports plus two management ports. Each LED processor includes a two-wire (clock and data) LED interface to control system LEDs. Both LED_CLK and LED_DATA are outputs. When active, LED_CLK is a 5 MHz clock. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED_DATA bits. The LED_DATA signal is pulsed high at the start of each LED refresh cycle. The LED refresh cycle is repeated approximately every 30 ms to refresh the LEDs. The LED timing diagrams are shown in the following two figures.

Figure 5: Single LED Refresh Cycle

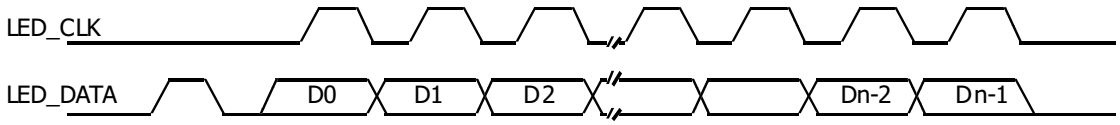
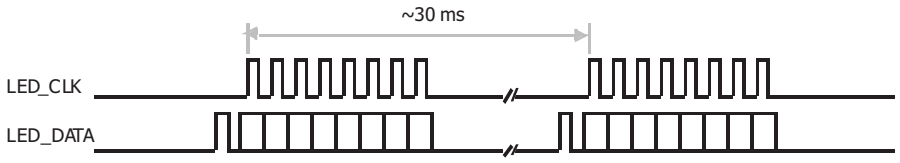


Figure 6: LED Refresh Timing



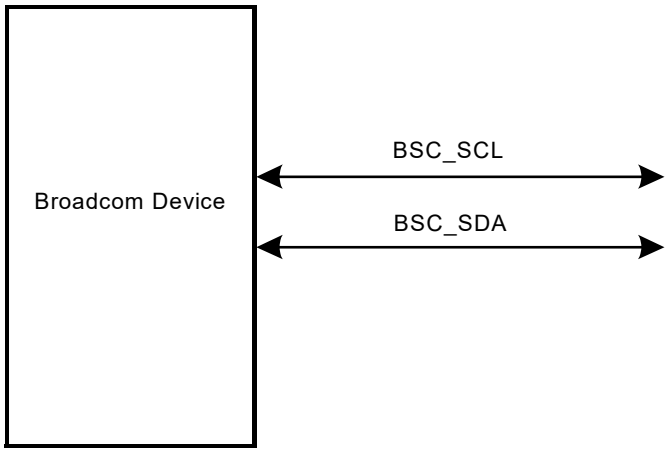
3.6 MIIM

The CPU Management Interface Controller (CMIC) supports the IEEE 802.3u standard MIIM interface: a two-wire serial bus controlled by the CMIC that allows register access to all the PHYs in the system. Data from the PHY can be read/write using this interface. The two signals for MIIM are MDC (clock) and MDIO (bidirectional data). The CPU uses this interface to program the internal and external PHY registers. The MIIM interface can be configured to support Clause 45.

3.7 Broadcom Serial Controller

The BCM56980 switch provides a Broadcom Serial Control (BSC) interface to communicate with other devices that support a similar interface. This interface is a NXP I^2C-compatible interface. The signals supported are shown in the following figure.

Figure 7: BSC Interface



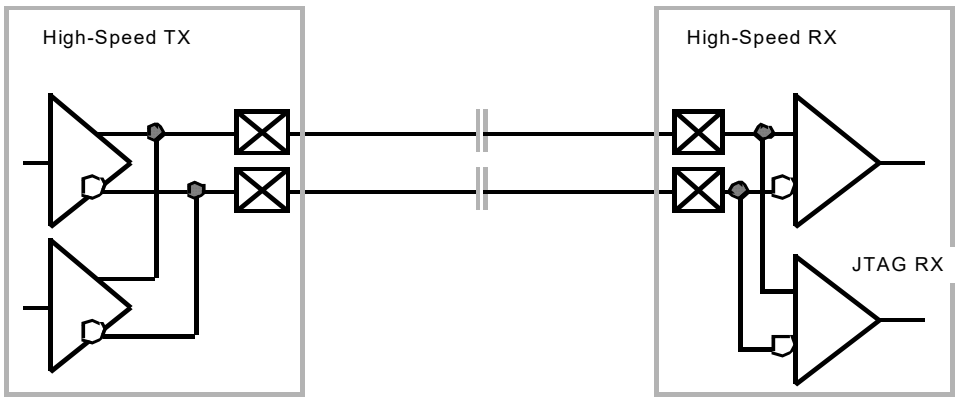
The BSC interface is supported in master mode only. The supported BSC data protocol format is big endian, which is consistent with the NXP I^2C protocol supported by other vendors.

3.8 JTAG

A standard JTAG interface is provided for boundary scan operations. This interface uses a standard five-pin interface and supports operational speeds up to 12.5 MHz.

Traditional JTAG provides the capability to test for opens and shorts when the device is mounted on the PCB. Because current technology requires that most high-speed differential signals must be AC-coupled, the traditional DC test for opens and shorts can produce false results. To provide a means of testing high-speed differential signals, the BCM56980 family supports the latest JTAG specification, IEEE 1149.6 (also known as AC-JTAG). AC-JTAG can enable the detection of manufacturing faults on high-speed differential lines on the PCB. The device incorporates independent transceivers with low-load capacitance to avoid any adverse effect on the high-speed differential signals. The signals supported are shown in the following figure.

Figure 8: AC JTAG Test Block



3.9 BroadSync

The BroadSync interface provides a way to externalize the timing information and clock signals generated by the global timing module, an internal clock adjustment block. The interface can also be used as an input to receive timing from an external source or synchronize timing information in a multichip system. The BroadSync interface is used by ordinary clocks (OCs) in either a master or slave role. When the OC is a master, the BroadSync interface is configured as an input, accepting timing information from external hardware. When the OC is a slave, BroadSync is configured as an output, providing timing information to external hardware.

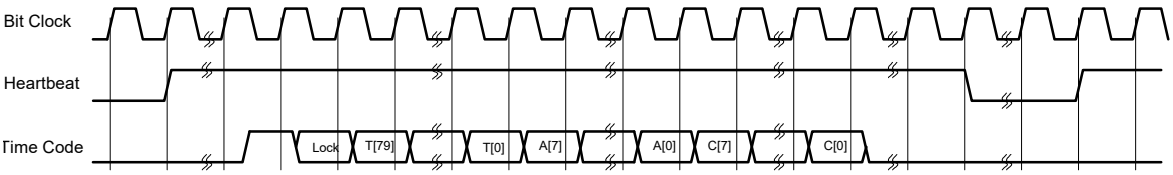
The BroadSync interface consists of three bidirectional signals that can be configured as outputs (master mode) or inputs (slave mode):

- TS_SYNC – Heartbeat clock. Signals the start of the transmission of the synchronized time value.
- TS_BIT_CLK – Bit clock. Used for the data transfer of the synchronized time value.
- TS_TIME_VAL – Time code or synchronized time value.

3.9.1 Slave Mode – BroadSync Signals as Inputs

In slave mode, the external hardware provides the bit clock and heartbeat clock signals as shown in the following figure. During each heartbeat period, the external hardware also shifts in the time code values. The shifted time value corresponds to the time of the most recent rising edge of the heartbeat signal. The heartbeat and time code signals are sampled off the negative edge of the bit clock.

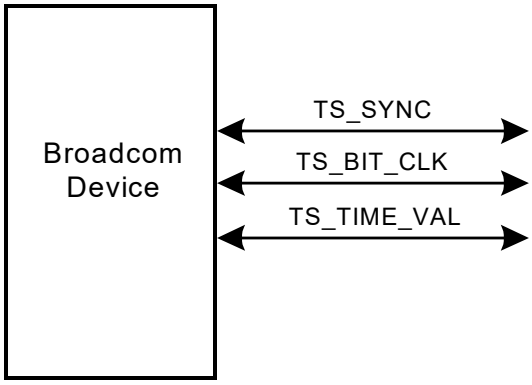
Figure 9: BroadSync Interface Timing Diagram



3.9.2 Master Mode – BroadSync Signals as Outputs

In master mode, the device provides the bit clock, heartbeat, and time code signals and enables the external devices to synchronize their behavior with that of the master. The signals supported are shown in the following figure.

Figure 10: BroadSync Interface



Chapter 4: Signal Descriptions

This section describes the device hardware signals. Table 8 lists signal type conventions, and Table 9 provides the signal name descriptions.

Table 8: Signal Types

Abbreviation	Description
I	Input
O	Output
B	Bidirectional signal
B_{OD}	Open drain bidirectional signal
B_{PU}	Bidirectional signal with internal pull-up
I_{PD}	Input with internal pull-down
I_{PU}	Input with internal pull-up
O_{OD}	Output with open drain
PWR/GND	Power/ground plane
NC	No connect
P	Positive leg
N	Negative leg

4.1 Pin Description

The signal descriptions in this section apply to all devices in the BCM56980 family.

Table 9: Device Signal Descriptions

Names	Qty.	I/O	Voltage	Description
System Signals				
SYS_RST_L	1	I_{PU}	3.3V	Device reset (active low).
AVS[7:0]	8	O	3.3V	Adaptive Voltage Scaling output. These outputs are expected to be connected to a VRM 11.1 compliant module to configure the appropriate core supply voltage for this part (Table 11, Operating Conditions for default voltage settings).
RESCAL[8:0]_REXT	9	I	0.8V	For each RESCAL pin, and a nearest GND pin, connect a 4.53 kΩ resistor through a low-impedance path to ground. Each resistor is used to calibrate the impedance of the SerDes cores in the device. A total of nine separate resistors are required.
PCIE_INTR_L	1	O	3.3	Active low-interrupt signal that asserts whenever the PCIe core sends an interrupt via an in-band mechanism like INT-X or MSI.
Subtotal	19	—	—	—

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
Required Clocks				
CORE_PLL_FREFp/n	2	I	1.8V	50 MHz differential clock to drive core logic. Refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for external AC-coupling capacitor and termination resistor requirements.
PCIe_REFCLKp/n	2	I	0.8V	100 MHz PCI Express differential reference clock. Refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for external AC-coupling capacitor and termination resistor requirements.
BC_A_REFCLKp/n BC_B_REFCLKp/n BC_C_REFCLKp/n BC_D_REFCLKp/n BC_E_REFCLKp/n BC_F_REFCLKp/n BC_G_REFCLKp/n BC_H_REFCLKp/n	16	I	0.8V	156.25 MHz differential reference clock for the BlackhawkCore. The BC*REFCLK internal connection are different between A0 and B0 devices and the difference does not affect the device functionality. The BC*REFCLK definition are as follows: BC_A_REFCLK: BC1-2_PLL0_REFCLK(A0), BC3-4_PLL1_REFCLK(B0). BC_B_REFCLK: BC5-6_PLL0_REFCLK(A0), BC3-4_PLL0_REFCLK(B0). BC_C_REFCLK: BC9-10_PLL0_REFCLK(A0), BC11-12_PLL0_REFCLK(B0). BC_D_REFCLK: BC13-14_PLL0_REFCLK(A0), BC11-12_PLL1_REFCLK(B0). BC_E_REFCLK: BC17-18_PLL0_REFCLK(A0), BC19-20_PLL1_REFCLK(B0). BC_F_REFCLK: BC21-22_PLL0_REFCLK(A0), BC19-20_PLL0_REFCLK(B0). BC_G_REFCLK: BC25-26_PLL0_REFCLK(A0), BC27-28_PLL1_REFCLK(B0). BC_H_REFCLK: BC29-30_PLL0_REFCLK(A0), BC27-28_PLL0_REFCLK(B0). Refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for external AC-coupling capacitor and termination resistor requirements.
MGMT_REFCLKp/n	2	I	0.8V	156.25 MHz differential reference clock for the MerlinCore. Refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for external AC-coupling capacitor and termination resistor requirements.
Subtotal	22	—	—	—
Optional Clocks				
BS_PLL0_FREFp/n	2	I	1.8V	12.8 MHz, 20 MHz, 25 MHz, 32 MHz, or 50 MHz differential reference clock used for the BroadSync0 logic. When this clock is not supplied, the device can be configured to use a buffered version of the 50 MHz reference clock supplied via the CORE_PLL_FREFp/n inputs. Refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for external AC-coupling capacitor and termination resistor requirements.

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
BS_PLL1_FREFp/n	2	I	1.8V	12.8 MHz, 20 MHz, 25 MHz, 32 MHz, or 50 MHz differential reference clock used for the BroadSync1 logic. When this clock is not supplied, the device can be configured to use a buffered version of the 50 MHz reference clock supplied via the CORE_PLL_FREFp/n inputs. Refer to *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for external AC-coupling capacitor and termination resistor requirements.
TS_PLL_FREFp/n	2	I	1.8V	25 MHz or 50 MHz differential reference clock used for the TimeSync logic. When this clock is not supplied, the device can be configured to use a buffered version of the 50 MHz reference clock supplied by the CORE_PLL_FREFp/n inputs. Refer to *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for external AC-coupling capacitor and termination resistor requirements.
Subtotal	6	—	—	—
Strap Signals				
PCIE_FORCE_GEN[1:0]	2	I_{PD}	3.3	Selects the maximum operating rate of the PCI Express interface: ■ 2'b00: Interface can operate at PCI Express Gen1, Gen2, or Gen3 speeds. ■ 2'b01: Interface can operate at PCI Express Gen1 speed. ■ 2'b10: Interface can operate at PCI Express Gen1 or Gen2 speeds. ■ (Others): Reserved. **NOTE:** When the PCI Express interface is configured to support Gen3 speeds, it is a requirement that the MHOST0_BOOT_DEV strap signal is pulled high, the BOOT_DEV[2:0] signals are all pulled low, and a QSPI flash memory is connected to the IP_QSPI interface and contains the PCIe Gen3 microcode
PCIE_FORCE_LANE[1:0]	2	I_{PD}	3.3	Selects the maximum link width of the PCI Express interface: ■ 2'b00: Interface can operate at x1, x2, or x4 link widths. ■ 2'b01: Interface can operate at x1 link width only. ■ 2'b10: Interface can operate at x1 or x2 link widths. ■ (others): Reserved.
MHOST0_BOOT_DEV	1	I_{PD}	3.3V	Selects the way that mHost0 (the first internal ARM R5) is brought out of reset: ■ 1'b0: mHost0 is held in reset. ■ 1'b1: mHost0 comes out of reset and begins executing code based on the setting of the BOOT_DEV[2:0] strap signals. **NOTE:** This signal must be pulled high.
MHOST1_BOOT_DEV	1	I_{PD}	3.3V	Selects the way that mHost1 is brought out of reset: ■ 0: Tightly Coupled Memory or TCM in iProc (default). ■ 1: Boot ROM inside iProc (reserved).

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
BOOT_DEV[2:0]	3	I_{PD}	3.3V	Selects the boot flow for mHost0 (the first internal ARM R5): ■ 3'b000: Load all necessary code from QSPI flash attached to IP_QSPI interface and begin execution. ■ (others): Reserved. **NOTE:** It is a requirement that these signals are set to 3'b000.
QSPI_4BYTE_ADDR	1	I_{PD}	3.3V	Selects the operating mode of the QSPI flash device connected to the IP_QSPI interface: ■ 1'b0: QSPI flash is operating in 3 byte address mode. ■ 1'b1: QSPI flash is operating in 4 byte address mode.
IP_QSPI_ADDR_BPC_MODE	1	I_{PD}	3.3V	Selects the mode that is used for sending commands and addresses to the QSPI flash device connected to the IP_QSPI interface: ■ 1'b0: Commands and addresses are sent serially, data is sent in parallel. ■ 1'b1: Commands, addresses, and data are sent in parallel.
IP_QSPI_DUAL_LANE	1	I_{PD}	3.3V	Selects the IP_QSPI interface's operating mode: ■ 1'b0: IP_QSPI interface operates using a serial interface. ■ 1'b1: IP_QSPI interface operates using a two bit parallel interface. **NOTE:** If this signal is pulled high, the IP_QSPI_QUAD_LANE signal must be pulled low.
IP_QSPI_QUAD_LANE	1	I_{PD}	3.3V	Selects the IP_QSPI interface's operating mode: ■ 1'b0: IP_QSPI interface operates using a serial interface. ■ 1'b1: IP_QSPI interface operates using a four bit parallel interface. **NOTE:** If this signal is pulled high, the IP_QSPI_DUAL_LANE signal must be pulled low.
Subtotal	13	—	—	—
PCIe Interface				
PCIe_RDn[3:0]	4	I	0.8V	PCI Express receive serial data. Four-lanes of 2.5 Gb/s or 5 Gb/s differential interface negative leg of lanes 3, 2, 1 and 0.
PCIe_RDp[3:0]	4	I	0.8V	PCI Express receive serial data. Four-lanes 2.5 Gb/s or 5 Gb/s differential interface positive leg of lanes 3, 2, 1, and 0.
PCIe_TDn[3:0]	4	O	0.8V	PCI Express transmit serial data. Four-lanes 2.5 Gb/s or 5 Gb/s differential interface negative leg of lanes 3, 2, 1, and 0.
PCIe_TDp[3:0]	4	O	0.8V	PCI Express transmit serial data. Four-lanes 2.5 Gb/s or 5 Gb/s differential interface positive leg of lanes 3, 2, 1, and 0.
PCIe_PERST_L	1	I_{PU}	3.3	PCIe reset signal. Connect this pin to PCIe_PERST_L from root complex.

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
PCIe_WAKE_L	1	O_{OD}	3.3	Bidirectional Open Drain, active-low PCI Express interface wake signal. Need external pull-up.
Subtotal	18	—	—	—
JTAG Signals				
JTRST_L	1	I_{PU}	3.3V	JTAG test controller reset (active low). When asserted, the test controller is held in reset. This signal should be made accessible for JTAG debugging. For normal operation, this signal should be pulled low.
JTCE[1:0]	2	I_{PD}	3.3V	JTAG test controller enable: ■ 2'b0x: Functional mode / ARM R5 debug mode. ■ 2'b10: Non-functional mode / Logicvision TAP mode. ■ (others): Reserved. These signals should be brought to pads with the ability to stuff a pull up resistor. These resistors should not be stuffed for normal operation.
JTCK	1	I_{PD}	3.3V	JTAG test clock.
JTDI	1	I_{PU}	3.3V	JTAG test data in.
JTDO	1	O	3.3V	JTAG test data out.
JTMS	1	I_{PU}	3.3V	JTAG test mode select.
Subtotal	7	—	—	—
BSC Signals				
IP_BSC[1:0]_SCL	2	B_{OD}	3.3V	Broadcom Serial Controller interface clocks (100 kHz/400 kHz). These interfaces can only function as master interfaces. These signals requires an external pull-up to 3.3V, even if the interface is unused.
IP_BSC[1:0]_SDA	2	B_{OD}	3.3V	Broadcom Serial Controller interface data. These interfaces only function as master interfaces. These signals requires an external pull-up to 3.3V, even if the interface is unused.
IP_BSC2_SCL	1	B_{OD}	3.3V	Broadcom Serial Controller interface clock. This interface only function as a slave interface. This signal requires an external pull-up to 3.3V, even if the interface is unused.
IP_BSC2_SDA	1	B_{OD}	3.3V	Broadcom Serial Controller interface data. This interface only function as a slave interface. This signal requires an external pull-up to 3.3V, even if the interface is unused.
BSC_SA[1:0]	2	B_{OD}	3.3V	Broadcom Serial Controller interface slave address selects the lower two bits of the BSC slave address used on the BSC2 interface.
Subtotal	8	—	—	—

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
LED Interface				
IP_LED[4:0]_CLK	5	O_{PD}	3.3V	Clocks for serial bit streams for port status LEDs. Each clock corresponds to the associated IP_LED[4:0]_DATA data signal. Port status information is all brought to a common microcontroller which can then choose which IP_LED[4:0] interfaces to drive for full flexibility.
IP_LED[4:0]_DATA	5	O_{PD}	3.3V	Data signals for serial bit streams for port status LEDs. Each data signal corresponds to the associated IP_LED[4:0]_CLK clock. Port status information is all brought to a common microcontroller which can then choose which IP_LED[4:0] interfaces to drive for full flexibility.
Subtotal	10	—	—	—
Network Timing Signals				
IP_BS[1:0]_CLK	2	B_{PD}	3.3V	BroadSync clocks. Synchronizes time code data transfer with the associated IP_BS[1:0]_HB and IP_BS[1:0]_TC signals. When configured as outputs, the BroadSync heartbeat and time code signals are driven off the rising edge of the bit clock. When configured as inputs, the heartbeat and time code signals are sampled off the negative edge of the bit clock.
IP_BS[1:0]_HB	2	B_{PD}	3.3V	BroadSync heartbeat clock that signals start of the synchronized time value transmission. Each signal is configurable as an output or an input via a register. When configured as output, this signal is driven off the rising edge of the bit clock. When configured as input, this signal is sampled off the negative edge of the bit clock.
IP_BS[1:0]_TC	2	B_{PD}	3.3V	BroadSync synchronized time code. Serially shifts time value, one bit per rising edge of bit clock. Each signal is configurable as an output or an input via a register. When configured as output, this signal is driven off the rising edge of the bit clock. When configured as input, this signal is sampled off the negative edge of the bit clock.

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
IP_TS_GPIO[5:0]	6	B_{PU}	3.3V	General-purpose I/O signals with the ability to trigger internal timestamp capture in input mode or be automatically controlled by the TimeSync logic in output mode. These signals can also be configured as general-purpose outputs or inputs (with interrupt generation capability). When configured as an input, a weak internal pull-up or pull-down resistor can be enabled. By default, these signals are configured as inputs with an internal pull-up resistor enabled. These signals return to the default state when the SYS_RST_N signal is asserted.
L1_RCVRD_CLK	1	O	3.3V	Primary recovered clock from a user-selectable Ethernet SerDes receiver. This is primarily used to enable L1 clock synchronization. The output clock frequency is user configurable through a fractional divider and supports frequencies from 25 MHz to 156.25 MHz.
L1_RCVRD_CLK_VALID	1	O	3.3V	Status signal associated with the L1_RCVRD_CLK clock output. When this signal is high, it is an indication that the output clock is valid and is usable. When this signal is low, the output clock should not be used.
L1_RCVRD_CLK_BKUP	1	O	3.3V	Secondary recovered clock from a user-selectable Ethernet SerDes receiver. This is primarily used to enable L1 clock synchronization. The output clock frequency is user configurable through a fractional divider and supports frequencies from 25 MHz to 156.25 MHz.
L1_RCVRD_CLK_VALID_BKUP	1	O	3.3V	Status signal associated with the L1_RCVRD_CLK_BKUP clock output. When this signal is high, it is an indication that the output clock is valid and is usable. When this signal is low, the output clock should not be used.
Subtotal	16	—	—	—
General-Purpose I/Os				
IP_G_GPIO[9:0]	10	B_{PU}	3.3V	General-purpose I/O signals. These signals can be configured as outputs or inputs (with interrupt generation capability). When configured as an input, a weak internal pull-up or pull-down resistor can be enabled. By default, these signals are configured as inputs with an internal pull-up resistor enabled. These signals are reset back to inputs upon the assertion of the SYS_RST_L signal.
Subtotal	10	—	—	—

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
QSPI Signals				
IP_QSPI_CS_L	1	O	3.3V	QSPI slave select (active low).
IP_QSPI_HOLD_L	1	B_{PD}	3.3V	When the QSPI interface is operating in single- or dual-lane mode, this is the QSPI pause active low output signal. When operating in quad-lane mode, this is a bidirectional signal used as DQ[3].
IP_QSPI_MISO	1	B_{PD}	3.3V	When the QSPI interface is operating in single-lane mode, this is the serial input from the slave. When operating in dual- or quad-lane mode, this is a bidirectional signal used as DQ[1]. **NOTE:** The QSPI interface only supports operating as a master.
IP_QSPI_MOSI	1	B_{PD}	3.3V	When the QSPI interface is operating in single-lane mode, this is the serial output to the slave. When operating in dual- or quad-lane mode, this is a bidirectional signal used as DQ[0]. **NOTE:** The QSPI interface only supports operating as a master.
IP_QSPI_SCK	1	O	3.3V	QSPI clock.
IP_QSPI_WP_L	1	B_{PD}	3.3V	When the QSPI interface is operating in single- or dual-lane mode, this is the QSPI write protect active low output signal. When operating in quad-lane mode this is a bidirectional signal used as DQ[2].
Subtotal	6	—	—	—
SPI Signals				
IP_SPI0_SCK	1	B_{PU}	3.3V	SPI serial clock.
IP_SPI0_MISO	1	B_{PU}	3.3V	SPI serial input from the slave. **NOTE:** The SPI interface only supports operating as a master.
IP_SPI0_MOSI	1	B_{PU}	3.3V	SPI serial output to the slave. **NOTE:** The SPI interface only supports operating as a master.
IP_SPI0_SS_L	1	B_{PU}	3.3V	SPI slave select (active low).
Subtotal	4	—	—	—
UART Signals				
IP_UART0_CTS_L	1	I_{PU}	3.3V	Active low, Clear to Send signal used by first general-purpose UART.
IP_UART0_SIN	1	I_{PD}	3.3V	Serial input used by first general-purpose UART.
IP_UART0_RTS_L	1	O	3.3V	Active low, Request to Send signal used by first general-purpose UART.
IP_UART0_SOUT	1	O	3.3V	Serial output used by first general-purpose UART.

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
IP_UART1_SIN	1	I_{PD}	3.3V	Serial input used by second general-purpose UART.
IP_UART1_SOUT	1	O	3.3V	Serial output used by second general-purpose UART.
IP_UART2_CTS_L	1	I_{PU}	3.3V	Active low, Clear to Send signal used by the UART dedicated to mHost0 (the first internal ARM R5).
IP_UART2_SIN	1	I_{PD}	3.3V	Serial input used by the UART dedicated to mHost0 (the first internal ARM R5).
IP_UART2_RTS_L	1	O	3.3V	Active low, Request to Send signal used by the UART dedicated to mHost0 (the first internal ARM R5).
IP_UART2_SOUT	1	O	3.3V	Serial output used by the UART dedicated to mHost0 (the first internal ARM R5).
IP_UART3_CTS_L	1	I_{PU}	3.3V	Active low, Clear to Send signal used by the UART dedicated to mHost1 (the second internal ARM R5).
IP_UART3_SIN	1	I_{PD}	3.3V	Serial input used by the UART dedicated to mHost1 (the second internal ARM R5).
IP_UART3_RTS_L	1	O	3.3V	Active low, Request to Send signal used by the UART dedicated to mHost1 (the second internal ARM R5).
IP_UART3_SOUT	1	O	3.3V	Serial output used by the UART dedicated to mHost1 (the second internal ARM R5).
Subtotal	14	—	—	—
NOTE: All UART pins/features are for dedicated IEEE 1588 applications only. They do not support generic use.				

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
MIIM Signals				
IP_MDC[11:0]	12	O	1.2V	Serial management clocks for external PHY management. These signals conform to the Clause 45 electrical specification and protocol. Each clock corresponds to the associated IP_MDIO[11:0] signal. An external pull-up resistor on each signal to the IP_VDDO_[2:1] supply is recommended. The internal MDIO to BlackhawkCore, MGMT, and PCIe connection are in the following list. The external PHY mapping can be configured by SDK software. MDIO[0]: BC[0,1,2] MDIO[1]: BC[3,4,5] MDIO[2]: BC[6,7,8] MDIO[3]: BC[9,10,11] MDIO[4]: BC[12,13,14] MDIO[5]: BC[15,16,17] MDIO[6]: BC[18,19,20] MDIO[7]: BC[21,22,23] MDIO[8]: BC[24,25,26] MDIO[9]: BC[27,28,29] MDIO[10]: BC[30,31] MDIO[11]: MGMT, PCIe
IP_MDIO[11:0]	12	B_{OD}	1.2V	Serial management clocks for external PHY management. These signals conform to the Clause 45 electrical specification and protocol. An external pull-up resistor on each signal to the IP_VDDO_[2:1] supply is recommended.
Subtotal	24	—	—	—
BlackhawkCore Signals				
BC[31:0]_RD[7:0]p/n	512	I	0.8V	BlackhawkCore[31:0] lane [7:0] receive differential pair.
BC[31:0]_TD[7:0]p/n	512	O	0.8V	BlackhawkCore[31:0] lane [7:0] transmit differential pair.
Subtotal	1024	—	—	—
MerlinCore Signals				
MGMT_RD[3:0]p/n	8	I	0.8V	MerlinCore lane [3:0] receive differential pair.
MGMT_TD[3:0]p/n	8	O	0.8V	MerlinCore lane [3:0] transmit differential pair.
Subtotal	16	—	—	—

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
Miscellaneous Signals				
TESTIO[55:0]	56	I	3.3V	TESTIO pins.
NC_ORIENTATION_CHECK	1	—	—	No connect.
Subtotal	57	—	—	—
Test/Reserved Signals				
BC0_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC1_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC_[I,J]_PLL[1:0]_REFCLKp/n_RESERVED	4	I	0.8V	Signal should be left unconnected; for factory use only. A0 and B0 device BC_[I,J]_REFCLK definition are as follows: ■ BC_I_REFCLK_p/n_RESERVED: BC3-4_PLL0_REFCLK(A0), BC7_PLL0_REFCLK(B0). ■ BC_J_REFCLK_p/n_RESERVED: BC3-4_PLL1_REFCLK(A0), BC5_PLL1_REFCLK(B0).
BC8-9_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC_[K,L]_PLL[1:0]_REFCLKp/n_RESERVED	4	I	0.8V	Signal should be left unconnected; for factory use only. A0 and B0 device BC_[K,L]_REFCLK definition are as follows: ■ BC_K_REFCLK_p/n_RESERVED: BC11-12_PLL0_REFCLK(A0), BC10_PLL1_REFCLK(B0). ■ BC_L_REFCLK_p/n_RESERVED: BC11-12_PLL1_REFCLK(A0), BC13_PLL1_REFCLK(B0).
BC14-15_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC16-17_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC18-19_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC23_PLL[1:0]_REFCLKp/n_RESERVED	4	I	0.8V	Signal should be left unconnected; for factory use only.
BC26-27_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC30-31_PLL[1:0]_PTESTp/n_RESERVED	4	O	0.8V	Signal should be left unconnected; for factory use only.
BC31_PLL[1:0]_REFCLKp/n_RESERVED	4	I	0.8V	Signal should be left unconnected; for factory use only.
BS_PLL[1:0]_TESTp/n_RESERVED	4	O	1.8V	Signal should be left unconnected; for factory use only.
BYP_OTP_AUTOLOAD_RESERVED	1	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.
CORE_PLL_TESTp/n_RESERVED	2	O	1.8V	Signal should be left unconnected; for factory use only.
DFT_GATING_RESERVED	1	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
GLOBAL_DISABLE_L_RESERVED	1	I_{PU}	3.3V	Signal should be left unconnected; for factory use only.
IDDQ_RESERVED	1	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.
IP_PLL_REFCLKp/n_RESERVED	2	I	1.8V	Signal should be left unconnected; for factory use only.
IP_PLL_TESTp/n_RESERVED	2	O	1.8V	Signal should be left unconnected; for factory use only.
MAX_TEMP_CLK_RESERVED	1	O	3.3V	Signal should be left unconnected; for factory use only.
MGMT_TESTp/n_RESERVED	2	O	0.8V	Signal should be left unconnected; for factory use only.
MIN_TEMP_CLK_RESERVED	1	O	3.3V	Signal should be left unconnected; for factory use only.
OTP_LVM_RESERVED	1	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.
PCIe_TESTp/n_RESERVED	2	O	0.8V	Signal should be left unconnected; for factory use only.
PLL_BYP_RESERVED	1	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.
PP_PLL_FREFKp/n_RESERVED	2	I	1.8V	Signal should be left unconnected; for factory use only.
PP_PLL_TESTp/n_RESERVED	2	O	1.8V	Signal should be left unconnected; for factory use only.
SWCLKTCK_RESERVED	1	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.
SWD_RESERVED	1	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.
TEMPDIODE0_FORCE_p/n_RESERVED	2	O	3.3V	Signal should be left unconnected; for factory use only.
TEMPDIODE1_FORCE_p/n_RESERVED	2	O	3.3V	Signal should be left unconnected; for factory use only.
TESTMODE[3:0]_RESERVED	4	I_{PD}	3.3V	Signal should be left unconnected; for factory use only.
TS_PLL_TESTp/n_RESERVED	2	O	1.8V	Signal should be left unconnected; for factory use only.
TX_OOBFC_CLK_RESERVED	1	O	3.3V	Signal should be left unconnected; for factory use only.
TX_OOBFC_SYNC_RESERVED	1	O	3.3V	Signal should be left unconnected; for factory use only.
TX_OOBFC_DATA_[1:0]_RESERVED	2	O	3.3V	Signal should be left unconnected; for factory use only.
Subtotal	90	—	—	—

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
System Monitoring				
AVS_PVTMON_ADC	1	I	various	Input to analog to digital converter in adaptive voltage scaling monitor block. This input can be left unconnected; for factory use only.
AVS_PVTMON_VDAC	1	O	various	Output from digital to analog converter in adaptive voltage scaling monitor block. This output can be left unconnected; for factory use only.
TRVDD0p8_SENSE[3:0]	4	O	various	TRVDD0p8 supply sense output used as a feedback voltage to the voltage regulator module for transmit and receive analog supplies.
VDD_SENSE	1	O	various	Core VDD supply sense output used as a feedback voltage to the voltage regulator module.
GND_SENSE	1	O	various	Core VDD ground sense output used as a ground feedback to the voltage regulator module.
VTMON[3:0]_ADC_VDAC VTMON4_VDAC_ADC	5	B	various	Input/outputs to analog to digital and digital to analog converters in process/ temperature/voltage monitoring blocks. These I/Os can be left unconnected; for factory use only.
VTMON13_VDAC VTMON14_VDAC	2	O	various	Outputs from digital to analog converters in process/temperature/voltage monitoring blocks. These outputs can be left unconnected; for factory use only.
Subtotal	15	—	—	—
Digital Power Supplies				
VDDO33	15	PWR	3.3V	3.3V I/O power. Requires a clean power rail with minimal noise.
VDD18	1	PWR	1.8V	1.8V power. Requires a clean power rail with minimal noise.
IP_VDDO_2	2	PWR	1.2V	IP_VDDO_2: Voltage Setting for MDIO interfaces. Connect IP_VDDO_0 pins to 1.2V.
IP_VDDO_1	2	PWR	1.2V	IP_VDDO_1: Voltage Setting for MDIO interfaces. Connect IP_VDDO_1 pins to1.2V.
IP_VDDO_0	13	PWR	3.3V	3.3V IP_VDDO_0 voltage.
VDD (Programmable)	336	PWR	0.75V-0.90V	Core VDD, can operate at ROV or AVS output setting. Requires a clean programmable voltage rail with minimal noise. Refer to the “Recommended Operating Voltage” section of the *BCM56980 Hardware Design Guidelines* (56980-DG1xx).
Subtotal	369	—	—	—

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
Analog Power Supplies				
BC[63:0]_PVDD0p8	64	PWR	0.8V	Filtered 0.8V voltage source for BlackhawkCore PLL.
MGMT_PVDD0p8	1	PWR	0.8V	Filtered 0.8V voltage source for MerlinCore PLL.
MGMT_TRVDD0p8	4	PWR	0.8V	Filtered 0.8V voltage source for MerlinCore transmitter and receiver.
PCIe_PVDD0p8	1	PWR	0.8V	Filtered 0.8V source for PCIe PLL.
PCIe_VDD0p8	4	PWR	0.8V	Filtered 0.8V source for PCIe transmitter and receiver.
TRVDD0P8_[3:0]	388	PWR	0.8V	Filtered 0.8V voltage source for BlackhawkCore analog transmitter and receiver.
TVDD1P2_[3:0]	66	PWR	1.2V	Filtered 1.2V voltage source for BlackhawkCore analog transmitter.
BS_PLL[1:0]_AVDD1p8	2	PWR	1.8V	Filtered BroadSync 1.8V voltage source.
CORE_PLL_AVDD1p8	1	PWR	1.8V	Filtered Core PLL 1.8V voltage source.
PP_PLL_AVDD1p8	1	PWR	1.8V	Filtered PP PLL 1.8V voltage source.
IP_PLL_AVDD1p8	1	PWR	1.8V	Filtered IP PLL 1.8V voltage source.
TS_PLL_AVDD1p8	1	PWR	1.8V	Filtered TimeSync PLL 1.8V voltage source.

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
BC0_PLL_PVDD1P8 BC1_PLL_PVDD1P8 BC2_PLL_PVDD1P8 BC3_PLL_PVDD1P8 BC4_PLL_PVDD1P8 BC5_PLL_PVDD1P8 BC6_PLL_PVDD1P8 BC7_PLL_PVDD1P8 BC8_PLL_PVDD1P8 BC9_PLL_PVDD1P8 BC10_PLL_PVDD1P8 BC11_PLL_PVDD1P8 BC12_PLL_PVDD1P8 BC13_PLL_PVDD1P8 BC14_PLL_PVDD1P8 BC15_PLL_PVDD1P8 BC16_PLL_PVDD1P8 BC17_PLL_PVDD1P8 BC18_PLL_PVDD1P8 BC19_PLL_PVDD1P8 BC20_PLL_PVDD1P8 BC21_PLL_PVDD1P8 BC22_PLL_PVDD1P8 BC23_PLL_PVDD1P8 BC24_PLL_PVDD1P8 BC25_PLL_PVDD1P8 BC26_PLL_PVDD1P8 BC27_PLL_PVDD1P8 BC28_PLL_PVDD1P8 BC29_PLL_PVDD1P8 BC30_PLL_PVDD1P8 BC31_PLL_PVDD1P8	32	PWR	1.8V	Filtered Blackhawk core PLL 1.8V voltage source.
Subtotal	566	—	—	—

Table 9: Device Signal Descriptions (Continued)

Names	Qty.	I/O	Voltage	Description
Diagnostics/Monitoring Supplies				
AVS_PVTMON_AVDD1p8	1	PWR	1.8V	Filtered AVS monitor 1.8V voltage source.
VTMON0-5_AVDD1p8 VTMON1-2_AVDD1p8 VTMON2-9_AVDD1p8 VTMON3-11_AVDD1p8 VTMON4_AVDD1p8 VTMON6-13_AVDD1p8 VTMON8-14_AVDD1p8 VTMON10_AVDD1p8 VTMON12_AVDD1p8	9	PWR	1.8V	Filtered VT Monitor 1.8V voltage source.
Subtotal	10	—	—	—
Ground				
GND	2020	GND	—	Ground
Subtotal	2020	—	—	—
TOTAL	4344	—	—	—

4.2 BCM56980 Pin List by Ball Number

The pin list and ballout diagram for all devices in the BCM56980 family are provided in spreadsheet form. Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads and Support site. The spreadsheet serves as the official document containing the device's signal mapping. Refer to *BCM56980_ballout_revxx* (see Related Documents).

4.3 Device Differences

The following table shows which ports are enabled for devices in the BCM56980 device family.

Table 10: BCM56980, BCM56982, BCM56983, and BCM56984 Differences

P/N	BCM56980/BCM56984	BCM56982	BCM56983
BlackhawkCore0	Enable	Disable	Enable
BlackhawkCore1	Enable	Disable	Enable
BlackhawkCore2	Enable	Enable	Enable
BlackhawkCore3	Enable	Enable	Enable
BlackhawkCore4	Enable	Enable	Enable
BlackhawkCore5	Enable	Enable	Enable
BlackhawkCore6	Enable	Enable	Enable
BlackhawkCore7	Enable	Disable	Enable
BlackhawkCore8	Enable	Disable	Disable
BlackhawkCore9	Enable	Enable	Disable
BlackhawkCore10	Enable	Enable	Disable
BlackhawkCore11	Enable	Enable	Disable
BlackhawkCore12	Enable	Enable	Disable
BlackhawkCore13	Enable	Enable	Disable
BlackhawkCore14	Enable	Disable	Disable
BlackhawkCore15	Enable	Disable	Disable
BlackhawkCore16	Enable	Disable	Disable
BlackhawkCore17	Enable	Disable	Disable
BlackhawkCore18	Enable	Enable	Disable
BlackhawkCore19	Enable	Enable	Disable
BlackhawkCore20	Enable	Enable	Disable
BlackhawkCore21	Enable	Enable	Disable
BlackhawkCore22	Enable	Enable	Disable
BlackhawkCore23	Enable	Disable	Disable
BlackhawkCore24	Enable	Disable	Enable
BlackhawkCore25	Enable	Enable	Enable
BlackhawkCore26	Enable	Enable	Enable
BlackhawkCore27	Enable	Enable	Enable
BlackhawkCore28	Enable	Enable	Enable
BlackhawkCore29	Enable	Enable	Enable
BlackhawkCore30	Enable	Disable	Enable
BlackhawkCore31	Enable	Disable	Enable

Chapter 5: Electrical Specifications

5.1 Operating Conditions

The following table lists and describes the recommended operation conditions for the BCM56980.

Table 11: Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
0.75V to 0.90V ±3%, AVS core voltage	—	–3%	AVS voltage	+3%	V
0.80V ±3%, analog voltage	—	0.776	0.80	0.824	V
1.2V ±3%, (analog and I/O) voltage	—	1.164	1.2	1.236	V
1.80V ±3%, analog voltage	—	1.746	1.80	1.854	V
1.80V ±3%, digital voltage	—	1.746	1.80	1.854	V
3.30V ±5%, I/O voltage	—	3.135	3.30	3.465	V
Ambient temperature	T_A	0	—	70	°C
Junction temperature	T_J	0	—	110	°C
NOTE: VRM 11.1 compliant Voltage Regulator Module can be controlled through BSC interface or AVS pins to provide the AVS core voltage. VRM must be set to the AVS voltage based on the AVS[7:0] I/O pin or AVS register to power up the device. Refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for details.					

5.2 Absolute Maximum Ratings

The specifications shown in the following table indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect device long-term reliability.

Table 12: Absolute Maximum Ratings

Parameters	Min.	Max.	Units
Supply voltage (3.30V)	–0.3	+3.80	V
Supply voltage (1.80V)	–0.3	+2.07	V
Supply voltage (1.20V)	–0.3	+1.38	V
Supply voltage (Core VDD)	–0.3	+0.98	V
Supply voltage (0.80V)	–0.3	+0.92	V
Storage temperature	–40	+125	°C
Electrostatic Discharge (ESD) (Human Body Model (HBM) per EIA/JS-001-2012)			
■ BC*_TESTP/N_RESERVED	±1000	—	V
■ All other I/Os	±2000	—	V
Electrostatic Discharge (ESD) (Charge Device Model (CDM) per EIA/JESD22-C101F)			
■ BC*_TD[3:0]P/N, FC*_RD[3:0]P/N	±300	—	V
■ BC*_TESTP/N_RESERVED	±250	—	V
■ MGMT_TD[3:0]P/N, MGMT_RD[3:0]P/N, MGMT_TESTP/N_RESERVED	±250	—	V
■ PCIe_TD[3:0]P/N, PCIe_RD[3:0]P/N, PCIe_TESTP/N_RESERVED	±250	—	V
■ All other I/Os	±250	—	V
■ Latch Up (125C)	200	—	mA

5.3 Power-Up and Power-Down Specifications

The device requires a power-up and power-down sequence. Violating the power sequencing requirement can cause latch-up damage. See Section 5.6.1, Reset Timing and *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for additional details.

5.4 Device Power Supply Requirement

Table 13: BCM56980 Maximum Per Rail Current for Power Supply Design

Rail	Supply Name	Voltage	Maximum Power Supply Current (A)
AVS core digital	VDD	0.75-0.90	401.5
1.8V analog	*AVDD1p8	1.8	0.3
1.2V analog	TVDD1p2*	1.2	5.4
0.8V analog PVDD	*PVDD0p8	0.8	11.0
0.8V analog TRVDD	TRVDD0p8*	0.8	68.0
3.3V I/O	VDDO33	3.3	0.3
1.2V MIIM I/O	IP_VDDO*	1.2	0.4
1.8V digital	VDD18	1.8	0.1

NOTE: The maximum per rail current in Table 13 is used to design system power supply. Each supply rail current may not track each other with process variations (that is, analog current goes up while digital current goes down). The maximum system power in Table 14 is used for thermal design calculation.

Table 14: System Thermal Design Maximum Power

Device	Low-Latency Mode System Power[a]	Normal-Latency Mode System Power[a]
BCM56980	365W	350W
BCM56982 (estimated)	265W	—
BCM56983 (estimated)	220W	—
BCM56984 (estimated)	260W	—

a. Low-latency mode is the default mode and uses the maximum internal clocks of 1325 MHz core and 1000 MHz PP. Normal-latency mode reduces the PP clock to 662.5 MHz, while keeping the core clock at 1325 MHz.

NOTE: These maximum power values assume the use of the mandatory AVS feature. Refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx) for AVS details.

Table 15: Per SerDes (Eight Lanes), Per Voltage Rail Maximum Power Numbers

Voltage Rail	Maximum Power (mW)
BlackhawkCore (TVDD1P2)	201
BlackhawkCore (TRVDD0P8) ■ PVDD0P8 ■ TRDD0P8	1974 274 1700
BlackhawkCore (PVDD1P8)	16
MerlinCore (PTRVDD0P8)	180
PCIe SerDes (PVDD0P8 and VDD0P8)	116 (PCIe_PVDD0P8 = 16 mW and PCIe_VDD0P8 = 100 mW) optional
NOTE: It is a design requirement that all SerDes cores must be connected to their specified supply rails. The Broadcom SDK ensures the digital portion of unused SerDes cores are held in reset and the analog portion of the core is placed into a power-down mode. This achieves the desired power savings automatically for unused SerDes cores.	

5.5 DC Characteristics

5.5.1 Standard 3.3V Signals

The specifications shown in the following table apply to all CMOS 3.3V general I/O signals along with synchronous Ethernet interface, BroadSync, UART, GPIO, JTAG, and LED signals, except for BSC and MDIO/MDC.

Table 16: Standard 3.3V Signals

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	0.0	—	+3.63	V
Input low voltage	V_{IL}	0.0	—	0.8	V
Input high voltage	V_{IH}	2.0	—	+3.63	V
Output low voltage	V_{OL}	—	—	0.4	V
Output high voltage	V_{OH}	VDDO33 – 0.4	—	—	V
Pull-up or pull-down resistor	R_p	—	~50	—	kΩ
Output low current	IOL	8.0	—	—	mA
Output high current	IOH	-8.0	—	—	mA

5.5.2 Management Interface

Table 17: MIIM (XG), Clause 45 Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	—	–0.3	—	1.5	V
Input low voltage	V_{IL}	—	–0.3	—	0.36	V
Input high voltage	V_{IH}	—	0.84	—	1.5	V
Output low voltage	V_{OL}	I_{OL} = 100 μA	–0.3	—	0.20	V
Output low current	I_{OL}	V_{OL} = 0.2V	4.0	—	—	mA
Output high voltage	V_{OH}	I_{OH} = –100 μA	1.0	—	1.5	V
Output high current	I_{OH}	V_{OH} = IP_VDDO–0.2V	—	—	–4.0	mA

5.5.3 BSC Interface

Table 18: BSC Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	—	–0.3	—	3.63	V
Input low voltage	V_{IL}	—	–0.3	—	0.8	V
Input high voltage	V_{IH}	—	VDDO33 × 0.7	—	3.63	V
Output low voltage	V_{OL}	I_{OL} = 6 mA	—	—	0.4	V
Output low current	I_{OL}	V_{OL} = 0.4V	6.0	—	—	mA

5.5.4 Reference Clocks

The following two figures apply to all reference clocks in this subsection.

Figure 11: Reference Clock Single Ended DC Parameters

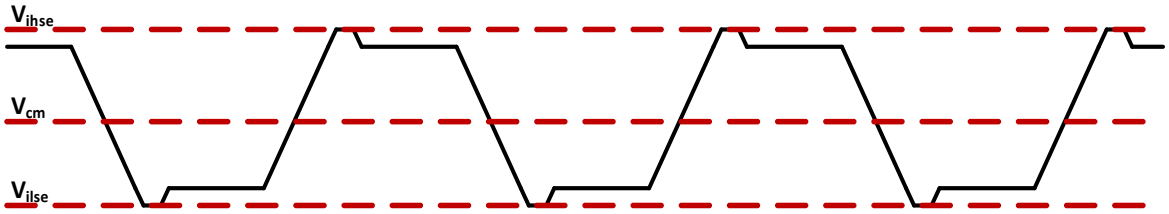
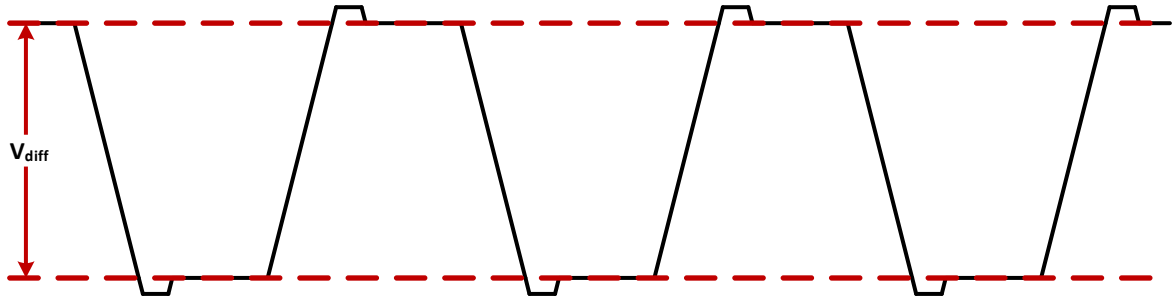


Figure 12: Reference Clock Differential DC Parameters



5.5.4.1 Core PLL Reference Clock (CORE_PLL_FREF)

The core PLL clocks all switching and iProc logic and has the input structure shown in following figure.

Figure 13: Core PLL Input Structure

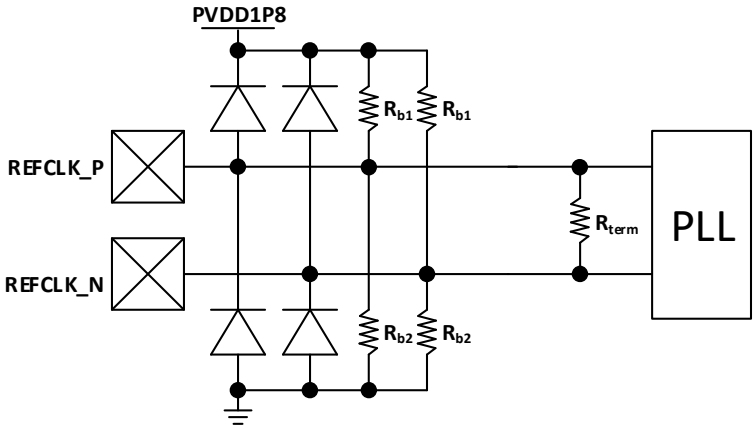


Table 19: Core PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage	V_{cm}	—	900	—	mVse[a]
Single ended swing	V_{ilse} / V_{ihse}	0	—	1800	mVse
Differential swing	V_{diff}	500	—	1800	mVppd[b]
Internal AC coupling[c]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	—	100	—	Ω
Internal bias resistors	R_{b1} / R_{b2}	—	5520	—	Ω

a. mVse denotes mV single-ended.

b. mVppd denotes mV peak-to-peak differential.

c. There is no on-die AC coupling, so external AC coupling is required. The recommended AC coupling capacitor value is 10 nF.

5.5.4.2 TimeSync PLL Reference Clock (TS_PLL_FREF)

The TimeSync PLL clocks the TimeSync and timestamp logic distributed throughout the device. It has the input structure shown in the following figure.

Figure 14: TimeSync PLL Input Structure

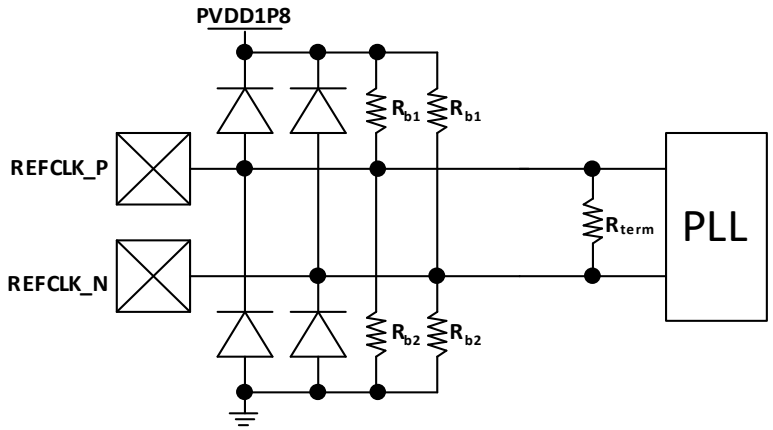


Table 20: TimeSync PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage	V_{cm}	—	900	—	mVse
Single ended swing	V^{ilse} / V_{ihse}	0	—	1800	mVse
Differential swing	V_{diff}	500	—	1800	mVppd
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	—	100	—	Ω
Internal bias resistors	R_{b1} / R_{b2}	—	5520	—	Ω

a. There is no on-die AC coupling, so external AC coupling is required. The recommended AC coupling capacitor value is 10 nF.

5.5.4.3 BroadSync PLL Reference Clocks (BS_PLL0_REFCLK / BS_PLL1_REFCLK)

The BroadSync PLLs clock the associated BroadSync block used to transmit or receive timing information from an external entity. They have the input structure shown in the following figure.

Figure 15: BroadSync PLL Input Structure

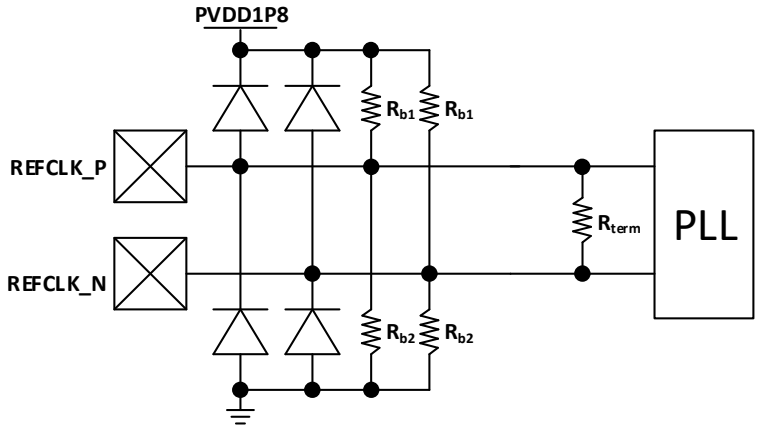


Table 21: BroadSync PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage	V_{cm}	—	900	—	mVse
Single ended swing	V_{ilse} / V_{ihse}	0	—	1800	mVse
Differential swing	V_{diff}	500	—	1800	mVppd
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	—	100	—	Ω
Internal bias resistors	R_{b1} / R_b2	—	5520	—	Ω

a. There is no on-die AC coupling, so external AC coupling is required. The recommended AC coupling capacitor value is 10 nF.

5.5.4.4 PCI Express PLL Reference Clock (PCIe_REFCLK)

The PCI Express PLL clocks the SerDes used for PCI Express connectivity. It has the input structure shown in the following figure.

Figure 16: PCI Express PLL Input Structure

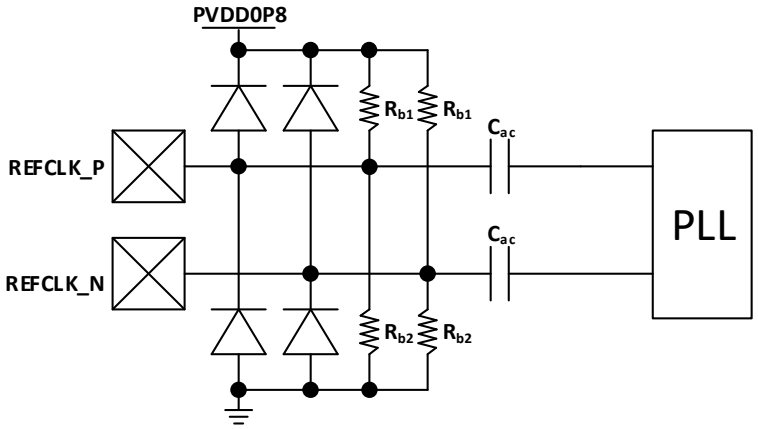


Table 22: PCI Express PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage[a]	V_{cm}	—	400	—	mVse
Single ended swing[b]	V_{ilse} / V_{ihse}	0	—	800	mVse
Differential swing	V_{diff}	600	—	1200	mVppd
Internal AC coupling	C_ac	—	6	—	pF
Internal differential termination	R_{term}	—	—	—	Ω
Internal bias resistors	R_{b1} / R_{b2}	—	6.6	—	kΩ

a. For AC coupled applications, the inputs are internally biased to 400mV. For DC coupled applications, the common mode voltage must be within the specified minimum and maximum values.

b. Maximum overshoot: 300mV (10% of T_high); Minimum undershoot: -300mV (10% of T_low).

5.5.4.5 BlackhawkCore PLL Reference Clocks (BC*_REFCLK)

The BlackhawkCore PLL reference clocks are used to clock all of BlackhawkCore SerDes used for Ethernet connectivity. They have the input structure shown in the following figure.

Figure 17: BlackhawkCore PLL Input Structure

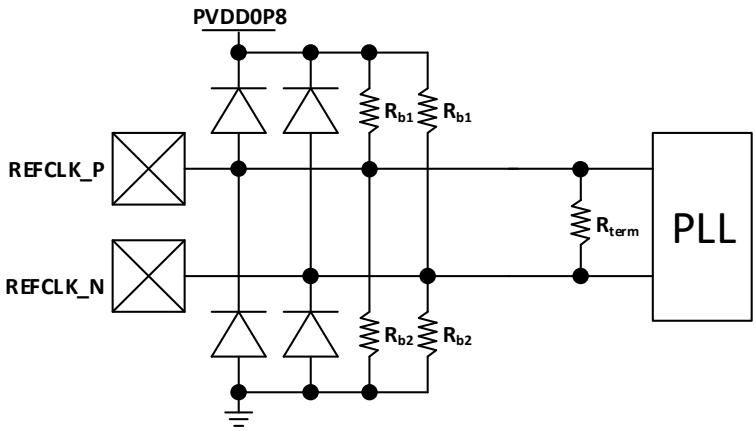


Table 23: BlackhawkCore PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage	V_{cm}	—	400	—	mVse
Single ended swing	V_{ilse} / V_{ihse}	0	—	800	mVse
Differential swing	V_{diff}	800	—	1400	mVppd
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	80	100	120	Ω
Internal bias resistors	R_{b1} / R_{b2}	—	6.6	—	kΩ

a. On-die AC capacitors included for BC*_REFCLK. External AC capacitors are required when the input voltage is > 1.1V.

5.5.4.6 MerlinCore PLL Reference Clock (MGMT_REFCLK)

The MerlinCore PLL reference clock is used to clock the MerlinCore SerDes used for Ethernet connectivity. It has the input structure shown in the following figure.

Figure 18: MerlinCore PLL Input Structure

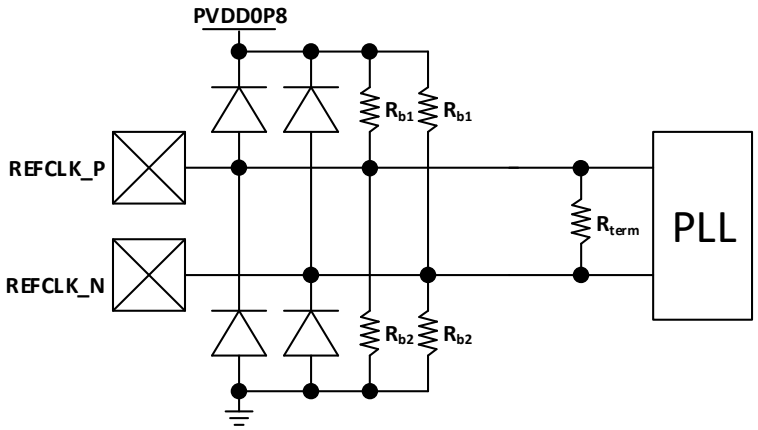


Table 24: MerlinCore PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common mode voltage	V_{cm}	—	400	—	mVse
Single ended swing	V_{ilse} / V_{ihse}	0	—	800	mVse
Differential swing	V_{diff}	300	—	1200	mVppd
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	80	100	120	Ω
Internal bias resistors	R_{b1} / R_{b2}	—	6.6	—	kΩ

a. There is no on-die AC coupling, so external AC coupling is required. The recommended AC coupling capacitor value is 10 nF.

5.5.5 PCIe

Table 25: PCIe DC Characteristics

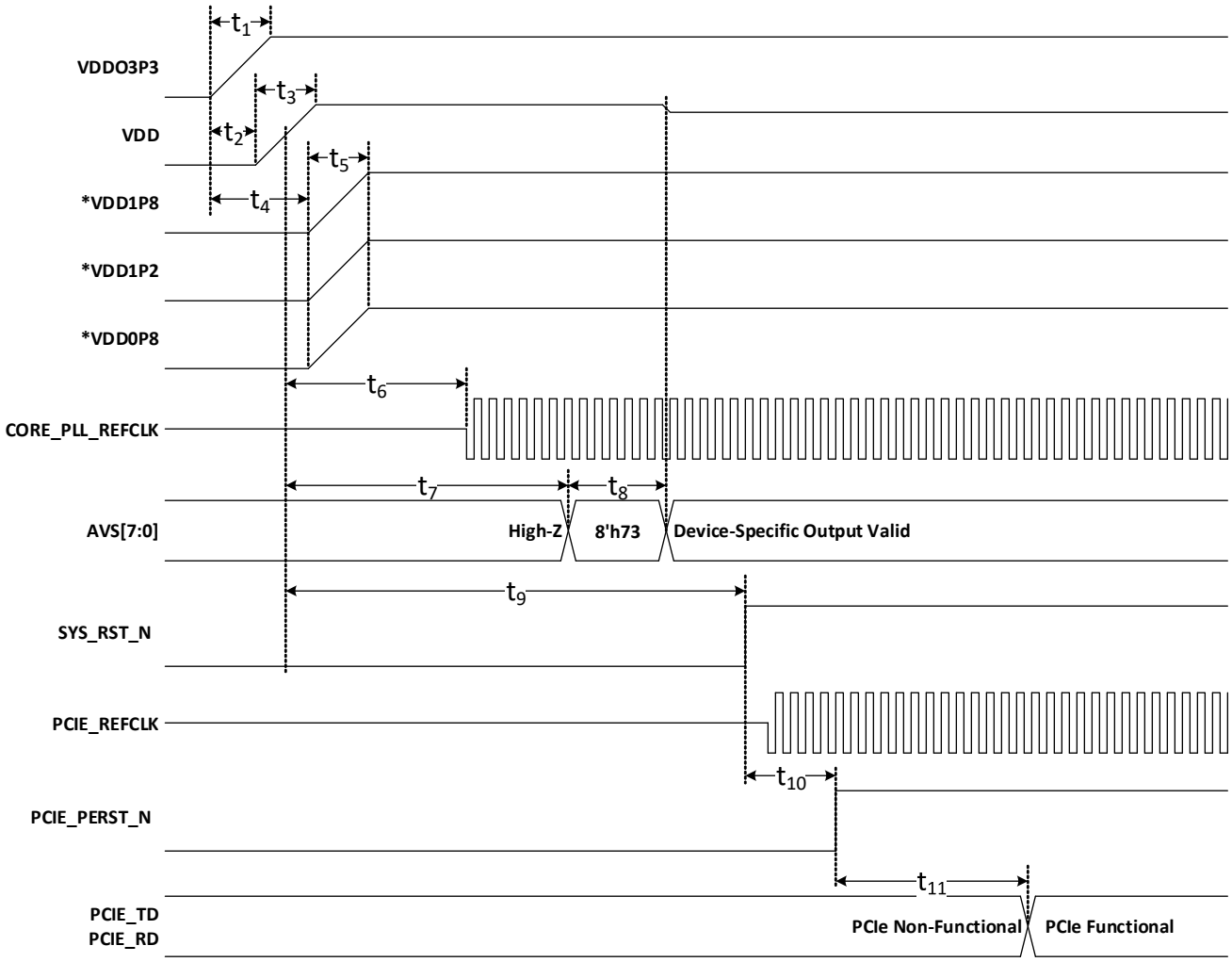
Parameter	Symbol	Min.	Typ.	Max.	Unit
Transmitter					
Output impedance (differential)	R_{OUT}	80	100	120	Ω
Output voltage (differential peak-to-peak)	V_{OD}	400	—	1200	mVp-p
Receiver					
Input impedance (differential)	RIN	80	100	120	Ω
Input voltage (differential peak-to-peak)	VID	100	—	1200	mVp-p

5.6 AC Characteristics

5.6.1 Reset Timing

The following figure illustrates power-up and reset timing.

Figure 19: Power-Up and Reset Timing Diagram



The following table shows power-up and reset timing requirements.

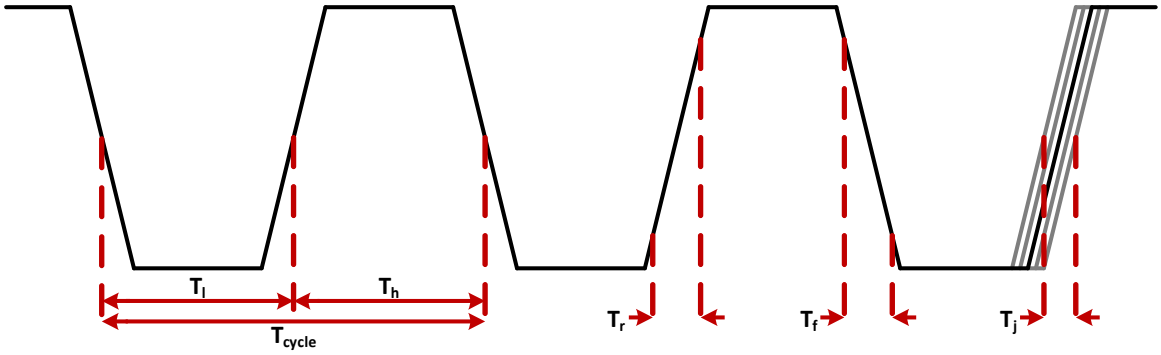
Table 26: Power-Up and Reset Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ramp time for 3.3V supplies	t_1	0.66	—	10	ms
Delay from start of 3.3V ramp to start of VDD supply ramp	t_2	0	—	—	ms
Ramp time for VDD supply	t_3	0.05	—	10	ms
Delay from start of 3.3V ramp to start of 0.8V, 1.2V, and 1.8V supplies ramp	t_4	VDD reaches 0.55V	—	—	—
Time from first supply starting to ramp to last supply finishing ramp.	$t_4 + t_5$	—	—	10	ms
Ramp time for 0.8V, 1.2V, and 1.8V supplies	t_5	0.1	—	10	ms
CORE_PLL_REFCLK is stable	t_6	—	—	12.8	ms
AVS[7:0] transitions to device-independent power-up default of 8'h73	t_7	6.4	12.8	25.6	ms
AVS[7:0] transitions to valid device-specific output	t_8	6.4	12.8	25.6	ms
System reset signal deasserted	t_9	80	—	—	ms
PCIE reset signal deasserted	t_{10}	100	—	—	ms
PCIe interface is functional	t_{11}	—	—	20	ms

5.6.2 Reference Clocks

The following figure applies to all reference clocks in this subsection.

Figure 20: Reference Clock AC Parameters



5.6.2.1 Core PLL Reference Clock (CORE_PLL_FREF)

Table 27: Core PLL Reference Clock AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency (1/Tcycle)	—	—	50	—	MHz
Tolerance	—	–50	—	50	PPM
Duty cycle	T_l / T_h	40	50	60	%
Rise/fall time (20% to 80%)	T_r / T_f	—	—	1	ns/V_{ppd}
RMS Jitter (12 kHz to 20 MHz)	T_j	—	—	10	ps

5.6.2.2 TimeSync PLL Reference Clock (TS_PLL_FREF)

Table 28: TimeSync PLL Reference Clock AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency (1/Tcycle)[a]	—	—	25	—	MHz
Frequency (1/Tcycle)[a]	—	—	50	—	MHz
Tolerance	—	–50	—	50	PPM
Duty cycle	T_l / T_h	40	50	60	%
Rise/fall time (20% to 80%)	T_r / T_f	—	—	1	ns/V_{ppd}
RMS Jitter (12 kHz to 20 MHz)	T_j	—	—	10	ps

a. The Broadcom SDK automatically programs the PLL appropriately for the provided reference clock frequency.

5.6.2.3 BroadSync PLL Reference Clocks (BS_PLL0_FREF / BS_PLL1_FREF)

Table 29: BroadSync PLL Reference Clock AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency (1 / Tcycle)[a]	—	—	12.8	—	MHz
Frequency (1 / Tcycle)[a]	—	—	20	—	MHz
Frequency (1 / Tcycle)[a]	—	—	25	—	MHz
Frequency (1 / Tcycle)[a]	—	—	32	—	MHz
Frequency (1 / Tcycle)[a]	—	—	50	—	MHz
Tolerance	—	–50	—	50	PPM
Duty cycle	T_l / T_h	40	50	60	%
Rise/fall time (20% to 80%)	T_r / T^f	—	—	1	ns/V_{ppd}
RMS Jitter (12 kHz to 20 MHz)	T_j	—	—	10	ps

a. The Broadcom SDK automatically programs the PLL appropriately for the provided reference clock frequency.

5.6.2.4 PCI Express PLL Reference Clock (PCIe_REFCLK)

Table 30: PCI Express PLL Reference Clock AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency (1 / Tcycle)	—	—	100	—	MHz
Tolerance	—	–300	—	300	PPM
Duty cycle	T_l / T_h	40	50	60	%
Rise/fall time (20% to 80%)	T_r / T_f	—	—	0.9	ns
RMS Jitter (10 kHz to 1.5 MHz) (Gen3 – 8 Gb/s)	T_j	—	—	1.0	ps
RMS Jitter (10 kHz to 1.5 MHz) (Gen2 – 5 Gb/s)	T_j	—	—	3.0	ps
RMS jitter (Cycle-to-Cycle) (Gen1 – 2.5 Gb/s)	T_j	—	—	150	ps

5.6.2.5 BlackhawkCore PLL Reference Clocks (BC*_REFCLK)

Table 31: BlackhawkCore PLL Reference Clock AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency (1 / Tcycle)	—	—	156.25	—	MHz
Tolerance	—	–50	—	50	PPM
Duty cycle	T_l / T_h	40	50	60	%
Rise/fall time (20% to 80%)	T_r / T_f	—	0.3	0.5	ns/V_{ppd}
RMS Jitter (12 kHz to 20 MHz)	T_j	—	—	0.3	ps

5.6.2.6 MerlinCore PLL Reference Clocks (MGMT_REFCLK)

Table 32: MerlinCore PLL Reference Clock AC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency (1 / Tcycle)	—	—	156.25	—	MHz
Tolerance	—	–50	—	50	PPM
Duty cycle	T_l / T_h	40	50	60	%
Rise/fall time (20% to 80%)	T_r / T_f	—	—	0.9	ns
RMS Jitter (12 kHz to 20 MHz)	T_j	—	—	0.3	ps

5.6.3 BlackhawkCore (50G) Interface

The device serial interface confirms to IEEE 802.3bs and 802.3cd specifications:

- Octal SerDes block supporting eight serial links.
- Supports line rates from 10.3125 Gb/s to 56.25 Gb/s (PAM4 56.25 Gb/s or NRZ 28.125 Gb/s).
- Includes a 14-tap DFE with adaptive control and VGA with AGC.
- Programmable RX equalizer with 0 to 8 dB boost, approximately 0.5 dB/step.
- Transmitter, 5-tap FIR with precursor, main, and post cursor taps.
- CML driver with 2 × 50Ω internal termination.
- Controlled peak-to-peak amplitude.
- The receiver inputs includes on-die AC caps with a low corner freq, ~70 kHz, and in most cases, an external AC cap is not needed. The main limitation is that the absolute maximum RX input voltage must not exceed 1.1V, and so limits the maximum input Vcm to ~0.9V. The peak amplitude limit should not be exceeded over all PVT and any transient effects, such as reflections and power supply ramps.

5.6.4 MerlinCore (TSC4-M) Interface

The device serial interface supports the following features:

- Quad SerDes block supporting four serial links.
- Supports line rates of 1.25G, up to 12.5 Gbaud per serial link. Oversampling mode is used if the speed is below 2.5G.
- Includes a 5-tap DFE with adaptive control and VGA with AGC.
- Programmable RX equalizer with 0 dB to 8 dB boost, approximately 0.5 dB/step.
- Transmitter with 5-tap FIR.
- SST driver with 2 × 50Ω internal termination.
- Controlled peak-to-peak amplitude.

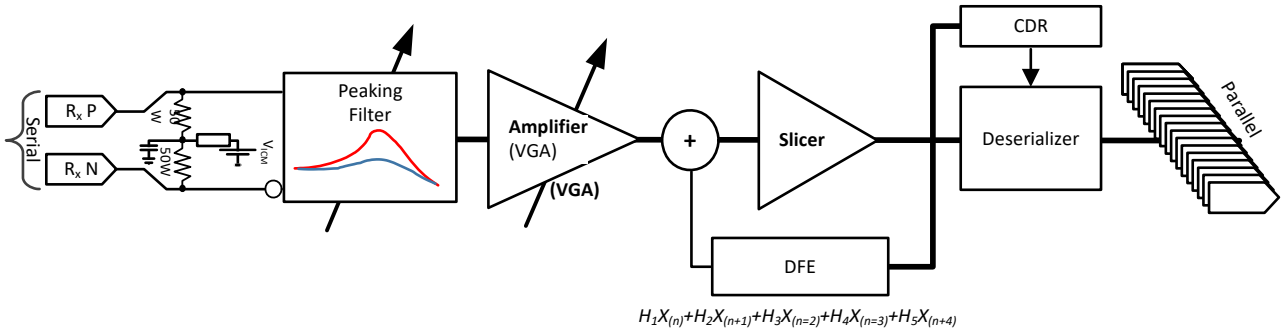
The serial interface operating conditions are shown in the following table and figure.

Table 33: MerlinCore Technology Serial Interface Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud, symbol rate	B_{PS}	1.25	—	12.5	Gbaud
Unit interval	UI	—	97	—	ps

5.6.4.1 MerlinCore Receiver

Figure 21: SerDes Receiver Conceptual Diagram



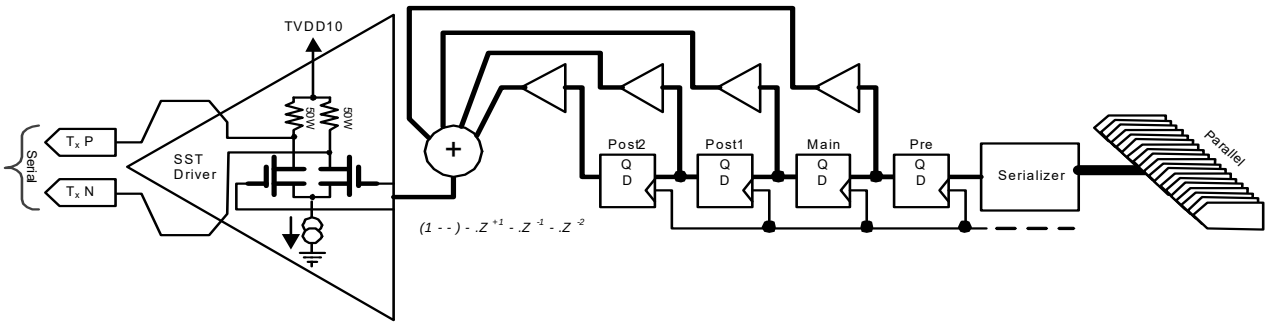
The serial interface receive characteristics are shown in the following table and figure.

Table 34: Serial Interface Receive Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Jitter tolerance	Δt_{RXtot}	Total, peak-to-peak	—	—	0.65	UI
	Δt_{RXdet}	Deterministic, peak-to-peak	—	—	0.42	UI

5.6.4.2 MerlinCore Transmitter

Figure 22: SerDes Transmitter Conceptual Diagram



The serial interface transmit characteristics are shown in the following table.

Table 35: Serial Interface Transmit Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Output voltage fall time	t_{fall}	80% to 20% (based on 10GBASE-KR waveform, 8–1s, 8–0s)	24	—	36	ps
Output voltage rise time	t_{rise}	20% to 80% (based on 10GBASE-KR waveform, 8–1s, 8–0s)	24	—	36	ps
Output differential skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge	—	—	5	ps
Transmit output jitter	Δt_{TXRND}	Random, wideband, RMS	—	0.008	0.130	UI
	Δt_{TXtot}	Total, peak-to-peak	—	—	0.18	UI
	Δt_{TXdet}	Deterministic, peak-to-peak	—	0.05	—	UI

5.6.5 PCIe Interface

5.6.5.1 PCIe Receiver Input

Figure 23: PCIe_RX Timing Diagram

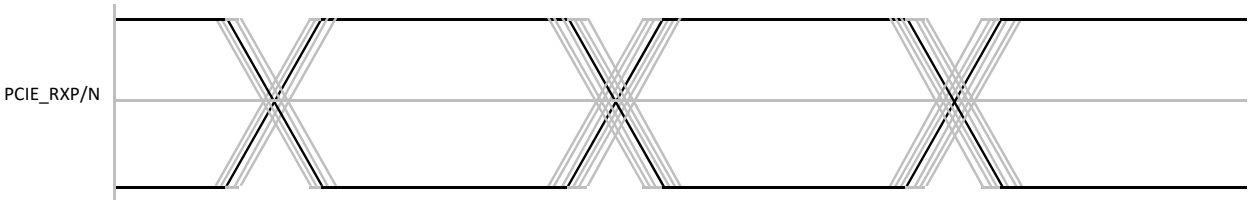


Table 36: PCIe_RX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Baud rate	FREQ	—	2.5, 5.0, or 8.0	—	Gbaud
Minimum RX total jitter	T_J	0.6	—	—	UI
NOTE: Includes on-chip AC coupling capacitors.					

5.6.5.2 PCIe Transmitter Output

Figure 24: PCIe_TX Timing Diagram

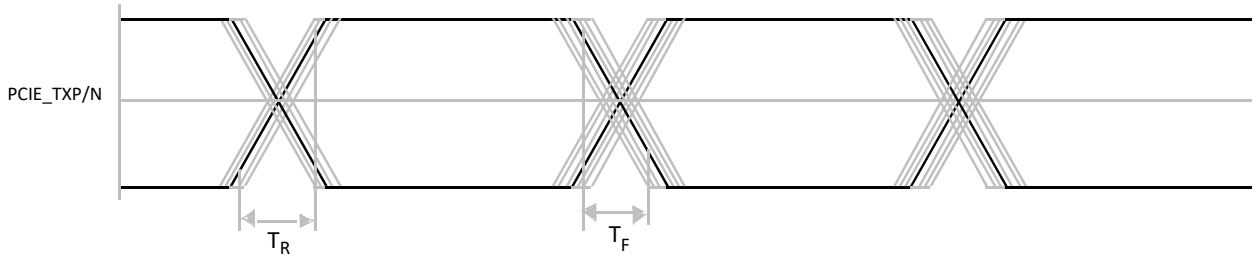


Table 37: PCIe_Transmitter Output Timing

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Baud rate	FREQ	—	—	2.5, 5.0, or 8.0	—	Gbaud
Output rise/fall time (20% to 80%)	T_R/T_F	—	30	—	90	ps
Output deemphasis[a]	V_{OEQ}	Gen1 2.5 Gb/s Gen1 5.0 Gb/s	–3.0 –5.5	–3.5 –6.0	–4.0 –6.5	dB
Minimum TX total jitter	T_J	—	0.75	—	—	UI

a. The output deemphasis values listed in this table are the default settings. TX deemphasis can be software configured in the range of 0 db to 8 dB, overriding the defaults.

5.6.6 BroadSync Interface

The following figure and table show the slave mode input timing.

Figure 25: BroadSync Input Timing – Slave Mode

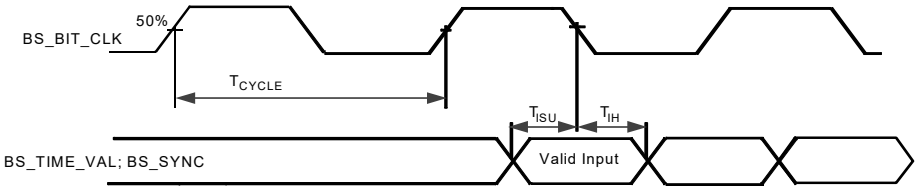


Table 38: BroadSync Input Timing – Slave Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	500	—	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	%
BS_TIME_VAL; BS_SYNC input setup time	t_{ISU}	20	—	—	ns
BS_TIME_VAL; BS_SYNC input hold time	t_{IH}	0	—	—	ns

The following figure and table show the master mode input timing.

Figure 26: BroadSync Output Timing – Master Mode

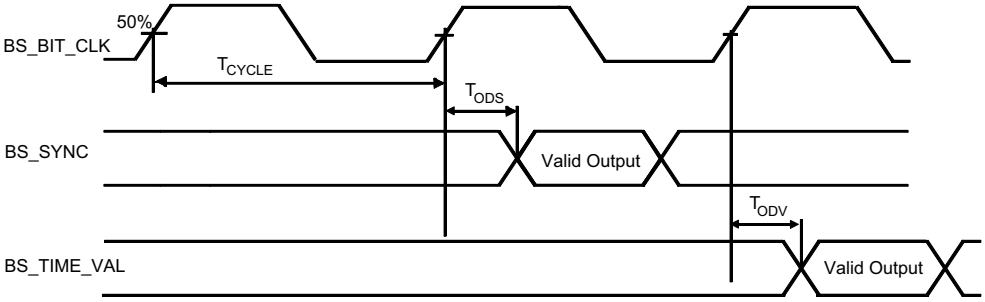


Table 39: BroadSync Output Timing – Master Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	500	—	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	%
BS_SYNC output delay	t_{ODS}	0	—	25	ns
BS_TIME_VAL output delay	t_{ODV}	0	—	25	ns

5.6.7 BSC Interface

The BSC interface can operate in two modes:

- Slave mode
- CPU-controlled master/slave mode

The external master drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

Figure 27: BSC Timing Diagram

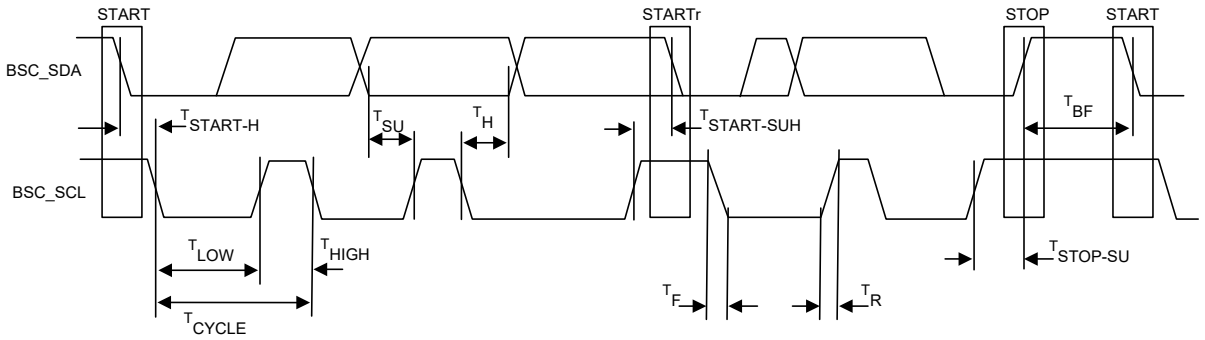


Table 40: BSC Master/Slave Fast-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	400	kHz
BSC_SCL cycle time	T_{CYCLE}	2.5	—	—	µs
BSC_SCL low time	T_{LOW}	1.3	—	—	µs
BSC_SCL high time	T_{HIGH}	0.6	—	—	µs
Data hold time	T_H	0	—	—	µs
Data setup time	T_{SU}	100	—	—	ns
Rise time, clock, and data (see note)	T_R	—	—	300	ns
Fall time, clock, and data (GBD)	T_F	—	—	300	ns
Hold time, start or repeated start	$T_{START–H}$	0.6	—	—	µs
Setup time, repeated start	$T_{START–SU}$	0.6	—	—	µs
Setup time, stop	$T_{STOP–SU}$	0.6	—	—	µs
Bus free time (between stop and start)	T_{BF}	1.3	—	—	µs

Table 41: BSC Master/Slave Standard-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	100	kHz
BSC_SCL cycle time	T_{CYCLE}	10	—	—	µs
BSC_SCL low time	T_{LOW}	4.7	—	—	µs
BSC_SCL high time	T_{HIGH}	4.0	—	—	µs
Data hold time	T_H	0.0	—	—	µs
Data setup time	T_{SU}	250	—	—	ns
Rise time, clock, and data (see note)	T_R	—	—	1000	ns
Fall time, clock, and data (GBD)	T_F	—	—	300	ns
Hold time, start, or repeated start	$T_{START–H}$	4.0	—	—	µs
Setup time, repeated start	$T_{START–SU}$	4.7	—	—	µs
Setup time, stop	$T_{STOP–SU}$	4.0	—	—	µs
Bus free time (between stop and start)	T_{BF}	4.7	—	—	µs

NOTE: BSC_SCL and BSC_SDA are open-drain outputs. The rise time is dependent on the strength of the external pull-up resistor, which must be selected to meet the rise-time requirement.

The device drives the BSC_SCL clock with a programmable speed of 100 kHz or 400 kHz based on the mode bit called MODE_400. The device drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

5.6.8 LED Interface

LED[4:0]_CLK and LED[4:0]_DATA are outputs. The LED[4:0]_CLK output clock period is 200 ns (5.0 MHz).

Figure 28: LED Timing Diagram

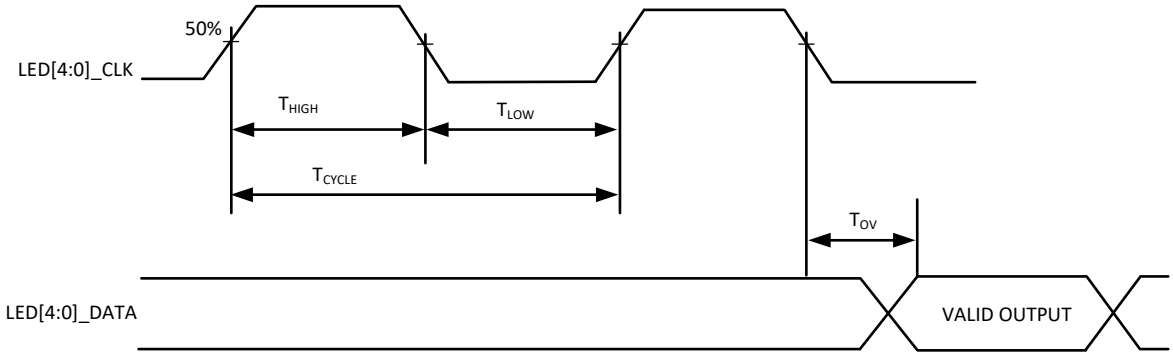


Table 42: LED Timing[a]

Parameter	Symbol	Min.	Typ.	Max.	Unit
LED[4:0]_CLK clock frequency	f_{CLK}	—	5	5	MHz
LED[4:0]_CLK cycle time	T_{CYCLE}	—	200	200	ns
LED[4:0]_CLK high time	T_{HIGH}	70	100	130	ns
LED[4:0]_CLK low time	T_{LOW}	70	100	130	ns
LED[4:0]_DATA output valid time	T_{OV}	0	—	30	ns

a. Timing values are specified at the 50% crossing thresholds.

5.6.9 Management Interface (MIIM)

5.6.9.0.1 MDIO AC Characteristics

Figure 29: MIIM Interface Timing Diagram

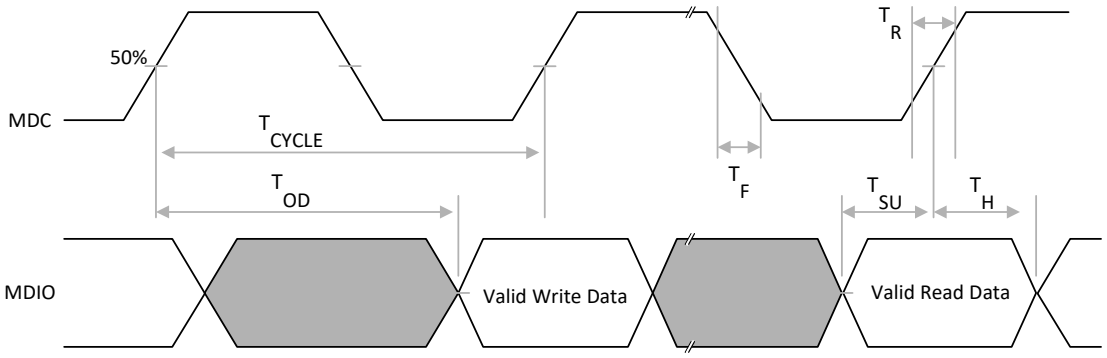


Table 43: 1.2V MDC/MDIO Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
MDC clock frequency	f_{CLK}	—	2.5	12.5	MHz
MDC cycle time	T_{CYCLE}	80	400	—	ns
MDC duty cycle	—	40	—	60	%
MDIO setup time	T_{SU}	20	—	—	ns
MDIO hold time	T_H	0	—	—	ns
MDIO output delay	T_{OD}	10	—	30	ns

NOTE: The following notes apply to MDC/MDIO timing:

- Output load conditions = 25 pF.
- External device to conform to IEEE specifications.
- MDIO output delay is programmable.

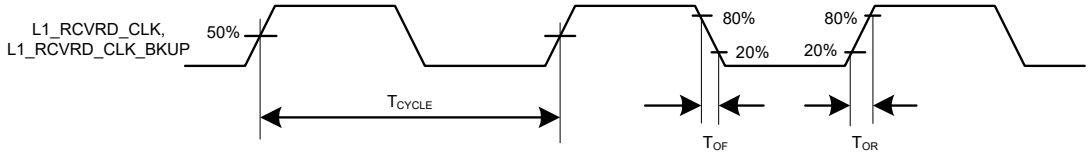
5.6.10 Synchronous Ethernet Interface

5.6.10.1 L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Table 44: L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP cycle time	T_{CYCLE}	6.4	—	40	ns
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP duty cycle	T_{HIGH}	40	—	60	%

Figure 30: Synchronous Ethernet Output Timing Diagram



5.6.11 JTAG Interface

Figure 31: JTAG Timing Diagram

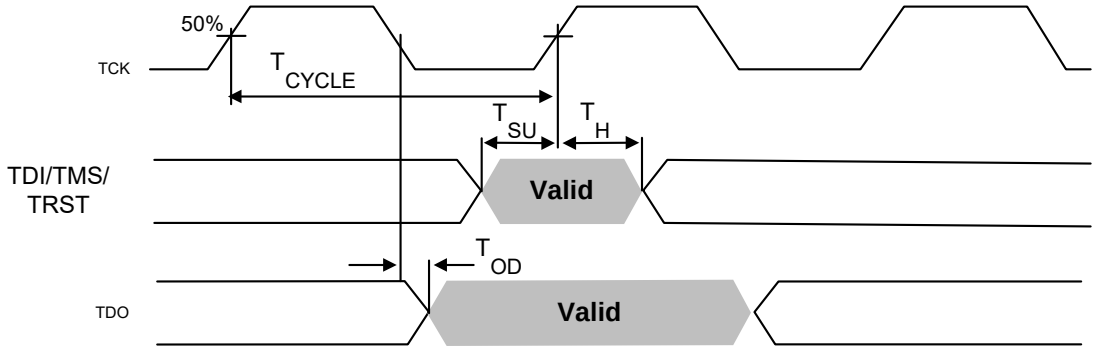


Table 45: JTAG AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
JTCK clock frequency	f_{CLK}	—	—	12.5	MHz
JTCK duty cycle	—	45	—	55	%
JTCK cycle time	t_{CYCLE}	80.0	—	—	ns
JTCK falling edge to output valid Applicable to *JTDO*	t_{OD}	0	—	25	ns
Data input setup time before *JTCK* Applicable to *JTDI and JTMS*	t_{SU_JT}	15	—	—	ns
Data hold time after *JTCK* rise Applicable to *JTDI and JTMS*	t_{H_JT}	5	—	—	ns
Input setup time before *JTCK* rising edge Applicable to *JTRST_N*	t_{SU_JTRS}	15	—	—	ns

Table 45: JTAG AC Characteristics (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input hold time after *JTCK* rising edge Applicable to *JTRST_N*	t_{H_JTRS}	5	—	—	ns
NOTE: Unless otherwise noted, the specifications are valid across the following operating conditions: ■ The threshold value is at 50% of the applicable I/O rail voltage. ■ The default loading on an output is 5 pF.					

5.6.12 QSPI Interface

Figure 32: IP_QSPI Timing (Read/Write Mode Using MSPI Controller)

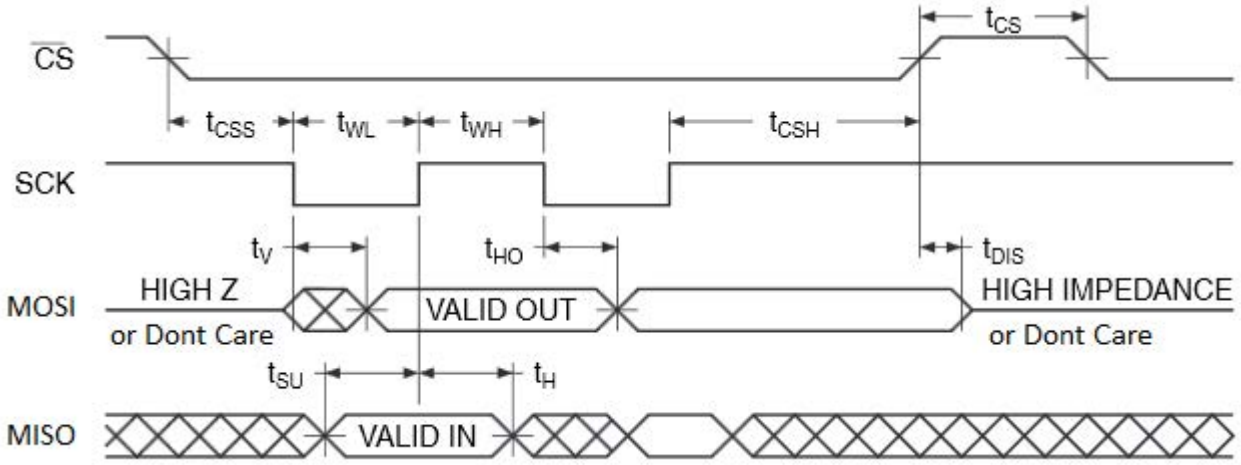
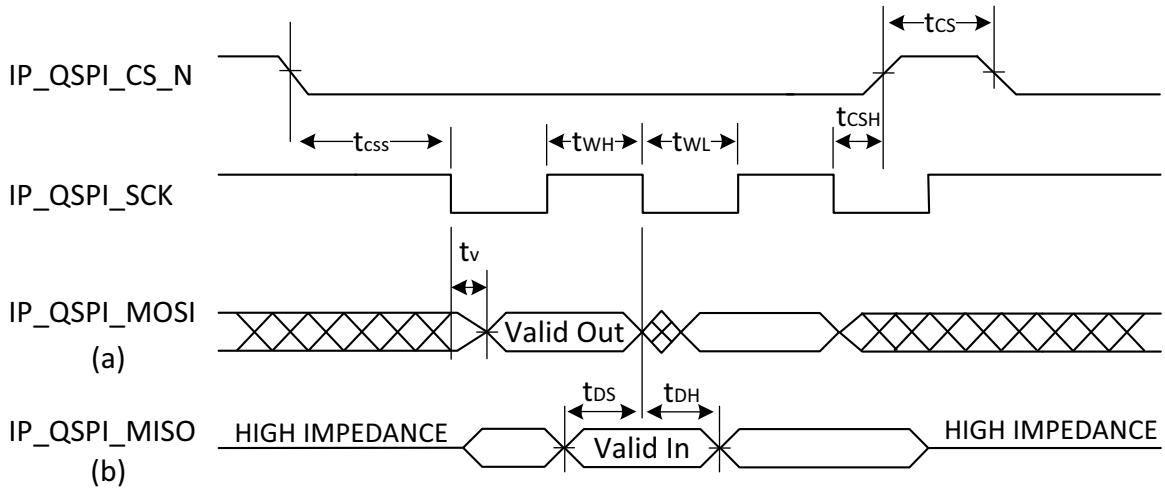


Table 46: IP_QSPI Timing (Read/Write Mode Using MSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	15.625	MHz
SCK Clock LOW period	t_{WL}	0.5/Fsck – 0.5	—	—	ns
SCK Clock HIGH period	t_{WH}	0.5/Fsck – 0.5	—	—	ns
CS lead time	t_{CSS}	0.5/Fsck – 4	—	—	ns
CS trail time	t_{CSH}	9.6	—	—	ns
CS high time	t_{CS}	81	—	—	ns
MOSI output valid	t_V	—	—	11	ns
MOSI output hold	t_{HO}	4	—	—	ns
MISO input setup	t_{SU}	9	—	—	ns
MISO input hold	t_H	2	—	—	ns
MOSI output disable[a]	t_{DIS}	—	—	—	ns

a. The IP_QSPI_MOSI signal is always driven.

Figure 33: IP_QSPI Timing (Boot Read Mode Using BSPI Controller)



a): also valid for IP_QSPI_MISO in dual/quad mode; also valid for IP_QSPI_WP_N, IP_QSPI_HOLD_N in quad mode
b): also valid for IP_QSPI_MOSI in dual/quad mode; also valid for IP_QSPI_WP_N, IP_QSPI_HOLD_N in quad mode

Table 47: IP_QSPI Timing (Boot Read Mode Using BSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	62.5	MHz
SCK clock LOW period	t_{WL}	0.5/Fsck – 0.5	—	—	ns
SCK clock HIGH period	t_{WH}	0.5/Fsck – 0.5	—	—	ns
CS lead time	t_{CSS}	1/Fsck – 2.9	—	—	ns
CS trail time	t_{CSH}	–1.6	—	—	ns
MOSI output valid	t_V	–1.6	—	3	ns
MISO input setup	t_{SU}	4	—	—	ns
MISO input hold	t_H	1	—	—	ns

5.6.13 SPI Interface

Figure 34: IP_SPI Timing (SPI Master – Mode 0)

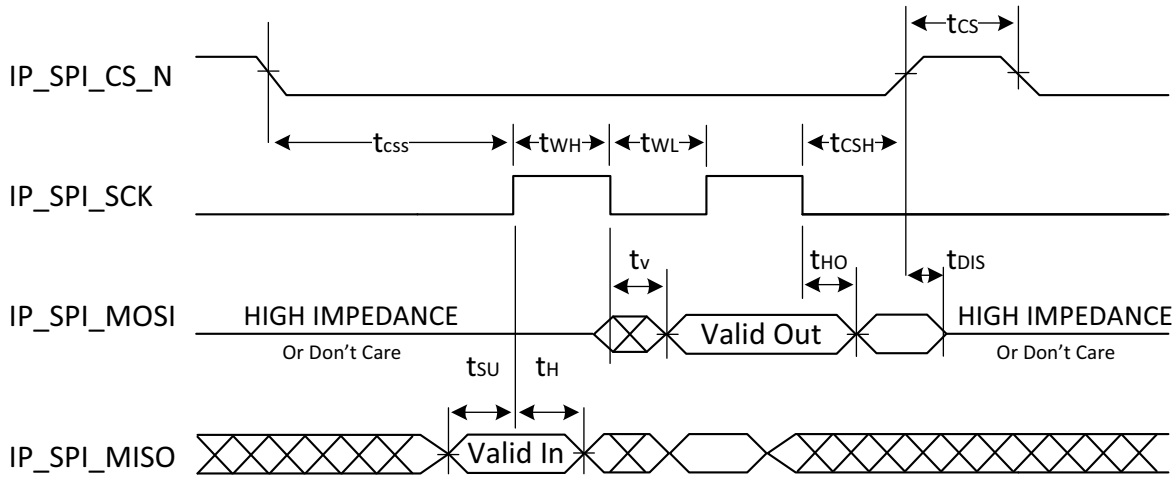


Figure 35: IP_SPI Timing (SPI Master – Mode 3)

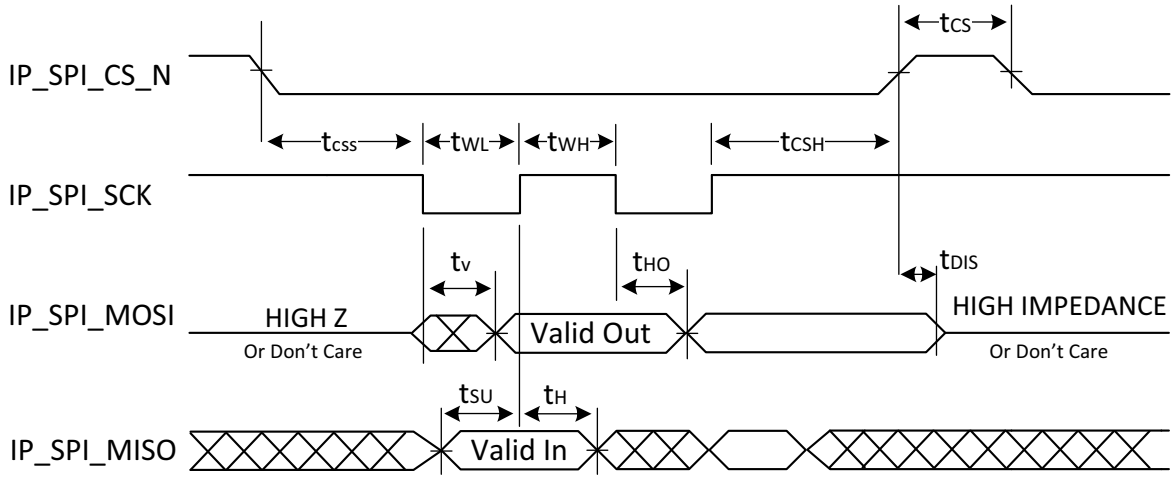


Table 48: IP_SPI Timing (Master Mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK Frequency	F_{SCK}	—	—	26.78	MHz
SCK Clock LOW period	t_{WL}	0.5/Fsck – 1	—	—	ns
SCK Clock HIGH period	t_{WH}	0.5/Fsck – 1	—	—	ns
CS lead time	t_{CSS}	0.5/Fsck – 4	—	—	ns
CS trail time	t_{CSH}	0.5/Fsck – 4	—	—	ns
CS high time (SPH = 0)	t_{CS}	0.5/Fsck	—	—	ns
CS high time (SPH = 1)	t_{CS}	0	—	—	ns

Table 48: IP_SPI Timing (Master Mode) (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MOSI output valid	t_V	—	—	4	ns
MOSI output hold	t_{HO}	–4	—	—	ns
MISO input setup	t_{SU}	—	—	9	ns
MISO input hold	t_H	0	—	—	ns
MOSI output disable	t_{DIS}	—	—	4	ns

Chapter 6: Standard Electrical Characteristics

6.1 PAM4 Electrical Characteristics

The device is designed in compliance with CEI-56G-VSR, CEI-56G-LR, IEEE 802.3bs CDAUI-8 C2C/C2M, and IEEE 802.3cd standards.

6.2 40G XLAUI Electrical Characteristics

6.2.1 Transmitter

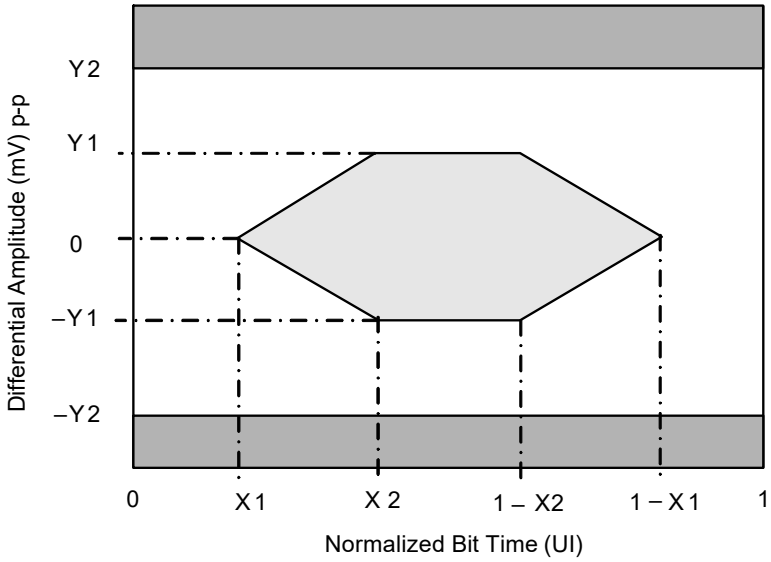
Table 49: XLAUI TX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Output speed per lane	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Differential output voltage (peak-to-peak)	VOD	—	—	760	mVp-p
Transmit eye mask (Figure 36)	X1	—	—	0.16	UI
Transmit eye mask (Figure 36)	X2	—	—	0.38	UI
Transmit eye mask (Figure 36)	Y1	200	—	—	mV
Transmit eye mask (Figure 36)	Y2	—	—	380	mV
Common mode voltage	VCM	—	0.65	—	V
Differential output return loss (minimum)	Equation[a]	—	—	—	δB
Common-mode output return loss (minimum)	Equation[b]	—	—	—	δB
Output rise time (20% to 80%)	Tr	24	—	—	pS
Output fall time (20% to 80%)	Tf	24	—	—	pS
Output jitter at $1e^{-12}$ BER					
Deterministic	sDJ	—	—	0.17	UI
Total	sTJ	—	—	0.32	UI

a. Return loss (f) ≤ 12 dB for 10 MHz ≤ f < 2.125 GHz.
Return loss ≤ [6.5 – 13.33 log (f/5.5)] dB for 2.125 GHz ≤ f ≤ 11.1 GHz.

b. Return loss (f) ≤ 9 dB for 10 MHz ≤ f < 2.125 GHz.
Return loss ≤ [3.5 – 13.33 log (f/5.5)] dB for 2.125 GHz ≤ f ≤ 7.1 GHz.
Return loss ≤ 2 dB for 7.1 GHz < f < 11.1 GHz.

Figure 36: XLAUI Transmit Eye Mask



6.2.2 Receiver

Table 50: XLAUI RX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Receiver coupling	AC	0.05	—	0.1	µF
Receive eye mask (Figure 37)	X1	—	—	0.31	UI
Receive eye mask (Figure 37)	X2	—	—	0.5	UI
Receive eye mask (Figure 37)	Y1	42.5	—	—	mV
Receive eye mask (Figure 37)	Y2	—	—	425	mV
Differential input return loss	Equation[a]	—	—	—	dB
Common mode input return loss	Equation[b]	—	—	—	dB
Receiving speed per Lane	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Sinusoidal jitter tolerance	Figure 38	—	—	—	bps
Bit error rate based channel characteristics per Clause 83A in IEEE 802.3ba.	—	—	—	1e-12	bps

a. Return loss (f) ≤ 12 dB for 10 MHz ≤ f < 2.125 GHz.
Return loss ≤ [6.5 – 13.33 log (f/5.5)] dB for 2.125 GHz ≤ f ≤ 11.1 GHz, where f is in GHz.

b. Return loss (f) ≤ 15 dB for 10 MHz ≤ f < 11.1 GHz, where f is in GHz.

Figure 37: XLAUI Receive Eye Mask

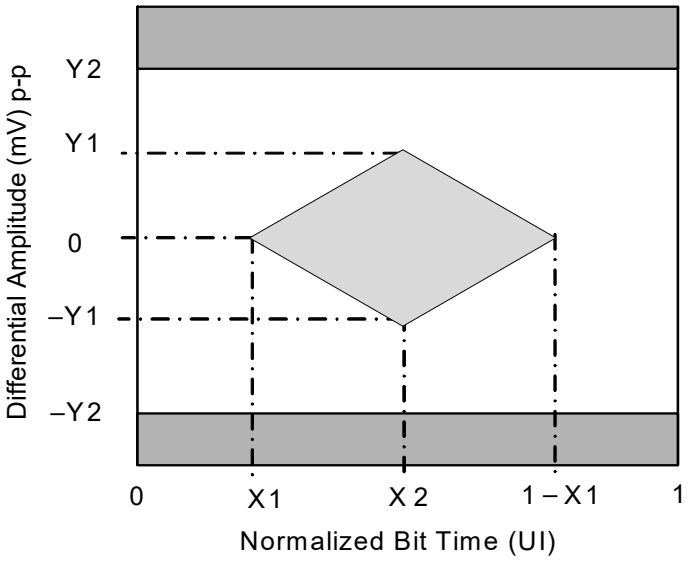
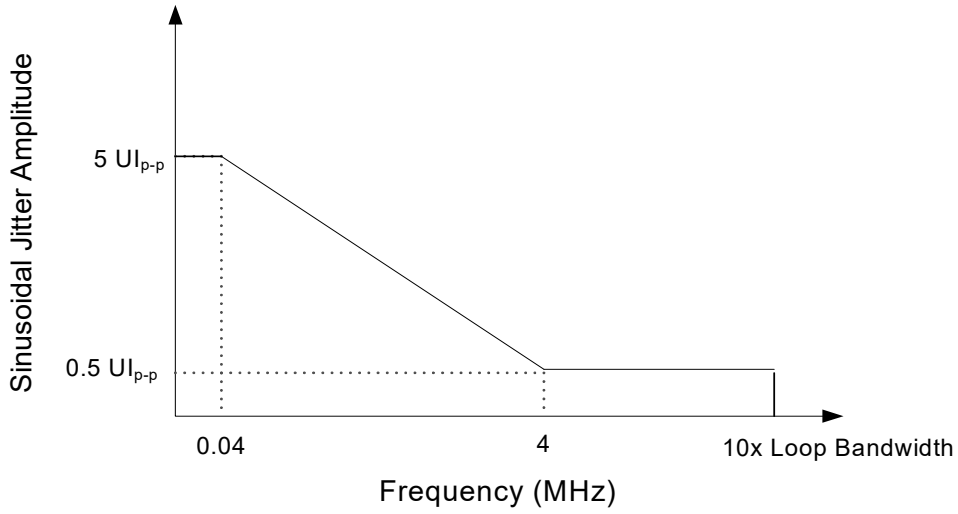


Figure 38: Single-Tone Sinusoidal Jitter Mask



6.3 10GBASE-KR Electrical Characteristics

6.3.1 Transmitter

Table 51: 10GBASE-KR TX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Output speed	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Differential output voltage (peak-to-peak) based on 101010 pattern	VOD	—	—	1200	mVp-p
Output voltage (peak-to-peak) when TX is disabled	VOD	—	—	30	mVp-p
Common mode voltage	VCM	—	0.55	—	V
Differential output return loss (min)	Equation[a]	—	—	—	dB
Common-mode output return loss (min)	Equation[b]	—	—	—	dB
Output rise time (20% to 80%)	Tr	24	—	47	pS
Output fall time (20% to 80%)	Tf	24	—	47	pS
Output jitter at 1e-12 BER					
Random	sRJ	—	—	0.15	UI
Deterministic	sDJ	—	—	0.15	UI
Duty cycle distortion	sDCD	—	—	0.035	UI
Total	sTJ	—	—	0.28	UI

a. Return loss (f) ≥ 9 dB for 50 MHz ≤ f < 2500 MHz.
Return loss ≥ [9 – 12 log (f/2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz.

b. Return loss (f) ≥ 6 dB for 50 MHz ≤ f < 2500 MHz.
Return Loss ≥ [6 – 12 log (f/2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz.

6.3.2 Receiver

Table 52: 10GBASE-KR RX

Parameters	Symbol	Min.	Typ.	Max.	Unit
Receiver coupling	AC	0.05	—	0.1	μF
Differential input voltage (peak-to-peak)	VID	—	—	1200	mVp-p
Differential input return loss (min)	Equation[a]	—	—	—	dB
Receiving speed	—	–100 ppm	10.3125 ppm	+100 ppm	Gbaud

a. Return loss (f) ≥ 9 dB for 50 MHz ≤ f < 2500 MHz.
Return loss ≥ [9 – 12 log (f/2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz.

Chapter 7: Thermal Specifications

7.1 Thermal Requirements

The following two tables provide device thermal specifications. The maximum θ_{JA} is a function of the maximum allowed ambient air temperature of the system and is given for ambient air temperatures of 50°C and 70°C. The device requires steady state maximum junction temperature at 110°C. It allows an excursion of Junction temperature up to 125°C with maximum period of four days per year. During the excursion period, the device continues to operate but its performance may degrade.

Table 53: Estimated Package Thermal Specifications for T_A = 70°C

Parameters	Symbol	Min.	Typ.	Max.	Unit
Power dissipation	P	—	—	365	W
Maximum junction temperature	T	—	—	110	°C
Maximum ambient temperature	A	—	—	70	°C
Maximum calculated θ_{JA}: (T-A)/P	O	—	—	0.11	°C/W

Table 54: Estimated Thermal Specifications for T_A = 50°C

Parameters	Symbol	Min.	Typ.	Max.	Unit
Power dissipation	P	—	—	365	W
Maximum junction temperature	T	—	—	110	°C
Maximum ambient temperature	A	—	—	50	°C
Maximum calculated θ_{JA}: (T-A)/P	O	—	—	0.16	°C/W

7.2 Package Thermal Specifications

The following table shows the preliminary package thermal specifications with a heat sink for various airflow levels. To maintain a junction temperature below the maximum specified junction temperature, the θ_{JA} must be smaller than the maximum calculated θ_{JA} for the device. A heat sink and airflow is required (see Section 7.3, Heat Sink).

Table 55: Estimated Package Thermal Specifications (220x160x29 mm Heat Sink with Vapor Chamber, 2s2p PCB)

Parameters	Symbol	Value	Unit
θ_{JB} (junction-to-board)	θ_{JB}	0.24	°C/W
θ_{JC} (junction-to-case)	θ_{JC}	0.06	°C/W
θ_{JA} (junction-to-ambient), 200 LFM	θ_{JA}	0.22	°C/W
θ_{JA} (junction-to-ambient), 400 LFM	θ_{JA}	0.16	°C/W
θ_{JA} (junction-to-ambient), 600 LFM	θ_{JA}	0.14	°C/W
θ_{JA} (junction-to-ambient), 800 LFM	θ_{JA}	0.14	°C/W
θ_{JA} (junction-to-ambient), 1000 LFM	θ_{JA}	0.13	°C/W

NOTE: The package thermal number is based on a 220 mm × 160 mm × 29 mm heat sink with a vapor chamber base. The data in Table 55 is intended as a starting point for thermal analysis. Further simulation is required for each specific application.

7.3 Heat Sink

7.3.1 Heat Sink Selection

The device is required to be used with a heat sink. The end-use thermal environment combined with the operating mode of the device dictates the required thermal characteristics (size, thermal resistance, and so forth) of the heat sink.

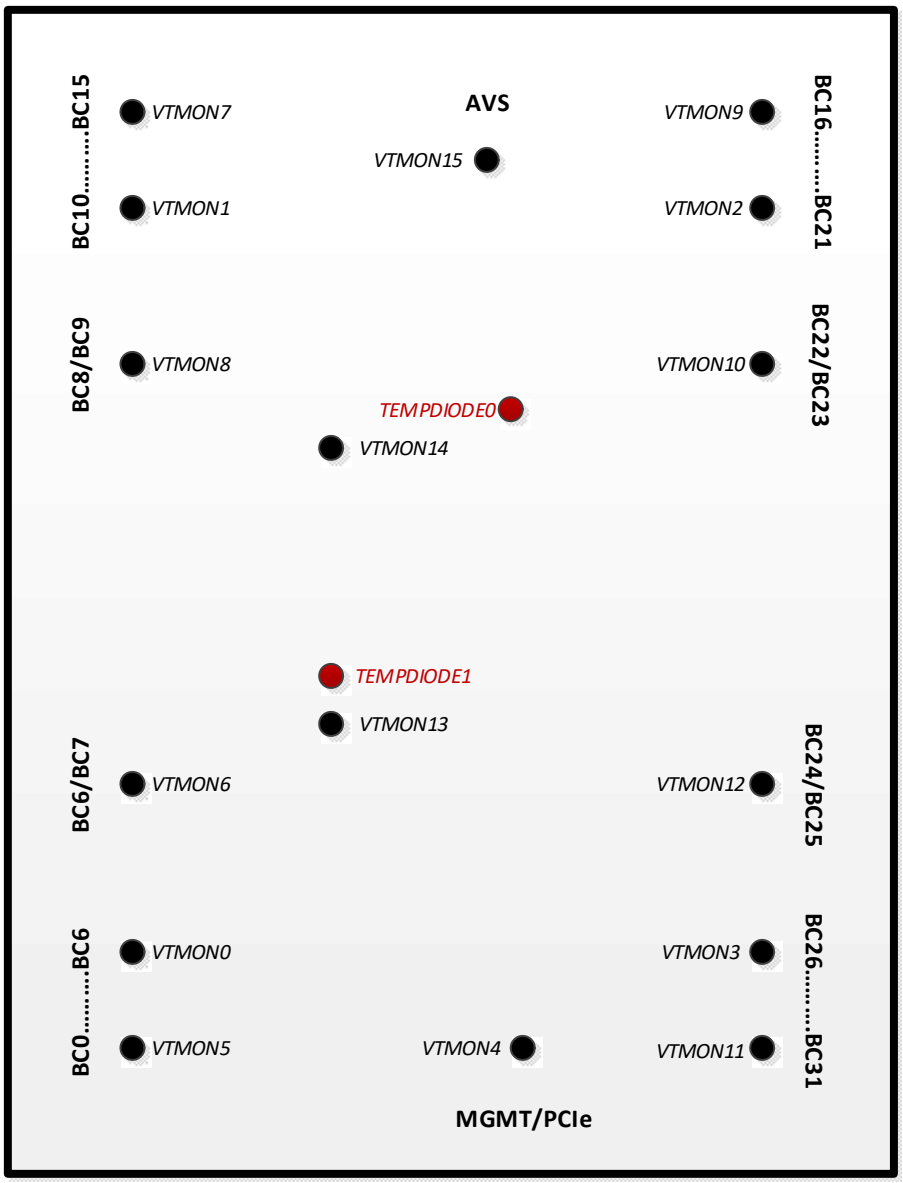
7.3.2 Heat Sink Attachment

For heat sink attachment guidelines (including loading forces up to 110 lb), refer to the *BCM56980 Hardware Design Guidelines* (56980-DG1xx).

7.4 On-Die Thermal Monitors

The device contains numerous on-die thermal monitors. These thermal monitors provide junction temperature information from fixed locations across the die. The output from some of the thermal monitors is used by the various SerDes cores to perform real-time adaptation of the receiver as a function of die temperature. The other thermal monitors are provided as a means of allowing software to monitor the junction temperature of the device. The locations of the thermal monitors relative to the device's die and package are shown in Figure 39.

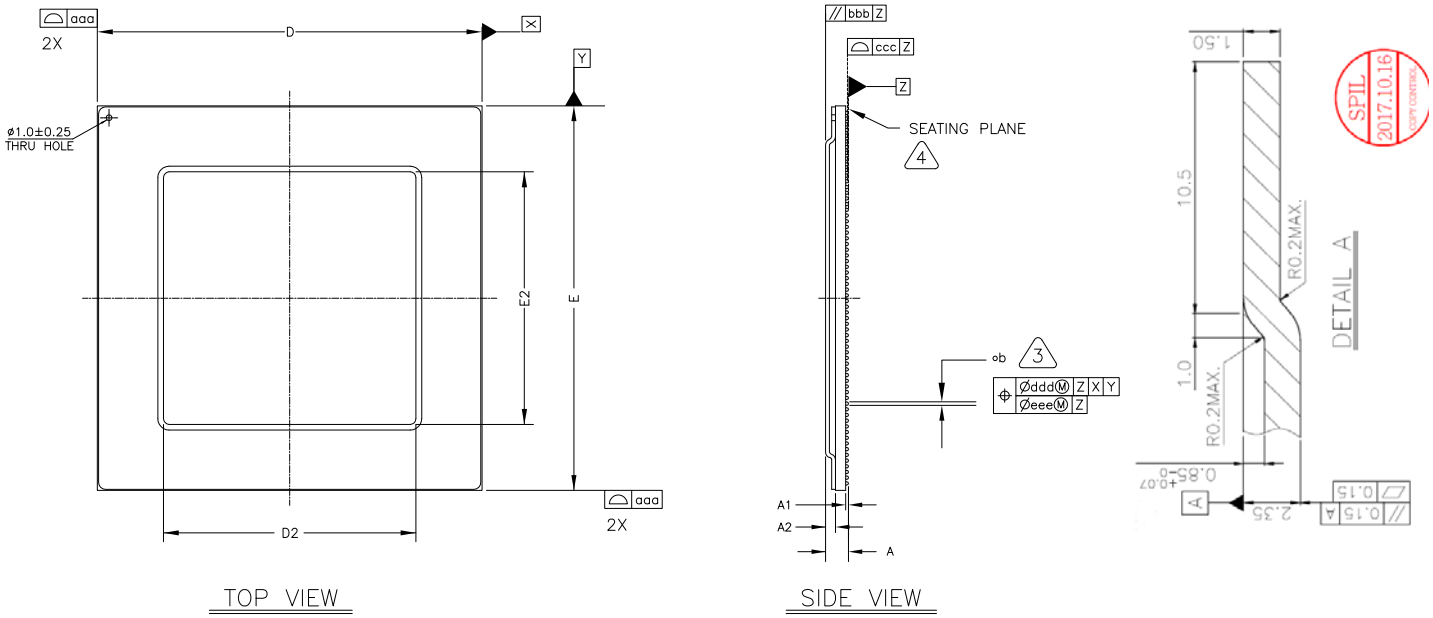
Figure 39: BCM56980 On-Die Thermal Monitors

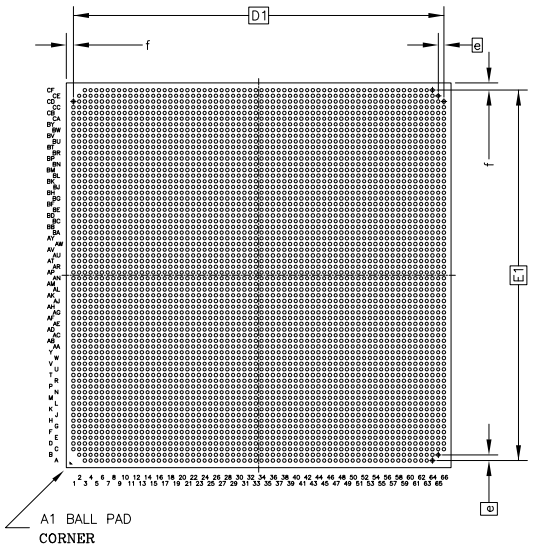


Chapter 8: Mechanical Information

8.1 4344-Ball FCBGA

Figure 40: BCM56980 4344-Ball FCBGA (67.5 mm x 67.5 mm)





BOTTOM VIEW
(4344 SOLDER BALLS)

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	4.227	4.469	4.711
A1	0.435	0.535	0.635
A2	2.33	2.40	2.47
D	67.30	67.50	67.70
D1		65.00 BSC	
D2		44.30 BSC	
E	67.30	67.50	67.70
E1		65.00 BSC	
E2		44.30 BSC	
b	0.50	0.635	0.70
e		1.00 BSC	
f	–	1.25	–
aaa	–	–	0.20
bbb	–	–	0.25
ccc	–	–	0.20
ddd	–	–	0.25
eee	–	–	0.10

Filename: BCM56980B0KFSBG_MOD_000

5. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY E REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

4 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-318B.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Chapter 9: Ordering Information

The following table lists the product part numbers available for order, their descriptions, and selected specifications.

Table 56: Device Ordering Information

Part Number	Package	Description	I/O Bandwidth	Temp
BCM56980B0KFSBG	4344-ball, 67.5 mm × 67.5 mm RoHS-compliant	32 × 400GbE, RoHS 6/6-compliant	12,800G	0°C to 70°C
BCM56983B0KFSBG	4344-ball, 67.5 mm × 67.5 mm RoHS-compliant	16 × 400GbE RoHS 6/6-compliant	6,400G	0°C to 70°C

9.1 PB-Free Packaging

Broadcom offers Pb-free package. Pb-free parts have a letter G added to the top line of the part marking. Refer to the *Reflow Process Guidelines for Surface Mount Assemblies* application note (PACKAGING-AN1xx) for details. Broadcom Pb-free parts comply with RoHS and Waste Electrical and Electronic Equipment (WEEE) directives. Broadcom Pb-free parts are fully RoHS 6/6 compatible and require no exemption to comply with European limitations on hazardous substances. The following table shows the solder ball composition and maximum reflow temperature Pb-free parts.

Table 57: Solder Ball Composition and Recommended and Maximum Reflow Temperature

Part Number	Solder Ball Composition	Recommended Reflow Peak Temperature	Maximum Allowed Reflow Peak Temperature
Pb-free RoHS-compliant package	95.5% Sn, 3% Ag, 0.5% Cu	232°C to 237°C	245°C

For more information, refer to the *BCM56980 SMT Preliminary Recommendations* (BCM56980-SMT-Guide_xxx).

Glossary

Table 58: Acronyms and Abbreviations

Term	Description
ACL	Access Control List
AGC	Automatic gain control
ARM	Advanced RISC Machines
ARP	Address Resolution Protocol
ASF	Alternate Store & Forward
AUI	Attachment Unit Interface
B-MAC	Backbone MAC
BC	Blackhawk PAM4 SerDes Core
BCB	Backbone Core Bridge
BPDU	Bridge Protocol Data Unit
BSC	Broadcom Serial Controller
CAUI	100 Gb/s Attachment Unit Interface
C-MAC	Customer MAC
CFI	Canonical Field Indicator
CMIC	CPU Management Interface Controller
CML	Computer Managed Learning
CMOS	Complimentary metal-oxide semiconductor
CoS	Class of Service
CPPI	100 Gb/s Parallel Physical Interface at the PMD layer
DFE	Decision-Feedback Equalization
DHCP	Dynamic Host Configuration Protocol
DIP	Destination IP address
DLF	Destination Lookup Failure
DNAT	Destination NAT
DSCP	Differentiated services code point
DSL	Digital subscriber line
DVMRP	Distance Vector Multicast Routing Protocol
DVMVO	Distance Vector
DXAUI	Altera's XAUI PHY solution
ECMP	Equal Cost Multiple Paths
ECN	Explicit Congestion Notification
ENNI	External Network to Network Interface
EPON	Ethernet Passive Optical network
ERSPAN	Encapsulated Remote SPAN
ETS	Enhanced Transmission Selection
FCBGA	Flip Chip Ball Grid Array
FCID	Fibre Channel ID
FCoE	Fiber Channel over Ethernet
FEC	Forward Error Correction

Table 58: Acronyms and Abbreviations (Continued)

Term	Description
FIP	FCoE Initialization Protocol
FRR	Fast ReRoute
GBD	Guaranteed by Design
GPIO	General-purpose input/output
GPON	Gigabit PON
GRE	Generic Routing Encapsulation
HOL	Head of Line
HOLB	Head of Line Blocking
HPAE	Host Posture Assessment and Enforcement
HTLS	Hierarchical Transparent LAN Services
I-SID	I Domain SID
IETF	Internet Engineering Task Force
IGMP	Internet Group Management Protocol
IPMC	IP Muliticast
JTAG	Joint Test Action Group
KR	A specification defining a single backplane lane/physical layer coding as defined in IEEE 802.3 Clause 49
L2MC	Layer 2 Multicast
LAG	Link Aggregation Group
LLS	Linked List Scheduler
LoF	Loss of Frame
LoS	Loss of Signal
LPM	Longest Prefix Match
MAC	Media access control
MAC_DA	MAC Destination Address
MAC_SA	MAC Source Address
MDIO	Management data input/output
MIIM	Media Independent Interface Management
MLD	Multicast Listener Discovery
MPLS	Multi-Protocol Label Switching
MTP	Mirror To Port
NAND	Special form of flash memory
NAPT	Network Address Port Translator
NAT	Network address translation
NVGRE	Network Virtualized Generic Route Encapsulation (GRE)
OLT	Optical Line Termination
OOBFC	Out-of-Band Flow Control
PAM4	Four-Level Pulse Amplitude Modulation
PBB	Provider Backbone Bridges
PBB-TE	Provider Backbone Bridging with Traffic Engineering
PCIe	Peripheral Component Interconnect Express (PC bus)
PFC	Priority-based Flow Control
PFM	Port Filter Mode
PHY	Physical Layer Interface

Table 58: Acronyms and Abbreviations (Continued)

Term	Description
PIM	Protocol-Independent Multicast
PIM-BIDR	Protocol-Independent Multicast BiDirectional
PIM-DM	Protocol-Independent Multicast Dense Mode
PIM-SM	Protocol-Independent Multicast Sparse Mode
PIM-SSM	Protocol-Independent Multicast Single Source Multicast
PLL	Phase Loop Lock
QCN	Quantized Congestion Notification/Notifier
QoS	Quality of Service
QSGMII	Quad Serial Gigabit Media Independent Interface
RIOT	Routing In and Out of Tunnel
RMON MIB	Remote MONitoring Management Information Base
RSPAN	Remote Switched Port Analyzer
RSSI	Receive Signal Strength Indication
RX	Receiver
RXAUI	Reduced XAUI
S-VID	Service VLAN ID
SAFC	Service Aware Flow Control
SerDes	Serialize Deserialize
SFI	SerDes Framer Interface
SGMII	Serial Gigabit Media Independent Interface
SIP	Source IP address
SLA	Service Level Agreement
SMON MIB	Switched network MONitoring Management Information Base
SNAT	Source NAT
SNMP	Simple Network Management Protocol
SP	Strict Priority
srTCM	single rate Three Color Marker/Marking
SSTL	Stub Series Terminated Logic
TCAM	Ternary Content Addressable Memory
TDM	Time Division Multiplexor
ToR	Top of Rack
TPID	Tag Protocol ID
TRILL	Transparent Interconnection of Lots of Links
trTCM	two rate Three Color Marker/Marking
TSC	TDM SerDes Core
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
uRPF	unicast Reverse Path Forwarding
VCO	Voltage Controlled Oscillator
VFI	Virtual Forwarding Instance
VFP	VLAN Filter Processor (or VCAP)
VLAN	Virtual Local Area Network
VOQ	Virtual Output Queue

Table 58: Acronyms and Abbreviations (Continued)

Term	Description
VRF	Virtual Route Forwarding or VPN Routing and Forwarding
VXLAN	Virtual eXtensible LAN
WCMP	Weighted Cost Multiple Paths
WDRR	Weighted Deficit Round Robin
WEEE	Waste Electrical and Electronic Equipment
WRED	Weighted Random Early Detection
WRR	Weighted Round Robin
XFI	10-Gigabit serial electrical interface
XGMII	XGMII extender sublayer
XLPPI	40G (XL) Parallel Physical Interface

Related Documents

The references in this section may be used in conjunction with this document.

NOTE: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads and Support site.

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Broadcom Items		
[1] Reflow Process Guidelines for Surface Mount Assemblies, Application Note	PACKAGING-AN1xx	Broadcom CSP
[2] BCM56980 SMT Preliminary Recommendations	BCM56980-SMT-Guide_xxx	Broadcom CSP
[3] BCM56980 Hardware Design Guidelines	56980-DG1xx	Broadcom CSP
[4] BCM56980 Theory of Operations	56980-PG1xx	Broadcom CSP
[5] IBIS-AMI Model for Blackhawk	BRCM_AMI_Blackhawk_vx.x.zip	Broadcom CSP
[6] IBIS-AMI Model for Merlin	BRCM_AMI_Merlin_vx.x.zip	Broadcom CSP
[7] BCM56980_ballout_revx.x.xlsx	BRCM56980_ballout_revx.x	Broadcom CSP
[8] Power_estimator_BCM5698x-x.x-R.xlsm	power_estimator_BCM5698x-x-R	Broadcom CSP
[9] Delphi Thermal Model	BCM56980_Delphi_Model_r0.pdf	Broadcom CSP
[10] StrataXGS® 32x 400GbE Switch SVK schematic	956980KS-PB10x	Broadcom CSP
[11] SerDes Debugging Guide	56980-AN1xx	Broadcom CSP
[12] Heat Sink Attachment and Rework Guidelines Using Thermal Epoxy (Application Note)	PACKAGING-AN7xx	Broadcom CSP
[13] Heat Sink Application (Application Note)	Heat_Sink-AN1xx	Broadcom CSP

Revision History

56980-DS111; July 19, 2019

- Updated Table 3, BCM56980 Features to remove the MMU size and added a reference to Table 4, BCM56980 Family Device Scalability.
- Updated Table 4, BCM56980 Family Device Scalability title to include all devices in the BCM56980 family and to add the following:
  - Number of SerDes for the BCM56983.
  - Integrated Packet Buffer Memory for the BCM56983.
- Updated Table 15, Per SerDes (Eight Lanes), Per Voltage Rail Maximum Power Numbers to show the PCIe SerDes maximum power option.
- Updated the following tables to correct a unit typo for duty cycle from ns to %:
  - Table 38, BroadSync Input Timing – Slave Mode
  - Table 39, BroadSync Output Timing – Master Mode

56980-DS110; March 27, 2019

- Updated the BCM56983 device's typical configuration in Table 1, BCM56980 Family I/O Bandwidth and Throughput.
- Updated the BCM56983 device's maximum number of front-panel ports from 128 to 72 in the following locations:
  - Table 2, BCM56980 Device Family Port Configurations.
  - Section 3.2, BlackhawkCore Octal SerDes Configuration Guidelines.
- Updated Figure 3, BlackhawkCore (BC) Configuration, to add the BCM56983 device BC/pipeline restriction.
- Updated Table 7, BlackhawkCore Configurations, to remove support for 50G PAM4 non-FEC mode.
- Updated Table 9, Device Signal Descriptions:
  - Corrected the typo from BroadSync0 to BroadSync1 for the BS_PLL1_FREFp/n pin description.
  - Clarified the description for the MHOST1_BOOT_DEV pin.
- Updated Table 56, Device Ordering Information:
  - Modified the BCM56983 description.
  - Removed the BCM56982 and BCM56984 SKUs.

56980-DS109; January 17, 2019

- Updated Table 15, Per SerDes (Eight Lanes), Per Voltage Rail Maximum Power Numbers, to clarify PCIe SerDes rail names.
- Updated Section 7.3.2, Heat Sink Attachment, to provide additional information and to correct the typo in the *Hardware Design Guidelines* document number.

56980-DS108; October 16, 2018

- Removed “Advance” designation from data sheet because the BCM56980B0KFSBG is now production qualified. All SKUs other than the BCM56980B0KFSBG are still pre-production.
- Updated the Features section on the cover page to remove Unified Forwarding Database with High-Density LPM Route Table because this is an unsupported mode of operation.
- Updated Table 1, BCM56980 Family I/O Bandwidth and Throughput, to add BCM56983 device information.
- Updated Table 2, BCM56980 Device Family Port Configurations, to add BCM56983 device information.

- Updated Table 3, BCM56980 Features:
  - For the port configuration, 40GbE can also be 2-lane.
  - Removed Unified Forwarding Database with High-Density LPM Route Table because this is an unsupported mode of operation.
  - Added low-latency mode.
  - Added EFP bypass
  - Added stacking/chassis information.
- Updated Table 4, BCM56980 Device Scalability, to remove the footnote regarding unsupported operation mode that increases the MAC address feature.
- Updated Table 7, BlackhawkCore Configurations:
  - Added support for reduced lane mode for 400G and 200G speeds.
  - Added note regarding condition for operating RS272 FEC.
  - Added note regarding restrictions for port-mode coexistence.
- Updated Table 9, Device Signal Descriptions, to require the PCIe_PERST_L signal to be connected for Gen2 and Gen3 PCIe.
- Updated Table 10, BCM56980, BCM56982, BCM56983, and BCM56984 Differences, to add BCM56983 device information.
- Updated Table 14, System Thermal Design Maximum Power:
  - Added preliminary power values for the BCM56982, BCM56983, and BCM56984 devices.
  - Added footnote.
- Updated Figure 19, Power-Up and Reset Timing Diagram, to clarify AVS output time frame.
- Updated Table 26, Power-Up and Reset Timing Requirements:
  - Added t4 + t5 parameter.
  - Clarified AVS output time frame.
- Updated Table 56, Device Ordering Information:
  - Removed A0 devices (only B0 silicon is going to production).
  - Added the BCM56983 SKU.

56980-DS107; July 5, 2018

- Removed information regarding the Out-of-Band Flow Control feature. Due to lack of customer demand, the Out-of-Band Flow Control feature has been deprecated. OOBFC information has been removed from:
  - Chapter 3, System Interfaces (note in beginning of chapter and Section 3.10 Out-of-Band Flow Control in previous data sheet).
  - Table 9, BCM56980 Signal Descriptions.
  - Table 16, Standard 3.3V Signals.
  - Section 5.6, AC Characteristics (Section 5.6.12 OOBFC Interface in previous data sheet).
- Removed heat sink attachment information. This information has been moved to the *Hardware Design Guidelines* document (56980-DG1xx).
- Updated Section 8.1, 4344-Ball FCBGA package drawing dimension A from (3.637mm–4.121mm) to (4.227mm–4.711mm).

56980-DS106; June 11, 2018

- Removed 32x200G support for BCM56984 in Table 2, BCM56980 Device Family Port Configurations.
- Corrected the VCO frequency from 25.78125G to 20.625G for 40G XLAUI2 mode in Table 7, BlackhawkCore Configurations.

- Separated Table 13: BCM56980 Per Voltage Rail Maximum Power Numbers into Table 13, BCM56980 Maximum Per Rail Current for Power Supply Design and Table 14, BCM56980 Maximum System Power used for system thermal design. Added note to clarify the differences.
- Updated Table 54, Estimated Package Thermal Specifications for TA = 70°C and Table 55, Estimated Thermal Specifications for TA = 50°C with updated power.
- Added package lid dimension to Figure 41, BCM56980 4344-Ball FCBGA (67.5 mm x 67.5 mm).

56980-DS105; May 17, 2018

- Added 40G XLAUI2 support in Table 7, BlackhawkCore Configurations.
- Changed names of BC*PLL*_REFCLK* pins in Table 9, BCM56980 Signal Descriptions. Changes do not affect the functionality of the device.
- Changed VDD to 0.75V-0.90V +/- 3% tolerance in Table 11, Operating Conditions.
- Updated estimated power in Table 13, BCM56980 Per Voltage Rail Maximum Power Numbers.
- Changed footnote to indicate there is an on-die capacitor included in Table 26, BlackhawkCore PLL Reference Clock DC Parameters.
- Corrected the max swing to 1200 mV per specification in Table 27, MerlinCore PLL Reference Clock DC Parameters.
- Corrected the PCIE REFCLK Tr/Tf max swing to 0.9ns in Table 33, PCI Express PLL Reference Clock AC Parameters.
- Corrected the typo for BC*REFCLK typical Rise/Fall time to 0.3ns and max Rise/Fall time to 0.5ns in Table 34, BlackhawkCore PLL Reference Clock AC Parameters.
- Corrected the MGMT_REFCLK Tr/Tf max swing to 0.9ns in Table 35, MerlinCore PLL Reference Clock AC Parameters.
- Changed the maximum frequency to 62.5 MHz for IP_QSPI_SCK pin in Table 51, IP_QSPI Timing (Boot Read Mode Using BSPI Controller).
- Added B0 devices in Table 60, Device Ordering Information and Table 10, BCM56980 and BCM56982 Differences.

56980-DS104; March 23, 2018

- Added 50GBASE-KR2 and 50GBASE-CR2 interface types for 50G in Table 7, BlackhawkCore Configurations.
- Added 40GBASE-KR4 interface types for 40G in Table 7, BlackhawkCore Configurations.
- Changed PCIe_WAKE_L signal I/O type from BOD to OOD in Table 9, BCM56980 Signal Descriptions.
- Updated PCIe_WAKE_L, JTRST_L, IP_BSC[1:0]_SCL, BSC_SA[1:0], L1_RCVRD_CLK, L1_RCVRD_CLK_VALID, L1_RCVRD_CLK_BKUP, L1_RCVRD_CLK_VALID_BKUP, IP_G_GPIO[9:0], IP_QSPI_WP_L, IP_MDC[11:0], IP_MDIO[11:0], TX_OOBFC_CLK, TX_OOBFC_SYNC, and TX_OOBFC_DATA_[1:0] signal descriptions to reflect up to date information in Table 9, BCM56980 Signal Descriptions.
- Updated footnote in Table 18, Core PLL Reference Clock DC Parameters.
- Added Section 7.4, On-Die Thermal Monitors.
- Changed VDD AVS voltage range from 0.81V-0.89V to 0.76V-0.89V in Table 11, Operating Conditions and Table 9, BCM56980 Signal Descriptions.
- Added additional note on AVS voltage range in Table 11, Operating Conditions.
- Added new BCM56984 part number in Table 1, BCM56980 Family I/O Bandwidth and Throughput, Table 2, BCM56980 Device Family Port Configurations, Table 10, BCM56980 and BCM56982 Differences, and Table 56, Device Ordering Information.

56980-DS103; January 4, 2018

- Added new BCM56982 part number in Table 1, BCM56980 Family I/O Bandwidth and Throughput, Table 2, BCM56980 Device Family Port Configurations, and Table 56, Device Ordering Information.
- Removed duplicity in Protocols and added 25GbE speed in Configuration row of Table 3, BCM56980 Features.

- Clarify supported protocol in Table 6, BCM56980 External Interfaces.
- Removed Laneswap restriction for 2-lane and 4-lane port in Table 7, BlackhawkCore Configurations.
- Changed the name of the Protocol column to Interface Type with additional interfaces in Table 7, BlackhawkCore Configurations.
- Rephrased Mixed port speed in Section 3.2.1, Flexport Configuration and removed Table 8: BlackhawkCore PLL Restrictions.
- Added additional requirement in Section 3.4, PCIe to emphasize on requirement of QSPI interface with Flash.
- Add “The external PHY mapping can be configured by SDK software” in description of IP_MDC[11:0] in Table 9, BCM56980 Signal Descriptions.
- Added AVS pin default voltage reference in Table 9, BCM56980 Signal Descriptions.
- Clarified MHOST0_BOOT_DEV pin usage in regard to boot up in Table 9, BCM56980 Signal Descriptions.
- Added 25MHz as a supporting frequency to TS_PLL_FREFp/n pin description in Table 9, BCM56980 Signal Descriptions.
- Changed the Note in BOOT_DEV[2:0] in regard to strapping while in boot up in Table 9, BCM56980 Signal Descriptions.
- Changed AVS_PVTMON_ADC, AVS_PVTMON_VDAC, VTMON[3:0]_ADC_VDAC, VTMON4_VDAC_ADC, VTMON13_VDAC and VTMON14_VDAC description as for factory use only in Table 9, BCM56980 Signal Descriptions.
- Added Section 4.3, Device Differences to illustrate different device port usage.
- Corrected the typo of Master and Slave in Section 3.9.1, Slave Mode – BroadSync Signals as Inputs and Section 3.9.2, Master Mode – BroadSync Signals as Outputs title headings.
- Added additional Note for VRM default voltage requirement for power up in Section 11, Operating Conditions.
- Added ESD and latchup specification in Table 12, Absolute Maximum Ratings.
- Added Current specs for Table 15, Standard 3.3V Signals.
- Corrected typo from “IP_VDDO o.2” to “1” in Table 16, MIIM (XG), Clause 45 Electrical Characteristics row Output High Voltage.
- Corrected typo from “-200” to “0” and “2000” to “1800” in Table 18, Core PLL Reference Clock DC Parameters row Single Ended Swing.
- Corrected typo from “950” to “5520” in Table 18, Core PLL Reference Clock DC Parameters row Internal Bias Resistors.
- Corrected typo from “-200” to “0” and “2000” to “1800” in Table 19, TimeSync PLL Reference Clock DC Parameters row Single Ended Swing.
- Corrected typo from “950” to “5520” in Table 19, TimeSync PLL Reference Clock DC Parameters row Internal Bias Resistors.
- Corrected typo from “-200” to “0” and “2000” to “1800” in Table 20, BroadSync PLL Reference Clock DC Parameters row Single Ended Swing.
- Corrected typo from “950” to “5520” in Table 20, BroadSync PLL Reference Clock DC Parameters row Internal Bias Resistors.
- Corrected typo from “-200” to “0” and “1000” to “800” in Table 22, BlackhawkCore PLL Reference Clock DC Parameters row Single Ended Swing.
- Corrected typo from “-200” to “0” and “1000” to “800” in Table 23, MerlinCore PLL Reference Clock DC Parameters row Single Ended Swing.
- Corrected typo of “a” to superscript font in Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 27, and Table 28.
- Corrected typo from “0.6” to “0.5” in Table 29, PCI Express PLL Reference Clock AC Parameters row Rise/fall time (20% - 80%).
- Corrected typo from “-” to “2.5” and “2.5” to “12.5” in Table 42, 1.2V MDC/MDIO Timing row MDC Clock Frequency.
- Corrected typo from “400” to “80” and “-” to “400” in Table 42, 1.2V MDC/MDIO Timing row MDC Cycle Time.
- Corrected typo from “100” to “20” in Table 42, 1.2V MDC/MDIO Timing row MDIO Setup Time.

- Corrected typo from “35” to “30” in Table 42, 1.2V MDC/MDIO Timing row MDIO Output Delay.
- Corrected typo from “45” to “40” and “55” to “60” in Table 43, L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing row L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP duty cycle.
- Added requirement for undershoot and overshoot as part of PCIe specification under footnote in Table 21, PCI Express PLL Reference Clock DC Parameters.
- Corrected PCIe_REFCLK Differential swing from 800/1400 to 600/1200 mV, single ended swing from -200/1000 to 0/800 mV in Table 21, PCI Express PLL Reference Clock DC Parameters.
- Changed the max differential swing from 1200 to 1600 and notation on internal termination in Table 23, MerlinCore PLL Reference Clock DC Parameters.
- Added cycle-to-cycle RMS jitter specification in Section 5.6.2.4, PCI Express PLL Reference Clock (PCIe_REFCLK).
- Added Section 5.6.4, MerlinCore (TSC4-M) Interface timing specification.
- Added Section 5.6.13, QSPI Interface and Section 5.6.14, SPI Interface specification.
- Change “Base” to “BASE” throughout the data sheet.

56980-DS102; November 6, 2017

- Corrected typo from “A total of four” to “A total of nine” in RESCAL[8:0]_REXT row of Table 9, BCM56980 Signal Descriptions.
- Corrected typo from 13.3V to 3.3V in row IP_VDDO_0 (Digital Power Supplies) of Table 9, BCM56980 Signal Descriptions.
- Corrected typo from 337 to 388 in row TRVDD0P8_[3:0] (Analog Power Supplies) of Table 9, BCM56980 Signal Descriptions.
- Corrected QTY typo from 50 to 66 in row TVDD1P2_[3:0] (Analog Power Supplies) of Table 9, BCM56980 Signal Descriptions.
- Corrected typo from Subtotal from 499 to 566 under Analog Power Supplies in Table 9, BCM56980 Signal Descriptions.
- Corrected typo from 1 to 5 for IP_LED[4:0]_CLK and IP_LED[4:0]_DATA of Table 9, BCM56980 Signal Descriptions.
- Added up to date description for IP_MDC[11:0] signal of Table 9, BCM56980 Signal Descriptions.
- Replaced Table 8, BlackhawkCore PLL Restrictions with a new formated table.
- Updated PLL0, PLL1 restriction in Flexport Configuration.
- Created Table 8, BlackhawkCore PLL Restrictions.
- Replaced Table 7, BlackhawkCore Configurations with a newly formated table.
- Updated Description for AVS[7:0], RESCAL[8:0]_REXT and Optional Clocks in Table 9, BCM56980 Signal Descriptions.
- Removed not supported 3.3V supply from IP_VDDO_1/2 in Table 9, BCM56980 Signal Descriptions.
- Removed not supported previous Table 17: MIIM, Clause 22 Electrical Characteristics.
- Updated estimated thermal values from "TBD" in Table 47, Estimated Package Thermal Specifications (220x160x29 mm Heat Sink with Vapor Chamber, 2s2p PCB).
- Removed not supported description bullet from L2 Multicast line of Table 3, BCM56980 Features.
- Replaced BCM56980 column information in line L3 LPM with updated route and type in Table 4, BCM56980 Device Scalability.
- Added 2.5G and 1G support to Description of line 10G Merlin Quad SerDes in Table 6, BCM56980 External Interfaces.
- Reworded and added 2.5G and 1G support under 10G Quad MerlinCore SerDes.
- Replaced BCM56980 Per Voltage Rail Maximum Power Numbers (Estimated).
- Updated Max power number and deleted “Typical Power” column from Per SerDes (Eight Lanes), Per Voltage Rail Maximum Power Numbers (Estimated).
- Replaced Figure 19, Power-Up and Reset Timing Diagram with new requirements.
- Replaced Table 24, Power-Up and Reset Timing Requirements with new requirements.

- Changed Max column specs in Table 45, Estimated Package Thermal Specifications for TA = 70°C and Table 46, Estimated Thermal Specifications for TA = 50°C.
- Removed text about about axuiliary ports from note under Table 2, BCM56980 Device Family Port Configurations.
- Added new bullets to line “10G Merlin Quad SerDes” in Table 6, BCM56980 External Interfaces.
- Updated “Maximum Power” column with latest power in Per SerDes (Eight Lanes), Per Voltage Rail Maximum Power Numbers (Estimated).
- Changed BCM56980 column data for lines L2MC for clarification in Table 4, BCM56980 Device Scalability.
- Updated beginning of line beneath the bullets with corrected port configuration in BlackhawkCore SerDes.
- Changed the mis-typed number of ports from 128 to 256 in first line under LED.
- Changed "N" and "P" typo in the first column of last two lines in Table 8, Signal Types.
- Corrected the mistakes in I/O and Descriptions of lines PCIe_PERST_L (from O to Ipu), PCIe_WAKE_L (from Ipu to Bod), JTRST_L from "should be pulled low" to "can be No Connect"), IP_QSPI_HOLD_L (from Bpu to Bpd), IP_QSPI_MOSI (from Bpu to Bpd), IP_QSPI_SCK (from Bpu to O), P_QSPI_WP_L (from Bpu to Bpd). IP_MDC[11:0] (remove 3.3V), updated following reserved pin voltage IP_PLL_REFCLKp/n_RESERVED/IP_PLL_TESTp/ n_RESERVED/PP_PLL_FREFKp/n_RESERVED/PP_PLL_TESTp/n_RESERVED/TS_PLL_TESTp/n_RESERVED to 1.8V instead of 0.8V, and corrected the I/O type for BC3-4/BC23/BC31_PLL[1:0]_REFCLKp/n_RESERVED from O to I., in Table 9, BCM56980 Signal Descriptions.
- Replaced sections 5.5.4, 5.5.5, 5.5.6, 5.5.7, 5.5.8, 5.5.9 with new formated Reference Clock section. Additional spec: TS/BS_PLL_FREF Vdiff 500-1800mVppd, BC*_REFCLK Vdiff 800-1400mVppd, and MGMT_REFCLK spec.
- Deleted Figure OOBFC Input Timing Diagram, Table OOBFC Input Timing and Section OOBSTAT Interface Timing as device do not support these modes.
- Replace Reference Clocks with new formated Reference Clock section. Corrected PCIE_REFCLK min Vref to 0.3Vppd, BC*_REFCLK rise/fall time to 0.4ns, and added MGMT_REFCLK spec.
- Updated the AVS operation voltage from "0.96V–0.88V" to "0.81V-0.89V" in Table 8, Signal Types and Table 10, Operating Conditions.

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- Changed Maximum Power Number to TBD due to incorrect placeholder numbers.
- Updated Table 11, BCM56980 Signal Descriptions.
- Updated Table 15, BCM56980 Per Voltage Rail Maximum Power Numbers (Estimated).
- Updated Table 16, Per SerDes (Eight Lanes), Per Voltage Rail Maximum Power Numbers (Estimated).
- Updated Table 54, Estimated Package Thermal Specifications for TA = 70°C.
- Updated Table 55, Estimated Thermal Specifications for TA = 50°C.

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Initial release.