BCM56980

Hardware Design Guidelines

Design Guide

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Chapter 1: Introduction

This document describes the hardware design guidelines for the BCM56980 family of devices. It describes the requirements for the high-speed external I/O interface used on these devices, provides a diagram of how each high-speed interface must be connected, and shows routing examples when applicable.

For a complete and detailed functional description on each interface within the devices, refer to the latest *BCM56980 Data Sheet* (56980-DS1xx).

Chapter 2: High-Speed SerDes Cores

The BCM56980 device family incorporates three different SerDes cores:

- Blackhawk SerDes core
- Merlin SerDes core
- PCIe SerDes core

Blackhawk and Merlin cores allow the device to support low-latency throughput, oversubscription capability, and Flexport™ configuration. These SerDes cores consist of digital control logic and an analog front end.

The Blackhawk cores are used for all front-panel ports. There are up to 32 instances of this core, depending on specific devices within the BCM56980 family.

There is a single instance of the Merlin core that is used for the two management ports.

The Blackhawk and Merlin cores require controlled differential trace impedance of 95Ω. These SerDes cores have on-chip termination, eliminating the need for external resistors in typical applications.

The Blackhawk and Merlin cores also have on-die AC capacitors in the receive path; consequently, external AC-coupling capacitors are not required in most cases. This on-die AC-coupling cannot be bypassed.

External capacitors may also be required in the receiver path (Blackhawk and Merlin Cores), if the following exists:

VIN_CM + VIN_DIFF / 4 > 1.2V

This limits the input VCM to ~0.8V maximum, where VIN_CM = Common Mode Voltage and VIN_DIFF = Differential Voltage pk-pk.

If an external capacitor is required, use a 100-nF capacitor with a 0201 footprint to minimize reflections.

AC coupling is required in the TX path from the SerDes core to the link partner receiver. This is achieved through either an external capacitor on the PCB or an on-chip capacitor in the remote receiver.

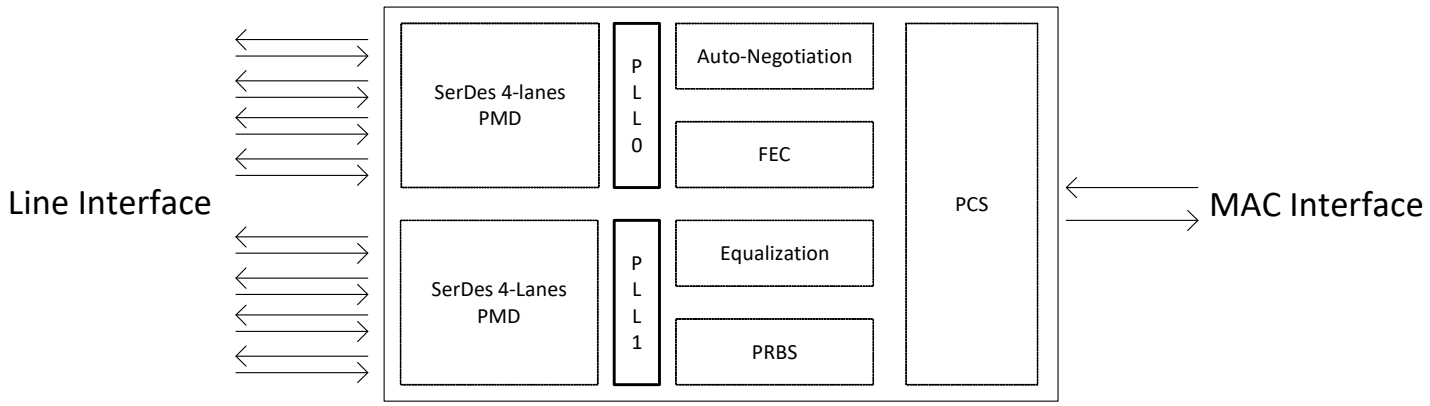
NOTE:

- Refer to the latest version of the BCM56980 data sheet for a complete list of supported speeds and restrictions regarding Blackhawk and Merlin core configurations.
- Half-duplex operation is not supported at any speed.
- If there are any discrepancies between this document and the latest data sheet, the data sheet information takes precedence.

2.1 Blackhawk SerDes Core

The following figure illustrates the SerDes block in the device. It is composed of two quad SerDes PMD blocks (8 lanes) and the supporting digital logic.

Figure 1: Blackhawk SerDes Core Block Diagram



The Blackhawk core can support 1-lane, 2-lane, 4-lane, and 8-lane modes of operation. Refer to the latest data sheet for a complete list of supported port speeds. For convenience, some example port speed modes are shown in the following table.

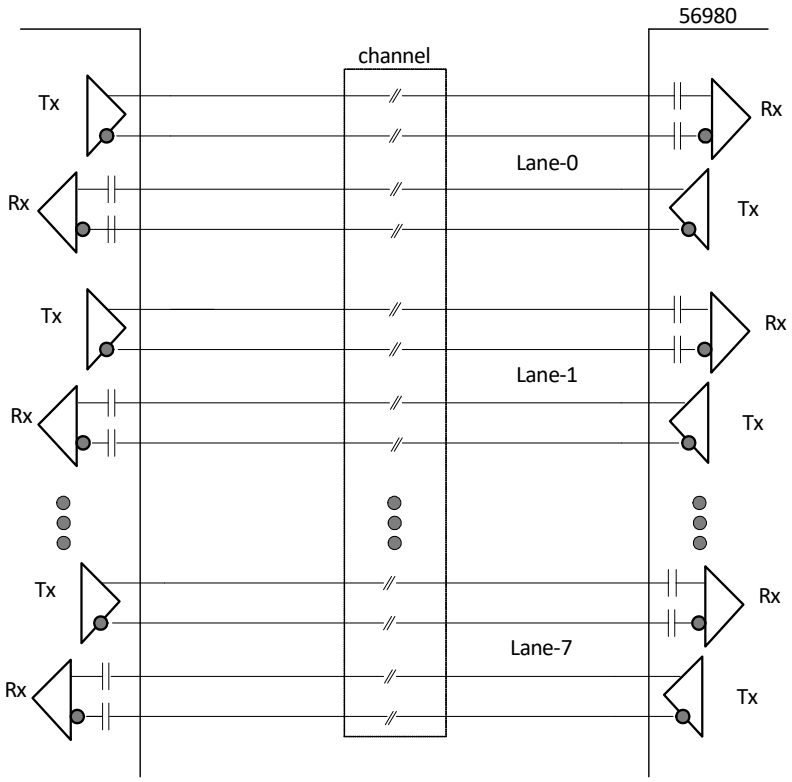
Table 1: Speed Mode Examples

Interface	Number of Lanes	Mode	Lane Baud Rate	VCO Freq
10G-SFI	1	NRZ	10.3125G	20.6250G (OSx2)
25G-KR, CR	1	NRZ	25.78125G	25.78125G
50G-KR2, CR2	2	NRZ	25.78125G	25.78125G
50G w/RS-544 FEC	1	PAM4	26.5625G	26.5625G
40G-KR4, CR4	4	NRZ	10.3125G	20.625G (OSx2)
100G-KR4, CR4	4	NRZ	25.78125G	25.78125G
200G w/RS-544 FEC	4	PAM4	53.125G	26.5625G
400G w/RS-544 FEC	8	PAM4	53.125G	26.5625G

NOTE: Refer to the latest data sheet for any port/speed restrictions. In case of conflict, the data sheet takes precedence.

A typical connection diagram is shown in the following figure. This is applicable for 1-lane, 2-lane, 4-lane, and 8-lane modes. In most cases, a direct connection can be made without the need for any external components.

Figure 2: Typical Blackhawk Connection Diagram



2.1.1 Blackhawk PLL

The Blackhawk SerDes cores have dual PLLs, so any of the eight lanes can be configured to use any one of the two PLLs as its reference clock. This allows for a mixture of port speeds across the lanes.

Some limitations may still occur if a port speed cannot be derived from the two PLL frequencies. For example, the following port speed combination could not be supported within a single Blackhawk core at the same time. There are other port speed combinations that are not supported, this is an example of one such port speed combination.

- 200G PAM4 (4-lanes) with RS-544 FEC – Requires 26.5625G.
- 25G NRZ (1-lane) – Requires 25.78125G.
- 10G NRZ (1-lane) – Requires 10.3125G (20.6250G with OSx2).

NOTE: A frequency change to the primary VCO requires a reset of the PortMacro (PM), but a reset to the secondary VCO does not require a PM reset.

2.1.2 Polarity Inversion

Blackhawk supports SerDes TX and RX polarity inversion. The polarity of the P and N taps of each pair can be individually inverted. The configuration is software controlled via dedicated registers/bit on an individual pair basis.

2.1.3 Lane Swapping

The TSC cores support both polarity flip and lane swap capabilities. These features are typically needed in order to ease the layout requirements.

The lane swap capability is restricted to RX lanes in the receive path and TX lanes in the transmit path. Lane swapping across TX and RX lanes is not supported.

There are no restrictions when swapping TX lanes with other TX lanes or when swapping RX lanes with other RX lanes, but lane swapping affects PMD loopback modes.

- PMD remote loopback is not supported with lane swaps.
- PMD local loopback can be supported with lane swaps; however, this requires all the lane swap configuration to be removed for the port-under-test before putting it into loopback mode. When the PMD loopback test is complete, the lane swap configuration can be reapplied for normal operation. This affects all ports within a Blackhawk core.

NOTE: PCS loopback modes are not supported by the hardware.

2.1.4 Blackhawk Lane/Port Restrictions

- Ports must be aligned to Blackhawk core boundaries. This means that a single port cannot span multiple Blackhawk cores. A 4-lane port (that is, 40G-CR4) cannot have two lanes in Blackhawk core 0 and two lanes in Blackhawk core 1.
- All ports are oversubscription ports. There are no guaranteed line-rate ports.

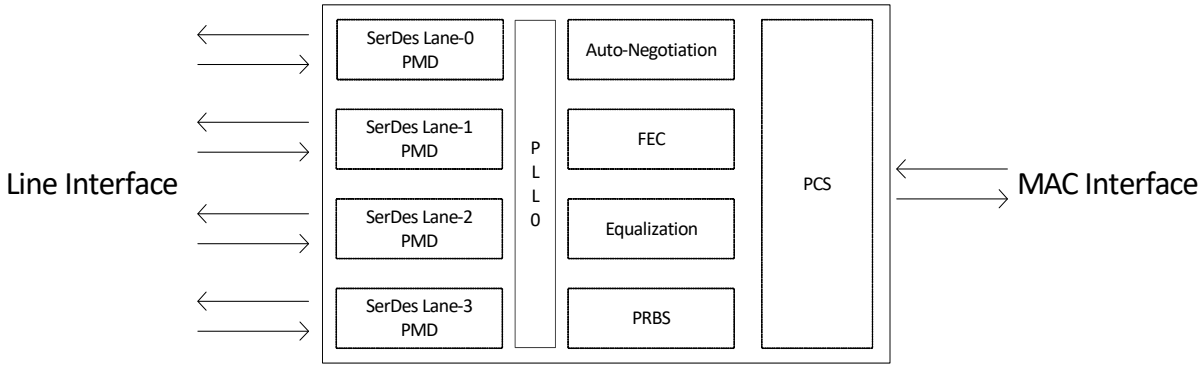
2.1.5 Port and Bandwidth Distribution

To optimize switch performance, distribute the port usage and bandwidth evenly across the eight pipelines and the two ingress traffic managers (ITM0 and ITM1). For additional information, refer to the MMU and Port Numbering sections in the *BCM56980 Theory of Operations* (56980-PG1xx).

2.2 Merlin Core (Management Port)

The following figure illustrates the SerDes block in the device. It is composed of a single quad SerDes PMD blocks (four lanes) and the supporting digital logic.

Figure 3: Merlin SerDes Core Block Diagram



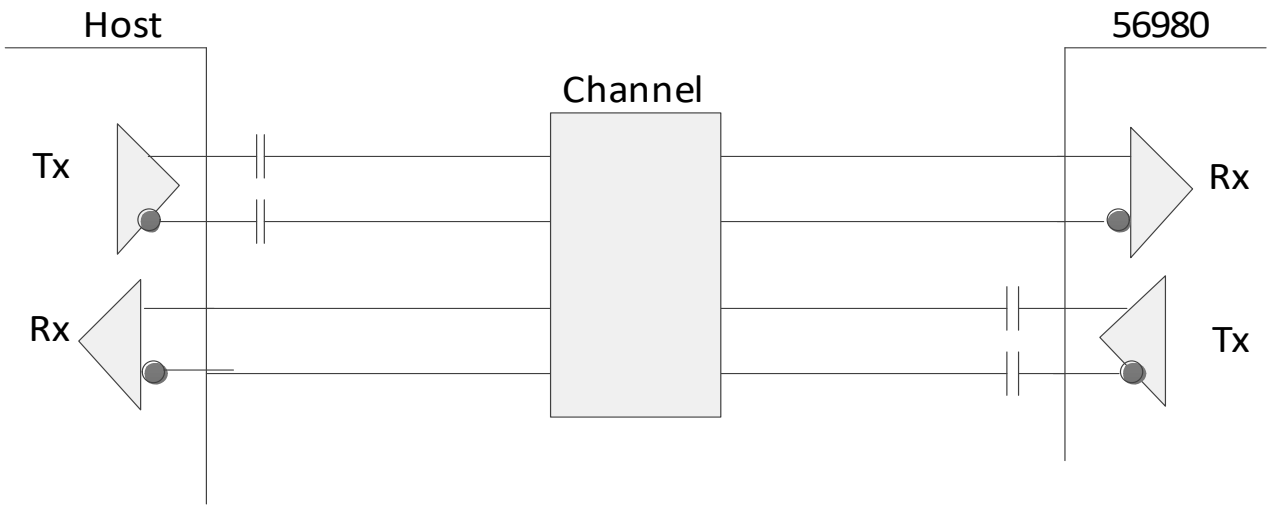
Up to two management ports are supported in the device by this quad core SerDes module. The management ports have limited modes of operation compared to the Blackhawk cores. Refer to the latest data sheet for a complete list of supported port speeds and supported lanes.

2.3 PCIe SerDes Interface

The BCM56980 is a x4 PCIe Gen3-capable device. The PCIe interface provided by the switch conforms to the PCIe version 3.0 specification. The device supports up to four lanes of PCIe (8 Gb/s in each direction).

A two-lane (x2) PCIe interface is supported using lanes 0 and 1, and a single-lane (x1) interface is supported using lane 0. The protocols and electrical requirements of the PCIe specifications are strictly implemented. The PCIe interface consists of a serial point-to-point interface that propagates data through differential pairs.

Figure 4: Typical PCIe Connection



Series AC-coupling capacitors are required in the data path. The capacitor is typically 75 nF to 200 nF. All PCIe differential pairs must be routed as a closely coupled pair with a differential impedance of 100Ω.

The within-pair trace lengths must be length-matched within 5 mils to minimize skew.

On-chip 100Ω differential termination resistors are already provided. External termination resistors are not required. Minimize the number of vias in the trace path. Vias must always match in number on each differential pair and be collocated whenever possible.

2.3.1 PCIe Gen3 Specific Information

PCIe Gen3 supports speeds of 8 Gb/s, thus routing guidelines for 10 Gb/s should be followed. For more information, see Section 6.3, 10G PCB Layout Guidelines.

PCIe Gen3 requires microcode to be loaded into the PCIe SerDes during initialization. This is achieved by using mHost0 to fetch microcode from an external flash memory (EEPROM) and push it into the PCIe SerDes.

This QSPI Flash device is connected to the IP_QSPI interface and must be strapped, such that the device downloads from this memory. The firmware configures the PCIe interface into a functionally compliant Gen3 mode.

The strap settings are shown below.

- BOOT_DEV[2:0] = 3’b000.
- MHOST0_BOOT_DEV = 1’b1.
- PCIE_FORCE_GEN[1:0] = 2’b00.
- QSPI flash memory is programmed with firmware provided by Broadcom®.
- QSPI flash memory is connected to the IP_QSPI interface.

Given that this sequence is the only way to initialize PCIe Gen3, designs should include an EEPROM device connect using the IP_QSPI interface. If the device is strapped to operate at Gen1 or Gen2 speeds, it is still required to populate and connect the QSPI Flash device, as this is used in case any hard-reset register settings need to be tuned for optimal PCIe Gen2/Gen1 operation.

NOTE: It is a design requirement to include a QSPI flash memory containing the Broadcom-provided PCIe firmware. The device must also be strapped to download and execute the code from this flash memory for the PCIe interface to be functional. Refer to the BCM956980K SVK schematic for the connection circuit and example part number.

2.3.2 PCIe TX and RX Routing and AC-Coupling

The *PCI Express Base Specification Revision 1.0a,* Section 4.3.1.2, dictates that AC-coupling be placed as close to the transmitter buffer as practical. This ensures that the DC bias levels of the transmitted signal do not adversely affect the receiver.

2.3.3 Active State Power Management

Active State Power Management (ASPM) should be disabled for normal operation. The device does not support this feature. If this feature is enabled, the device may not initialize properly.

2.3.4 PCIe Reset

The device supports the following three reset modes per PCIe standards:

- Cold Reset – Applies the fundamental reset mechanism by toggling the PERST# signal following the application of power to the component.
- Warm Reset – Applies the fundamental reset mechanism by toggling the PERST# signal without the removal and application of power to the component. The timing requirements must be similar to that of Cold Reset, except that there are no changes in power events.
- Hot Reset – An in-band mechanism where a reset is propagated across the link by software. The in-band mechanism forces a link into the electrical idle state while going through a Hot Reset. When the switch device operates as an End Point (EP), the Root Complex (RC/CPU) issues either a Warm Reset or Hot Reset. Regardless of any reset modes, it is a requirement to connect the PERST# signal directly from the switch to the CPU.

NOTE: Although the PCIe standards do not require toggling the PERST# signal during Hot Reset, it is Broadcom requirement so as to support the Hot-Swap function. Failure to toggle PERST# will not reset the PCIe core within the switch.

All power-up and reset sequences must adhere to the timing diagram specified in the data sheet. Refer to the data sheet for timing on VDD, SYS_RST, PERST#, PCIe_CLOCK, and CORE_CLK.

Chapter 3: Clock Requirements

There are several clock/PLL sources required by the BCM56980. Refer to the BCM56980 data sheet for the clock input electrical requirements.

Table 2: 56980 Reference Clock Summary

Clock Name	Clock Requirement	Description
CORE_PLL_FREF	Input Type = Differential Frequency = 50 MHz	Provides clock signal for the digital core. AC coupling: Needs external 0.01-µF capacitors. Termination: 100Ω differential, on-chip.
BS_PLL[1:0]_FREF	Input Type = Differential Frequency = 50 MHz	BroadSync® reference clock Input. AC coupling: Needs external 0.01-µF capacitors. Termination: 100Ω differential, on-chip.
TS_PLL_FREF	Input Type = Differential Frequency = 50 MHz	Time Sync reference clock Input. AC coupling: Needs external 0.01-µF capacitors. Termination: 100Ω differential, on-chip.
BC_A_REFCLK A0: BC1-2_PLL0_REFCLK B0: BC3-4_PLL1_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 0 to 3. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V. Termination: 100Ω differential, on-chip.
BC_B_REFCLK A0: BC5-6_PLL0_REFCLK B0: BC3-4_PLL0_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 4 to 7. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V. Termination: 100Ω differential, on-chip.
BC_C_REFCLK A0: BC9-10_PLL0_REFCLK B0: BC11-12_PLL0_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 8 to 11. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V. Termination: 100Ω differential, on-chip.
BC_D_REFCLK A0: BC13-14_PLL0_REFCLK B0: BC11-12_PLL1_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 12 to 15. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V. Termination: 100Ω differential, on-chip.
BC_E_REFCLK A0: BC17-18_PLL0_REFCLK B0: BC19-20_PLL1_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 16 to 19. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V. Termination: 100Ω differential, on-chip.
BC_F_REFCLK A0: BC21-22_PLL0_REFCLK B0: BC19-20_PLL0_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 20 to 23. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V. Termination: 100Ω differential, on-chip.
BC_G_REFCLK A0: BC25-26_PLL0_REFCLK B0: BC27-28_PLL1_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 24 to 27. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V. Termination: 100Ω differential, on-chip.

Table 2: 56980 Reference Clock Summary (Continued)

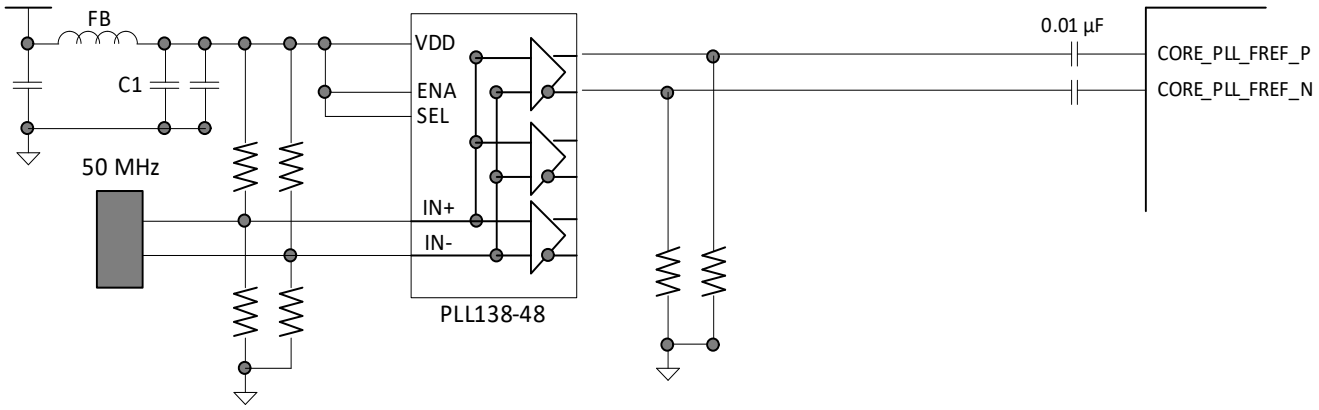
Clock Name	Clock Requirement	Description
BC_H_REFCLK A0: BC29-30_PLL0_REFCLK B0: BC27-28_PLL0_REFCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for Blackhawk cores 28 to 31. AC coupling: On-chip AC coupling, but requires external 0.01-µF capacitors if the input voltage is > 1.2V Termination. Termination: 100Ω differential, on-chip.
TSC_MGMT_REFLCLK	Input Type = Differential Frequency = 156.25 MHz	SerDes reference clock input for management ports using Merlin core. AC coupling: Needs external 0.01-µF capacitors. Termination: 100Ω differential, on-chip.
PCIE_REFCLK	Input Type = Differential Frequency = 100 MHz	PCIe SerDes reference clock Input. AC coupling: Requires external AC coupling. Termination: External 100Ω termination is recommended, but not required, as long as the data sheet input requirements are met.

Sample connection diagrams are shown in the following figures.

3.1 CORE_PLL_FREF Connection

The core clock is a differential clock required to drive the core logic. Its voltage swing cannot exceed the values specified in the data sheet. It must be routed with controlled impedance. The following figure shows an example using a single oscillator with a clock buffer to drive the CORE_PLL_REFCLK input. See Table 2 for information related to this input and refer to the data sheet for the CORE_PLL_REFCLK electrical requirements

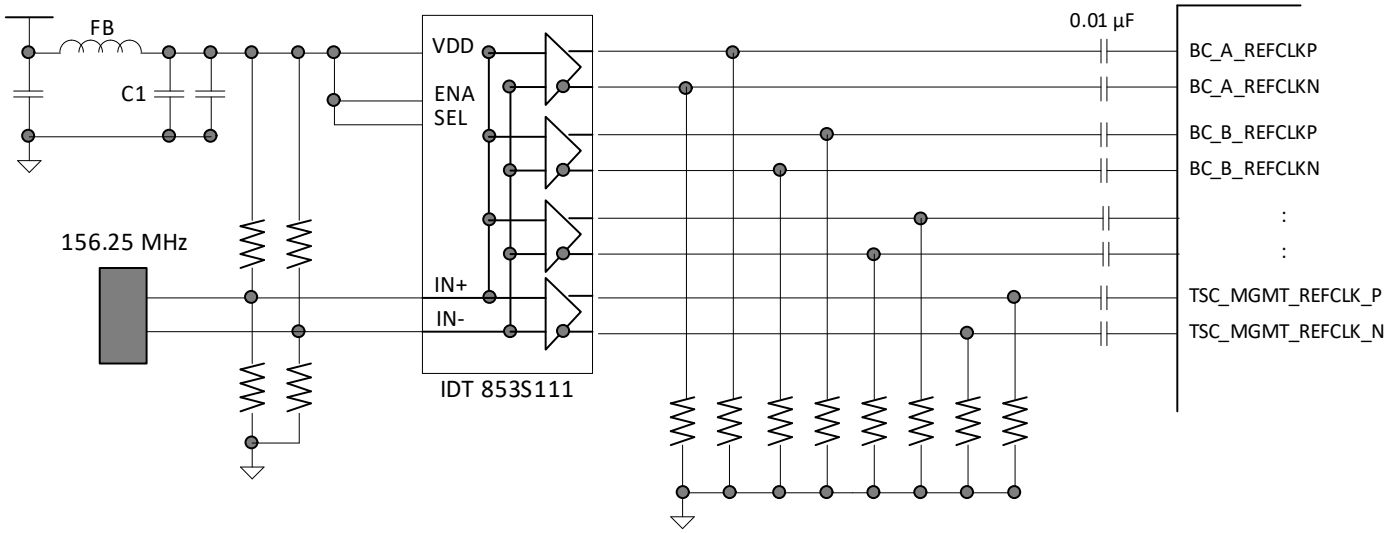
Figure 5: CORE_PLL_FREF Connection



3.2 BC_[A:H]_REFCLK and TSC_MGMT_REFCLK Connection

These differential clocks are required to drive the SerDes cores. Their voltage swing cannot exceed the values specified in the data sheet. It must be routed with controlled impedance. The following figure shows an example of an oscillator with a clock buffer to drive the BC_[A:H]_REFCLK and TSC_MGMT_REFCLK inputs. Refer to the data sheet for the electrical requirements.

Figure 6: BC_[A:H]_REFCLK and TSC_MGMT_REFCLK Connection



NOTE: The Connor-Winfield (PB223-156.25M) clock source should meet the jitter requirements. However, Broadcom recommends to consult with clock vendors to ensure all electrical requirements are met.

NOTE: The BC_[A:H]_REFCLK and TSC_MGMT_REFLCK differential reference clocks are critical high-speed clocks with very fast rise and fall times. Good PCB layout practices are required for these clocks, including the use of back drilling vias to minimize reflections due to via stubs.

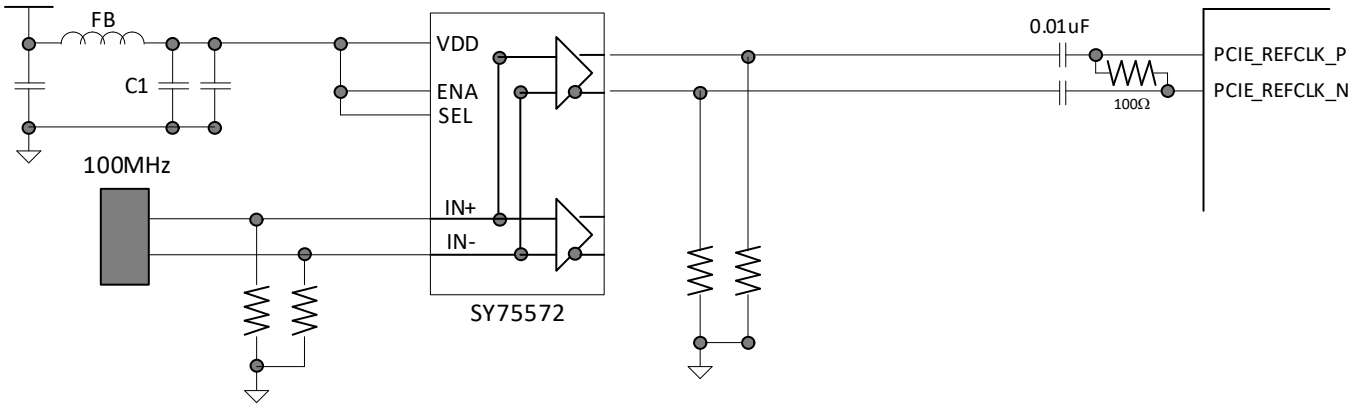
3.3 PCIE_REFCLK Clock Connection

This is a differential 100-MHz clock that is required to drive the PCIe interface. Refer to the data sheet for the electrical requirements.

Example components are shown in the following text:

- Oscillator: MICROCHIP MX555ABD100M000
- Clock buffer: MICROCHIP SY75572

Figure 7: PCIE_REFCLK Clock Connection



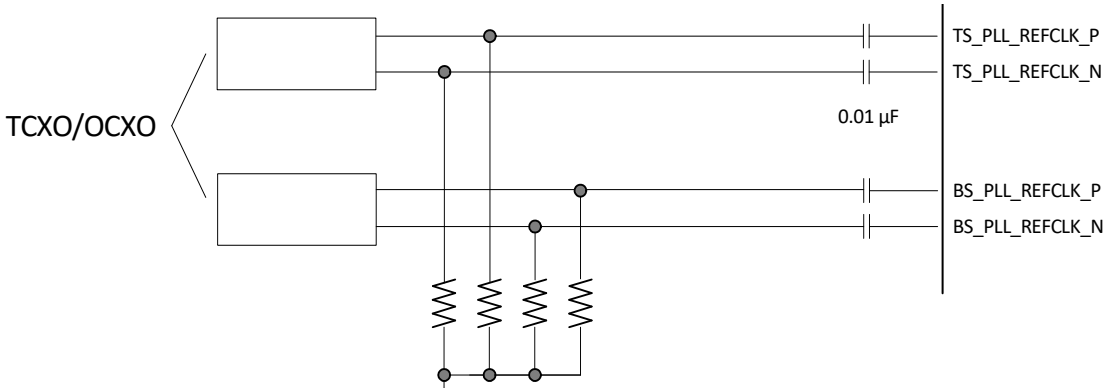
NOTE: All components shown are example components.

3.4 Time Sync and BroadSync Reference Clock Information

For Timing-over-Packet (ToP) and boundary clock applications, it is critical to have a stable crystal oscillator output. For these applications, a mini-OCXO is required.

A typical connection diagram is shown in the following figure.

Figure 8: TS_PLL and BS_PLL Reference Clock Connection



3.4.1 Mini OCXO Requirements

Use either the Rakon M5860LF (12.8 MHz DIL Mercury mini OCXO) or the Rakon STP2920LF (12.8-MHz, 25 mm × 22 mm OCXO) as sources for TS_PLL_REFCLK and BS_PLL_REFCLK. The M5860LF and STP2920LF have been tested by Broadcom in the IEEE 1588 clock recovery application.

The output behavior of the OCXO can be altered by external conditions such as temperature variation, reference voltage, and/or electrical noise. The following recommendations minimize the external influences as much as possible, given that there are other devices and signals that can create disturbances.

NOTE: The propagation delay of the buffers for frame sync and 4-kHz outputs must be less than 1 ns.

3.4.2 OCXO Power Supply and Voltage

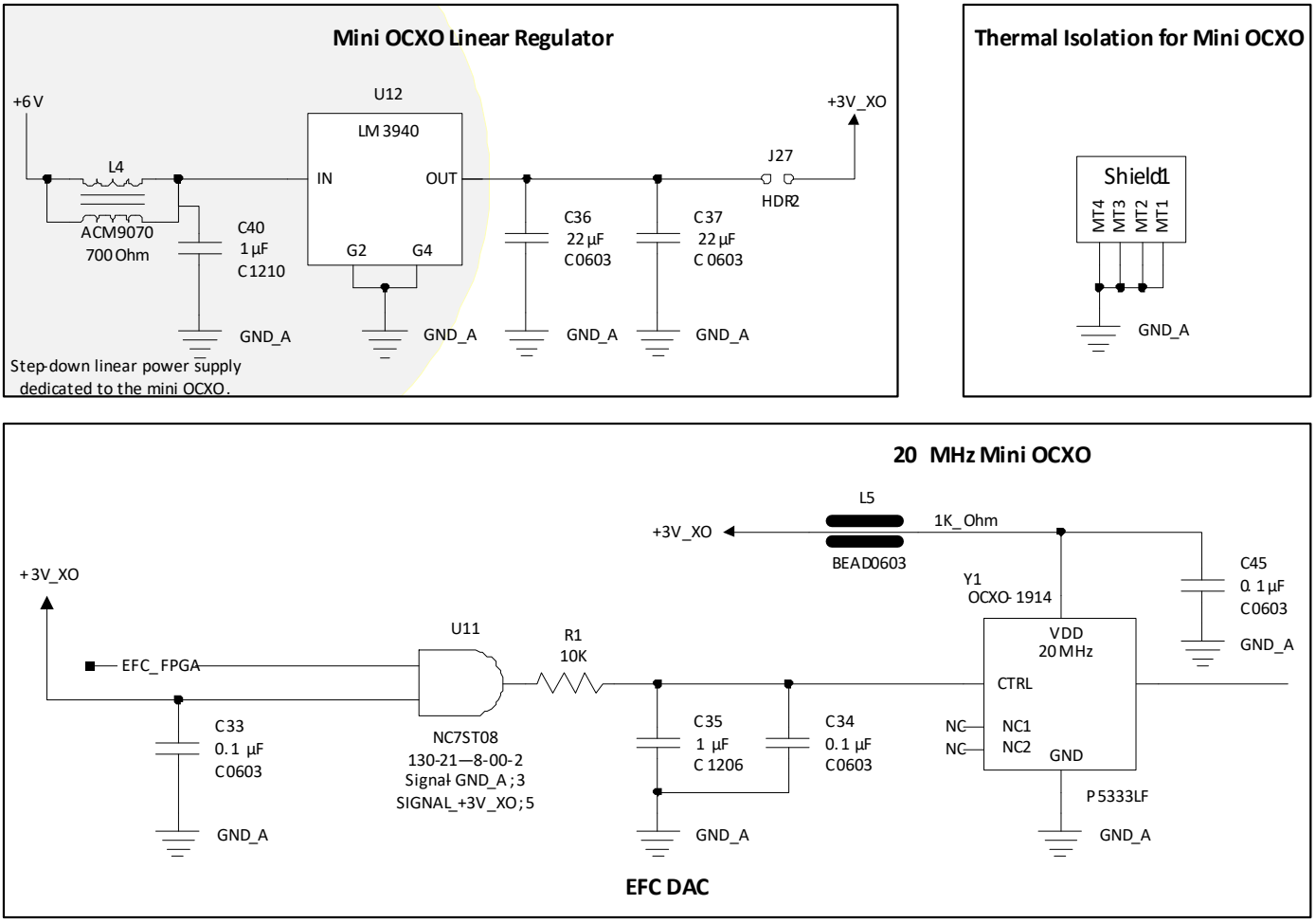
The power supply rail for the OCXO must be isolated from the power rails of all other devices. The recommended circuit is shown in the following figure.

When a 3.3V supply is shared with other devices, filtering is critical to minimize noise and load variation.

A dedicated step-down linear supply using a 5V-to-12V input supply is recommended, rather than inductor isolation from an existing 3.3V supply rail. Use good RF design practices when designing the circuit board and place the OCXO close to the destination clock input to minimize noise injection across the long trace length.

The OCXO can have an initial voltage anywhere within the typical operating voltage range of ± 5% of the 3.3V supply. However, deviation from the initial voltage level during normal operation adversely affects the stability of the output frequency. For example, the M5860LF and the STP2920LF both specify an operating voltage range of 3.3V ± 5%. If the operating voltage changes by ± 2%, then the output frequency typically changes by ± 10 ppb.

Figure 9: Recommended Isolation Circuit

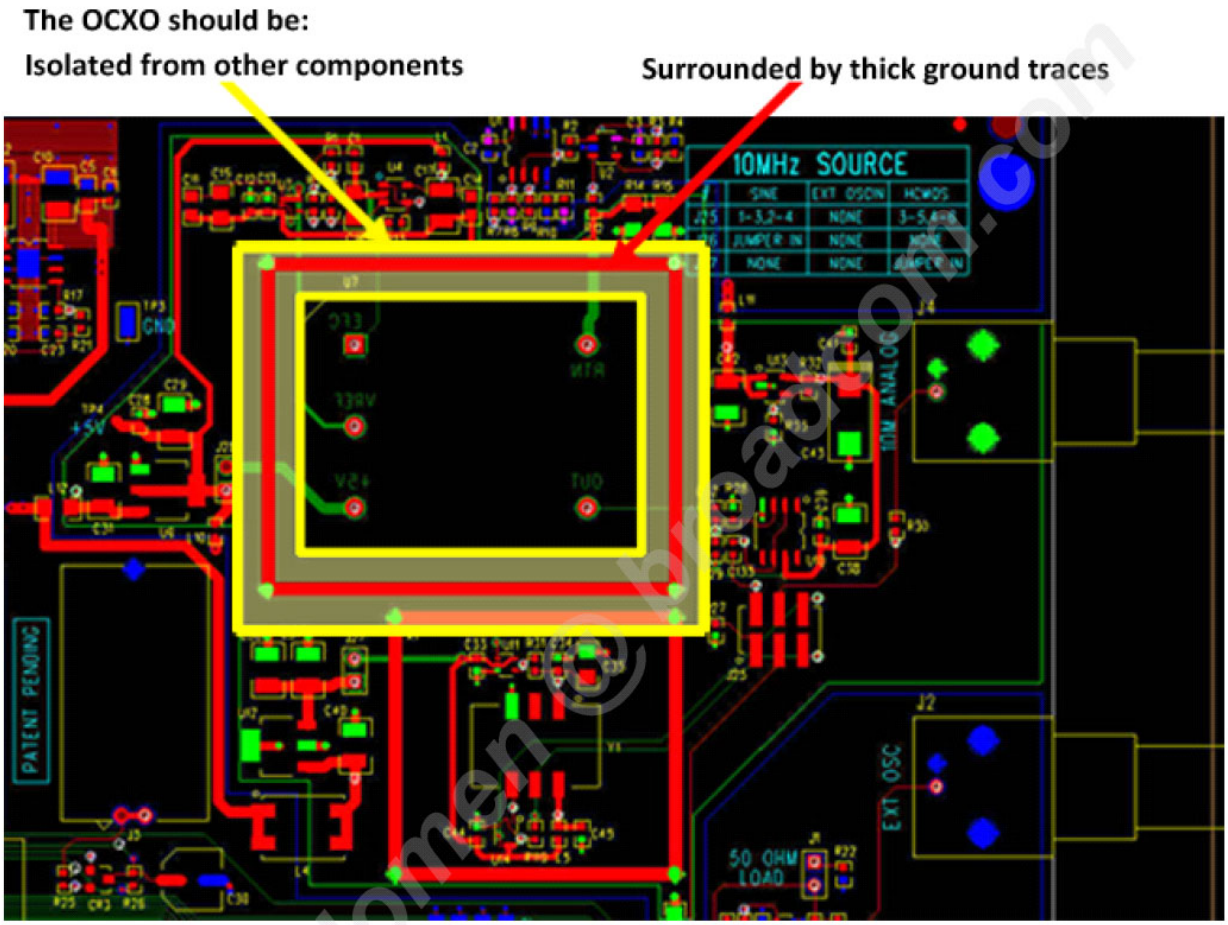


3.4.3 Mini OXCO PCB Layout Guidelines

Placement of the OCXO device must be as far away as possible from noise sources. For example, avoid placement near fans, clock runs, other power supply rails, and devices that emit high temperatures.

The layout example in the following figure illustrates how the OCXO must be isolated from the surrounding circuits.

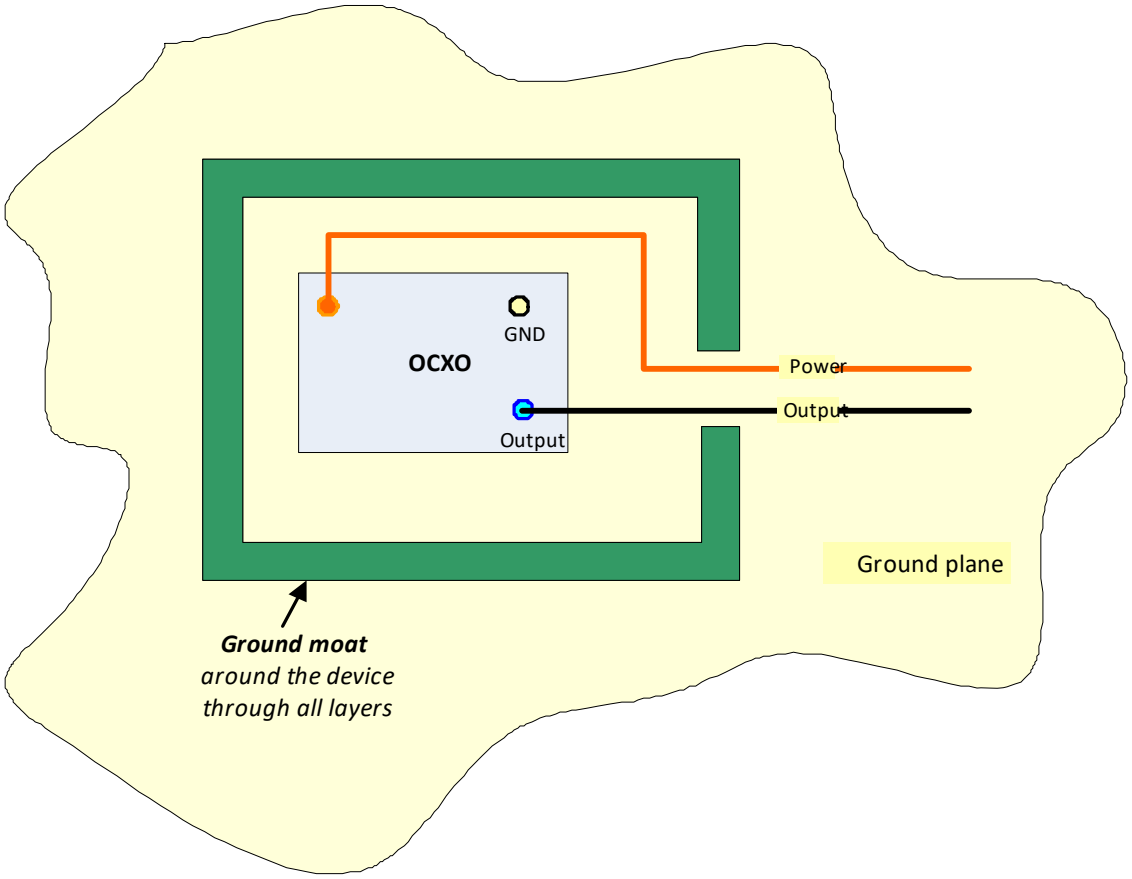
Figure 10: OXCO Component Placement on PCB



3.4.4 Alternative Mini OXCO PCB Layout

An alternative layout can be used to isolate the OCXO from the balance of the circuits. The OCXO must be separated from all noise sources. A ground moat (on all layers) must be created around the OCXO. In addition, void the ground connection only on the layer where the clock output path exists. No signal, power, or ground must go over the moat area on any layer. The following figure illustrates this approach.

Figure 11: Alternative PCB Layout



3.4.5 OCXO Temperature Sensitivity

Temperature variation is a major factor that can impact the output frequency of the OCXO resulting in phase and frequency variations (wander). The following recommendations are suggested to minimize the temperature variation on the OCXO. Generally, the OCXO must be placed where the least temperature variation is anticipated:

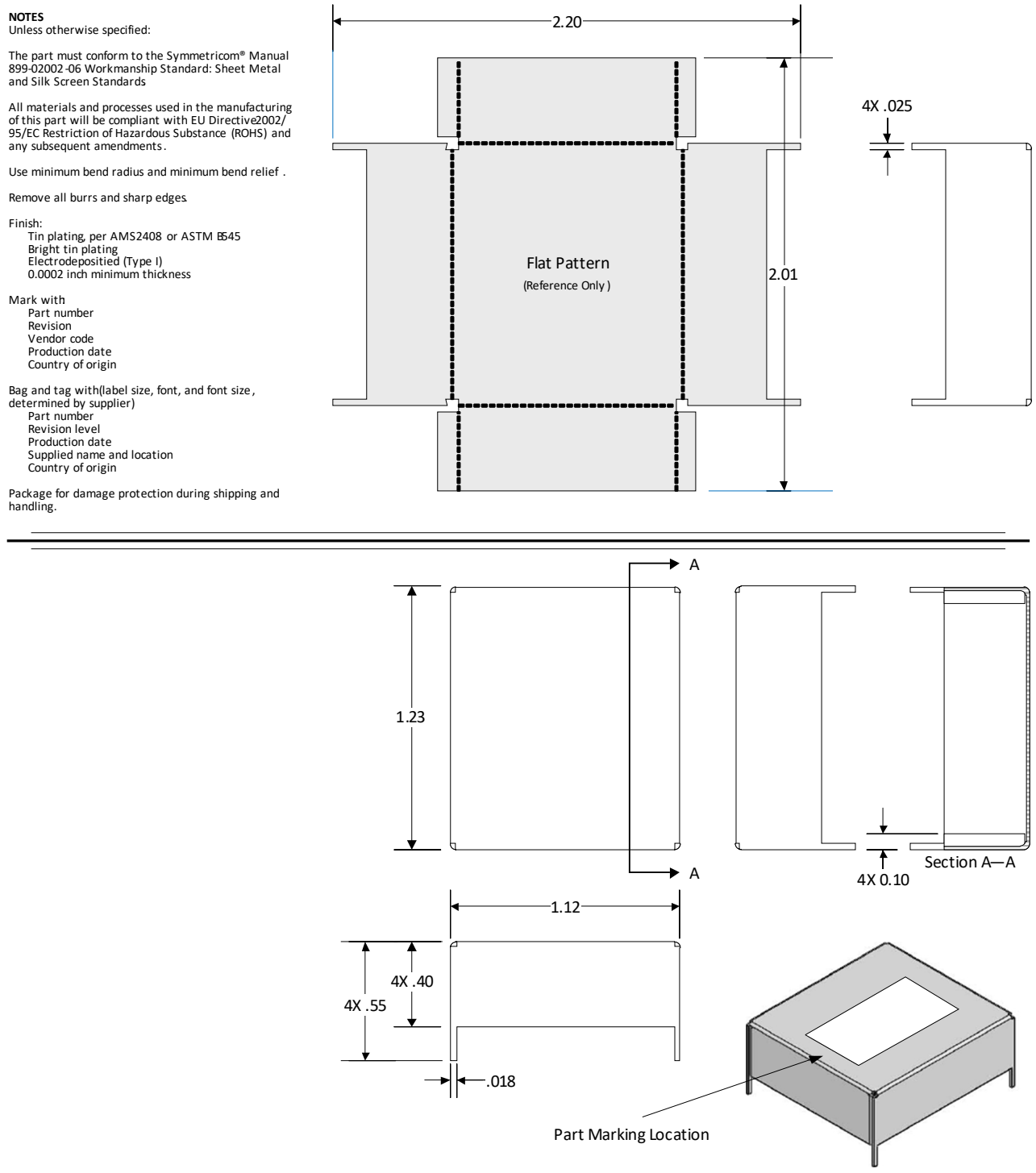
- Away from air vents and fans.
- Where airflow is low.
- In a location where the OCXO is fitted with an environmental cover to help isolate it from external influences (see Section 3.4.6, Environmental Protection Cover).

NOTE: Ensure the internal temperature of the cover does not exceed the maximum operating temperature of the OCXO.

3.4.6 Environmental Protection Cover

To shield the OCXO from potential thermal variations and changes to airflow, enclose the device in a metal cover. The cover must be connected to the ground plane to avoid any electrical charge buildup. A mechanical drawing of a recommended cover is shown in the following figure.

Figure 12: Recommended Environmental Protection Cover



Chapter 4: Power Supply Filtering Information

Individual bypass or decoupling capacitors are recommended on each VDD pin whenever possible. These capacitors must be placed as close to the power pins as is practical. This is achieved by using 0402 placed in the ball field of the device.

Filter circuits are required for analog supplies. These filter circuits are used to attenuate noise on the power supply at frequencies where analog circuits are most sensitive. The power supply requirements are listed in the following table.

The overall noise ripple must not exceed the values listed in the following table. The filter must have adequate noise suppression such that a frequency from 50 kHz to 20 MHz meets the maximum allowable noise swing as described in the following table. The DCR of the ferrite should be selected to minimize the voltage drop associated with the filter circuit. The voltage drop due to any filter components must be considered such that the voltage specification (as measured at the device pins) is not exceeded. This implies that the power supply provided by the system must be rated better than the tolerance specified in the data sheet in order to compensate for the voltage drop across any filter circuit. The current rating of the ferrite bead should be at least 2x the expected current for the supply.

Table 3: Power Supply Filtering Information

Pin Name	Typical Voltage	Comments
Digital Power		
VDDO33_[14:0]	3.3V	Digital I/O power, Filter not required, noise < 100 mVp-p.
VDD1P8	1.8V	Digital I/O power. Filter not required.
IP_VDDO_1	1.2V	MDIO [5:0] voltage setting. Filter not required.
IP_VDDO_2	1.2V	MDIO [11:6] voltage setting. Filter not required.
VDDC	0.75V to 0.90V	Digital core voltage. This voltage should be adjusted based on the ROV/ AVS output status. Filter not required.
Analog Power		
TRVDD0P8_[3:0]	0.8V	Blackhawk transmitter/receiver voltage. Noise < 5 mVp-p, 50 kHz to 20 MHz. See the note on the following page.
TVDD1P2_[3:0]	1.2V	Blackhawk transmitter voltage. One per quadrant. Filter required, noise < 10 mVp-p, 50 kHz to 20 MHz.
BC[31:0]_PLL0_PVDD0P8 BC[31:0]_PLL1_PVDD0P8	0.8V	Blackhawk PLL voltage must be on a different supply from any other analog power rail (that is, TRVDD0P8). Filter required, one per Blackhawk core. Noise < 3 mVp-p, 50 kHz to 20 MHz.
TSC_MGMT_PVDD0P8	0.8V	Merlin core PLL voltage. Filter Required, noise < 3 mVp-p, 50 kHz to 20 MHz.
TSC_MGMT_TRVDD0P8	0.8V	Merlin core TX and RX voltage. Filter Required, noise < 10 mVp-p, 50 kHz to 20 MHz.
PCIE_TRVDD0P8	0.8V	PCIe transmitter/receiver voltage. Filter required, noise < 10 mVp-p, 50 kHz to 20 MHz.
PCIE_PVDD0P8	0.8V	PCIe PLL voltage. Filter required, noise < 3 mVp-p, 50 kHz to 20 MHz.

Table 3: Power Supply Filtering Information (Continued)

Pin Name	Typical Voltage	Comments
CORE_PLL_AVDD1P8	1.8V	Core clock PLL voltage. Filter required, noise < 30 mVp-p, 50 kHz to 20 MHz.
IP_PLL_AVDD1P8	1.8V	iProc PLL voltage. Filter required, noise < 30 mVp-p, 50 kHz to 20 MHz.
TS_PLL_AVDD1P8	1.8V	Time Sync PLL voltage. Filter required, noise < 30 mVp-p, 50 kHz to 20 MHz.
BS_PLL[1:0]_AVDD1P8	1.8V	BroadSync PLL voltage. Filter required, noise < 30 mVp-p, 50 kHz to 20 MHz.
VTMON*_AVDD1P8	1.8V	Filter required, noise < 30 mVp-p, 50 kHz to 20 MHz.

NOTE: The current requirement for the TRVDD0P8_[3:0] supply is greater than 15A per quadrant. Finding a suitable ferrite bead for the filter circuit may prove difficult. Therefore, filtering this supply is not required. However, the noise requirements for this supply must still be met. This implies that the voltage regulator design/output for this supply must be clean enough to meet the noise specification.

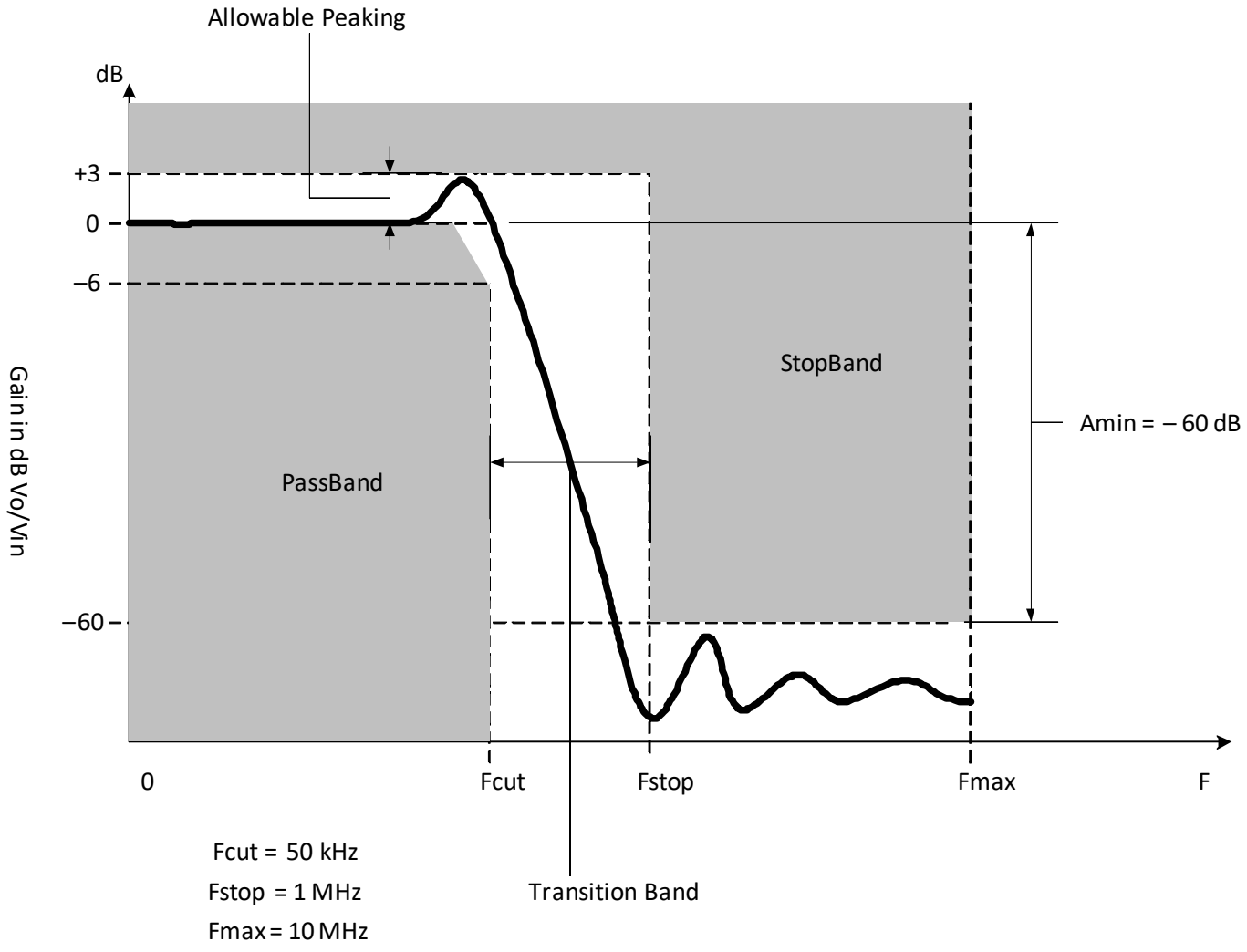
For the Blackhawk ball pattern, where the TRVDD and TVDD1P2 are located between the differential signals, control the crosstalk resonance by using the following:

- The TRVDD decoupling capacitor should be a 0402 type and should be soldered on the bottom side of the TRVDD and TVDD1P2 BGA via.
- The TRVDD and TVDD1P2 plane should be on the lower layers.

4.1 Analog Filter Requirements

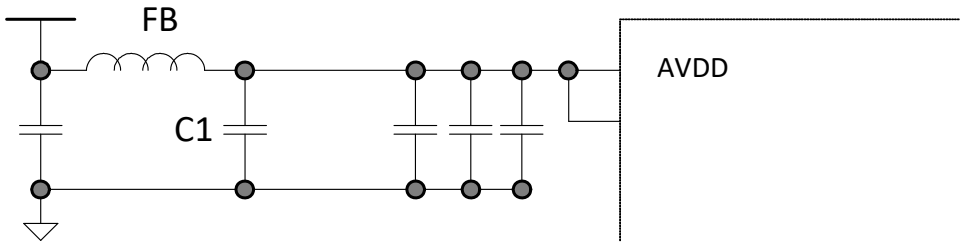
The following figure provides the AC requirements for the low-pass analog power filters along with all the PLL input pins on the device. This specification is designed to cover all of the analog power filters on Blackhawk and Merlin cores, and all individual PLL filtering requirements using external filter components.

Figure 13: AC Requirements for Analog Power Filters



A typical power supply filter circuit with decoupling capacitors are shown in the following figure.

Figure 14: Typical Power Supply Filtering Circuit



4.1.1 Power Supply Filter Component Examples

The following table lists examples of components that can be used for power-supply filtering.

Table 4: Example Components: Power Supply Filtering

Pin Name	FB	C1
TRVDD0P8_[3:0]	N/A	N/A
TVDD1P2	Taiyo Yuden FBMH2016HM121NT Z = 120Ω DCR = 15 mΩ i = 4.5A, 0805	22 µF
BC[63:0]_PVDD0P8	Murata BLM18KG331SN1D Z = 330Ω DCR = 80 mΩ i = 1700 mA, 0603	22 µF
PCIE_TRVDD0P8	TDK MMZ1608R601AT Z = 600Ω DCR = 400 mΩ i = 500 mA, 0603	22 µF
PCIE_PVDD0P8	TDK MMZ1608R601AT Z = 600Ω DCR = 400 mΩ i = 500 mA, 0603	22 µF
CORE_PLL_AVDD1P8	TDK MMZ1608R601AT Z = 600Ω DCR = 400 mΩ i = 500 mA, 0603	22 µF

Table 4: Example Components: Power Supply Filtering (Continued)

Pin Name	FB	C1
IP_PLL_AVDD1P8	TDK MMZ1608R601AT Z = 600Ω DCR = 400 mΩ i = 500 mA, 0603	22 µF
TS_PLL_AVDD1P8	TDK MMZ1608R601AT Z = 600Ω DCR = 400 mΩ i = 500 mA, 0603	22 µF
BS_PLL[1:0]_AVDD1P8	TDK MMZ1608R601AT Z = 600Ω DCR = 400 mΩ i = 500 mA, 0603	22 µF

Chapter 5: Power Supply Information

Additional information related to the supply voltages for the device are explained in the following sections.

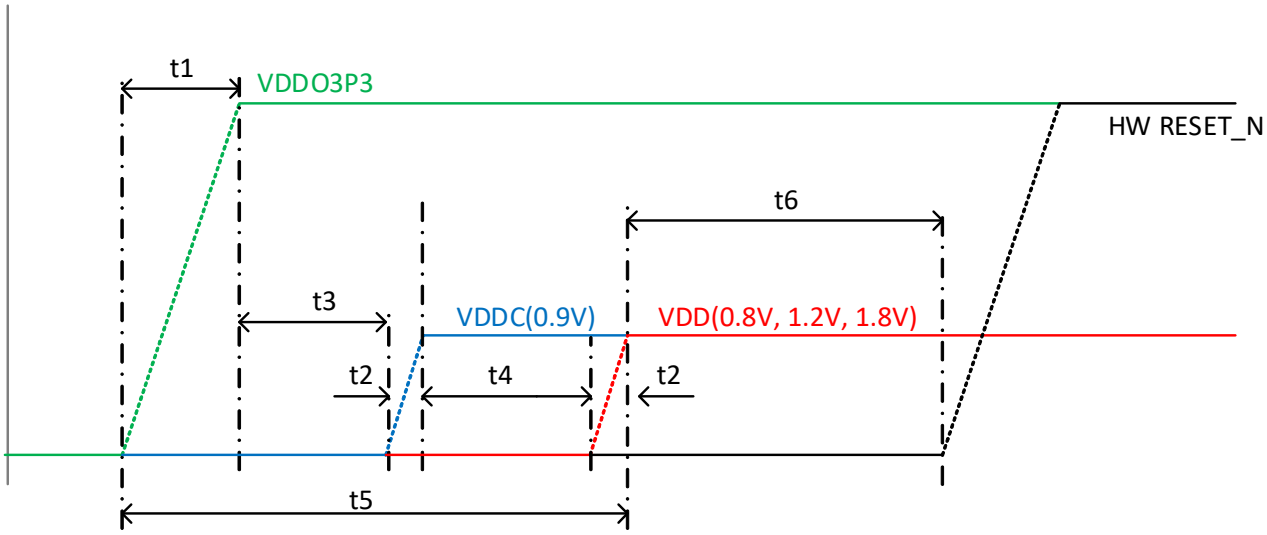
- Power-Up Sequence
- Power-Down Requirements
- Failsafe Requirements
- Recommended Operating Voltage (ROV)
- Power Distribution Network Requirements

5.1 Power-Up Sequence

As is common in multiple supply devices, the power supply pins may sink or source large amounts of current when a given supply is powered up while another is powered down. This may also be the case when supplies are partially powered at intermediate voltage levels (that is, when the 3.3V supply has ramped to 2.0V while the 1.0V supply is at 0.5V). This current is due to electrostatic discharge (ESD) diode paths and other supply-related current paths in the device.

In some cases, the power-up current may be on the order of several amps. This current does not damage the device, but it may affect the power supply or other related components. This high start-up current may cause damage to other board components (that is, the external transistor on a switching regulator if it is unable to support the current load).

Figure 15: Power-Up Sequence



t1: 3.3V supply ramp-up rate must be slower than 1V/200 µs → 660 µs min, (10 ms max.)
t2: Ramp-up rate for all other supplies must be slower than 1V/50 µs → @0.8V 40 µs min., @0.9V 45us min., @1.2V 60 µs min.
t3: Power-up delay of VDD core from VDDO3P3: 0 ms min
t4: Power-up delay of VDD0P8, VDD1P2, and VDD1P8 from VDD core: 0 ms min.
t5: All supplies must reach their final stable voltage levels within 10 ms
t6: Hardware reset must remain asserted for at least 80 ms after all supplies are up and stable

5.2 Power-Down Requirements

When the device is powered DOWN, the core voltage, VDDC, must ramp down to < 0.1V and maintain this level for at least 20 ms, before being powered back ON.

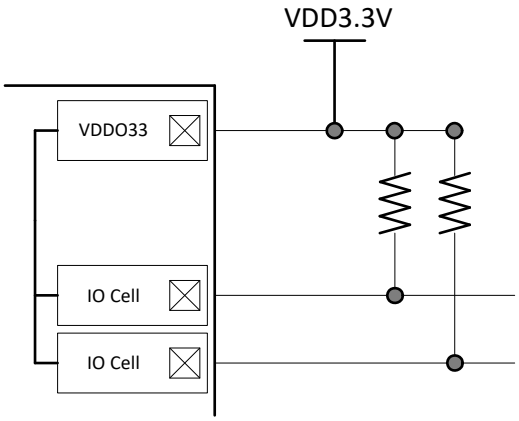
5.3 Failsafe Requirements

Failsafe I/O issues may occur when the power supplied to an I/O pad is removed, but the signal on the pin/pad is still present. This is applicable for 3.3V I/Os.

For the BCM56980, the following output pads require failsafe consideration. For these pins, any pull-ups attached to these pins must be connected to the same power rail as VDDO3P3.

- TX_OOBFC*
- L1_RCVRD_CLK*
- IP_LED*
- IP_QSPI*
- IP_UART*

Figure 16: 3.3V I/O Connection



5.4 Recommended Operating Voltage

The Recommended Operating Voltage (ROV) or Adjustable Voltage Scaling (AVS) feature helps reduce a device's power consumption and is mandatory for device operation.

The basic concept is that an AVS status is output from each device. This output represents the core voltage setting that ensures proper device operation to meet all data sheet specifications, minimizing the core current. This status can be obtained in two ways:

- Via AVS[7:0] pins.
- 8-bit register status.

For this feature to operate properly, the system must be designed with the capability to adjust the core voltage based on the AVS settings of a given chip.

When the AVS[7:0] pins are connected directly to the VRM, the output voltage is adjusted by the VRM to the proper level based on the state of the AVS pins.

If using the 8-bit status register to obtain the AVS state, it requires the host CPU to read the register, DMU_PCU_OTP_CONFIG_4 bits [15:8], in the switch chip containing the AVS value, then program the VRM using I2C/BSC to output the corresponding value.

The ROV feature is applicable to the core VDD rail and must not be applied to any of the analog or other non-core digital voltages.

Refer to the data sheet or the programmer's reference guide for operating voltage settings based on ROV pins or AVS status.

The following steps illustrate the procedure to adjust the voltage regulator:

1. Upon initialization, the CPU gets the ROV (AVS) status.
2. The CPU accesses the voltage regulator through the BSC/I2C interface.
3. Based on the 8-bit ROV status, the CPU issues a command to the voltage regulator to adjust its output voltage.

Frequently Asked Questions (FAQ):

- What is the default power-up voltage?
  - The default ROV voltage is specified in the data sheet.
- What is the minimum voltage that the regulator can be set without affecting the device from bootup at default?
  - The minimum is –3% of AVS_STATUS reading.
- Can this voltage scaling be applied to the analog voltage or just the digital core?
  - ROV is for the digital power (VDD and TSC*_VDD). This does not apply to voltage for PCIe and TRVDD0P8, PVDD0P8, TVDD1P2 analog blocks.
- Does the operating voltage tolerance range still apply irrespective of AVS_STATUS reading? For example, if it reads 0.90V, does ± 3% still apply?
  - Yes.
- Do noise tolerance requirements scale with voltage or remain the same?
  - Noise tolerance remains the same as per the hardware design guideline.
- Can it be operated at a higher voltage than AVS_STATUS indicates? For example, can it be operated at 0.90V with ± 3% when AVS_STATUS indicates 0.81V?
  - No, this is not allowed. This can lead to thermal runaway under heavy load.

- Does the ROV status indicate the center operating voltage or maximum operating voltage?
  - ROV status indicates the center operating voltage.
- What is the minimum/maximum range of the voltage regulator?
  - The adjustment range of the regulator should be greater than the data sheet specification for the AVS core voltage range.
- Does each part come with its ROV status preprogrammed and is this value permanent?
  - Yes. That means the CPU can read the AVS register once and permanently set the output of the regulator based on the reading. All subsequent power-up cycles can use the same ROV output setting without the need to adjust.

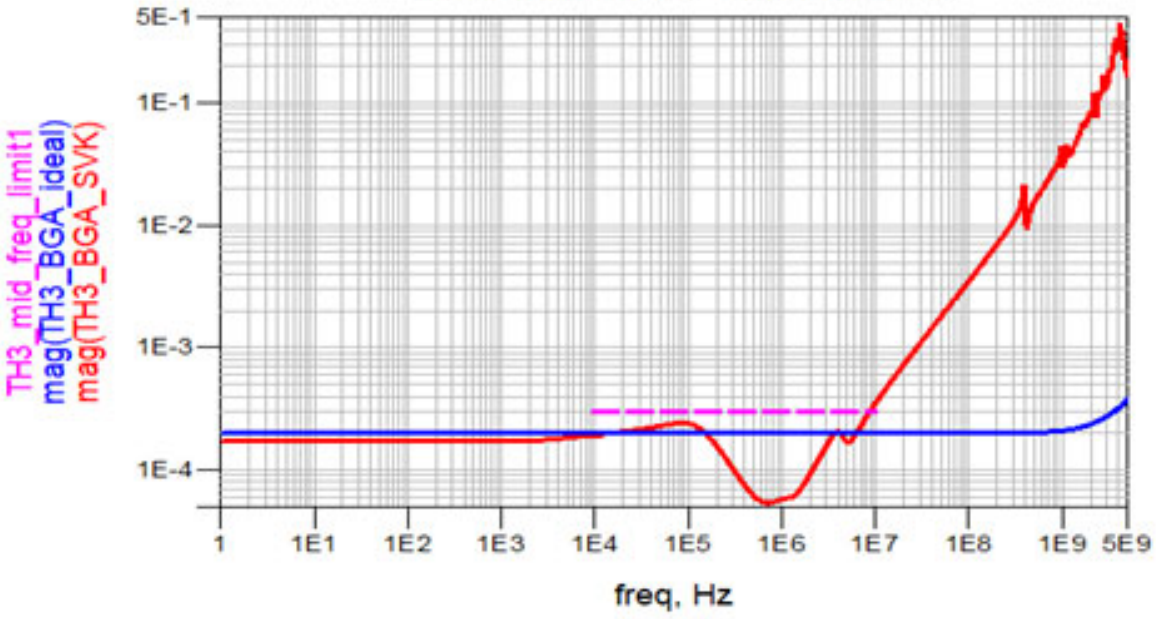
NOTE: If the AVS_STATUS indicates a voltage outside the operating range specified in the latest data sheet, the nominal voltage should be applied instead.

5.5 Power Distribution Network Requirements

As the operating frequency of digital systems increases, along with power demands, it becomes important to analyze power distribution networks (PDNs) of the PCB.

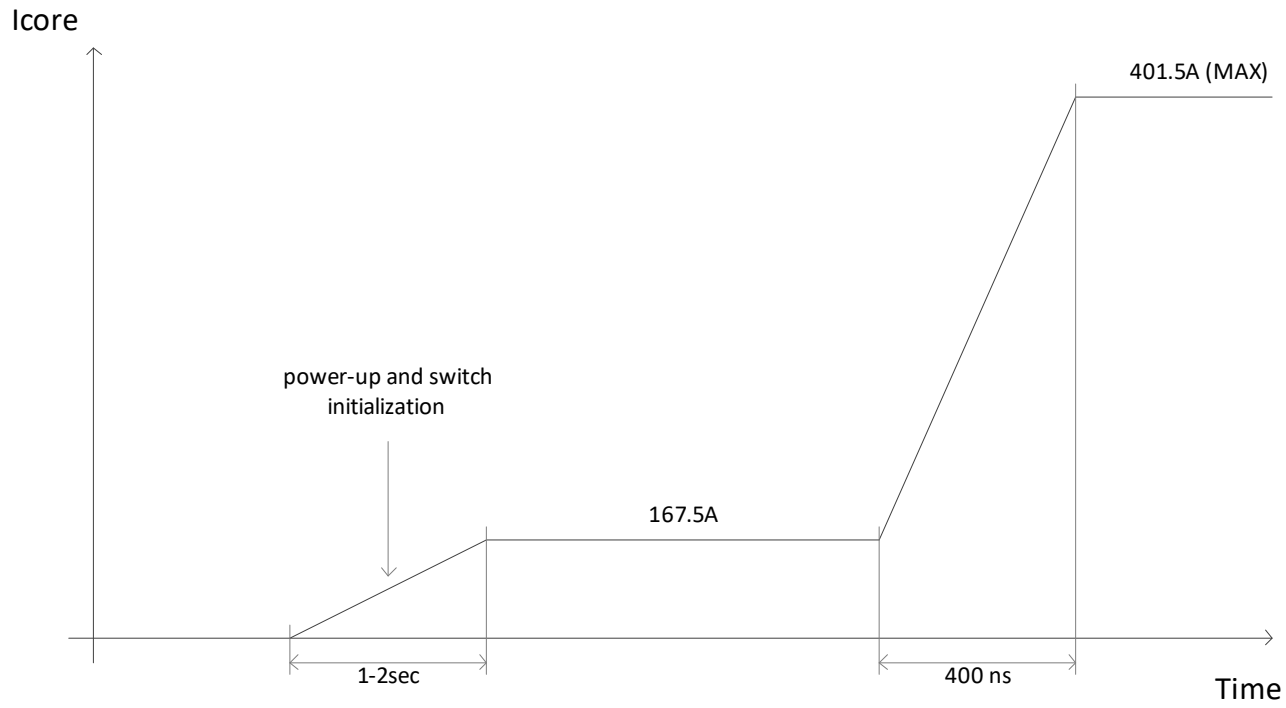
The BCM56980 SVK board core voltage impedance has the following profile, as shown in the graph in red. The blue line in the graph is the target impedance, 0.2 mΩ, at frequencies less than 10 kHz. The magenta line in the graph represents the target impedance of 0.3 mΩ, from 10 kHz to 10 MHz. Above 10 MHz, the impedance depends on the total capacitance.

Figure 17: BCM56980 Impedance Requirement



The following figure shows the expected current transients vs time. The worst case may occur when the device has completed initialization with all features enabled, then all ports start receiving maximum traffic at the same time.

Figure 18: Current Transients



NOTE: There is a high current consumption when the device is transitioned from steady-state to full-power mode. Because of this, the core voltage could momentarily dip below the specification level. Therefore, Broadcom recommends performing a proper simulation and work closely with your power supply vendor to employ the use of a load line feature, if necessary. Refer to the device SVK reference schematics for more details.

Chapter 6: PCB Layout Guidelines

The following section provides guidance for routing the high-speed SerDes signals on a PCB. Any routing scheme should be validated through IBIS AMI simulations.

- 50G PCB Layout Guidelines
- 25G PCB Layout Guidelines
- 10G PCB Layout Guidelines
- PCIe PCB Layout Guidelines

6.1 50G PCB Layout Guidelines

The 50G PAM4 speeds have the same UI as 25G. Therefore, refer to the 25G layout guidelines. AMI simulations are required for interfaces operating at this speed, consequently, these results may create additional layout requirements.

Although there are no IEEE channel crosstalk requirements for PAM4 53G, the following design practice may help to improve the margin and may mitigate possible issues in the PCB.

Pay special attention to the crosstalk of BGA escape via, QSFP via, and QSFP connector.

1. The BGA escape via needs careful optimization for RL and crosstalk. Use the TH3 SVK BGA escape as a reference. Note that the TH3 SVK: TX FEXT power sum is –40dB and the RX FEXT power sum is –47dB.
2. The QSFP via needs careful optimization for RL and crosstalk. Use the TH3 SVK QSFP-DD via design as a reference. The QSFP via crosstalk should be better than –40dB. In addition, use qualified QSFP connectors for PAM4 53G.
3. Verify the channel quality with IEEE COM simulations. Use a BER 1.5E-5 as the passing criteria, instead of a BER of 1E-4, as specified in the standard. This may provide some margin for any artifacts that might degrade performance.
4. Run AMI simulations of the full channel in Agilent/Keysight ADS: TH3 pkg + BH AMI model + channel model with crosstalk. The pre-FEC BER should be better than 1E-6 to have some guard band for the design.
5. The Blackhawk power, PVDD and TRVDD, must be referenced to GND (only). Any other voltage planes and shapes on an adjacent layer must not overlap with PVDD or TRVDD. For voltage planes/shapes on the same layer, there should be at least 40 mil separation from PVDD/TRVDD.
6. PCB differential target impedance 95Ω ± 10%.

6.2 25G PCB Layout Guidelines

This section describes the general PCB layout guidelines for Blackhawk applications for speeds up to 25 Gb/s. See the specific Blackhawk configuration section in this document for any additional PCB instructions. High-speed signal routing techniques are necessary when planning system layout and trace routing.

- PCB substrate recommendation is to use Megtron6.
- PCB glass should be selected such that it minimizes the effects of the fiber weave, such as 3313.
- Use hyper very low profile (HVLP) copper profile.
- Route high-speed signals as strip line.
- The maximum intra-pair signal length mismatch is 2 mils.
- The differential impedance target is 95Ω ± 10%.
- Trace width and intra-pair spacing is determined by the impedance target and board stack up.
- Wider traces are preferred to reduce copper loss, but should be < 10 mils.
- All signal via (pad, antipad) dimensions must be optimized for 95Ω impedance through simulation.
- The GND stitching vias must be included in the simulation.
- The simulation tool should be a 3D electromagnetic tool, such as HFSS.
- Vias for different layer transitions require separate optimization (that is, vias for L1–L4 transition may be different than vias for the L1 to L18 transition).
- Blind vias that have no via stubs are recommended.
- Via stubs must be removed by back-drilling. The worst-case via stub length should be included in the AMI simulation.
- To optimize channel performance, users should consider cutouts on BGA pads, connector SMT pads, and on AC coupling capacitors. The depth and dimension of the cutout should be determined by simulation to achieve optimal performance.
- All differential signals must be referenced to a GND plane.
- All GND islands along differential pairs must be stitched with a maximum spacing of 40 mils.
- Digital VDD and PVDD on adjacent PCB layers must not overlap.
- Digital VDD and PVDD on the same PCB layer should have a minimum spacing of 5x of PCB dielectric layer thickness.
- Use high-performance connectors that are certified for 25G.
- The trace breakout length should be as short as possible to minimize impedance discontinuities.
- Route traces with 50Ω geometries in break-out areas where traces are not tightly coupled.
- Via-in-pad is recommended, if possible.
- Avoid sharp bends in the trace routing; instead, use radius bend segments.
- Larger inter-pair spacing is preferred to reduce crosstalk. Minimum 4x trace-width spacing is recommended.
- If guard trace/ground patch is used between signal pairs, it must be stitched to GND. The distance between stitching vias should be less than 40 mils.
- Solid GND reference plane is required for signal traces. Splits or voids in the GND plane area under/above the signal trace are not allowed. The edge of a split/void in the reference plane must be at least 3x signal trace width from the signal trace.
- Match differential pair per segment close to the location of mismatch.
- The spacing between serpentine legs must be large enough, at least 5x trace width, to minimize the coupling between serpentine legs.
- The number of vias (layer transitions) in the signal path must be minimized.
- The number of vias within each leg of a differential pair must be the same. In addition, the via placement across the differential pair must be symmetric.
- Stitching vias at layer transitions are recommended.

- When placing series AC-coupling capacitors, sufficient lane-to-lane spacing should be maintained. Their placement in relation to those for an adjacent lane should not be so close as to enable coupling between lanes. The exact spacing is determined through simulation.
- The full channel should be simulated with SerDes AMI model to validate the system performance for both 10G and 25G.
- The recommended simulation tool is Agilent ADS. CSP LinkEye® is not available for this SerDes core.
- In ADS simulation, 15 mv/15 ps (HeightAtBER/WidthAtBER) margin is required for 10G, and 15 mV/6 ps (HeightAtBER/WidthAtBER) margin is required for 25G.

6.3 10G PCB Layout Guidelines

This section describes the general PCB layout guidelines for Blackhawk and Merlin core applications up to 10 Gb/s. High-speed signal routing techniques are necessary when planning system layout and trace routing:

- Board material recommendation is Nelco 4000-13.
- PCB trace is routed as a closely coupled differential pair (stripline or microstrip).
- PCB trace impedance – Nominal differential impedance of 95Ω ± 10%.
- For noise immunity, common mode noise, and current return path reasons, the high-speed signal traces must be referenced to the ground plane (if possible) for controlled characteristic impedance. At a minimum, the same reference plane must be used along the entire length of the trace path. Minimize the number of vias and avoid any discontinuities in the reference plane.
- Trace width/intra-pair spacing is dictated by the impedance target and board stackup. Wider traces are preferred to reduce loss, but do not use widths greater than 8 mils.
- Narrow differential trace width/spacing can be used to escape the ball field and must be kept as short as possible.
- Via-in-pad is recommended for escaping the package ball field.
- Avoid tight bends.
- Maximize inter-pair spacing to reduce crosstalk; at least 4x trace width spacing is recommended.
- Solid/continuous reference plane (GND) is required for signal traces. Splits or voids in the reference plane must be avoided.
- Blind vias, back-drilled vias, or both are recommended to remove the via stubs. At high data rates, via stubs can adversely impact the RL.
- The number of vias in the high-speed path must be minimized. Within the differential pair, there must be the same number of vias on the positive and negative signal traces with symmetrical via placement on the positive and negative signal trace.
- Stitching vias are recommended for signal layer transitions.
- Intra-differential pair length mismatch must be minimized. The length mismatch target between positive and negative signal is 4 mils (for SFI). Match differential pair per segment. Match near mismatch.
- Avoid overlapping VDD/GND islands/planes of different domains.
- Guard trace can be used to reduce crosstalk if board space is available. Guard trace needs to be connected to ground plane through stitching vias. The distance between stitching vias must not be bigger than 100 mils.
- When placing series AC-coupling capacitors, sufficient lane-to-lane spacing must be maintained. Their placement in relation to those for an adjacent lane must not be so close as to enable coupling between lanes. The exact spacing can be determined through simulation. This can be achieved by staggering their placement.

6.4 PCIe PCB Layout Guidelines

- All differential signals must have single-ended trace impedance of 50Ω and differential impedance of 100Ω.
- The trace lengths of each differential pair must be matched within 5 mils (0.005 in.).
- Do not put 50Ω termination resistors at the receiver inputs PCIE_RXDP and PCIE_RXDN. The PCIe core has integrated 50Ω termination resistors.
- Each TXDP signal must implement an on-board AC-coupling capacitor. Comply with the requirement of 75 nF to 200 nF, as stated in the PCI Express Base Specification Revision 1.0a, Section 4.3.3, Table 4-5.
- Vias must be kept to a minimum because a single via can contribute up to 1.0 dB loss to the overall loss budget, as specified in the PCI Express Base Specification Revision 1.0a, Section 4.3.2.1. Vias must always match in number on each differential pair.
- Vias must not have pads on unused layers when the differential signal must transition between layers of the PCB. The technique of removing all pads from unused layers helps prevent loss or helps reduce impedance discontinuities

6.5 High-Speed Clock Layout Guidelines

Take care when laying out the high-speed differential clocks for the device. Of critical importance are the BC6-7_REFCLK, BC24-25_REFCLK, BC38-39_REFCLK, and BC56-57_REFCLK differential pairs, because these are used to clock the Blackhawk and Merlin SerDes cores. Jitter on either of these reference clocks can significantly degrade the SerDes performance. Treat these clock nets as high-speed differential signals. As such, route these clocks as well-shielded differential pairs on an interior layer of the board. Additionally, back drill all vias associated with these clocks to minimize reflections caused by the fast rise and fall time required by these clocks.

6.6 Escaping the Ball Field

The BCM56980 ballout has been optimized to enable easier escape routes from the ball field. The package dimensions and ball pitch are the same as those used for the BCM56970 device. Similar signal escape routing techniques can be used for the BCM56980. For information, refer to the BCM56970 SVK schematic and layout.

Chapter 7: Guidelines for Unused Pins

This chapter provides guidance for the proper termination of any unused device pins.

Table 5: Unused Pin Connection

Pin Name	Direction	Connection
BS_PLL_REFCLK	IN	Each leg of the differential pair to GND through 0.01-µF capacitor
TS_PLL_REFCLK	IN	Each leg of the differential pair to GND through 0.01-µF capacitor
PCIE_RD	IN	NC
PCIE_TD	OUT	NC
IP_BSC_SCL	BOD	Pull up or down
IP_BSC_SDA	BOD	Pull up or down
LED_CLK	OUTPD	NC
LED_DATA	OUTPD	NC
IP_BS_CLK	BPD	NC
IP_BS_HB	BPD	NC
IP_BS_TC	BPD	NC
IP_TS_GPIO	BPU	NC
IP_G_GPIO	BPU	NC
MHOST_BOOT_DEV	IPD	NC
L1_RCVRD_CLK	OUT	NC
L1_RCVRD_CLK_VALID	OUT	NC
L1_RCVRD_CLK_BKUP	OUT	NC
L1_RCVRD_CLK_VALID_BKUP	OUT	NC
IP_QSPI_4BYTE_ADDR	IPD	NC
IP_QSPI_ADDR_BPC_MODE	IPD	NC
IP_QSPI_DUAL_LANE	IPD	NC
IP_QSPI_QUAD_LANE	IPD	NC
IP_UART_CTS_N	IPU	NC
IP_UART_SIN	IPD	NC
IP_UART_RTS_N	OUT	NC
IP_UART_SOUT	OUT	NC
IP_MDC	OUT	NC
IP_MDIO	BOD	NC
TX_OOB_STATS_CLK	OUT	NC
TX_OOB_STATS_DATA	OUT	NC
TX_OOB_STATS_SYNC	OUT	NC

7.1 Unused PCIe Pins

If some lanes of the PCIe interface are not used, it is preferable to leave the pins floating for RX or TX. The RX inputs use internal 50Ω to ground, and the TX outputs have internal 50Ω to VDD.

7.2 Unused Blackhawk and Merlin Core Pins

All Blackhawk and Merlin cores must be powered, even if they are not used. All RVDD, TVDD, PVDD, and (TSC) VDD supplies must be provided to their specified voltage levels with the recommended power supply filtering.

The unused RDP/N receiver input pins can be connected to GND, and the TDP/N transmitter output pins can be left NC.

Chapter 8: Blackhawk Modeling and Simulations

For a high-speed SerDes such as Blackhawk, simulations are required to validate the system design and to provide performance estimations in the form of bit error rate (BER).

The simulations should include the worst-case channel and a detailed analysis of the system should be performed.

8.1 Blackhawk IBIS-AMI Model

The Blackhawk IBIS-AMI model (available on the Broadcom Customer Support Portal [CSP]) includes the following:

- TX path:
  - Analog front end (AFE), modeled by a separate S-parameter.
  - TX pre-emphasis equalizer.
- RX path:
  - Analog front end (AFE), modeled by a separate S-parameter.
  - RX equalizer (PF, VGA, and DFE).

8.1.1 PAM4

The Blackhawk PAM4 IBIS-AMI is a pre-FEC model, so the BER at which eye-height and eye-width are evaluated is very high (for example, 10^{-4} or 10^{-5}). There is no RX eye opening as recommended pass/fail criteria, but instead, the overall BER is the only measurement of the RX performance. This is evaluated by the EDA tool on all eyes (based on the RX sensitivity) and should be used for pass/fail criteria.

In other words, the eye provided by the EDA tool should not be compared to any pass/fail criteria mask. The BER reported by the EDA tool is the pre-FEC BER of the link.

At this stage of the Blackhawk design validation, the requirement for PAM4 simulations is to have a pre-FEC BER of ~1.5×10^{-6}. This should translate to a post-FEC BER of ~10^{-15}.

Chapter 9: Heat Sink Selection and Attachment

The device is required to be used with a heat sink. The end-use thermal environment combined with the operating mode of the device dictates the required thermal characteristics (size, thermal resistance, and so forth) of the heat sink.

The heat sink used with the BCM56980 device package is required to be mechanically mounted to the device. Adhesive-based, or taped-based attachment schemes are not recommended. In a mechanically-mounted configuration, contact between the heat sink and the package is maintained using an externally applied mechanical force. The heat sink should be held in place by clamp or fixture to the printed circuit board. The heat sink must not be clamped to the package (the package/ heat sink combination must not be free-standing).

A non-adhesive thermal interface material, such as gap filler, phase change film, or thermal grease, is recommended between the heat sink and the package top to maintain a low thermal resistance path between the package and the heat sink. The applied operating force between the heat sink and the package must be sufficient to meet the thermal interface material manufacturer's recommendations. The exact configuration of the mounting scheme and clamping mechanism is at the user's discretion. For many applications, the recommended maximum force at steady state is 85 pounds with the condition that the solder ball diameter is less than 0.81 mm after surface mounting the BGA device. Using a higher force can be helpful in improving the heat sink to BCM56980 contact. However, a compression force greater than 85 pounds also reduces the BGA ball-to-ball clearance over the lifespan of the device and creates risks of leakage, short, and electrical coupling issues in dusty and high-humidity environments. A maximum instantaneous mounting force can not exceed 150 pounds. For applications requiring a compression force greater than 85 pounds, it is recommended that customers perform system-level compression force reliability tests. The guidelines for system-level compression force reliability tests can be found on the Broadcom Customer Support Portal (CSP), *SMT Load-Force Recommendations Ver 09272018* (BRCM-Load-Force-Qual-Requirement_9-27-2018).

- The applied operating force must be evenly distributed across the package top.
- Tooling holes, clamp locations, or both must be selected to minimize PCB warpage.
- The clamping mechanism must not clamp to the package underside.
- The clamping structure must withstand the user's mechanical testing requirements, such as shock and vibration.

Chapter 10: Debug and Bring-up Recommendations

The BCM56980 is a high-performance device with many industry-leading features. It is highly recommended to make certain signals accessible in the design to aid in system bring up and lab debug. The following table provides a list of signals that may be useful for debugging.

Table 6: Useful Signals for Debugging

Signal	Purpose
PCIE_INTR_N	Out-of-band mechanism to monitor interrupts.
MHOST0_BOOT_DEV BOOT_DEV[2:0]	Modify the PCIe boot process.
IP_QSPI_*	Allow PCIe firmware download.
PCIE_FORCE_GEN[1:0] PCIE_FORCE_LANE[1:0]	Override PCIe interface parameters.
IP_BSC2_SCL IP_BSC2_SDA	Low-level access to PCIe and iProc subsystems.
IP_G_GPIO[9:0]	Allow information to be output onto this interface.
IP_TS_GPIO[5:0]	GPIO from TS core.

Revision History

56980-DG108; October 30, 2019

- Updated Chapter 9, Heat Sink Selection and Attachment. Increased the maximum force at steady state from 50 pounds to 85 pounds.
- Updated Table 6, Useful Signals for Debugging.
  - IP_G_GPIO[15:0] → IP_G_GPIO[9:0]
  - Added IP_TS_GPIO[5:0].
- Added Section 2.3.3, Active State Power Management.
- Added Section 2.3.4, PCIe Reset.
- Added Chapter 10, Debug and Bring-up Recommendations.

56980-DG107; June 21, 2019

- Added Blackhawk ball pattern information to control crosstalk resonance to Chapter 4, Power Supply Filtering Information.

56980-DG106; November 27, 2018

- Updated Chapter 9, Heat Sink Selection and Attachment to provide recommendations for the operating force between the heat sink and the package.

56980-DG105; July 16, 2018

- Updated Blackhawk and Merlin cores PCB differential Trace Impedance requirements from 100Ω to 95Ω.
- Updated AVS voltage range to 0.75V-0.90V ±3% in Table 3, Power Supply Filtering Information and Section 5.4, Recommended Operating Voltage (ROV).
- Added Chapter 9, Heal Sink Selection and Attachment information from data sheet.

56980-DG104; May 14, 2018

- Updated Table 2, 56980 Reference Clock Summary
- Updated Section 3.2, BC_[A:H]_REFCLK and TSC_MGMT_REFCLK Connection
- Updated Figure 6, BC_[A:H]_REFCLK and TSC_MGMT_REFCLK Connection

56980-DG103; February 15, 2018

- Added a requirement for BC_PLL_PVDD0P8 to be on a different voltage source than TRVDD0P8. See Table 3, Power Supply Filtering Information.
- Added recommendation that TRVDD0P8, BC_PLL_PVDD0P8, TVDD1P2 not be on an adjacent layer to VDDC. See Section 6.1, 50G PCB Layout Guidelines.
- Added recommendation to have a GND layer above and below TRVDD0P8, TVDD1P2, and BC_PLL_PVDD0P8 layers. See Section 6.1, 50G PCB Layout Guidelines.
- Added additional clock connection diagrams for clarity (Figure 5, Figure 6, and Figure 7).
- Added second Note after Table 3, Power Supply Filtering Information.
- Added additional information to Section 6.1, 50G PCB Layout Guidelines.
- Updated Table 3, Power Supply Filtering Information. Corrected typo. Changed VDDC Typical Voltage from “0.81V—0.96V” to “0.81V—0.89V”.

- Updated Table 3, Power Supply Filtering Information. Updated comments for BC[31:0]_PLL0_PVDD0P8 and BC[31:0]_PLL1_PVDD0P8.
- Updated Table 4, Example Components: Power Supply Filtering. Updated comments for BC[63:0]_PVDD0P8.
- Changed “Questions and Answers” in Section 5.4, Recommended Operating Voltage (ROV) to Frequently Asked Questions (FAQ). The text in this section was also updated.

56980-DG102; November 29, 2017

- Modified Table 2 Reference Clock Summary, for PCIE_REFCLK to add external AC coupling to protect the internal ESD-protection diode circuit.
- Addition to Section 2.3.1, PCIe Gen3 Specific Information (see note), added a reference to SVK schematic for connection of the memory to the QSPI interface. This also includes an example part.
- Added Section 5.5, Power Distribution Network Requirements added PCB impedance profile for VDDC.
- Updated Section 6.2, 25G PCB Layout Guidelines, removed the via stub length and VIA cutout requirement. This should be determined through simulation for optimizing channel performance.

56980-DG101; October 6, 2017

- Updated Table 1, Speed Mode Examples to correct typos in 25G-KR, CR Lane Baud Rate and 40G-KR4, CR4 VCO Freq.
- Added last paragraph and two bullets to Section 2.1.3, Lane Swapping to clarify the restrictions on lane swap capability.
- Added Section 2.1.6, Port and Bandwidth Distribution to optimize switch performance.
- Changed Description column of (last) PCIE_REFCLK row of Table 2, 56980 Reference Clock Summary to emphasize on clock termination.
- Added Note about how to treat AVS_STATUS relative to operating voltage at the end of Section 5.4, Recommended Operating Voltage (ROV).

56980-DG100; August 31, 2017

Initial release.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