APPLICATION NOTE

BCM5226

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Revision AN01-R

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OVERVIEW

This application note provides detailed information regarding the use of Broadcom's highly integrated BCM5226 HEX-Φ .25 micron 10/100 Physical Layer Device. This six-channel integrated PHY is intended for applications demanding extensive horizontal integration. The BCM5226 is ideal for a variety of switch and dual-speed repeater implementations (see Figure 1 below). You can configure each of the six ports independently to operate in 10BASE-T, 100BASE-TX, or 100BASE-FX mode.

There are two versions of the BCM5226. The BCM5226R includes both the RMII™ (Reduced Media Independent Interface) and SMII™ (Serial Media Independent Interface) interfaces. These protocols allow for dramatically reduced pin count and interconnection complexity between the multi-port MAC or switch ASIC and the BCM5226. The BCM5226S version of the chip utilizes the SMII™ Interface in a smaller package.

The BCM5226R HEX-Φ is available in a 160-pin MQFP package and the BCM5226S HEX-Φ is available in a 128-pin MQFP package.

Read this application note in conjunction with the latest version of the BCM5226 Data Sheet.

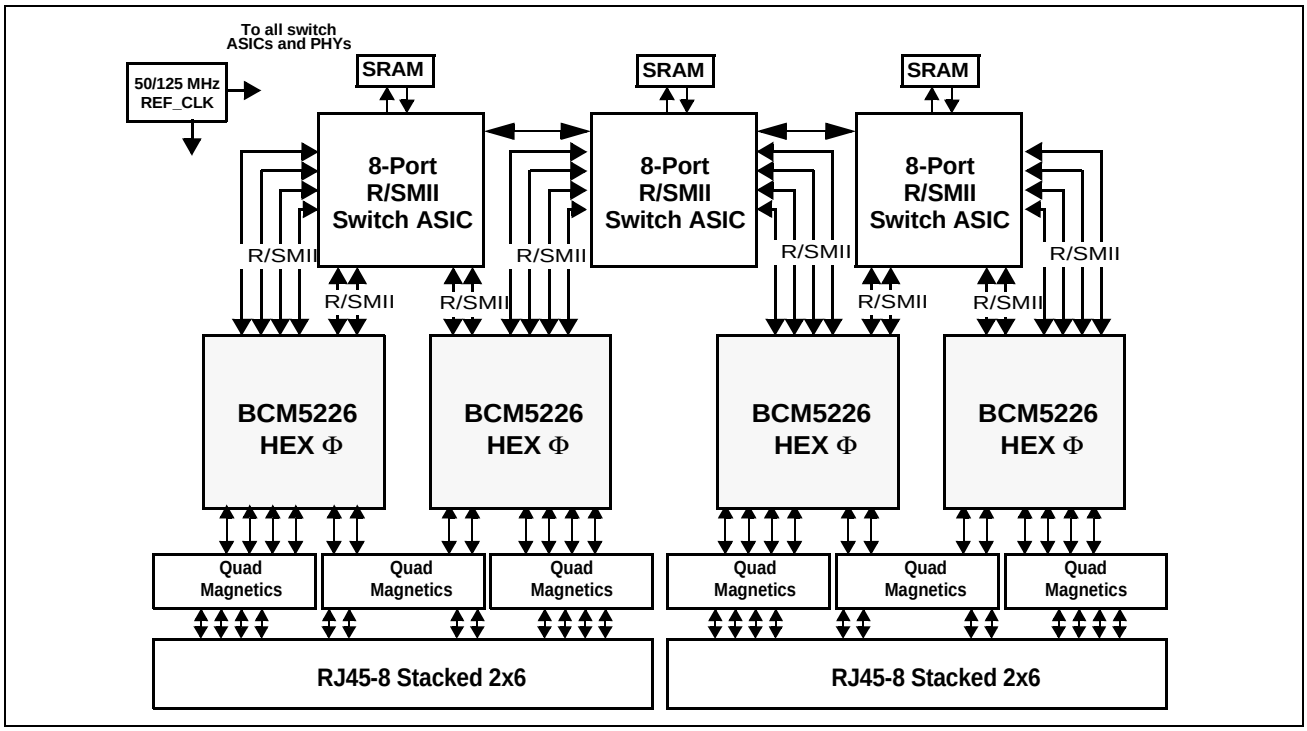

Figure 1: Typical 24-Port Switch (Unmanaged) System Diagram

2.5V/3.3V TOLERANCE

The BCM5226 is a dual-supply device utilizing both 2.5V and 3.3V supplies. This provides a significant power savings for the overall system. The BCM5226 is designed to interface with both 2.5V and 3.3V ASIC implementations. Note that presenting a 5V input level to any of the digital inputs of the BCM5226 may result in forward biasing the internal protection diode, resulting in a near short-circuit load and potential damage to the device.

LED CONSIDERATIONS

SERIAL LED MODE

The BCM5226 provides LED indications on a per-port basis via the Serial LED Mode. To configure the BCM5226 for Serial LED mode, the SERIAL_LED_EN pin must be tied high (4.7 KΩ to Vdd or direct connection to Vdd) during reset. Figure 2 below illustrates a typical implementation for supporting the serial LED mode. While cost is a factor in implementing the external circuitry required for serial LED operation, you gain a substantial savings in both board real estate and routing complexity. In this mode, the BCM5226 sources a serial data stream, the associated clock, and a framing signal, as follows:

Serial data stream: SLED_D0. An active low bit stream comprised of contiguous 36 bit frames (sourced from pin 68(BCM5226S) or pin 122(BCM5226R)).

Serial data clock: SLED_CLK. SLED_DO is clocked out on the falling edge of SLED_CLK which runs at 1MHz (sourced from pin 113(BCM5226S) or pin 18(BCM5226R)).

Framing Pulse: SLED_FRM. Logic high pulse occurring once every 36 SLED_DO bit times (sourced from pin 112(BCM5226S) or pin 17(BCM5226R)).

Note

If the SERIAL_LED_EN pin is left unconnected or pulled low during reset, the BCM5226 enters the PHY Interrupt Mode and no LED information is provided on the Serial LED Data line.

SFRM goes high coincident with bit zero of port 1.

The example in Figure 2 on page 4 is based on standard 3.3 V tolerant CMOS 74HC594 serial-to-parallel shift registers. The value for each of the series current limiting resistors that accompany each LED depends on the electrical parameters of the LED as well as the voltage the LED is connected to.

Because each BCM5226 produces a serial LED bit stream frame length of 36 bits (six bits per port), the remaining four outputs of the fifth 74HC594 shift register are unused in this example. Substituting the fifth 74HC594 with an equivalent four-bit parallel-to-serial shift register may be a practical substitution depending on manufacturing requirements.

The BCM5226 incorporates three options for providing LED and Interrupt information from the Serial LED bit stream. When Serial LED Mode is enabled (SERIAL_LED_EN pin sampled as a logic high during reset), and no further action is taken, the default Normal mode is selected. You can set Bit 14 and 15 in register 1Ah to select the other modes as defined in Table 1 below.

Table 1: Serial LED Mode Bit Framing

OPTION	*REG 1Ah*	*Serial Bit 5*	*Serial Bit 4*	*Serial Bit 3*	*Serial Bit 2*	*Serial Bit 1*	*Serial Bit 0*
Normal	Bit14 = 0 Bit15 = 0	FDX	COL	Speed100	Link	Transmit	Receive

Table 1: Serial LED Mode Bit Framing (Cont.)

OPTION	*REG 1Ah*	*Serial Bit 5*	*Serial Bit 4*	*Serial Bit 3*	*Serial Bit 2*	*Serial Bit 1*	*Serial Bit 0*
Interrupt	Bit14 = 1 Bit15 = 0	FDX	Global Interrupt	Speed100	Link	Slice Interrupt	Activity
Full-Duplex	Bit14 = 0 Bit15 = 1	FDX	COL	Speed100	Link	FDX	Activity

Note

A Global Interrupt indicates an interrupt from any of the six PHY slices as if they were ORed together. A Slice Interrupt is provided on a per-PHY basis. Refer to the register bit descriptions for register 1Ah in the BCM5226 datasheet for more information about interrupt handling.

The LED indicators in the example in Figure 2 on page 4 reflect the default Normal serial LED data stream content.

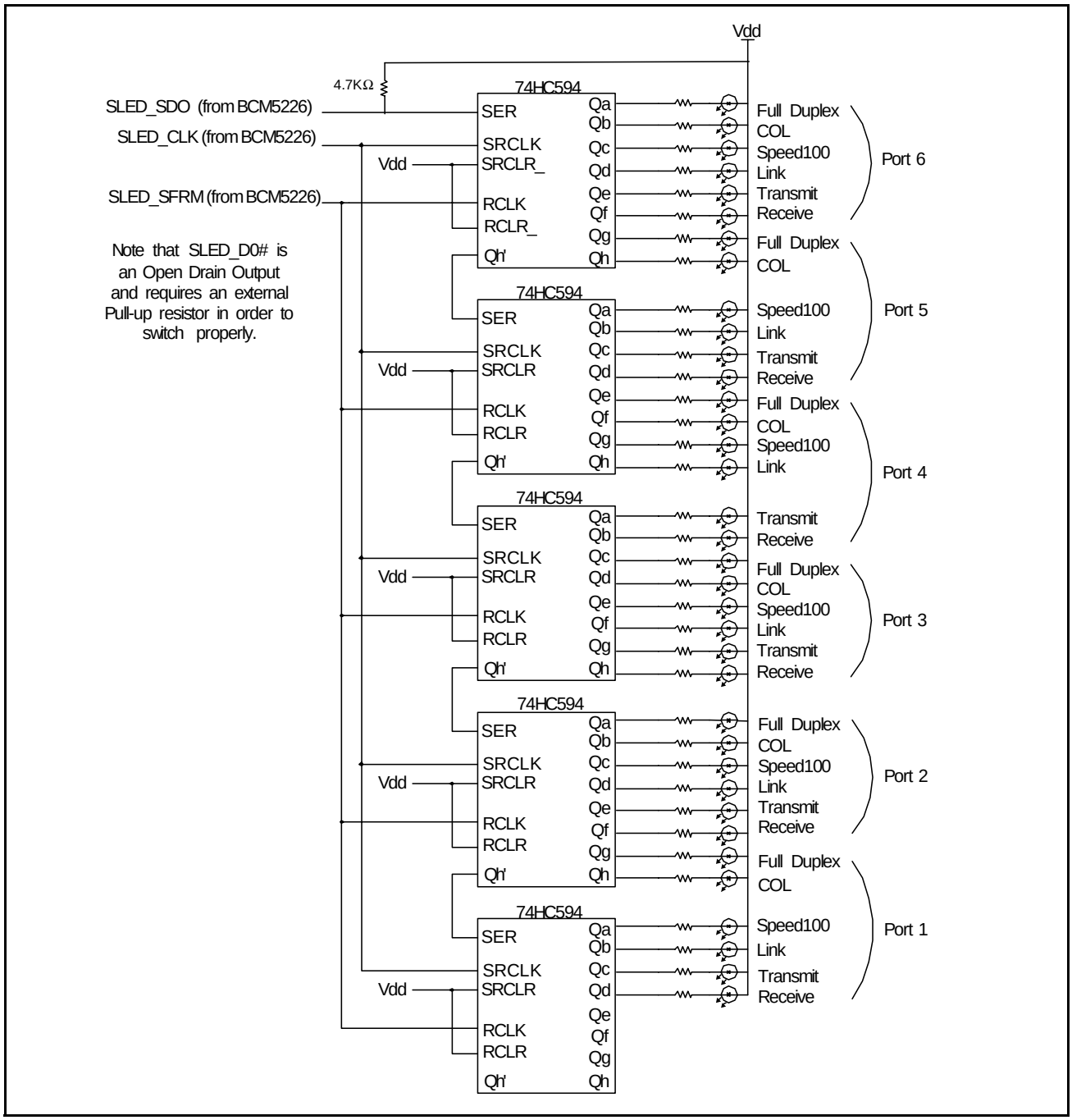

Figure 2: BCM5226 Serial LED Implementation (Normal Mode)

INTERNAL PULL-UPS AND PULL-DOWNS

This section lists the inputs, and combination input/outputs, that include internal resistive pull-ups or pull-downs. The value of each pull-up and pull-down is approximately 50 KΩ (+/-20%).These internal pull-ups and pull-downs have been included in order to minimize the number of external passive components that would otherwise be required.

Internal Pull-Ups.

- F100
- RESET#
- MDIO (combination I/O)
- ANEN
- ER[1:0]
- TDI (JTAG)
- TMS (JTAG)
- TCK (JTAG)
- TRST# (JTAG—this pin must be externally pulled low (1 KΩ to GND) for normal operation)
- SMII_EN/SLED_CLK (combination I/O)

Internal Pull-Downs.

- TXD[1:0]{1:6}
- TX_EN{1:6}
- TX_ER{1:6}
- MDC
- SERIAL_LED_EN (combination I/O)
- FDXEN (FDXEN pin level is logically ORed with bit 8 of register 00h for each port)
- MDIX_DIS (combination I/O)
- TESTEN
- SSYNC
- SD+{1:6}
- SD-{1:6}
- PHYAD{4:0}
- MST_PHY_ADR/SLED_FRM (combination I/O)

REFERENCE CLOCK

The BCM5226 REF_CLK input accepts different clock frequencies depending on the selected mode of operation. Because this is a single-ended clock input, there are no provisions for connecting a stand-alone crystal directly to the BCM5226.

The input frequency accuracy, regardless of the frequency, is +/-50ppm and the duty cycle must be between 35% and 65% inclusive.

Note

IIMPORTANT: The use of PLL based oscillators as a source for any Physical Layer devices' local Reference clock is strongly discouraged as this can result in Interoperability issues in the field.

When RMII operation is selected (version BCM5226R only), the REF_CLK requires a 50-MHz reference. Figure 18 on page 25 illustrates RMII clock interconnection. When SMII operation is selected (BCM5226R or BCM5226S), the REF_CLK input requires a 125-MHz reference. Figure 19 on page 27 illustrates a typical SMII clock interconnection.

RDAC PIN

The 100BASE-TX and 10BASE-T transmit amplitudes can be directly controlled by adjusting the amount of current allowed to flow from the RDAC pin to GND. It is recommended that in order to verify proper transmit signal amplitude for a given design, an initial value of 1.24 KΩ (+/- 1%) be used for the external RDAC resistor (refer to Figure 8 on page 15). It is important to note that the transmit signal amplitude can be affected by magnetics insertion loss, as well as stray capacitance in the front-end design. Therefore, it is always important to quantify these additional possible sources of attenuation and adjust the value of the RDAC resistor accordingly to compensate.

Note that a 1% change in RDAC current produces a 1% change in transmit amplitude at the TD+/- outputs. Additionally, it is not recommended that the RDAC resistor value be adjusted beyond 5% of nominal, as this also affects internal reference currents other than the Transmit DAC and may adversely affect device performance.

100BASE-FX

The BCM5226 supports 100BASE-FX operation via the SD+/-, RD+/-, and TX+/- pins. The connection diagrams in Figure 3 on page 8 illustrate the proper termination and level shifting required to interface the BCM5226 to a 3.3V fiber transceiver. Only the data interface and associated termination is illustrated, refer to the fiber transceiver manufacturer's guidelines for transceiver power supply connection and filtering recommendations.

The TD+/- and RD+/- signal traces between PHY and the fiber transceiver should each be routed with a characteristic impedance of 50 Ω in order to match the termination impedance. The SD+/- traces do not require special impedance considerations due to the static nature of signal detect.

The BCM5226 is configurable for 100BASE-FX operation on a per-port basis by using the Signal Detect input pins (SD+/-). A given port configures to 100BASE-FX mode if its corresponding SD+/- inputs are presented with a valid PECL differential signal (i.e., Signal Detect assertion or deassertion as sourced by the fiber transceiver). The BCM5226 configures to twisted pair operation when the SD+/- inputs are held low (<0.4V). Because the SD+/- inputs incorporate internal pull-down resistors, leaving them unconnected or pulling them to ground externally configures that port for twisted pair operation.

When configured for 100BASE-FX operation, the BCM5228 automatically disables Auto-Negotiation regardless of the state of the ANEN pin. This ensures graceful behavior when configured for 100BASE-FX both in terms of standard fiber signaling as well as during device reset.

Duplex mode of operation depends on the Link partner (note that there is no direct means of communicating duplex status between link partners at the PHY level while in 100BASE-FX mode). It is therefore up to the user to determine the appropriate duplex mode, perhaps as a function of the application layer of the system. While most 100BASE-FX links run in Full Duplex, it is not always the case as with fiber connections to half-duplex repeater domains.

Hewlett Packard and Infineon both manufacture high-quality 100BASE-FX transceivers. You can find more information about them at their websites:

Hewlett Packard	http://www.hp.com/HP-COMP/fiber/
Infineon	http://www.infineon.com/products/37/37.htm

The trend in Fast Ethernet 100BASE-FX transceiver modules is shifting toward the use of smaller footprint 3.3V Mini MT-RJ modules. These 10-pin miniature modules take the same amount of space as a single RJ45-8 media connector and are electrically equivalent to existing 3.3V 9-pin LCF transceiver modules. Further information on Mini MT-RJ modules is available on the following websites:

Hewlett Packard	http://www.hp.com/HP-COMP/fiber/
Amp, Inc.	http://www.amp.com/networking/pdf/mtrjwp.pdf

SD+/-

Assuming you use a 3.3 V fiber transceiver, be sure to properly level-shift the SD+ signal from the fiber transceiver to the BCM5226, as shown in Figure 3 on page 8. Because the SD signal from the transceiver is essentially static, you do not need to treat the SD+ trace as a transmission line. A simple level shifter is required, and its placement relative to either the BCM5226 or the fiber optic transceiver is non-critical. As with any interface, keep trace lengths to a minimum wherever possible. The SD- input of the BCM5226 requires an external bias of 1.25V to ensure that the differential SD+/- input functions properly. Should multiple BCM5226 ports be configured for 100BASE-FX operation, tying multiple SD- pins together and connecting this common point to a single voltage dividing resistor network is acceptable.

RD+/-

Because the RD+/- inputs of the BCM5226 are internally biased to 1.7 V, and because typical 3.3 V fiber transceivers normally source PECL with a Vbb (center of the voltage swing) of approximately 2.0 V, level shifting is required. Also, if the system layout requires that the RD+/- trace lengths to be more than approximately one inch, set up the termination to account for transmission line effects.

TD+/-

The BCM5226 employs current-sink outputs to transmit the 100BASE-FX signaling to the fiber transceiver, so a special level shifting and impedance matching termination network must be implemented, as shown in Figure 3. The slight mismatch in the voltage divider circuit for the TD+ versus TD- ensures that the TD+/- input of the fiber transceiver will not switch due to noise that may be present when the BCM5226 is quiet (for example, during device reset).

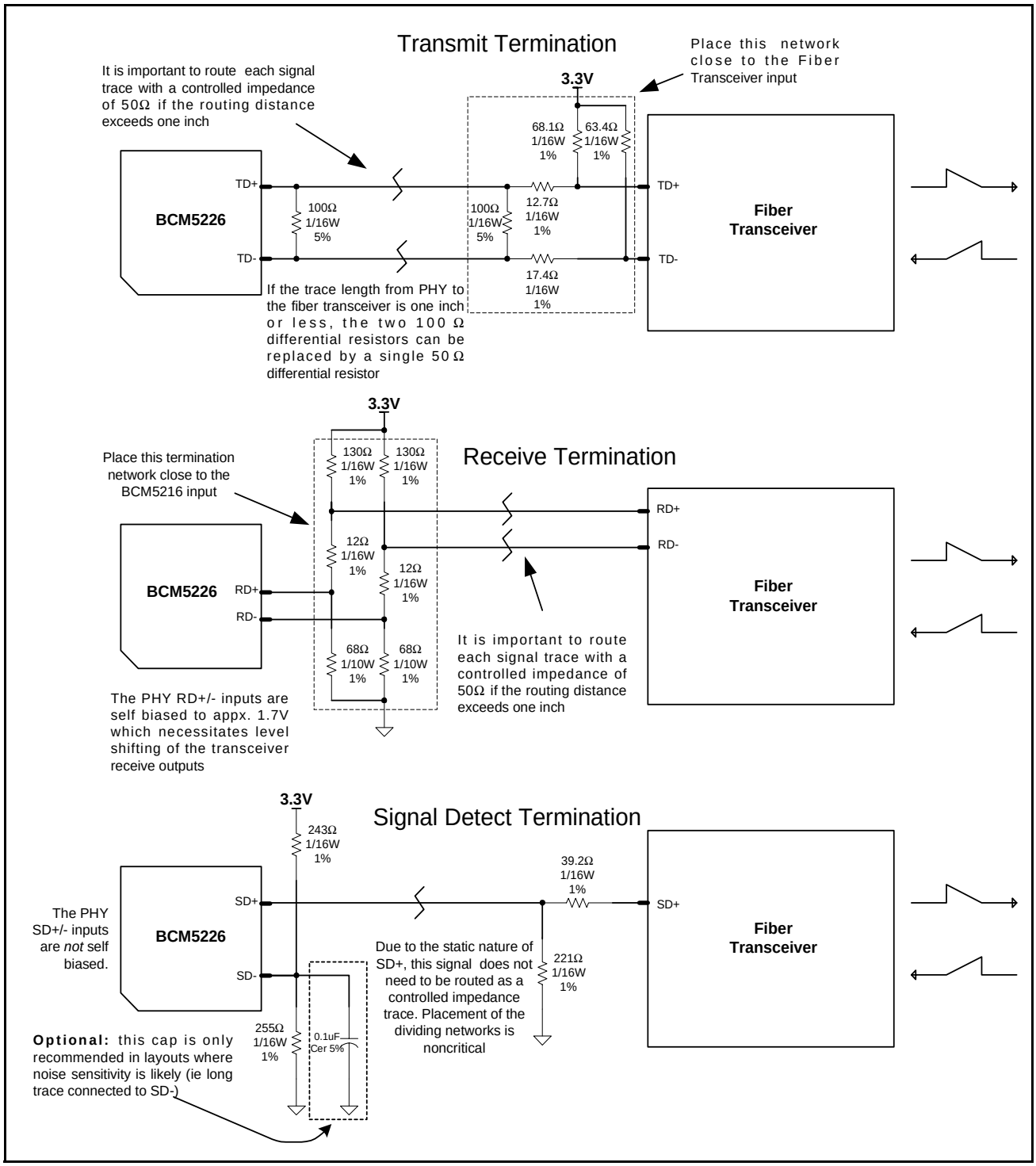

Figure 3: BCM5226 3.3 V 100BASE-FX Interface (One Port Shown)

RMII (REDUCED MEDIA INDEPENDENT INTERFACE)—BCM5226R ONLY

This section describes the RMII interface. You can find the latest draft of the RMII Specification on the World Wide Web at:

RMII Consortium http://www.rmii-consort.com

Additionally, Core-El offers an RMII Test Bench package, which you can find on the Web at:

Core-El http://www.coreel.com

The BCM5226R (160-pin package only) operates in RMII mode when not configured for SMII operation (SMII_EN [pin 18] pulled low).

For a given BCM5226R port, the RMII consists of seven pins:

- RXD[1:0]—di-bit (half-nibble) data bus for the receive data (two output pins)
- TXD[1:0] —di-bit (half-nibble) data bus for the transmit data (two input pins)
- CRS_DV—receive data control output pin
- RX_ER—receive error control output pin
- TX_EN—transmit data control input pin

Additionally, a single 50 ppm 50 MHz reference clock input, which is shared across all ports, is required. This clock can be sourced either by the switch or MAC ASIC, or by a separate clock source, such as a 50 MHz crystal oscillator.

During 100 Mbps operation, the di-bit receive data is transferred across the RMII at 50 MHz and is sampled by the switch or MAC ASIC once every 20 ns. During 10 Mbps operation, the data is also transferred across the RMII at 50 MHz; however, because the data rate is only 1/10th that of 100 Mbps operation, the switch or MAC ASIC samples the data once every 200 ns. The same speeds and sampling rates described for the RMII receive data apply to the RMII transmit data (from ASIC to PHY) as well.

TRANSMIT RMII

The RMII carries the transmit data (TXD[1:0]) and transmit enable control signal (TX_EN) from the switch or MAC ASIC to the BCM5226 synchronously based on the 50 MHz reference clock. This is essentially identical to the traditional transmit MII with the obvious exception of di-bits clocking at 50 MHz vs. nibbles clocking at 25 MHz for 100 Mbps operation. For 10 Mbps operation, the di-bits are still clocked out of the switch or MAC ASIC on the 50 MHz REF_CLK, however, these di-bits only change value once in every ten REF_CLK cycles for an effective data transfer rate of 5 MHz per di-bit.

The deassertion of TX_EN indicates “End Of Packet” to the BCM5226R, which, in turn, delimits the packet as it is transmitted onto the network medium.

RECEIVE RMII

The receive data is also transferred synchronously from the BCM5226R to the switch or MAC ASIC based on the REF_CLK. However, in order to synchronize the receive data to the local REF_CLK, the BCM5226R must buffer the receive data from the network with its internal FIFO. This is necessary because the receive data stream, which is referenced to the far-end station’s local clock, is asynchronous to the local REF_CLK. The FIFO allows the receive data to be buffered and re-timed such that it is synchronous to the local REF_CLK. Refer to ”Receive FIFO” on page 13 for more information.

Once re-timed, the receive di-bits are clocked out of the BCM5226R synchronously (relative to the local REF_CLK) to the switch or MAC ASIC. CRS_DV, which conveys both the carrier-sense and receive-data-valid packet delimiting control signals, is asserted asynchronously relative to the REF_CLK due to the detection of carrier (non-IDLE condition for 100BASE-X and receive signal surpassing squelch for 10BASE-T). While the receive RMII can also include the receive error control signal (RX_ER), it is not mandatory in switch or DTE applications, because the switch or MAC ASIC is not required to accommodate RX_ER. You can omit an RX_ER input at the ASIC because the BCM5226R will modify the data content of an

errored receive packet, such that its CRC will be detected as incorrect by the ASIC, thus flagging the error without the need for a separate RX_ER signal. For a full description of each RMII data and control signal, refer to the RMII specification.

The timing diagram provided in Figure 4 below illustrates 100 M packet reception (error free) over the receive RMII. Note that RMII signalling during packet transfer is similar to standard MII signalling with the obvious exception of CRS_DV behavior and different transfer rates and bus widths. Note that CRS_DV can toggle at one half the REF_CLK rate, while the receive FIFO flushes any buffered receive nibbles that may have accumulated due to frequency differences between REF_CLK and the far end link partner's local clock.

The toggling of CRS_DV is the mechanism the ASIC uses to delineate between CRS deassertion and continued RX_DV assertion while the receive FIFO is still flushing its contents. CRS_DV deasserts for cycles of REF_CLK, where RXD[1:0] is presenting the first di-bit of a buffered nibble, and re-assert for cycles of REF_CLK, where RXD[1:0] is presenting the second di-bit of a buffered nibble. CRS_DV, while shown toggling only once in Figure 4 below, can toggle several times at the end of a given packet if the frequency difference between link partners is significant.

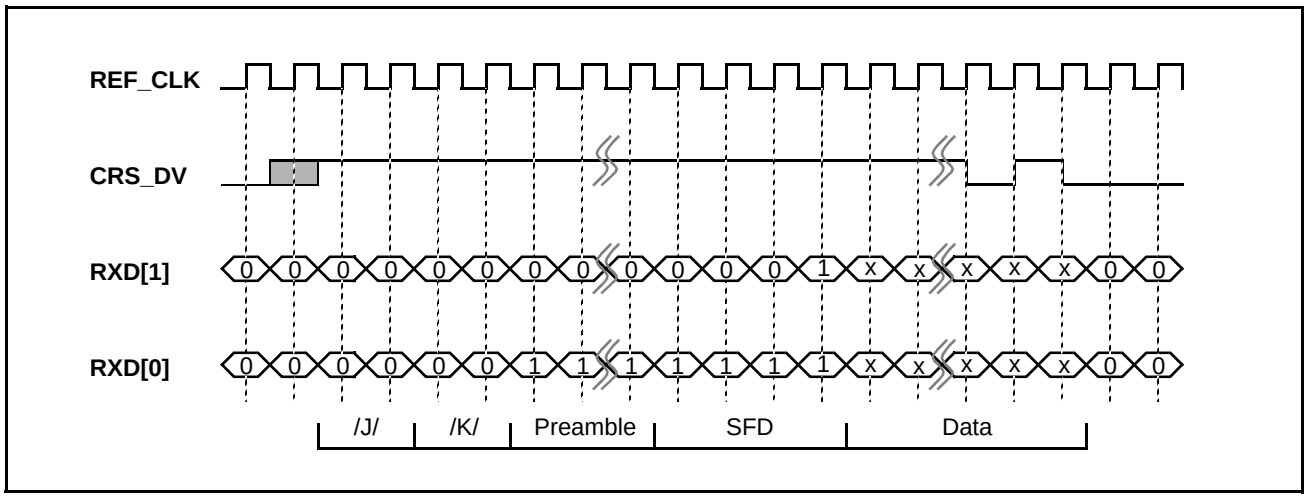

Figure 4: Receive RMII Packet Transfer Timing (No Errors)

RMII OUT-OF-BAND SIGNALING

The BCM5226R includes support for Out-of-Band signaling across the receive RMII (referenced in the RMII specification). This signaling allows the BCM5226R to communicate status information to the MAC layer at 100 Mbps. Note that the BCM5226R does not support Out-of-Band signaling *from* the MAC layer and will ignore data in TXD[1:0] when TX_EN is deasserted.

Out-of-Band Signaling consists of two di-bit pairs immediately following the last di-bit pair of a received packet. The two di-bit pairs consist of (Full Duplex, Link Speed: msb, lsb) and (RXER, FIFO Error: msb, lsb). Out-of-Band Signaling is enabled by setting bit 1 of register 10h. Figure 5 on page 11 illustrates the bit order and appearance of the receive RMII Out-of-Band Signaling relative to general RMII signaling (assuming final deassertion of CRS_DV).

The Out-Of-Band status bits are encoded as shown below.

Table 2: Out-of-Band Status Bits

Mode	*Status Bits*
Full Duplex	1 denotes Full Duplex 0 denotes Half Duplex
Link Speed	1 denotes 100BASE-X 0 denotes 10BASE-T

Table 2: Out-of-Band Status Bits (Cont.)

Mode	*Status Bits*
RXER	1 denotes a Receive Packet Error 0 denotes valid packet (no error)
FIFO Error	1 denotes FIFO overrun or underrun 0 denotes no FIFO error

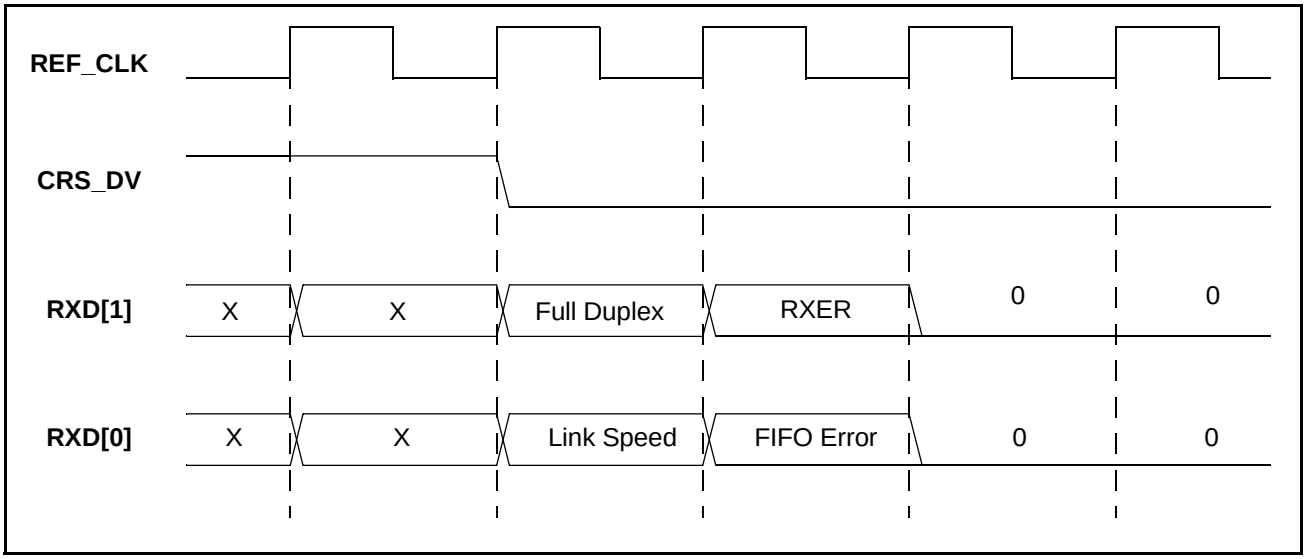

Figure 5: Receive RMII Out-Of-Band Signaling

SMII (SERIAL MEDIA INDEPENDENT INTERFACE)—BCM5226S ONLY

This section describes the SMII interface based on the Serial-MII specification currently proposed by Cisco Systems. This interface represents the minimum in interconnection between the switch ASIC and the BCM5226S at the cost of more complex state machine arbitration within both the PHY and MAC layers.

For a given BCM5226 port, the SMII consists of two pins:

- RXD[0]—a single receive data output pin
- TXD[0]—a single transmit data input pin

A single 125 MHz reference clock input and a single Sync input are also required; they are shared across all ports. The clock is specified as an externally sourced reference that is used to drive both the PHY(s) and the switch ASIC(s). The Sync input of the BCM5226 (SSYNC) accepts a timing pulse that is sourced by the switch ASIC. This sync pulse, a positive going 8 ns pulse that occurs once in every ten cycles of the 125-MHz reference clock, is used to delimit control code and packet data into 10-bit ‘SYNC Frames’.

The state of the TX_EN control bit within the transmit data stream indicates to the BCM5226 whether the content of a given 10-bit cycle is dedicated to control information or packet data. Similarly, the state of the RX_DV control bit within the receive data stream indicates to the switch ASIC whether the content of a given 10-bit cycle (SYNC Frame) is dedicated to control information or packet data. Figure 6 and Figure 7 below illustrate relative timing for the Transmit and Receive SMII respectively. These figures are followed by detailed description of the contents of each SYNC Frame type.

During 100 Mbps operation, the serial receive data is transferred across the SMII at 125 MHz and each bit within each SYNC Frame is sampled by the switch or MAC ASIC once every 8 ns. During 10 Mbps operation, data is still transferred across the

SMII at 125 MHz; however, because the data rate is only 1/10th that of 100 Mbps operation, the BCM5226 needs only to update the data once in every ten SYNC Frames. Therefore, the switch or MAC ASIC need only sample one out of every 10 SYNC frames. The same speeds and sampling rates described for the SMII receive data apply to the SMII transmit data (from ASIC to PHY) as well.

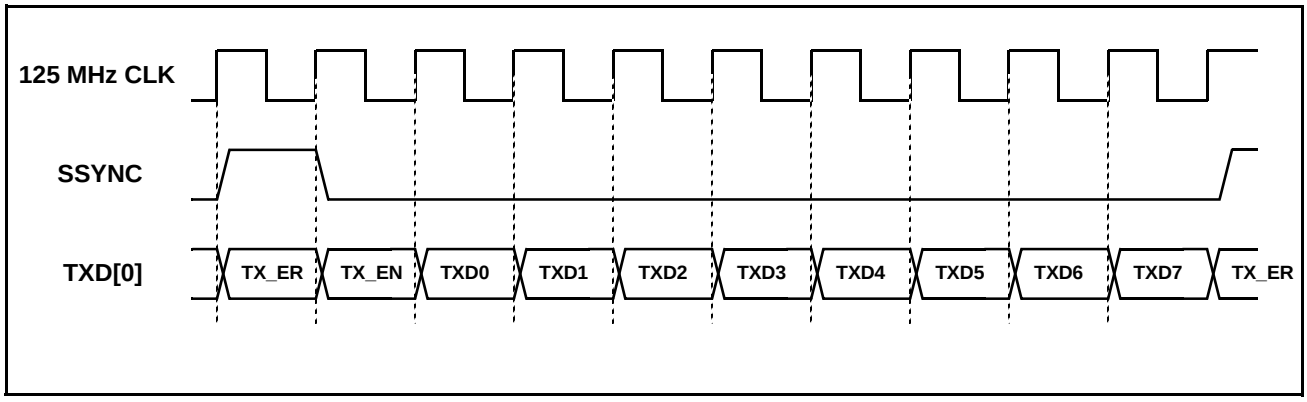

Figure 6: Transmit SMII SYNC Frame Timing

For typical SMII connections (MAC to PHY), SYNC Frames generated by the MAC are either IDLE (TX_EN = 0) or carry packet data in Byte long segments (TX_EN = 1). TX_ER can be used to force a transmit error line state (Halt Symbols generated when TX_ER = 1, and TX_EN = x) but are normally not utilized in typical Fast Ethernet switch applications.

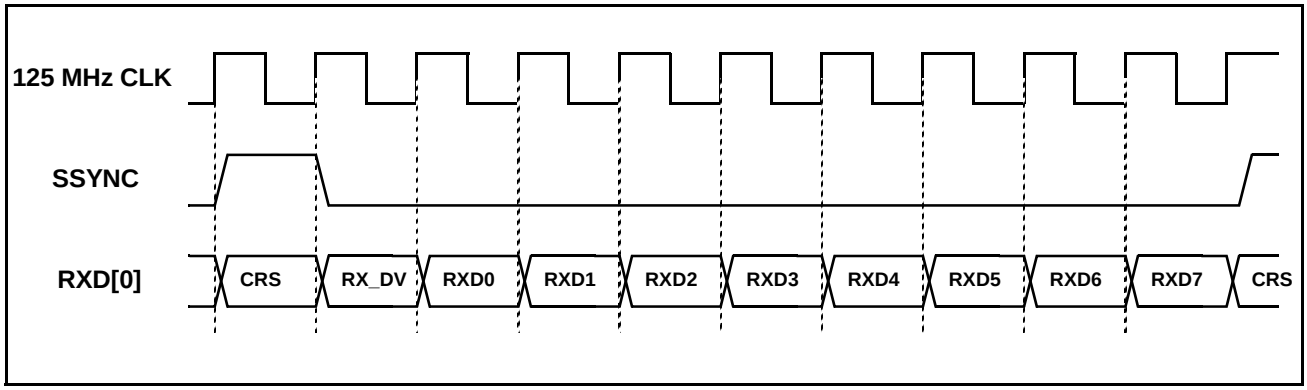

Figure 7: Receive SMII SYNC Frame Timing

Receive SMII SYNC Frames convey either packet data in byte-long segments during normal packet reception (RX_DV = 1, and CRS = 1) or PHY status between packet reception (RX_DV = 0, CRS = x). The PHY status is encoded as follows:

Table 3: PHY Status Coding

Status Bit	*Coding*
RXD0	RX_ER This is set either by a bad receive symbol(s) from the previous packet or FIFO underrun/overrun conditions.
RXD1	Speed indication (0 = 10 MB, 1 = 100 MB).
RXD2	Duplex indication (0 = half-duplex, 1 = full-duplex).
RXD3	Link indication (0 = invalid, 1 = valid).
RXD4	Jabber (0 = OK, 1 = error) This status bit pertains only to 10 Mbps operation and is a ‘don’t care’ for 100 Mbps.
RXD5	Upper Nibble of previous Frame (0 = invalid, 1 = valid).
RXD6	False Carrier Detected (0 = valid, 1 = False Carrier Event).
RXD7	Always set to a logic 1.

CRS is the only frame bit that is not passed through the receive FIFO. CRS is asserted for the duration of packet reception from the network.

An SMII compliant MAC will detect a half-duplex collision if both CRS and TX_EN are asserted simultaneously. This requires that, in half duplex operation, the PHY must not echo CRS back to the MAC during transmit activity.

RECEIVE FIFO

The six receive FIFOs internal to the BCM5226 (one per port—enabled during RMII and SMII modes of operation) are each capable of operating in two different modes: Normal or Extended.

When operating in Normal FIFO mode, a given port can buffer up to +/- 10 bits to accommodate mismatches between local clock frequency and link partner clock frequency. This is the default operating mode of the device and is more than sufficient to buffer any compliant 10BASE-T or 100BASE-X link. Compliant links can result in a maximum clock frequency delta between link partners of 100 ppm (one partner running at +50 ppm and the other running at -50 ppm).

When Extended FIFO mode is selected for a given port (by setting bit 2 of register 10h), the receive FIFO can dynamically track frequency error and effectively double in depth. This means that up to +/- 20 bits can be buffered with no loss of data in network links that suffer from more severe end-to-end clock frequency disparity. This ensures that underflow and/or overflow conditions are virtually eliminated even when communicating to link partners whose local reference clocks are well outside of the +/- 50 ppm frequency tolerance.

The following equation is used for FIFO criteria:

FIFO depth bits = (2 * max packet size) * (end station error + local station error)

Using this equation, FIFO depth can be calculated for a given link where both partners are operating within a clock tolerance of +/- 50ppm passing max size Ethernet packets across the network.

FIFO depth bits = (2 * 1518 * 8) * (0.005% + 0.005%)

FIFO depth bits = (24288) * (0.0001) = 2.5 bits

HSTR SUPPORT

The BCM5226R/BCM5226S supports high speed Token Ring applications. Setting bit 10 of register 1Bh enables a given port to transmit and receive maximum size Token Ring frames in a 100 Mbps Token Ring application. To support HSTR, the standard periodic check for IDLE symbols (once every 724 µs for Ethernet packets) is extended to 5792 µs within the descrambler of each transceiver's receive path. This ensures that even the largest Token Ring frames will not cause loss of synchronization in the descrambler during reception. While maximum size Ethernet packets are 1518 octets, maximum Token Ring frames can reach 18.2 K octets (and higher for certain applications). Typically, Token Ring frame size remains at 4096 octets or less.

The TXER input signal is available per port. This active high input can be used to generate HALT line state symbols onto the media, which are required for transmitting HSTR interrupts to the downstream node. The BCM5226 does not include integrated TX/RX pair swapping; this requirement must be implemented external to the PHY.

MASTER PHY ADDRESS MODE

This mode enables the use of global writes to all six PHY slices within the BCM5226. When this mode is enabled all writes to PHY address 0 affect the respective register in all six PHYs. To enable this mode, the MST_PHY_ADR pin (BCM5226R pin 17 or BCM5226S pin 112) must be held high during the power-up reset. If this pin is left unconnected, or held low during power-up reset, this selects the normal addressing mode. This bit is not under software control.

CABLE LENGTH METER CAPABILITY

The DSP nature of the 10/100 receiver within the BCM5226 allows real-time access to equalizer states that provide cable length estimate information. A valid link must be established for this feature to function properly.

Specifically, bits [14:12] in Shadow register 1Bh provide a +/- 10 meter length estimate of the Cat-5 cable connected to the 5226. This estimate is accessed by simply reading the afore mentioned bits. This provides the user with an easily accessed and powerful diagnostic tool for determining potential problems within the cable plant and/or associated connectors. Refer to Table 4 for decode.

Table 4: Cable Length Estimate

Register 1Bh 14, 13, 12	*Cable Length in Meters*
000	<20
001	20 to <40
010	40 to <60
011	60 to <80
100	80 to <100
010	100 to <120
100	120 to <140
010	>140

SMII TO TWISTED PAIR CONNECTION DIAGRAM

Figure 8 on page 15 shows the signal connections and strapping for a typical SMII based 10/100 twisted pair DTE implementation. This simplified diagram only shows connection of a single port to the network. A complete schematic would include all six ports for the SMII, Serial LED, and Twisted Pair interfaces. This connection diagram also includes several unique Test Point (TP) locations. These locations are only reference points for the waveform examples that follow; these test points would not physically be included in the actual system design.

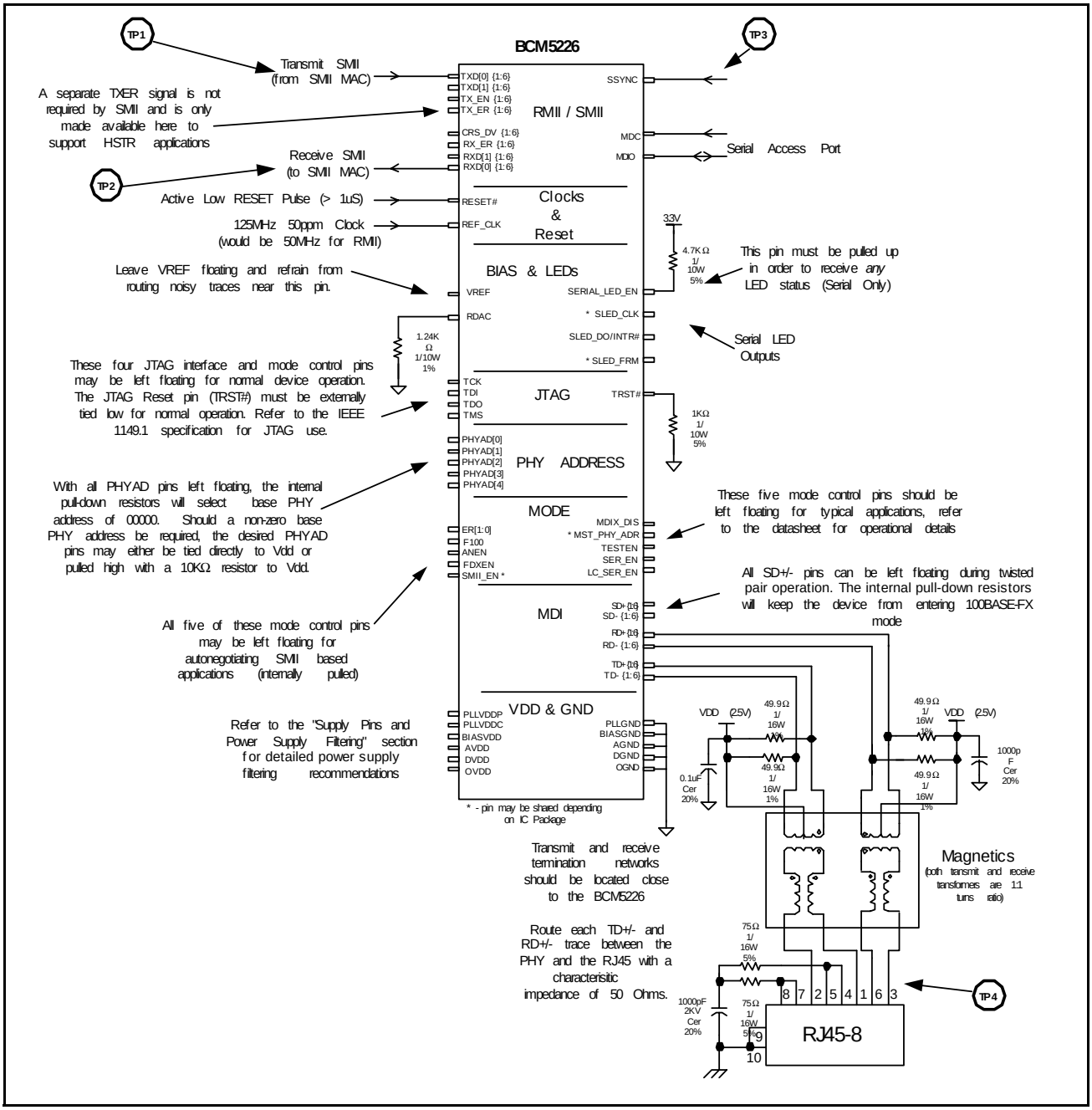

Figure 8: BCM5226S Typical SMII to Twisted Pair Connection

WAVEFORM EXAMPLES

The following figures consist of high-bandwidth scope plots of the various signal waveforms that should exist in a properly designed and operating system based on the BCM5226R. The Test Points (TP1 though TP6), shown in Figure 8 on page 15, indicate which pin or group of pins were measured to obtain the following waveform examples.

TP1 plots depict the RMII transmit signals. Figure 9 shows a Start of Frame sequence, and Figure 10 shows an End of Frame sequence.

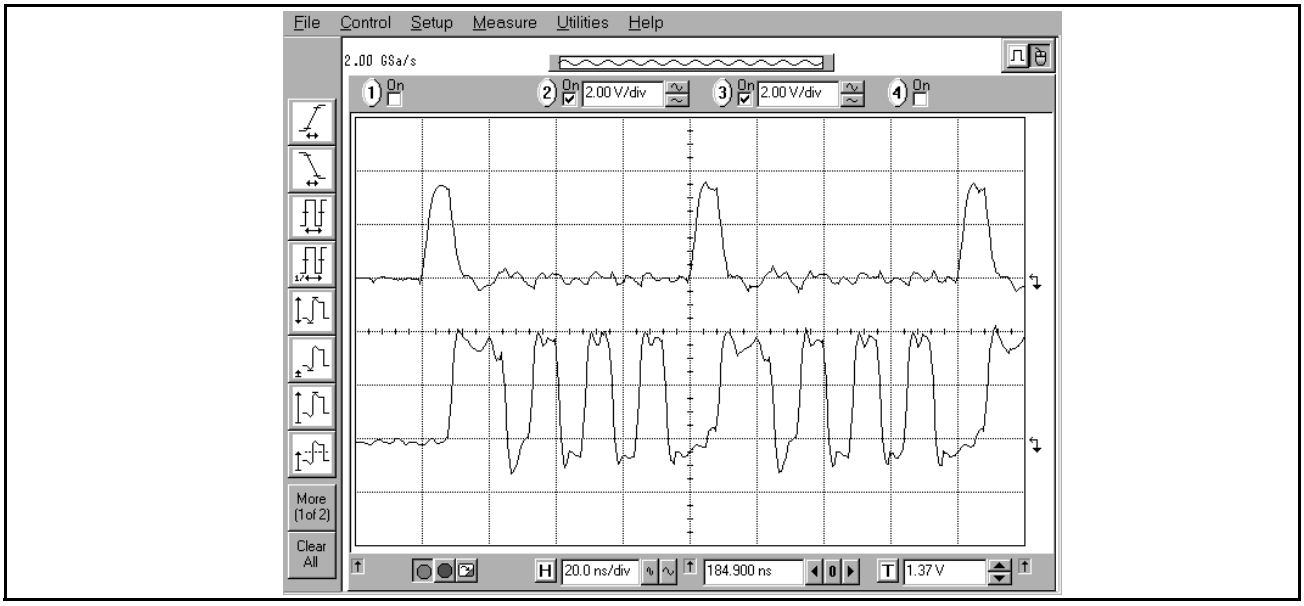

Figure 9: TP1—Transmit RMII Start of Frame

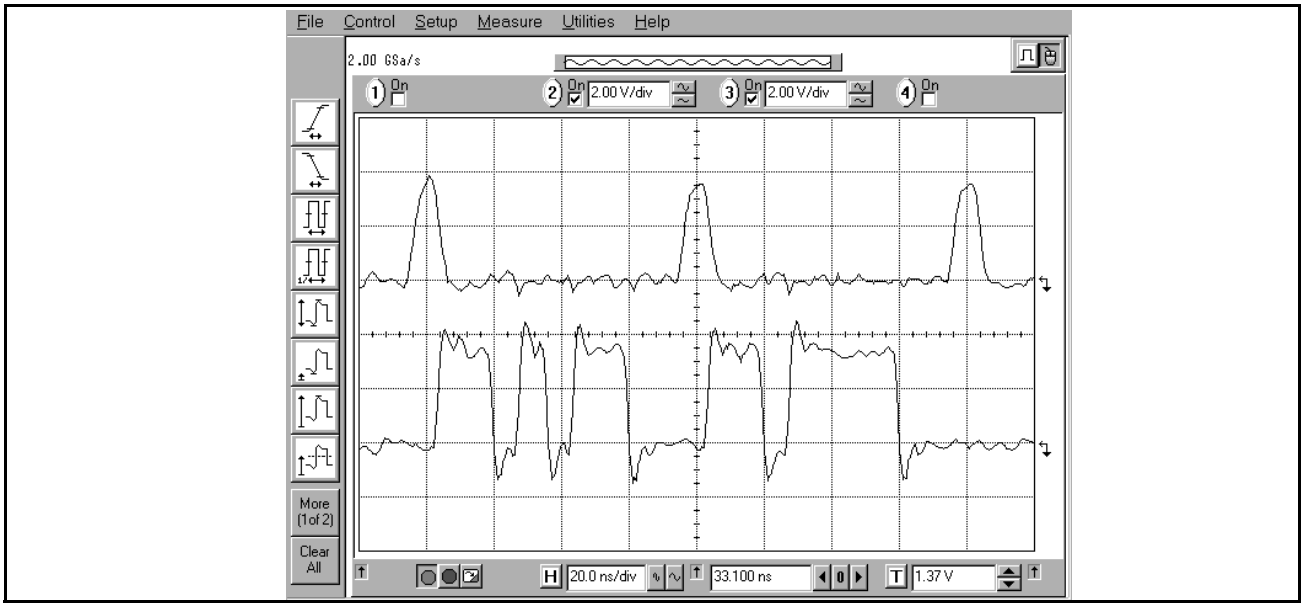

Figure 10: TP1—Transmit RMII End of Frame

TP2 plots show the RMII receive signals. Figure 11 shows a Start of Frame sequence, and Figure 12 shows an End of Frame sequence.

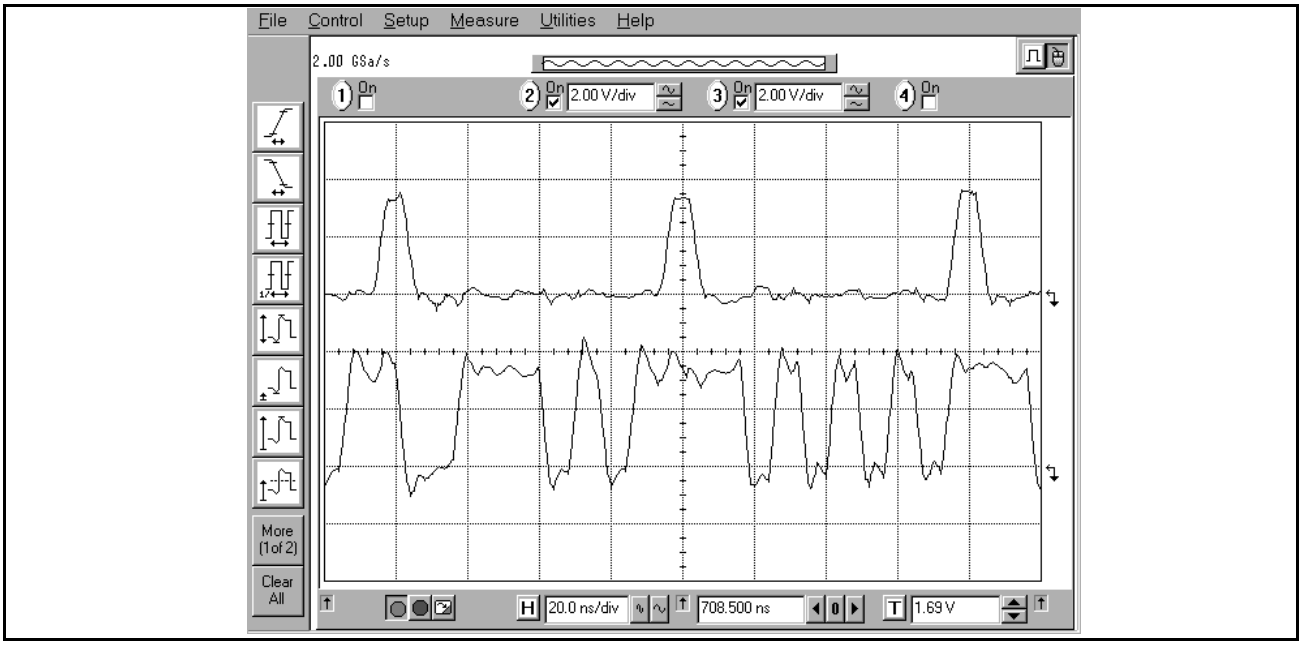

Figure 11: TP2—Receive RMII Start of Frame

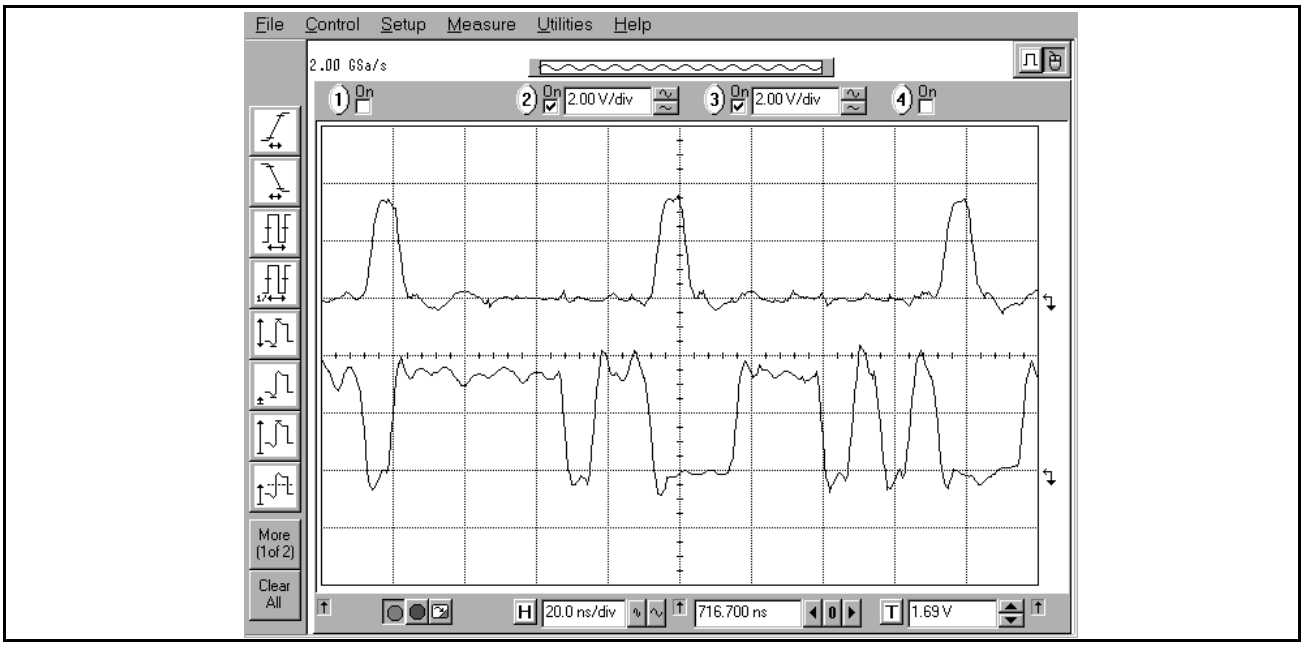

Figure 12: TP2—Receive RMII End of Frame

Figure 13 (TP3) shows a typical MDIO Write cycle.

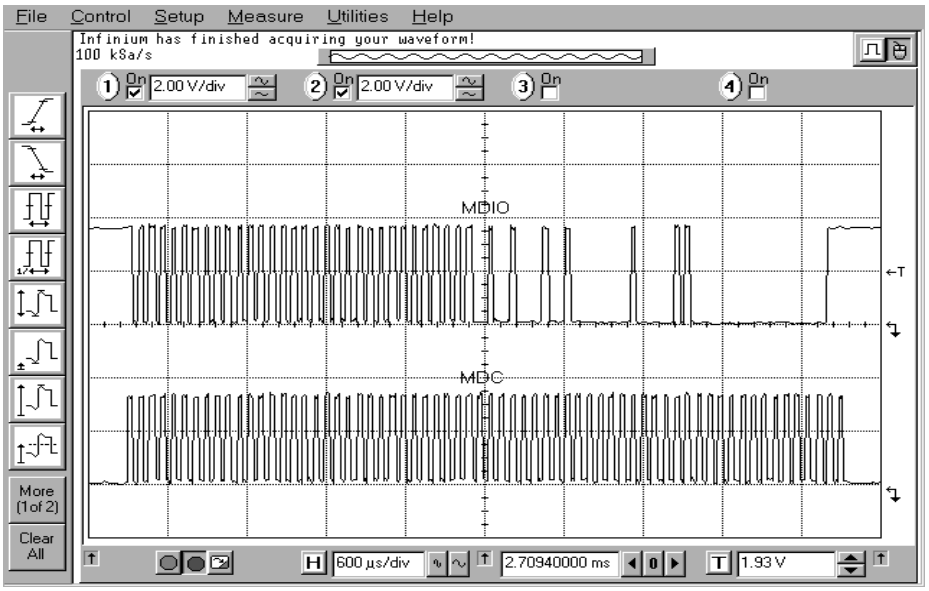

Figure 13: TP3—MDIO Write Cycle (with Preamble)

TP4 plots show the Twisted Pair Transmit signal as measured differentially across the transmit pins (3 & 6) of the RJ45.

Figure 14 shows an MLT-3 eye pattern for determining transmit jitter.

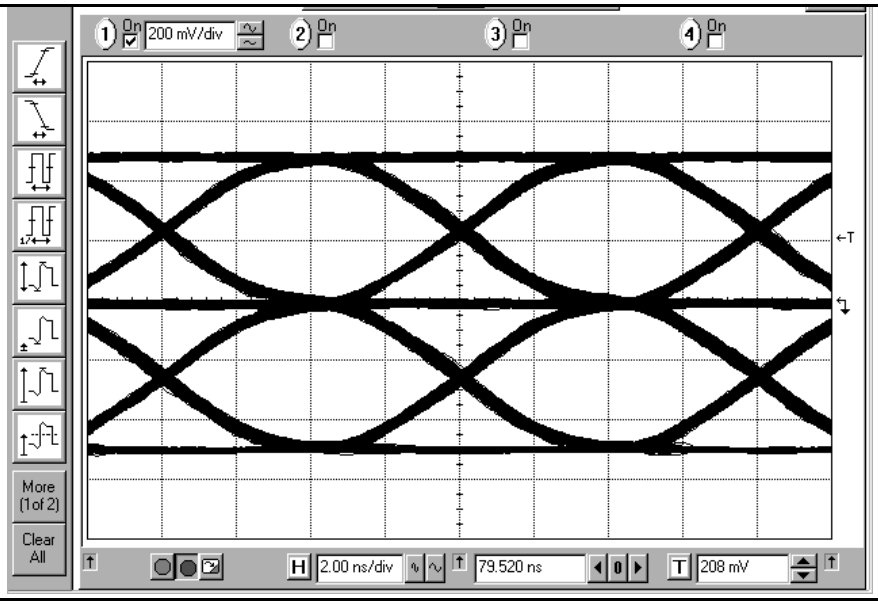

Figure 14: TP4—MLT-3 Eye Pattern (Transmit Jitter)

AUTOMATIC MDI CROSSOVER

During Auto-Negotiation and 10/100BASE-TX operation, one end of the link must perform an MDI (Medium Dependant Interface) crossover so that each transceiver's transmitter is connected to the other's receiver. The BCM5226 contains the ability to perform HP Auto-MDI/MDIX crossover, thus eliminating the need for crossover cables or cross-wired (MDIX) ports.

During Auto-Negotiation and 10/100BASE-TX operation, the BCM5226 normally transmits on TD+/- and receives on RD+/-. When connected to another device which does not perform the HP Auto-MDI/MDIX crossover, the BCM5226 automatically switches its transmitter to RD+/- and its receiver to TD+/- in order to communicate with the remote device. If two devices are connected that both have HP Auto-MDI/MDIX crossover capability, then a random algorithm determines which end performs the crossover function.

The HP Auto-MDI/MDIX crossover feature is a function of Auto-Negotiation. Therefore if the BCM5226 is configured not to perform Auto-Negotiation, the feature does not work, and a specific cable is required to ensure the Transmitter at one end of the cable is connected with the Receiver at the other end of the cable. The default mode for this feature is determined by the status of the MDIX-DIS pin during reset, but is always under software control, allowing the user to enable or disable it when needed. If the MDIX-DIS pin is pulled low or left floating, the HP Auto-MDI/MDIX feature is enabled. During operation the MDI state can be determined by reading bit 13 of Register 1Ch, as indicated in the BCM5226 Datasheet. Additionally, a manual MDI Swap can be forced by setting or clearing bit 12 of Register 1Ch.

The HP Auto-MDI/MDIX feature is implemented in the BCM5226 in accordance with the IEEE 802.3ab specification. The Automatic MDI/MDI-X state machine facilitates switching between which pair receives and which pair transmits, respectively, prior to the auto-negotiation mode of operation, so that Fast Link Pulses (FLPs) can be transmitted and received in compliance with Clause 28 Auto-Negotiation specification. The final state of the crossover circuit is determined by an algorithm that controls the switching function between the two pairs (transmit and receive). The algorithm uses an 11-bit Linear Feedback Shift Register (LFSR) to create a pseudo-random sequence that determines the BCM5226 initial configuration. In the BCM5226 care is taken to ensure the LFSR is seeded with a unique value during reset. This determines the initial state of MDI or MDIX. Per the specification, a sample timer is implemented in a manner that allows the BCM5226 to detect either valid Link Pulses or a Valid Link. If after 62+/-2 ms the receiver is unable to detect a valid Link Pulse or a valid Link, the LFSR is advanced, switching the pairs. Additionally, an asynchronous timer is used in case two PHYs should have identical reference clocks and reset circuits. When this timer expires, it resets the state machine to the MDI State and restarts the sample timer. This timer is free running and has no impact on the LFSR.

HP Auto-MDI/MDIX operates only on the transmit and receive data pairs (swapping them if required). It does not operate on the individual wires within a given pair and therefore cannot correct any polarity swap issues. However, other facilities within the BCM5226 do manage some polarity swapping while operating in 10BASE-T mode. Note that specific magnetics and cable termination issues must be considered when using the BCM5226 in HP Auto-MDI/MDIX mode. See Figure 15 on page 20 for details.

MAGNETICS

Most multi-port applications require Quad magnetics to support implementations based on one or more BCM5226 devices. Some applications may also require single channel magnetics. In some applications, single or dual channel magnetics may be required as well.

Care must be taken when selecting the magnetic to use with the BCM5226 in your design. One important restriction when pairing magnetics with the BCM5226 relates to the ordering of the isolation transformer and common mode choke in the transmit signal path (and receive signal path when HP Auto-MDI/MDIX is enabled). The transmit output signal from the BCM5226 must be connected to the isolation transformer first, followed by the common mode choke (as depicted in Figure 8 on page 15). If any common mode choke is placed between the TD+/- output pins and the isolation transformer, signal distortion will occur during Autonegotiation mode and in 10BASE-T mode. The ordering of the isolation transformer versus common mode choke is also critical in the receive signal path, regardless of whether you use the HP Auto-MDI/MDIX feature.

With this in mind, Broadcom recommends choosing magnetics that have symmetrical circuits for Transmit and Receive paths with the proper ordering of components mentioned above.

The following list includes a small list of Quad magnetics from various vendors, that can be used with the BCM5226. All major magnetic vendors have parts designed with the circuit configuration required by the BCM5226. Check the vendors' websites for the latest magnetic specifications.

Bel. S558-5999-Q9 (Quad—for use with single height or stacked RJ connectors).

Pulse. H1164 (Quad—for use with stacked RJ connectors).

Figure 15 on page 20 illustrates specific magnetics interconnect and differential cable termination requirements for applications that use HP Auto-MDI/MDIX.

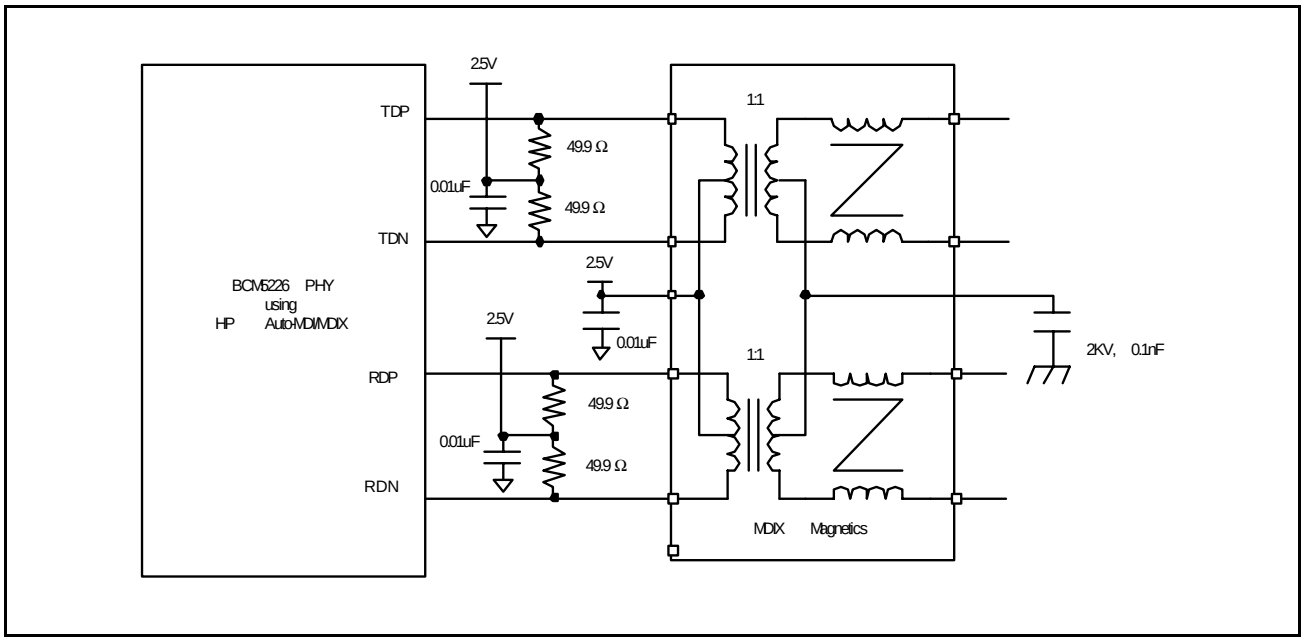

Figure 15: Magnetics Connection and Differential Cable Termination Requirements

SUPPLY PINS

This section describes the power pins and recommended power supply filtering for the BCM5226. Each power pin type is listed and defined below.

DVDD. These pins supply power to the digital core of the BCM5226, as well as to the DSP-based receive circuitry. These pins must always be connected to a 2.5V supply.

AVDD. These pins provide power to the analog circuitry within the BCM5226, such as the transmit DAC and receive ADC. These pins must always be connected to a 2.5V supply.

OVDD. These pins supply power to the digital output buffer stages and can be tied to either 2.5V or 3.3V, depending on the signaling requirements of the MAC or Switch ASIC interface to the BCM5226.

PLLVDDP. This pin supplies power to the REF_CLK input buffer stage. If the REF_CLK input signal has an amplitude of 3.3V, then this pin should be tied to a 3.3V supply. If the REF_CLK input signal is 2.5V, then PLLVDDP should be tied to a 2.5V supply.

PLLVDDC. This pin, which is the most sensitive to noise, supplies power to the Phase Locked Loop circuitry. Note that this is the only power pin on the BCM5226 where the use of special low pass filter (comprised of a series ferrite bead and shunt capacitance) is recommended. See Figure 20 on page 28 for more details. This pin will draw approximately 15 mA maximum.

BIASVDD. This pin supplies power to the internal Bias Generator within the BCM5226. The sensitivity of this pin is less than that of the PLLVDD pin but still more than the remaining VDD supply pins. The use of a series resistor between this pin and VDD is recommended to provide some degree of noise attenuation across a wide frequency range. The maximum value of the series resistor should not exceed 3.3 Ω, because this will result in an unacceptably large IR drop. This pin draws approximately 30 mA worst-case. See Figure 20 on page 28 for more information.

LAYOUT RECOMMENDATIONS

The following sections include recommendations and examples for BCM5226-based system layout, as well as guidelines for general board layout. These sections include:

- Twisted Pair Interface Layout
- RMII Layout
- SMII Layout
- Power Supply Filter Component Placement
- Analog Related Passive Component Placement
- Board Layer Allocation
- Bridging Chassis Ground to System Ground
- General Layout Recommendations

TWISTED PAIR INTERFACE LAYOUT

TD+/- Trace Routing. When routing the TD+/- signal traces from the PHY to the 1:1 transformer, the traces should be routed adjacent to the power plane (as opposed to the ground plane) for controlled characteristic impedance. This ensures that the return currents that occur during transmit switching remain within the 2.5 V power plane and, as a result, meet the lowest possible impedance. This approach is recommended because the transmit transformer is referenced to the 2.5 V rail and pulls current from VDD through its center tap.

Broadcom recommends that the TD+ and TD- signal traces be routed with matched length (as short as possible), and with a characteristic single-ended impedance of 50Ω each. The 49.9Ω termination resistors should be placed as close as possible to the TD+/- outputs of the BCM5226 for each port. Additionally, the center tap of the transmit transformer primary winding must be connected directly to the 2.5V power plane with local decoupling of 1000 pF (refer to Figure 8 on page 15).

In non-Auto-MDI/MDIX applications, both the TD+/- and RD+/- pairs may need to be routed on the same plane (adjacent to the 2.5V plane). Broadcom recommends that the TD+/- trace pair be routed so that the space between it and any other TD+/- or RD+/- pair is at least three times that of the distance that separates the individual TD+ and TD- traces from one another.

No further external filtering is recommended for the transmit channel. See Figure 16 on page 23 for an example of physical trace routing of the transmit pair from the BCM5226 to the RJ45 media connector.

RD+/- Trace Routing. For HP Auto-MDI/MDIX applications, the RD+ and RD- traces, which connect the receive transformer to the PHY, should each be routed with a single-ended characteristic impedance of 50Ω and should be routed adjacent to the VDD plane. The two traces should be matched in length and routed together.

For non-HP Auto-MDI/MDIX applications, the RD+ and RD- traces, which connect the receive transformer to the PHY, should each be routed with a single-ended characteristic impedance of 50Ω and can be routed adjacent to the ground plane. The two traces should be matched in length and routed together.

When routing both RD+/- and TD+/- traces on the same layer, Broadcom recommends that the RD+/- trace pair be routed so that the space between it and any other TD+/- or RD+/- pair is at least three times that of the distance that separates the individual RD+ and RD- traces from one another.

The two 49.9Ω receive termination resistors should be placed close to the RD+/- pins of the BCM5226 with the center point of these two resistor coupled to ground with a 0.1 µF capacitor, to enhance receive common mode filtering (see Figure 8 on page 15).

No further external filtering is recommended for the differential receive input. See Figure 17 on page 24 for an example of physical trace routing of the receive pair from the RJ45 media connector to the BCM5226.

Magnetics to RJ45 Connector. Broadcom recommends that properly grounded (usually to the chassis ground) shielded, Category 5 rated, RJ45 media connectors should be used to control EMI emissions.

When routing the transmit and receive pairs between magnetics and the RJ45, Broadcom recommends that an inner layer or layers be used. The outer layers (top and bottom) can be dedicated to chassis ground in the area between the magnetics and the RJ45. This helps shield the sensitive analog signals from external noise sources, and also helps reduce EMI emissions. See Figure 22 on page 31.

Some component pads (nominally 0805 package size) should be placed in the area between the chassis ground plane and system ground, between each set of magnetics. This allows you to place either resistive, inductive, or capacitive components for coupling chassis ground to system ground. Experimenting with different coupling components has been shown to bring a design that was not passing EMI emission test limits into the passing range. Because every design is different, a given component that helps reduce emissions for one design may not help reduce emissions for another design. Broadcom recommends that these component pads be left unpopulated initially. See Figure 22 on page 31 for more information.

TD+/- Trace Routing Example. The diagram in Figure 16 on page 23 illustrates one possible method for routing the TD+/- traces in a 12-port application. The TD+/- signals should be routed on a board layer adjacent to the 2.5V power plane layer. For example, in a typical four-layer board design, where VDD is usually allocated to layer 3, the TD+/- traces should be routed on the bottom layer (layer 4) in the area between the BCM5226 and the magnetics.

The continuation of these traces, between the magnetics and the RJ45 media connectors should be routed on layer 3. This is because the top and bottom layers (layers 1 and 4) should be dedicated to chassis ground in the area between the magnetics and the RJ45 connectors to provide some level of shielding for the transmit and receive pairs. See Figure 22 on page 31 for more information about board layer allocation.

In Figure 22, notice the use of vias, illustrated as small circular connections, located near the BCM5226 TD+/- pins as well as near the TD and TX pins of the magnetics. These are required to route the TD+/- traces on Layers 4 and 3 (in this exam-

ple). The transmit-side cable termination is not illustrated in Figure 16 on page 23. See ”Analog-Related Passive Component Placement” on page 29 for more information on placement of this termination.

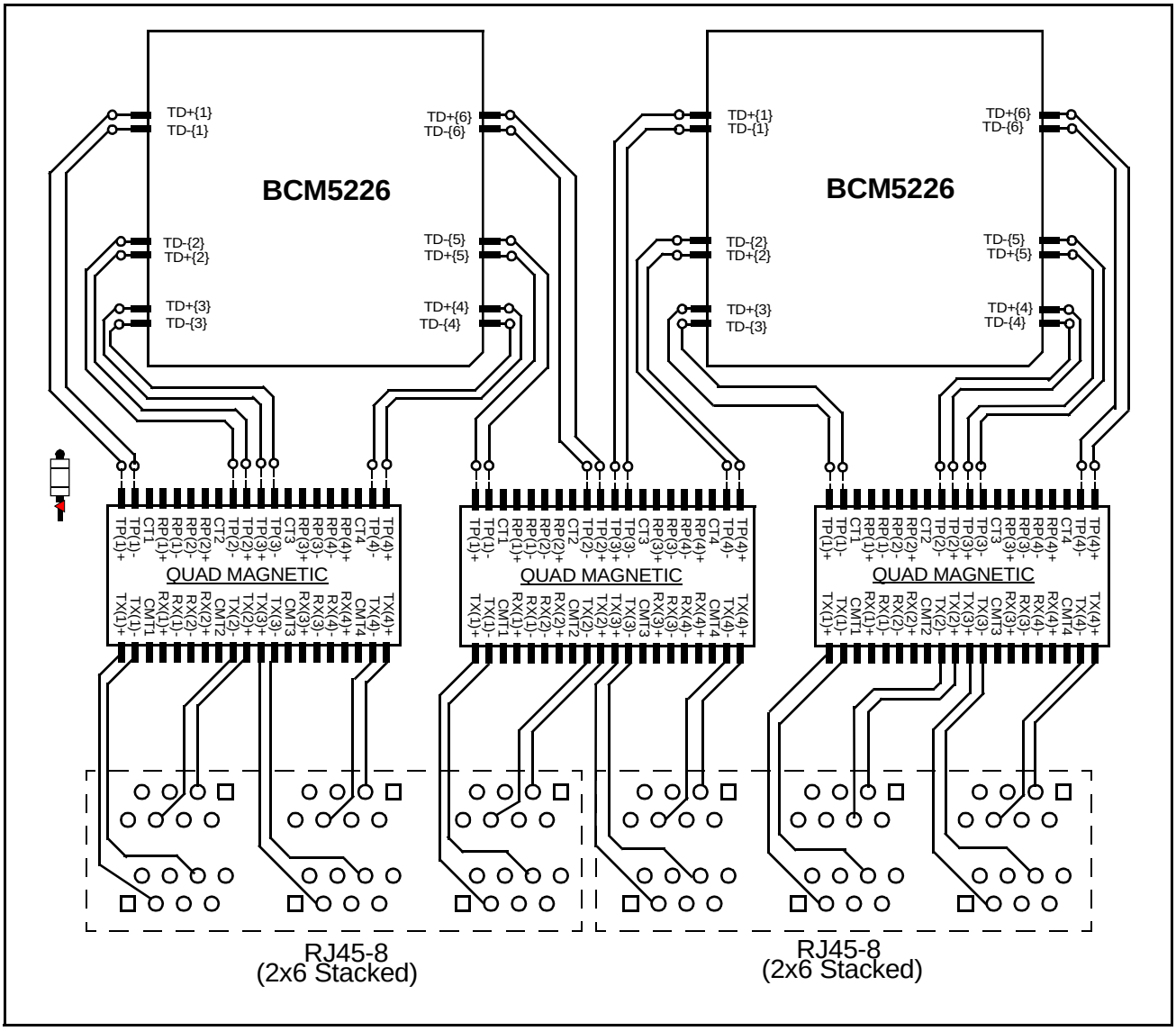

Figure 16: TD+/- Trace Routing (12-Port Example)

RD+/- Trace Routing Example. Figure 17 on page 24 illustrates one method for routing the RD+/- traces in a 12-port application.

If your design uses the HP Auto-MDI/MDIX feature, the RD+/- (& TD+/-) traces between the BCM5226 and the magnetics should both be routed on a plane adjacent to the 2.5V plane. In a typical four-layer board design for example, where the VDD supply is usually allocated to layer 3, the RD+/- traces should be routed on the bottom layer (layer 4).

If your design does not use he HP Auto-MDI/MDIX feature, then Broadcom recommends routing the RD+/- traces adjacent to the ground plane. Again using a typical four-layer board design as an example, where ground is usually allocated to layer 2, the RD+/- traces should be routed on the top layer (layer 1) in the area between the BCM5226 and the Magnetics.

The continuation of these traces, between the Magnetics and the RJ45 media connectors should be routed on layer 2 (assuming the four-layer board example). This is because the top and bottom layers (layers 1 and 4) should be dedicated to chassis ground in the area between the Magnetics and the RJ45 connectors to provide some level of shielding for the transmit and receive pairs. See Figure 22 on page 31 for more information on board layer allocation 100M and 10M operation. Actual systems may vary from this example.

Notice the use of vias, illustrated as small circular connections, located near the TX pins of the magnetics. These are required to route the TX+/- traces on Layer 2 (in this example). Also, the receive-side cable termination is not illustrated in Figure 17. See ”Analog-Related Passive Component Placement” on page 29 for information about placing this termination.

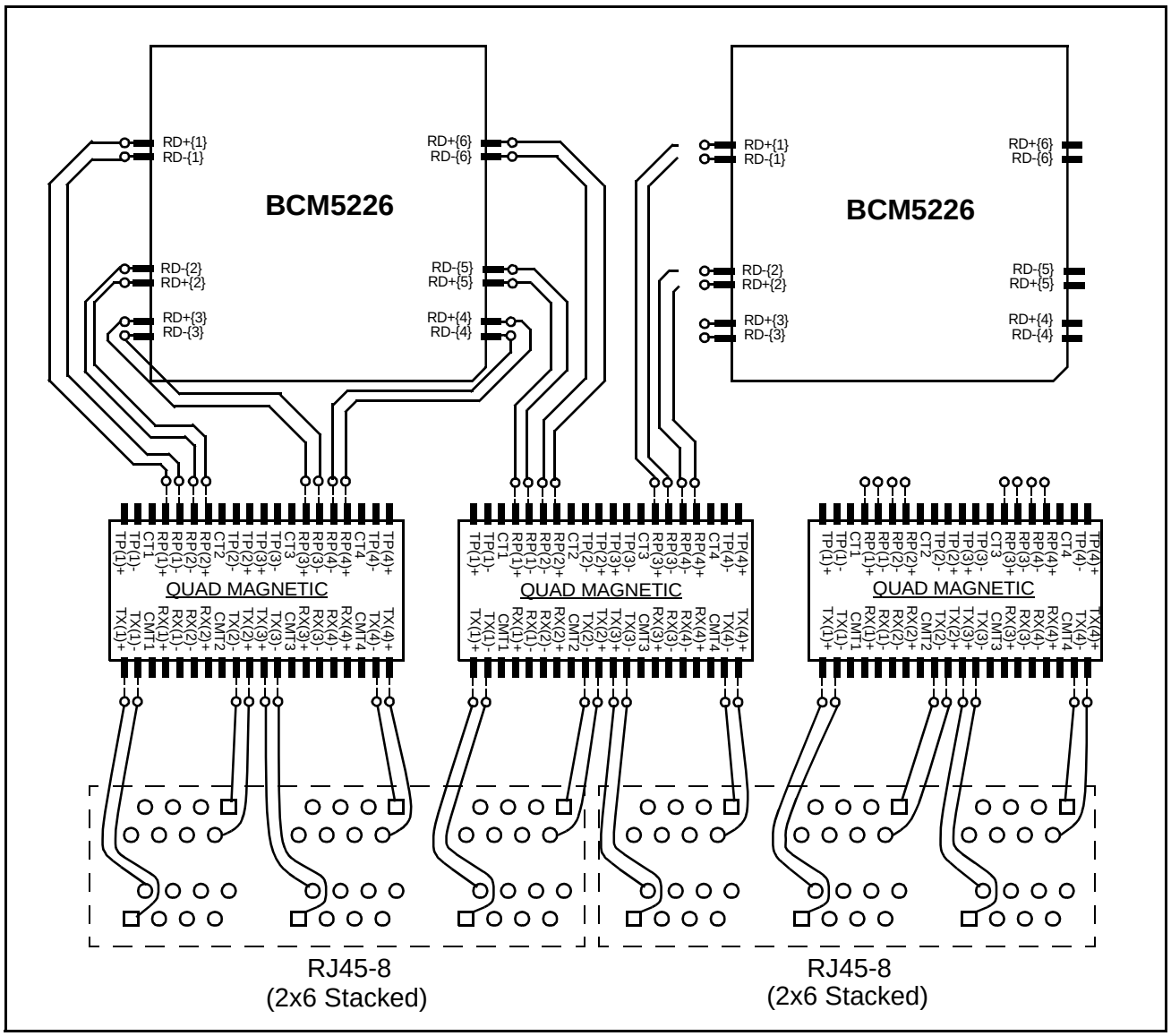

Figure 17: RD+/- Trace Routing (12-Port Example)

RMII LAYOUT

The use of high-speed signal routing techniques is recommended when considering system layout and trace routing for the single-ended, 50-MHz REF_CLK, as well as for the di-bit data lines. Because the single-ended, 50-Mbps data signals can conduct data frequency bursts of up to 25 MHz with rise and fall times as fast as 1 ns, the system designer may want to incorporate some means of controlling (slowing) the edge rates of both the REF_CLK and the di-bit data lines. This can help minimize emissions, especially in layouts that require some distance (beyond approximately one inch) between the BCM5226R and the switch ASIC.

Any R/C loading added to these signals must not cause a violation of RMII clock-to-data timing requirements.

While not specifically stated in the RMII specification, Broadcom suggests that trace routing between the PHY and the switch ASIC be controlled with a characteristic impedance of 68Ω, in keeping with section 22.4.2 of the 802.3u standard. Although the CRS_DV, TX_EN, and optional RX_ER lines do not necessarily require loading for the relatively low frequency nature of these signals, providing this option ensures the flexibility to control energy that is present.

The RMII data and control signal load values are best determined empirically during prototype evaluation. A reasonable starting value for the series source termination resistor is a value in the range of 10 to 22Ω. A starting value of 10 pF for the capacitor to ground is suggested.

A low-skew clock driver/buffer is recommended for distribution of the REF_CLK signal. The input of this buffer is sourced from either an external, crystal-based, 50-MHz oscillator (as shown in Figure 18 on page 25) or the switch ASIC. Source termination at the outputs of this buffer is recommended to control reflections that can occur on the individually buffered REF_CLK signal traces. As with the RMII data and control signals, a reasonable starting value for the series source termination resistor is a value in the range of 10 to 22Ω. A starting value of 10 pF for the capacitor to ground is suggested. Figure 18 illustrates suggested REF_CLK and per-port RMII interconnection between the switch ASIC and the BCM5226R.

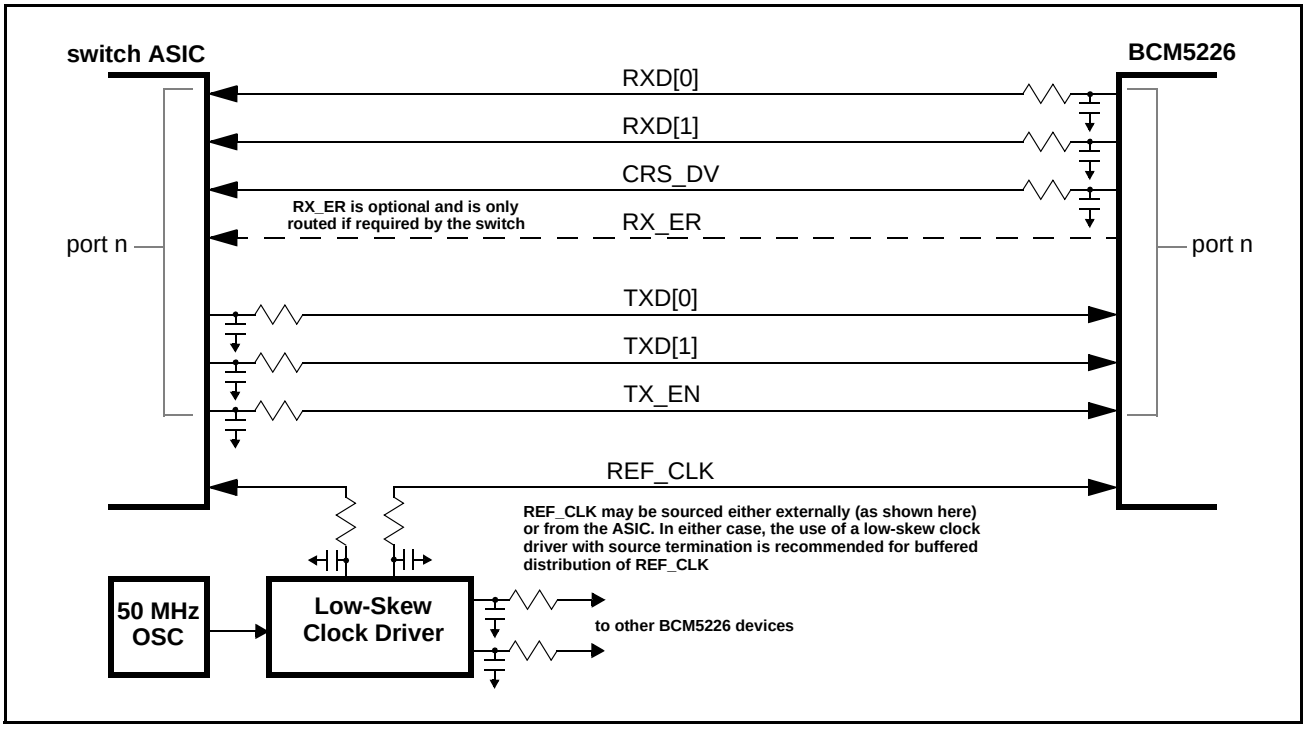

Figure 18: REF_CLK and Per-Port RMII Interconnection with Optional Loading

SMII LAYOUT

The 125-MHz SMII REF_CLK, SMII SYNC signal, and serial data lines (TXD[0] and RXD[0]) each require special layout consideration when implementing SMII.

The SMII REF_CLK must be routed so that the signal traces from the low-skew clock driver are matched in length to each ASIC and BCM5226 within a given design. This minimizes phase variation from device to device, which may produce data errors.

The input of this buffer should be sourced from a crystal-based, 125-MHz oscillator (as shown in Figure 19 on page 27). Source termination at the outputs of this buffer is recommended to control reflections that can occur on the individually buffered SMII REF_CLK signal traces. A reasonable starting value for the series source termination resistor is in the range of 10 to 22Ω. The ideal R value depends on the design layout, as well as on the output driver characteristics of the low-skew clock driver. Contact the manufacturer of the clock driver for further information regarding recommended signal loading.

The SMII SYNC signal deserves special consideration for systems based on the BCM5226. Typical multi-port ASICS are usually configured as quads or octals, and the BCM5226 is a six-port device, which means there is component overlap among the ASICs and the BCM5226 devices. Also, because the BCM5226 has a single SMII SYNC input, the ASIC must include an SMII SYNC input as well as an output (perhaps implemented as a configurable I/O). The SYNC inputs on the ASIC and BCM5226 devices can accept the SYNC signal generated from a master ASIC, which sources the SYNC signal.

The SYNC signal should be distributed to the target devices with an emphasis on minimizing phase variations from device to device (if connection to more than just one ASIC and one BCM5226 is required) to preserve the proper timing and timing margins required to support the SMII interface.

The most important layout aspect concerning the serial data lines, TXD[0] and RXD[0], is to keep the trace routing as short as possible. Contact the ASIC manufacturer for information regarding termination and trace routing recommendations for the transmit SMII data line, TXD[0].

The receive SMII data line, RXD[0], is driven by a high-current output structure in the BCM5226 that is designed to directly drive a 50Ω load. While this output can drive a 50Ω terminated signal trace, it also performs well when driving higher loads, such as 68Ω. This makes it convenient for most board design goals, where 68Ω characteristic impedance is often targeted for digital signal lines. RXD[0] loads less than 50Ω and greater than 100Ω are not recommended.

Assuming the requirement for a 68Ω characteristic impedance for the RXD[0] trace, Figure 19 on page 27 illustrates the proper termination scheme for best signal quality. For other trace impedances, modify the parallel termination values to create an equivalent load that matches the characteristic trace impedance. For example, if you want the trace impedance to be 50Ω, then the pull-up and pull-down resistors should each be 100Ω.

The SMII specification states that the total delay time of the signal traces carrying the SMII serial data streams, both transmit and receive, cannot exceed 1.0 ns. Therefore, Broadcom recommends that these trace lengths be kept as short as possible, and they must not exceed six inches in total length.

Figure 19 illustrates the suggested SMII REF_CLK and per-port SMII interconnection between the switch ASIC and the BCM5226.

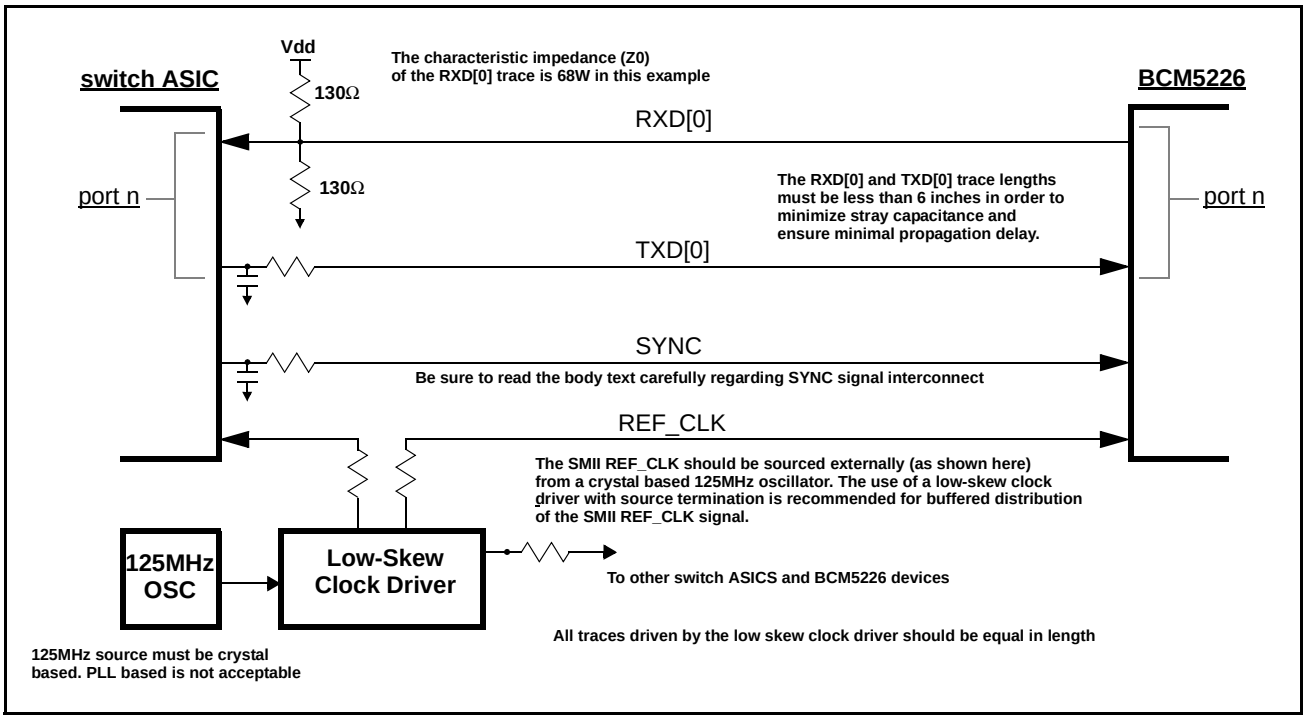

Figure 19: SMII REF_CLK and Per-Port SMII Interconnection with Optional Loading

POWER SUPPLY FILTER COMPONENT PLACEMENT

Figure 20 on page 28 illustrates the recommended placement of power supply filtering around the BCM5226S. Details on sensitive supply pins for both versions of BCM5226 packages are provided later in this section. While Broadcom suggests that new designs attempt to follow these recommendations, some prototype or first-run experimentation in reducing the total number of filtering caps may result in a robust design in terms of EMI compliance and BER performance, with the obvious benefits of fewer passive components.

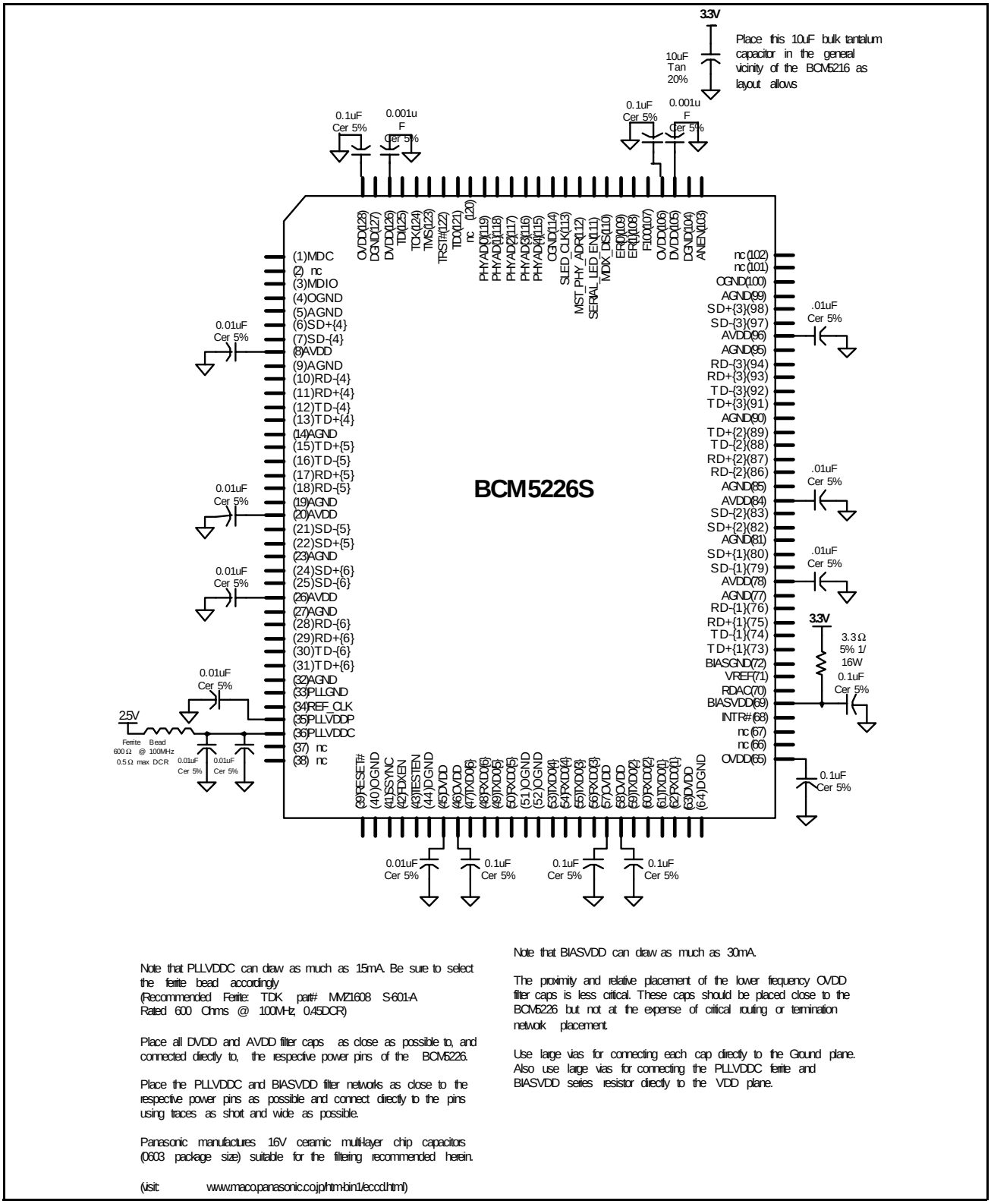

Figure 20: Relative Placement of Power Supply Filter Components

POWER SUPPLY FILTER COMPONENT RECOMMENDATIONS

Figure 21 illustrates the recommended power supply filtering and connection for the sensitive power supply pins of the BCM5226. It is important to adhere as closely as possible to these recommendations in order to ensure optimal performance. Note that placement of these components should take the highest priority of all external passive components. Additionally, it is best to refrain from routing noisy digital signal traces near these sensitive supply pins. A keep out of at least 100 mils is recommended.

Note that while the PLLVDDC pin requires special filtering as illustrated in Figure 21, the PLLVDDP pin does not require special filtering. PLLVDDP is adequately filtered as shown in Figure 20 on page 28.

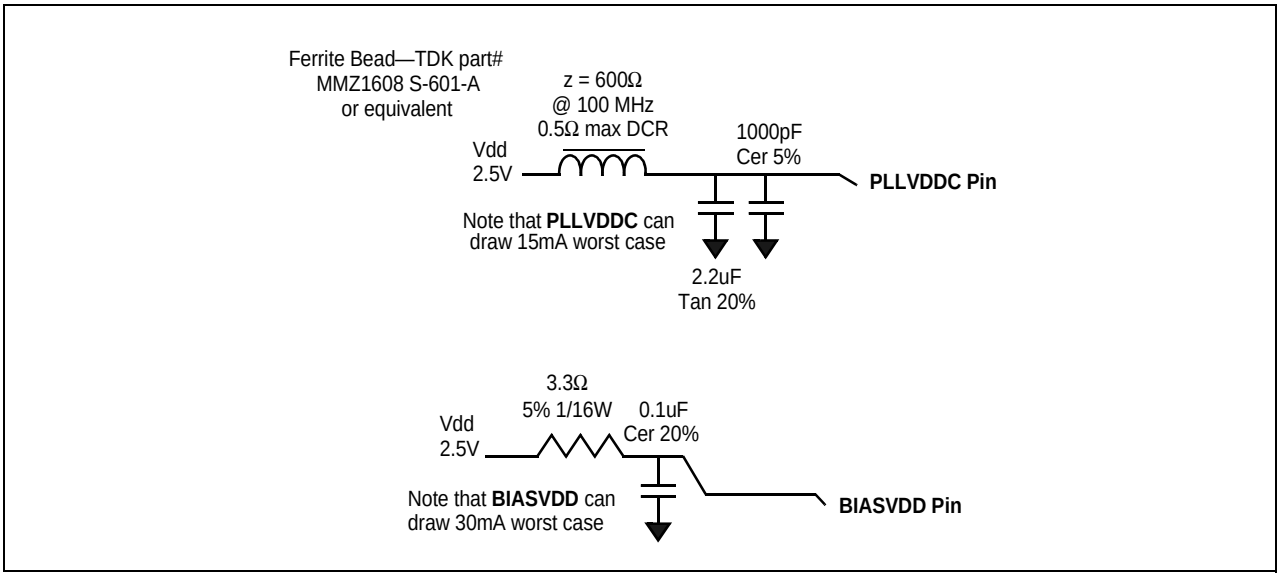

Figure 21: Sensitive Supply and Bias Pin Connection

ANALOG-RELATED PASSIVE COMPONENT PLACEMENT

Relative component placement across the analog sides of the BCM5226 is important and should be addressed with the following priorities in mind:

- Supply filter components and the RDAC resistor should be placed first and located closest to the PHY (highest priority).
- All Transmit termination resistors should be placed as close as possible to the TD+/- pins of the PHY. (the 1000pF filter cap connected between the transmit transformer primary center-tap and ground should be placed near the magnetics)
- All Receive termination network components should be placed as close as possible to the RD+/- pins of the PHY.

BOARD LAYER ALLOCATION

Figure 22 on page 31 illustrates one option for board layer allocation. This simplified example is based on a six-layer board and assumes that both a 2.5V and a 3.3V supply plane are required. Note that even though the BCM5226 does not always require a 3.3V supply, most system designs probably require 3.3V for some circuitry. Therefore, the 3.3V supply layer and accompanying ground layer are most likely necessary.

BRIDGING CHASSIS GROUND TO SYSTEM GROUND

When planning the placement of chassis ground in the layout, it is beneficial to consider placing component pads (805 size) across the void between chassis ground and system ground (see Layer 1 of Figure 22 on page 31). These component pads can be stuffed with a variety of components to experiment with reducing EMI emissions. Installing 0Ω resistors, high R value resistors, capacitors (typically 1000 pF), or leaving these pads unpopulated are options to be considered. These options can provide substantial flexibility when attempting to control EMI emissions.

GENERAL LAYOUT RECOMMENDATIONS

The following general layout recommendations ensure a robust overall system design:

- Keep all trace lengths to a practical minimum.
- Each signal trace routed between the PHY and the RJ45-8 should be controlled impedance of 50Ω.
- Refrain from routing traces with right-angle corners. Always chamfer trace corners as gradually as possible.
- Route differential pairs so that the + and – signals are matched in length.
- Route all RMII or SMII signal traces with a target characteristic impedance of 68Ω.
- Always attempt to route noisy digital traces away from sensitive power supply pins and associated filtering, such as AVDD and PLLVDD.
- If any two traces must cross each other, even though it would have to be on separate layers, always cross them at or near 90 degrees to minimize potential crosstalk.
- Always place power supply filter components as close as possible to the recommended pins (see Figure 20 on page 28) in order to maximize the filtering effects. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it via copper trace. Instead make the connection directly to the associated planes with vias.
- Avoid routing any signals (analog or digital) over non-contiguous power or ground planes, because this causes interruptions in the controlled impedance and results in reflections and a possible increase in EMI emissions.
- Leave the outer edges of the printed circuit board (approximately 200 mils) voided on all layers to minimize fringe effects, which can contribute to EMI emissions.
- Other than the chassis ground area, keep the system ground plane as a single uninterrupted plane of maximum area to create a low impedance path for all return currents. This also helps control EMI emissions. Connect all power and ground pins directly to their respective planes using large and/or multiple vias. Avoid routing traces for power and ground pin connections.
- Keep the power plane as a single, uninterrupted plane of maximum area. Splitting up power planes can create EMI problems.

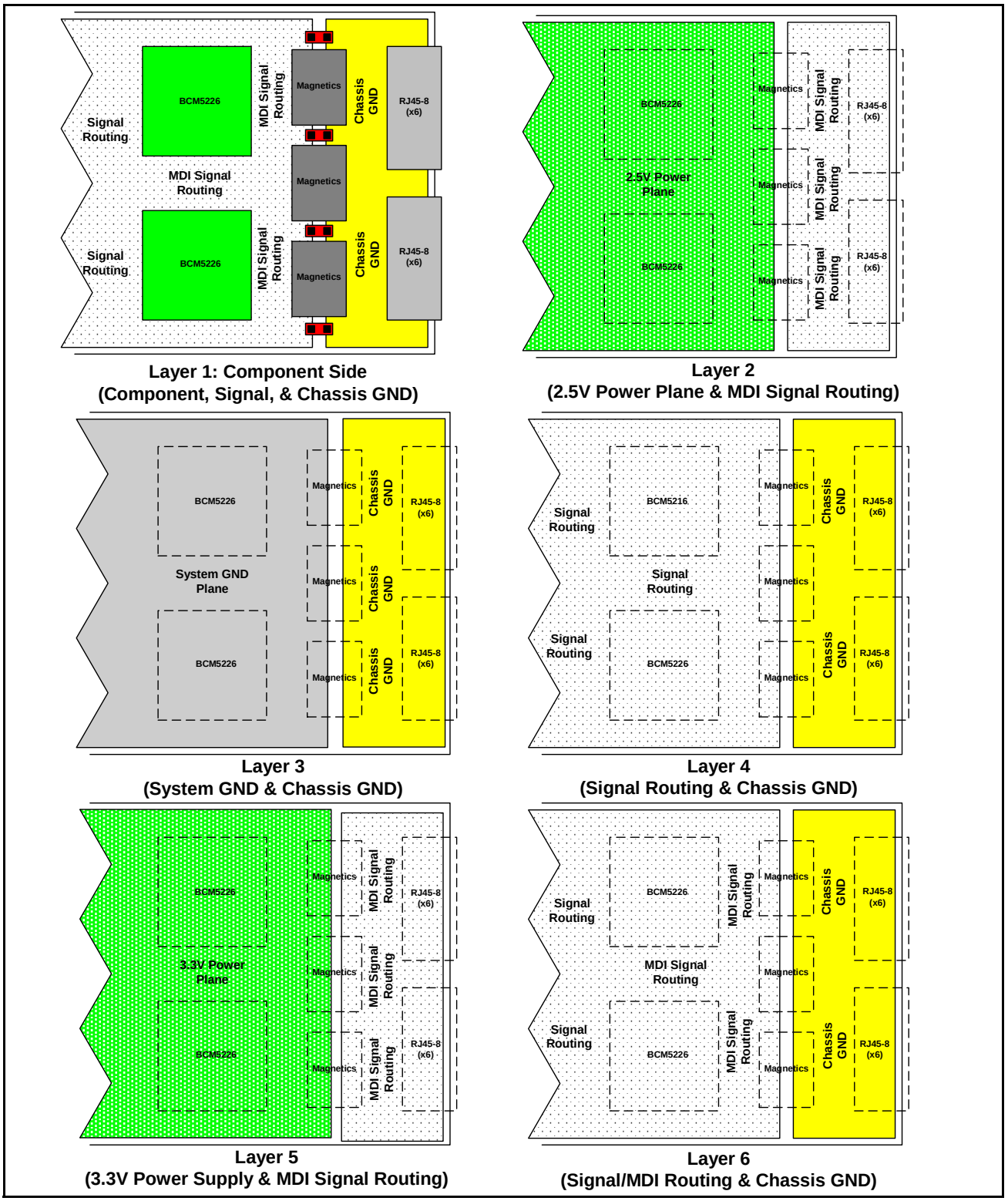

Figure 22: Board Layer Allocation Example

CONNECTING MULTIPLE BCM5226 PHYS TO MULTIPLE CONTROLLERS

This section includes simplified examples of mating multiple BCM5226 hex PHY devices to multiple quad, octal, and x16 RMII and SMII Switch ASICs. Interconnection issues including REF_CLK distribution, SSYNC distribution, and MDIO access are represented. While the examples given are based on 16-port examples, the general connection schemes apply equally to higher density port applications.

REF_CLK AND SYNC DISTRIBUTION

To support the data transfer and relative clock-to-data timing across the RMII or SMII, the 50-MHz RMII REF_CLK or the 125-MHz REF_CLK must be sourced from a crystal-based oscillator and buffered by a low-skew clock driver. This ensures that the REF_CLK phase, as received by each PHY and each MAC/switch ASIC, is maintained across all ports. For SMII applications, the system designer may choose to implement a buffered distribution for the SYNC signal as well as the REF_CLK.

If a quad or octal MAC/switch ASIC is designed to source the 50-MHz REF_CLK, then there is no way to guarantee the proper REF_CLK phase relationship for all ports. This is because of the overlapping effect of four hex PHYs (each with their own REF_CLK input) connected against, for example, three octal MAC/switch ASICs (each with their own REF_CLK output). The same problem exists between four hex PHYs and six quad MAC/switch ASICs.

It is important to use only quad or octal MAC/switch ASICs that include REF_CLK inputs, which should be the majority of those available on the market.

MDIO ACCESS

It is important to understand the requirements of the quad or octal MAC/switch ASIC with regards to MDIO serial management. In a 24-port system, a single MDIO/MDC management agent can be bussed to all four of the BCM5226 HEX PHYs to allow for individual PHY register access. In this example, each individual BCM5226 PHY requires a unique base PHYAD address, so that all 24 individual PHY ports are assigned unique addresses. This would be the preferred method of management, because it would minimize complexities in interconnect between PHYs and ASICs. The trade-off, however, is software complexity and control. The software or firmware used to access the individual PHY registers has to allow for this segmentation. As a result, the register access for a given PHY port would be managed through a given MAC/switch ASIC that is not necessarily exchanging data across the RMII with that specific PHY.

There is no standardized requirement mandating that a given MAC/switch ASIC device connected via RMII to a given PHY device must also supply the MDIO management agent. However, this aspect is important when planning system level architecture. Any RMII/SMII MAC/switch ASICs that require the MDIO access to be used in conjunction with RMII/SMII interconnect may require external work-around circuitry to implement them in a BCM5226-based design. Some MAC/switch devices include on-board MDIO arbitration to resolve this type of implementation issue.

UNUSED PORTS

When designing systems where the number of ports is not a multiple of six (for example, 16 ports) you can still use the BCM5226, because there may be cost/port and board layout advantages in using one half of a BCM5226 versus designing a system based on a mix of hex and quad PHY devices. In such an implementation, you can configure the unused ports of the BCM5226 so that none of the outputs is switching, to help reduce power and minimize system noise.

AUTO-NEGOTIATION CONFIGURATION NOTES

This section includes details about configuration and operation of the BCM5226 with Auto-Negotiation and Forced modes of operation.

- Auto-Negotiation can only be selected when the ANEN pin is high (or left floating).
- Auto-Negotiation can only be controlled by software (enabled or disabled) when the ANEN pin is high (or left floating).
- Auto-Negotiation cannot be controlled (enabled or disabled) via software if the ANEN pin is low.
- Auto-Negotiation is automatically disabled for any port that is configured for 100BASE-FX operation.
- Software configuration of a forced speed is only possible when ANEN is high (or left floating).
- Software configuration of duplex mode is independent of the state of the ANEN pin. However, the FDX pin must be tied low to allow software selection of half- or full-duplex.
- Auto-Negotiation is automatically disabled on a per-port basis when 100BASE-FX is selected.
- The Auto-Negotiation process can take up to three seconds to complete, worst-case (per IEEE 802.3u, clause 28).

THERMAL INFORMATION

This section includes basic thermal information pertaining to the BCM5226 and the 128-MQFP package. Table 5 provides a comparison of Theta-JA versus Airflow.

Table 5: 128-pin MQFP Theta-J_A vs. Airflow

128-pin MQFP Package	***AIR FLOW (feet per minute)***		
	0	***200***	***500***
Theta-J_A (C/W)	20.48	19.13	19.63
Power Dissipation (W)	1.8	1.8	1.8

Theta-JC for the 128-pin MQFP package is given as 20.48 C/W (@ 0 m/s airflow). Additionally, the BCM5226 is designed and rated for a maximum Junction Temperature of 125C°.

Table 6: 160-pin PQFP Theta-J_A vs. Airflow

160-pin PQFP Package	***AIR FLOW (feet per minute)***		
	0	***200***	***500***
Theta-J_A (C/W)	TBD	TBD	TBD
Power Dissipation (W)	TBD	TBD	TBD

Theta-JC for the 160-pin PQFP package is given as C/W (@ 0 m/s airflow). Additionally, the BCM5226 is designed and rated for a maximum Junction Temperature of 125C°.

An equation for determining whether a given ambient environment will provide safe operating conditions (to maintain reasonable die junction temperature) for the BCM5226 is given as:

Tj = Ta + (Tja * Pd)

where:

Tj = junction temp

Ta = ambient temp

Tja = Theta-JA

Pd = Power Dissipation

By using this equation and figures for the BCM5226 in the 128-pin MQFP package, it is observed that under worst case conditions (maximum power, maximum ambient temp, and no air flow), the maximum Junction temperature (which is rated at 125C°) is not exceeded.

Tj = (70C) + (20.48C/W * 1.8W) = 106.9degrees Celsius

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