BROADCOM®

APPLICATION NOTE

BCM5222
Design Guide

10/10/01

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REVISION HISTORY

Revision #	*Date*	*Change Description*
5222-AN00-R	01/19/01	Initial release
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TABLE OF CONTENTS

Overview 1
Internal Pull-ups and Pull-downs 1
25-MHz Reference Clock 2
RDAC 3
Low-Power Modes 4
Typical Power Consumption 4
Dual-Function Pins 4
Serial 10m (7-Wire Interface) 5
Auto-MDI / MDIX Crossover 5
Magnetics 6
Cable Length Monitoring Capability 7
JTAG Considerations 8
Supply Pins and Power Planes 8
10/100 Twisted Pair MII to MDI 9
General Layout Notes 9
Analog Related Passive Component Placement 9
TD± Trace Routing 9
100BASE-TX and 10BASE-T Signaling 9
RD± Trace Routing 9
Reference Clock 9
Magnetics to RJ45 9
Chassis Ground 10
Board Layer Allocation 10
Power Supply Filter Component Placement 10
General Layout Recommendations 10

LIST OF FIGURES

Figure 1: Typical Crystal Application 3
Figure 2: Typical Clock Module Application 3
Figure 3: BCM5222 Serial 10 (7-Wire) Interface 5
Figure 4: Magnetics Connection and Differential Cable Termination Requirements 7
Figure 5: BCM5222 Schematics 11
Figure 6: Power Decoupling and Filtering 12
Figure 7: PCB Layer Allocation 13

LIST OF TABLES

Table 1: BCM5222 Power Measurements 4
Table 2: Cable Length Estimate 7
Table 3: JTAG Signals 8

OVERVIEW

This application note contains detailed information regarding use of the BCM5222 dual-port 10/100BASE-TX transceiver. The BCM5222, running on 1.8V and 3.3V power supplies, includes two fully integrated, low-power transceivers, operating in half- or full-duplex with full Auto-Negotiation capability. This single-chip solution is targeted for a number of applications requiring low-power and robust network tolerance, including but not limited to IP phones, backplane bus communication, embedded telecom, and print servers.

The BCM5222 supports Auto-MDIX, special LED modes, multiple power management modes, loopback mode, and cable monitoring indicators.

The BCM5222 supports 100BASE-TX with MII interface, or 10BASE-T with either MII interface or serial interface (7-wire).

Broadcom highly recommends to read this application note in conjunction with the latest revision of the BCM5222 data sheet and product errata.

The BCM5222 is available in a 100-pin PQFP or 100-pin fpBGA.

INTERNAL PULL-UPS AND PULL-DOWNS

Some input pins on the BCM5222 include internal resistive pull-ups or pull-downs in order to set the chip into a known default if any of the pins are left floating. The value of each internal pull-up or pull-down is approximately 50 kΩ (± 20%).

- TXD[3:0]{1.2} > pull-down
- TXEN{1.2} > pull-down
- TXER{1.2} > pull-down
- MDC > pull-down
- PHYAD[4:2] > pull-down
- MDIX_DIS > pull-down
- $\overline{\text{TRST}}$ > pull-down
- TESTEN > pull-down
- LOW_PWR > pull-down
- MDIO > pull-up
- $\overline{\text{RESET}}$ > pull-up
- F100 > pull-up
- ANEN > pull-up
- DLLTEST > pull-up
- FDX > pull-up
- ADV_PAUSE{1.2} > pull-up
- PHYAD[1:0] > pull-up
- PAUSE{1.2} > output pull-down

25-MHz Reference Clock

The BCM5222 device accepts a 25-MHz reference clock from a low-cost crystal circuit with parallel resonance, operating in the fundamental mode. Alternatively, the reference clock can be driven by a 25-MHz single-ended clock oscillator. See Figure 5 on page 11 for a schematic of clock connection requirements.

Broadcom recommends that the crystal be located as close to the XTALI and XTALO pins of the BCM5222 as possible to minimize stray capacitance due to excessive trace routing that could interfere with crystal start-up as well as clock stability.

Broadcom recommends the use of a crystal rated for a total load capacitance of 18 pF. A calculation for deriving the approximate load capacitance is: $((C_{L1} \times C_{L2})/(C_{L1} + C_{L2})) + C_{s,}$ where $C_{L1} \times C_{L2}$ are the actual load capacitors connected to either side of the crystal, and C_s is the sum of the stray capacitance and input pin capacitance of the PHY device. Assuming load caps of 22 pF each and a total stray + parasitic capacitance of approximately 8pF, the above equation yields a total load capacitance of around 18pF. The load capacitor values may need to be adjusted from the example above to account for variations in parasitic capacitance and/or the crystal specification.

The electrical specifications recommended for the crystal clock source are as follows:

- Frequency tolerance: ±50 ppm
- 50% duty cycle: ±10%
- Edge rates: from 1 ns to 4 ns (10% to 90%)
- Voltage swing: limited to PLLAVDD maximum
- Crystal aging: ±5 ppm per year, maximum
- Crystal frequency stability (over temperature): ±10 ppm

A crystal clock device exhibiting good performance in a variety of Broadcom's evaluation platforms is the Epson part number MA-506-25.000M-C2 (http://www.epson-electronics.de/download/downcrys.htm), Digi-Key part number SE2639CT-ND.

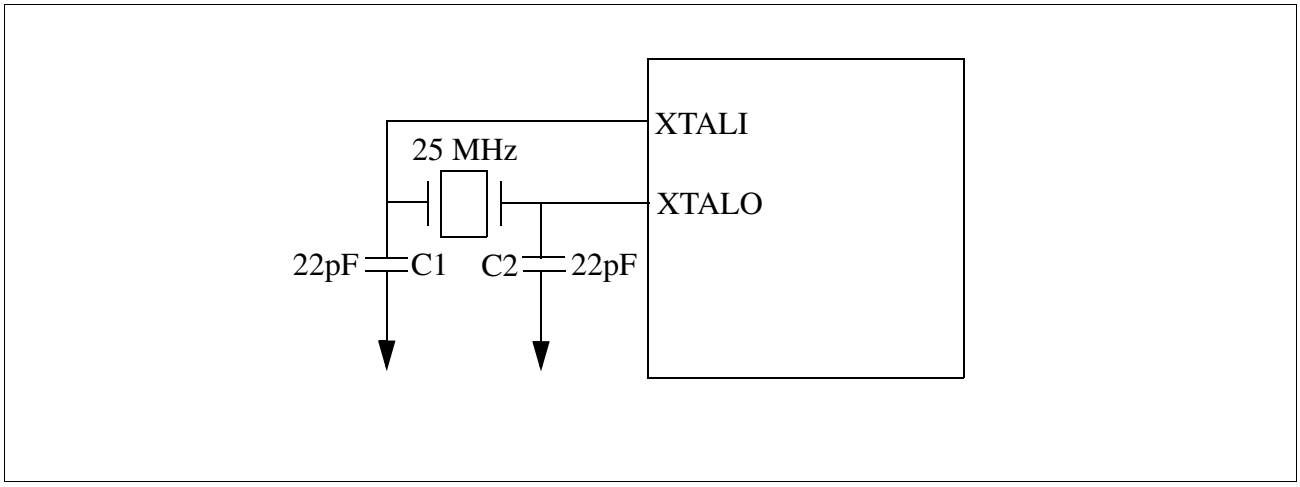

Figure 1: Typical Crystal Application

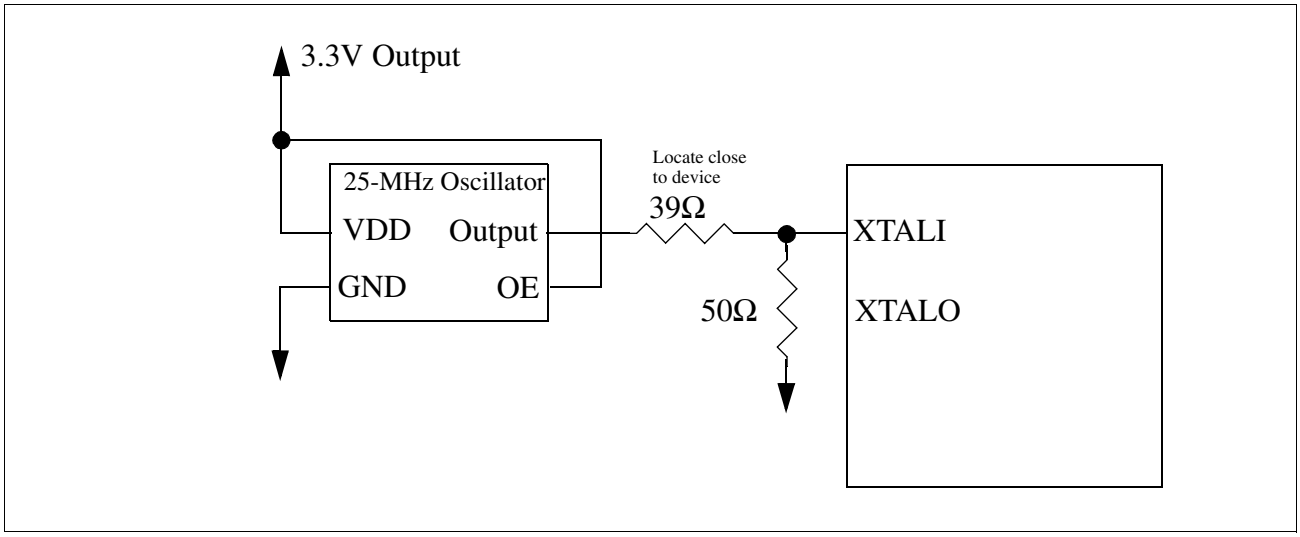

Figure 2: Typical Clock Module Application

RDAC

The 100BASE-TX and 10BASE-T transmit amplitudes can be directly controlled by adjusting the amount of current allowed to flow from the RDAC pin to GND. It is recommended that in order to verify proper transmit signal amplitude for a given design, an initial value of 1.31K Ω (1%) be used for the external RDAC resistor (see Figure 5 on page 11). It is important to note that the transmit signal amplitude can be affected by magnetics insertion loss as well as stray capacitance in the front-end design. Therefore, it is important to quantify these additional possible sources of attenuation and adjust the value of the RDAC resistor accordingly to compensate.

A 1% change in RDAC current results in a 1% change in transmit amplitude at the TD± outputs. Increasing the value of the RDAC resistor results in a proportional decrease in transmit amplitude, and vice-versa.

Low-Power Modes

The BCM5222 supports several power management modes as discussed in the data sheet.

Force IDDQ mode can be activated by writing a 1 to bit 0 of shadow register 1Ah. In Force IDDQ mode, all of the chip's circuitry is disabled including receive circuitry and MII management. The only way to exit this mode and return to normal functioning is to issue a hardware reset.

Activate low-power mode by writing a 1 to bit 1 of the shadow register 1Ah. In this mode the BCM5222 circuitry is disabled, including the management interface. By setting bit 2 of shadow register 1Ah to logic value 1 prior to entering low-power mode, the clocks are enabled in this state. If the clocks are enabled in low-power mode, the BCM5222 can return to normal mode by deasserting the low-power pin or by writing to register 1Ah, bit 1. Wait at least 2 ms before resuming normal activity. Otherwise, if the clocks are disabled, the BCM5222 can only return to normal operation mode by hardware reset.

Typical Power Consumption

The BCM5222 uses 1.8V and 3.3V to power the chip circuitry. The following table summarizes the estimated current and power used under typical conditions. These values are helpful to the system designer in determining the power supply requirements on the system board. The worst-case power consumption, with supplies at +5%, increases the typical power consumption by 10 – 15%.

The power estimates in the following table are based on an external transformer center-tap supply. This supply may sink approximately 90 mA additional current.

Table 1: BCM5222 Power Measurements

Nominal			
Supply	**Voltage**	**Current**	**Power**
AVDD	1.80V	66 mA	119 mW
PLLVDD	1.80V	11 mA	20 mW
DVDD	1.80V	32 mA	58 mW
BIASVDD	3.30V	11 mA	36 mW
OVDD	3.30V	33 mA	109 mW
Total Power		**341 mW =**	**171 mW/Port**

Dual-Function Pins

Several hardware pins on the BMC5222 have dual functions associated to them. They assume one function if the device is put into JTAG testing mode, by setting $\overline{\text{TRST}}$ pin high, and they have another function when the device is not in JTAG mode.

TDI/TXER{2}—The JTAG test data input pin serves as a serial data input to the JTAG controller. The TXER pin serves as a indicator to PHY2 when the MAC encounters an error in the transmitted data.

TCK/FDX—The JTAG test clock is used to synchronize the data transmitted to the JTAG controller. The full-duplex pin sets the device to full-duplex if the Auto-Negotiation bit is disabled. This function is logically ORd with bit 8 of register 0h.

TDO/PAUSE{1}—The JTAG test data output pin serves as a serial data output from the JTAG controller. The pause{1} pin serves as an output reflecting the status of the link partner's PAUSE bit, bit 10 of register 05h.

TMS/TXER{1}—The JTAG test mode select pin serves as a serial data input to the JTAG controller. The TXER pin serves as an indicator to PHY1 when the MAC encounters error in the transmitted data.

SERIAL 10M (7-WIRE INTERFACE)

The BCM5222 interfaces to most microprocessors via a serial 10M interface, also referred to as a 7-wire interface. This MAC interface allows minimal pin connections, but requires serial data to traverse the TXD and RXD data lines at 10 MHz speed. This mode can be enabled via the serial management interface by writing a 1 to bit 1 of register 1Eh.

Figure 3 illustrates the connection between the BCM5222 and a typical microprocessor. This figure represents connection with the commonly used Motorola microprocessors, such as the MPC850, the 860, and so on.

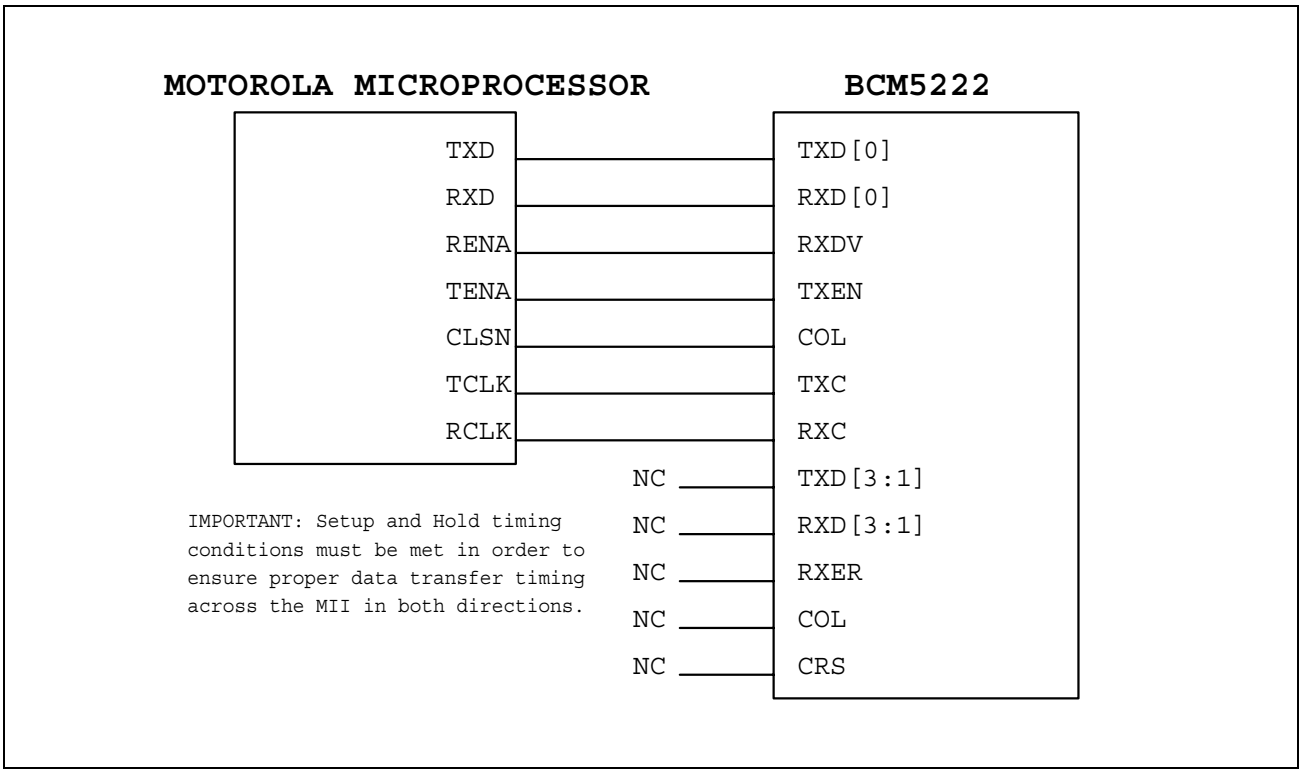

Figure 3: BCM5222 Serial 10 (7-Wire) Interface

AUTO-MDI / MDIX CROSSOVER

In most 10/100BASE-TX connections, one end of the link is configured as an MDI (Medium Dependent Interface) and the opposite end of the link is configured as a MDI crossover (MDIX), so that each transceiver's transmitter is connected to the other's receiver. This allows the end user to install straight-through cables. However, there are many instances where cross-over cables are required, and this can cause significant confusion and downtime in the field. The BCM5222 contains the ability to perform auto-MDI/MDIX crossover on-chip, thus eliminating the need for crossover cables or cross-wired (MDIX) ports. Auto-MDI/MDIX capability is available on both ports of the BCM5222.

During Auto-Negotiation and 10/100BASE-TX operation, the BCM5222 normally transmits on TD± pins and receives on RD± pins. When connected via a straight-through cable to another device that does not perform the auto-MDI/MDIX crossover, the BCM5222 automatically switches its transmitter to the RD± pins and its receiver to the TD± pins, if required, in order to communicate with the remote device. If two devices are connected that both have auto-MDI/MDIX crossover capability, then a random algorithm determines which end performs the crossover function.

The auto-MDI/MDIX crossover feature is a function of Auto-Negotiation. If the BCM5222 is configured not to perform Auto-Negotiation, the feature does not work, and a specific cable is required to ensure the transmit function at one end of the cable is connected with the receive function at the other end of the cable. This feature is enabled by default, but can be disabled by setting bit 11 in register 1Ch to a 1. During operation, the MDI state can be determined by reading bit 13 of register 1Ch, as indicated in the BCM5222 data sheet. Additionally, a manual MDI swap can be forced by setting or clearing bit 12 of register 1Ch.

Auto-MDI/MDIX operates only on the transmit and receive data pairs (swapping them if required). It does not operate on the individual wires within a given pair and therefore does not correct for polarity swap issues. However, the BCM5222 contains an additional polarity correction feature that will automatically correct this problem.

Specific magnetics and cable termination issues must be considered when using the BCM5222 in auto-MDI/MDIX mode. See the following section for further detail.

MAGNETICS

One important restriction in pairing magnetics with the BCM5222 relates to the ordering of isolation transformer and common mode choke in the transmit signal path, and in the receive signal path when auto-MDI/MDIX is enabled. The transmit output signal from the BCM5222 must be connected to the isolation transformer first, followed by the common mode choke (as depicted in Figure 4 on page 7). If any common mode choke is placed between the transmit output pins and the isolation transformer, potentially severe signal distortion results while operating in 10BASE-T and Auto-Negotiation modes.

The following list includes recommended channel magnetics components from various vendors for use with the BCM5222. The use of these magnetics is recommended regardless of whether auto-MDI/MDIX is enabled.

- **Bel** S558-5999-W2
- **Pulse Engineering** H1102
- **Halo** TG110-S050N2

Figure 4 on page 7 illustrates specific magnetics interconnect and differential cable termination requirements for applications that use auto-MDI/MDIX.

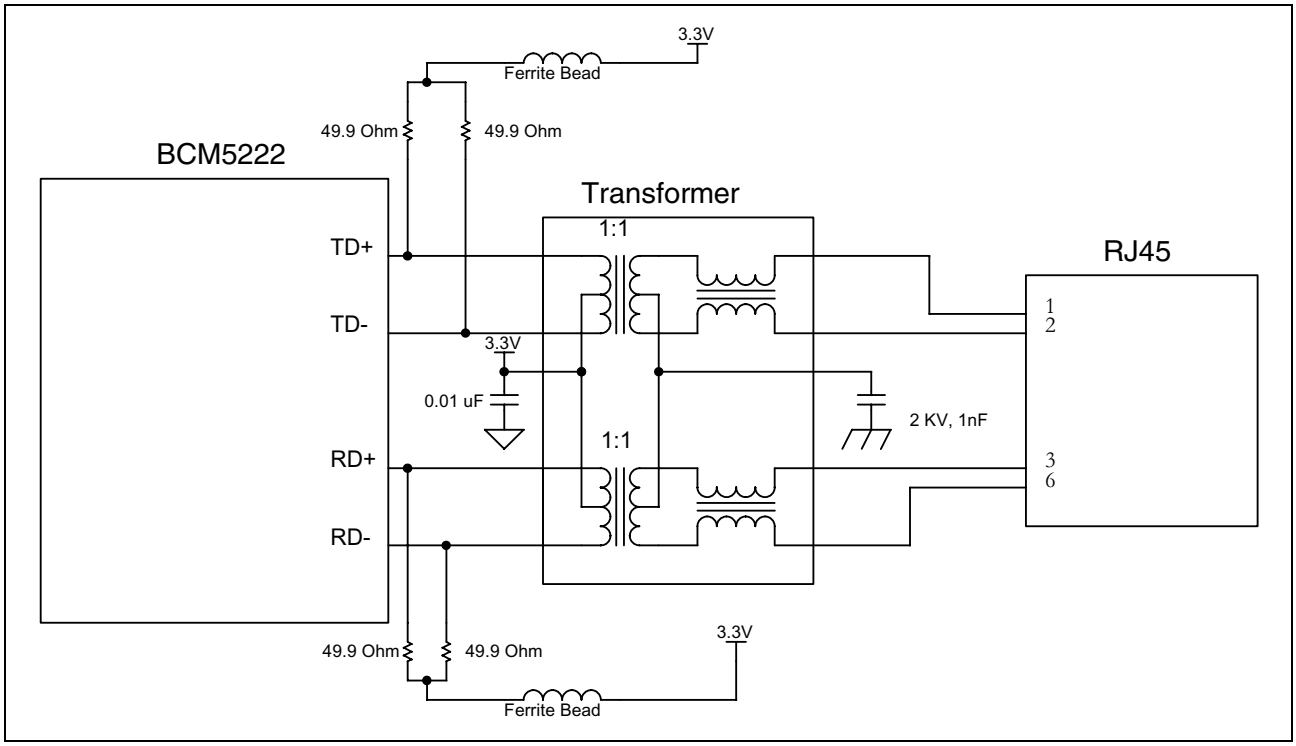

Figure 4: Magnetics Connection and Differential Cable Termination Requirements

CABLE LENGTH MONITORING CAPABILITY

The DSP nature of the 100M receiver within the BCM5222 allows real-time access to equalizer states that provide cable length estimate information.

Specifically, bits [14:12] in shadow register 1Bh provide a ±10 meter length estimate of the CAT 5 cable connected to the receiver inputs of the BMC5222, assuming of course that the far end station is operational. This estimate is accessed by simply reading the aforementioned bits. This provides the user with an easily accessed and powerful diagnostic tool for determining potential problems within the cable plant and/or associated connectors. See Table 2 for decode.

Table 2: Cable Length Estimate

Register 1Bh 14, 13, 12	*Cable Length in Meters*
000	<20
001	20 to <40
010	40 to <60
011	60 to <80
100	80 to <100
010	100 to <120
100	120 to <140
010	>140

JTAG CONSIDERATIONS

The BCM5222 has several pins dedicated to providing JTAG functionality. Each of these pins have a specific JTAG function, which is enabled only when the $\overline{TRST}$ pin is set high. When the $\overline{TRST}$ pin is driven to logic low, the JTAG functionality is disabled and an alternative pin function is enabled. This pin sharing provides for JTAG functionality without significantly increasing the device pin count on the feature rich BCM5222 (see "Dual-Function Pins" on page 4).

Table 3: JTAG Signals

JTAG Signal	*Type*	*Description*
TRST	I_{PD}	Test Reset. When this pin is pulled high, the JTAG circuitry is activated. When this pin is pulled low, the JTAG controller is reset, and the device returns to normal functioning.
TCK	I_{PU}	JTAG test clock input. This signal is multiplexed with the FDX signal.
TMS	I_{PD}	Test Mode Select input. This signal is multiplexed with the TXER{1} signal.
TDI	I_{PD}	Test Data Input. This signal is multiplexed with the TXER{2} signal.
TDO	I/O_{3S}	Test Data Output. This signal is multiplexed with PAUSE{1}.

I_{PD} = Input with internal pull-down. I_{PU} = Input with internal pull-up.

I/O_{3s} = Input/Output with a three state output

SUPPLY PINS AND POWER PLANES

The BCM5222 requires a 1.8V and a 3.3V power supply. A solid power supply plane is recommended for each supply. Fragmenting, segmenting, or otherwise interrupting a power supply plane is not recommended. The types of power supply pins are as follows:

DVDD - These pins supply a 1.8V supply to the internal digital core circuitry. Connect to decoupling capacitors as shown in Figure 6 on page 12.

AVDD—These pins supply a 1.8V supply to the internal analog core circuitry. Connect as shown in Figure 6 on page 12.

OVDD—These pins supply power to the digital output buffer stages and are to be connected to a 3.3V supply.

BIASVDD—This pin supplies power to the internal bias generator. Though this pin is not as sensitive as the PLLAVDD pin, described below, it is still more noise sensitive than the OVDD pins and deserves special consideration. Thus, it is recommended that a special low pass filter circuit be used as shown in Figure 6 on page 12.

PLLAVDD—This pin supplies power to the phase locked loop circuitry. This is the most sensitive power pin on the device, so Broadcom recommends that a special low-pass circuit filter be used, as shown in Figure 6 on page 12.

10/100 Twisted Pair MII to MDI

Figure 5 on page 11 represents a typical 10/100 twisted pair DTE implementations, MII to MDI inclusive, for the BCM5222.

General Layout Notes

When determining component placement and routing for a BCM5222-based design, the following recommendations help optimize system design and performance.

Analog Related Passive Component Placement. Relative component placement across the analog side of the BCM5222 is critical and should be addressed with the following priorities in mind:

- Power supply filter components should be placed first and located closest to the PHY (highest priority).
- Transmit termination resistors should be placed as close as possible to the TD± pins of the PHY.
- Receive termination network should be placed as close as possible to the RD± pins of the PHY.

TD± Trace Routing. When routing the TD± signal traces from the PHY to the 1:1 transformer, the traces should be routed adjacent to a ground plane for controlled characteristic impedance. Broadcom recommends that the TD+ and TD– signal traces be routed with matched length, as short as possible, and with a characteristic differential impedance of 100Ω.

100BASE-TX and 10BASE-T Signaling. The BCM5222 incorporates a unique transmit drive architecture that sinks current instead of sourcing current. In 100BASE-TX mode, 40 mA is always pulled down through the transmit transformer's primary winding (via the center tap connection to VDD) and is steered in one direction of the other, depending on the state of the transmit DAC. This generates a true differential 2V nominal peak-to-peak voltage swing that is centered around the VDD center tap potential of the transmit transformer.

When configured for 10BASE-T operation, the transmit DAC operates in class AB mode. This implementation conserves device power by reducing the total transmit current required to generate the IEEE compliant Manchester encoded signaling. In order to ensure that the transmit signal retains optimal integrity, it is recommended that the controlled impedance transmit path from the PHY to the magnetics be kept as short and direct as possible with minimum vias, and with properly placed termination.

RD± Trace Routing. The RD+ and RD– traces, which connect the receive transformer to the PHY, should be routed with a differential characteristic impedance of 100Ω and should be routed adjacent to a ground plane. Again, matched trace length is important.

Reference Clock. Minimize trace length from the crystal to the XTALI and XTALO pins of the BCM5222. This helps minimize stray capacitance and noise pick-up that might otherwise affect the reference clock integrity. In a worst case scenario, too much parasitic capacitance and/or inductance in the crystal traces could cause the crystal to suffer from start-up problems and/or instability.

Magnetics to RJ45. Broadcom recommends that properly grounded (usually to the chassis ground) shielded RJ45 media connectors are used to control EMI emissions.

When routing the transmit and receive pairs between magnetics and the RJ45, Broadcom recommends that an inner layer or layers be used. The outer layers (top and bottom) can then be dedicated to chassis ground in the area between the magnetics and the RJ45. This helps isolate the sensitive analog signals from external noise sources and helps to reduce EMI emissions. See Figure 7 on page 13.

Chassis Ground. When planning the placement of chassis ground in the layout, consider placing at least two component pads (1206 size) across the void between chassis ground and system ground (see Figure 7 on page 13). These component pads can be stuffed with a variety of components to reduce EMI emissions. Installing OΩ resistors, high R-value resistors, capacitors, or leaving these pads unpopulated are options that can provide substantial flexibility for controlling EMI emissions.

Board Layer Allocation. Figure 7 on page 13 illustrates one option for board layer allocation. Because the BCM5222 requires both 1.8V and 3.3V power supplies, two VDD planes are allocated.

Power Supply Filter Component Placement. Power supply filter component placement is illustrated in Figure 5 on page 11. Use these general placement guidelines to ensure optimal performance.

General Layout Recommendations. The following general layout recommendations help ensure a robust overall system design:

- Keep all trace lengths to a minimum, especially for the more sensitive signal traces between the PHY and RJ45.
- Each signal trace routed between the PHY and the RJ45 should be controlled impedance of 50Ω (100Ω differential).
- Refrain from routing traces with right-angle corners. Always chamfer trace corners as gradually as possible.
- Route differential pairs such that the + and – signals are matched in length.
- Route all MII signal traces with a target characteristic impedance of 50Ω.
- Always attempt to route noisy digital traces away from sensitive power supply pins and associated filtering such as AVDD.
- If any two traces must cross each other, even though it would have to be on separate layers, always cross them at 90 degrees to minimize potential crosstalk.
- Always place power supply filter components as close as possible to the recommended pins (see Figure 6 on page 12) in order to maximize the filtering effects. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it via copper trace. Instead make the connection directly to the associated planes with vias.
- Refrain from routing any signals (analog or digital) over noncontiguous power or ground planes as this causes interruptions in the controlled impedance and results in reflections and a possible increase in EMI emissions.
- Leave the outer edges of the PCB (approximately 200 mils) voided on all layers to minimize fringe effects that could otherwise contribute to fringe effects.
- Other than the chassis ground area, keep the system ground plane as a single uninterrupted plane of maximum area to create a low impedance path for all return currents. This will also help control EMI emissions.
- Connect all power and ground pins directly to their respective planes via large and/or multiple vias. Avoid routing traces for power and ground pin connections.

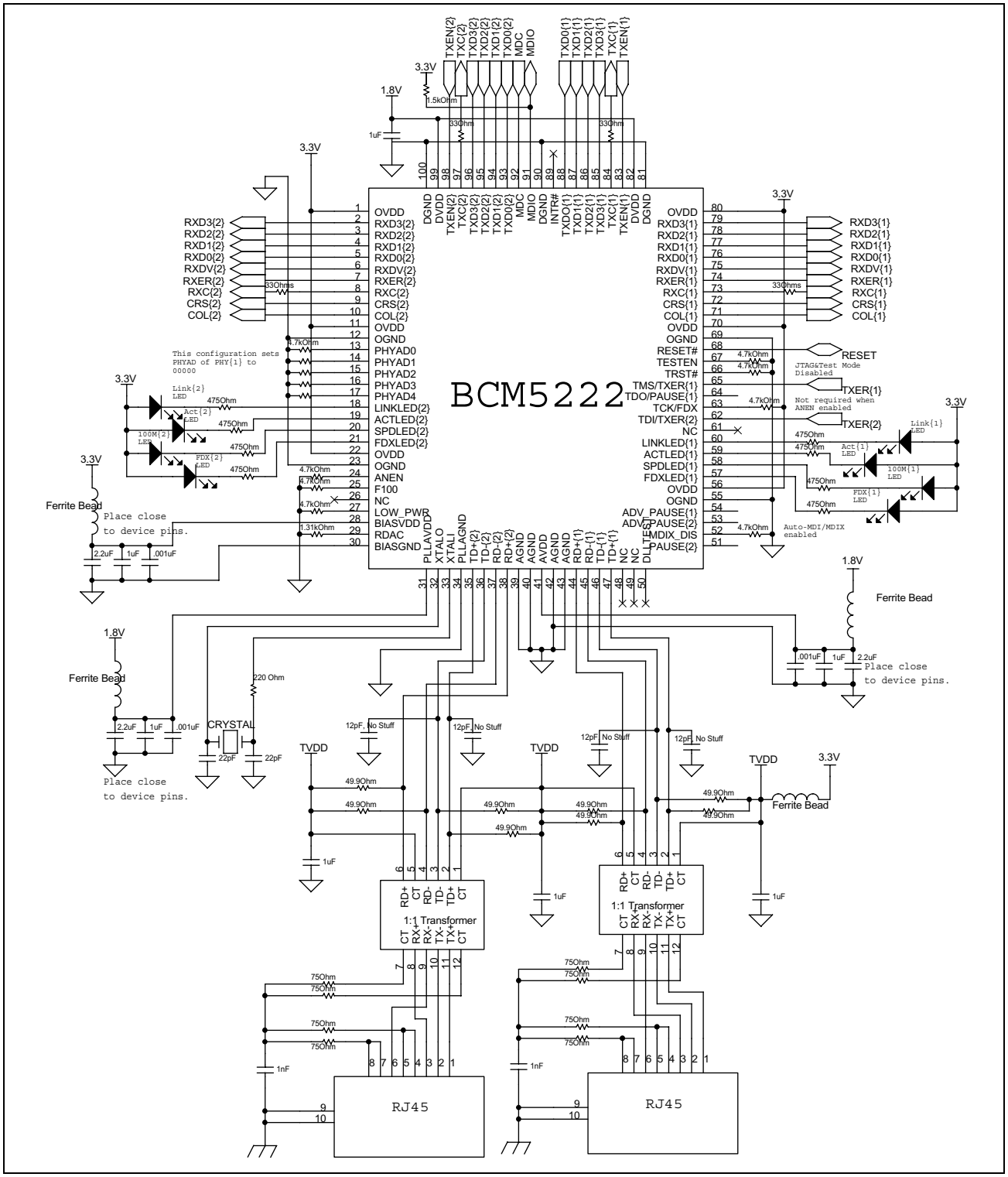

Figure 5: BCM5222 Schematics

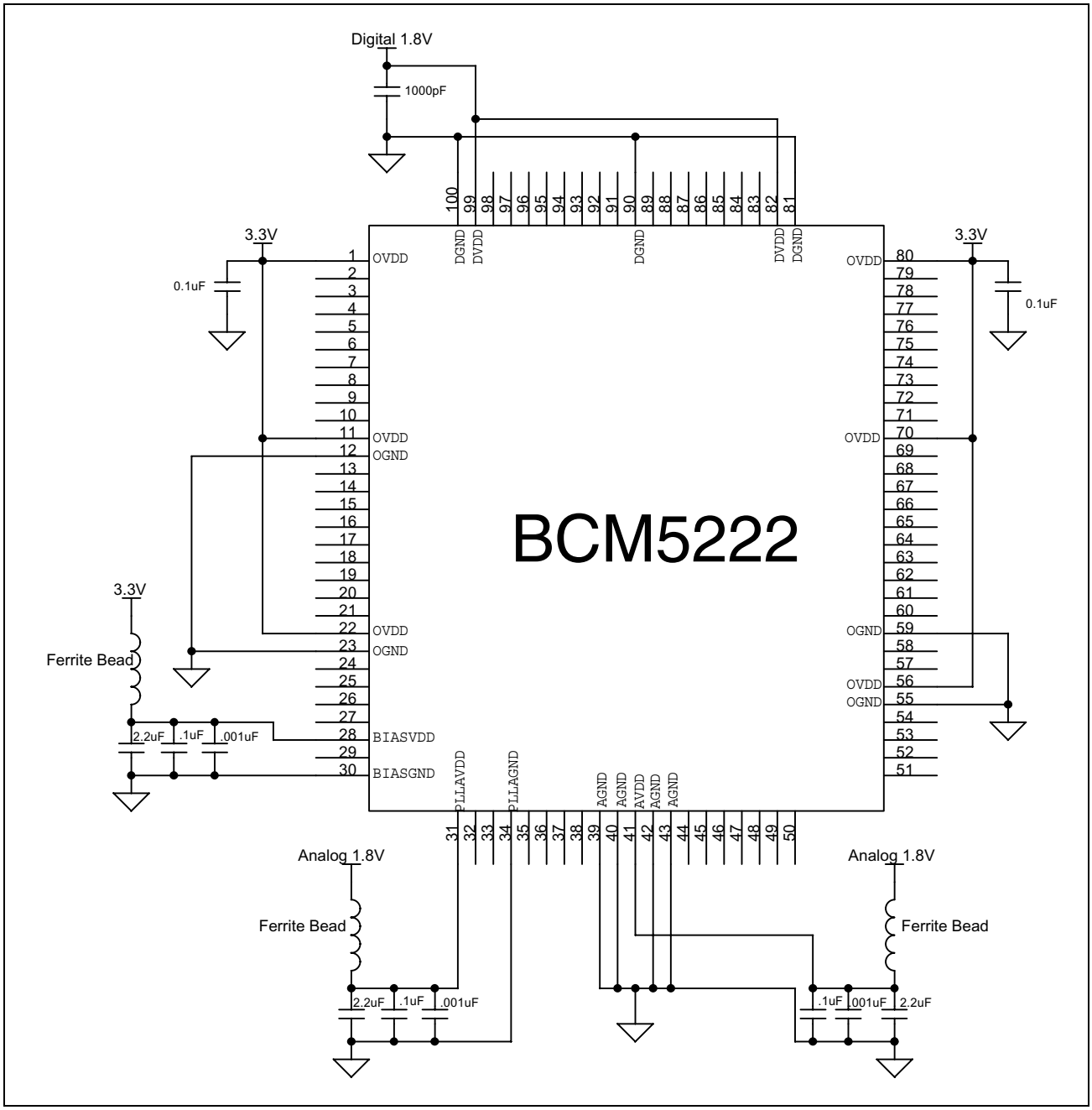

Figure 6: Power Decoupling and Filtering

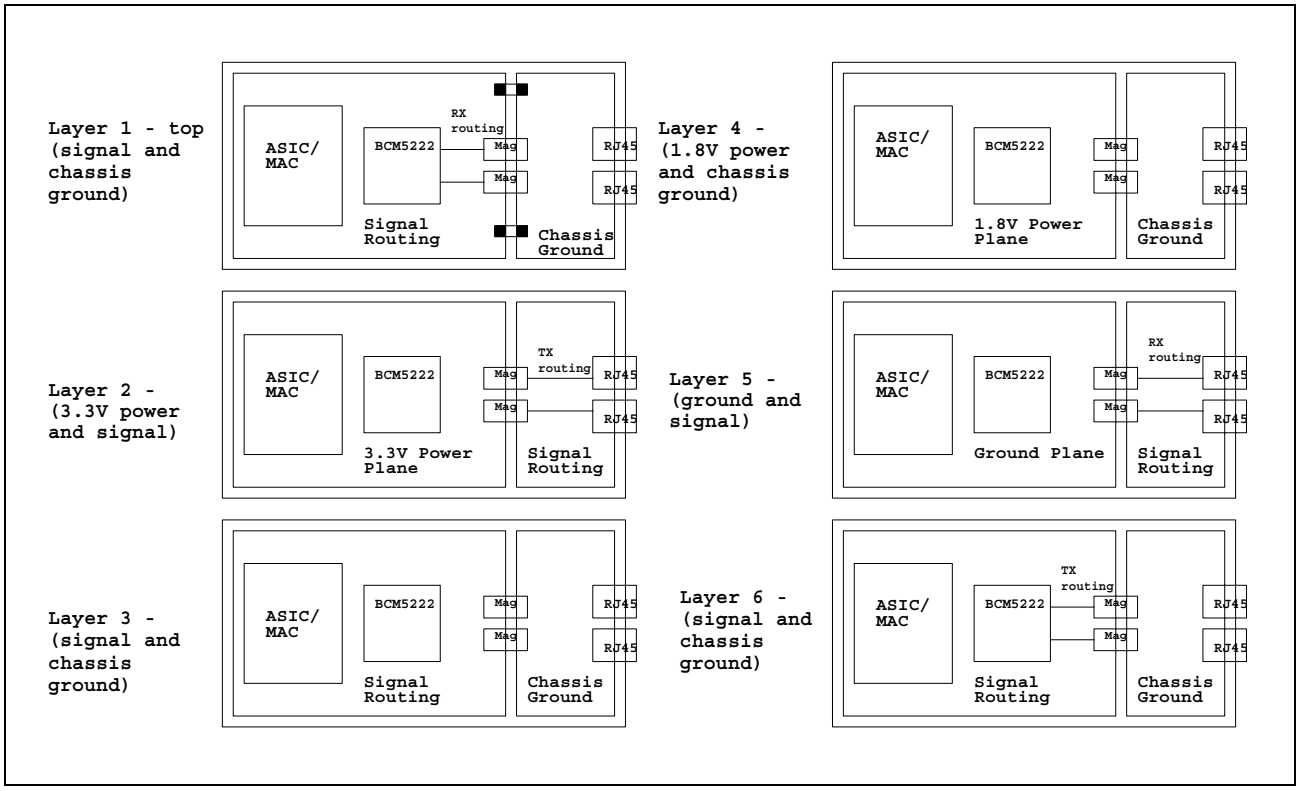

Figure 7: PCB Layer Allocation

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