APPLICATION NOTE

BCM5221/5220

7/7/00

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REVISION HISTORY

REVISION #	*DATE*	*CHANGE DESCRIPTION*
AN01-R	7/7/00	Initial release

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OVERVIEW

This application note contains detailed information regarding the use of the BCM5221 single channel 10/100 Physical Layer Device. The BCM5221, capable of either 2.5V or 3.3V operation is targeted for single port or odd port copper or fiber designs such as NIC, motherboard, additional switch port, and MAU type implementations. Dual port designs, such as a dual-port 10/100 uplinks are also discussed herein.

The BCM5221 includes the following features: Auto-MDIX switching capability, Glueless media conversion capability (100BASE-TX to 100BASE-FX), and Cable Quality Monitoring capability.

The BCM5221 is actually a 2.5V device that includes on-chip 3.3V to 2.5V regulators making it suitable for 3.3V system applications. The BCM5221 is not suitable for applications that run exclusively at 5.0V. The system designer should consider the BCM5201/02 for single chip 5.0V applications.

It is recommended that this application note be read in conjunction with the latest versions of the BCM5221 data sheet and other 5221 application notes in order to ensure the most robust design possible.

The BCM5221 is available in a 64-pin 10 mm^2 PQFP package (part number BCM5221KPT).

The BCM5221 is also available in a 64-ball 8 mm^2 FBGA package (part number BCM5221KPB). This is the lowest power, highest performing single channel PHY available today.

The BCM5220 is identical to the BCM5221 with the exception of a few features. These differences are described at the end of this application note.

2.5V/3.3V TOLERANCE

There are three basic power supply configurations that can be used with the BCM5221. It can operate exclusively at 2.5V, it can operate exclusively at 3.3V, or it can operate with the core running at 2.5V while the I/O runs at 3.3V. The latter configuration is the most typical where low power and 3.3V digital compatibility are required.

The BCM5221 digital inputs are 3.3V tolerant and can accept 3.3V CMOS logic levels as long as the OVDD pins are tied to 3.3V. Additionally, the digital outputs will source 3.3V CMOS levels when the OVDD pins are tied to 3.3V. If the OVDD pins are tied to 2.5V, then all digital inputs and outputs are limited to a 2.5V signal swing.

The BCM5221 is not 5V tolerant.

Figure 1 on page 2 illustrates power supply connections for the three configurations described above.

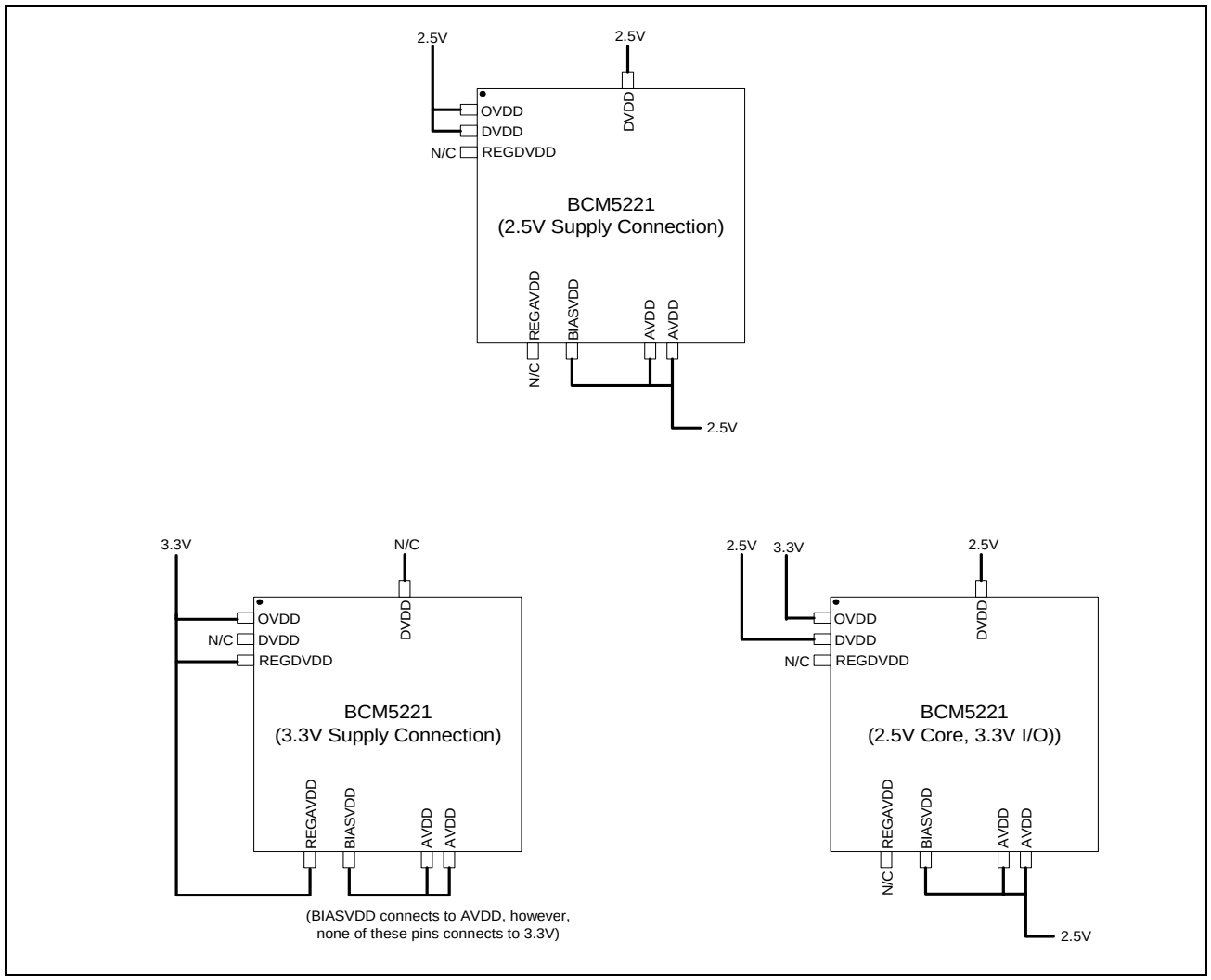

Figure 1: Power Supply Configuration Options

INTERNAL PULL-UPS AND PULL-DOWNS

- This section lists those Inputs, or combination Inputs/Outputs, that include internal resistive pull-ups or pull-downs. The value of each pull-up and pull-down is approximately 50 kΩ (+/-20%).
- REF_CLK > pull-down
- TXD[3:0] > pull-down
- TXEN > pull-down
- TXER > pull-down
- MDC > pull-down
- PHYAD[4:0] > pull-down
- FDX > pull-down
- SD+ > pull-down
- SD- > pull-down

- TESTEN > pull-down
- LOWPWR > pull-down
- MDIO > pull-up
- RESET# > pull-up
- F100 > pull-up
- ANEN > pull-up
- MII_EN > Pull-up
- LNKLED# > pull-up
- SPDLED# > pull-up
- RCVLED# > pull-up

The XMTLED#/INTR#/FDXLED# output is Open Drain

25 MHz Reference Clock

The BCM5221 device accepts a 25 MHz (or 50MHz for RMII applications) reference clock from either a low cost crystal circuit (parallel resonance operating in the fundamental mode) or a single ended clock source such as a 50 ppm self-contained oscillator or buffered system clock. See Figure 2 for clock connection requirements.

For stand-alone crystal applications, Broadcom recommends that the crystal is located as close to the XTALI and XTALO pins of the BCM5221 as possible to minimize stray capacitance due to excessive trace routing that could interfere with crystal start-up as well as clock stability.

Broadcom recommends the use of a crystal rated for a total load capacitance of 18 pF. A calculation for deriving the approximate load capacitance is: $((C_{L1} \times C_{L2})/(C_{L1} + C_{L2})) + C_S$ Where $C_{L1} \times C_{L2}$ are the actual load capacitors connected to either side of the crystal, and C_S is the sum of the stray capacitance and input pin capacitance of the PHY device. Assuming load caps of 20pF each and a total stray + parasitic capacitance of approximately 8pF, the above equation yields a total load capacitance of around 18pF. The load capacitor values may need to be adjusted from the example above to account for variations in parasitic capacitance and/or crystal specification.

For applications using an XTAL based oscillator or buffered system clock, the REF_CLK input should be used. In this instance, the XTALI input should be pulled to ground (4.7K) and the XTALO pin can remain unconnected. The input voltage swing of the reference clock must be no greater than the voltage at the OVDD power pin.

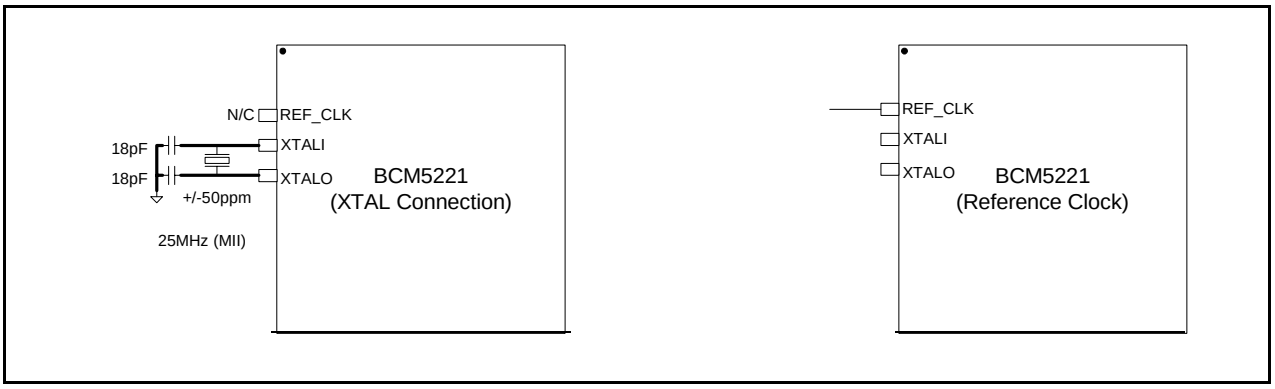

Figure 2: Oscillator Clock Considerations

The electrical specifications recommended for the crystal or oscillator clock source are as follows:

- Frequency tolerance: +/-50 ppm
- 50% Duty Cycle: +/- 10%

- Edge rates: from 1 ns to 4 ns (10% to 90%)
- Voltage swing: limited to OVDD maximum
- Crystal Aging: +/- 5 ppm per year, maximum
- Crystal Frequency Stability (over temperature): +/- 10 ppm

The following clock devices exhibit good performance in a variety of Broadcom's evaluation platforms.

- Oscillator: GED part number LM20001E/DI-25.000M (GED, San Marcos, CA, (760) 591-4170)
- Crystal: Epson part number MA-506-25.000M-C2 (http://www.epson-electronics.de/download/downcrys.htm) Digi-Key part number SE2639CT-ND

RDAC

The 100Base-TX and 10Base-T transmit amplitudes can be directly controlled by adjusting the amount of current allowed to flow from the RDAC pin to GND. It is recommended that in order to verify proper transmit signal amplitude for a given design, an initial value of 1.27K Ω (1%) be used for the external RDAC resistor (See Figure 8 on page 15 and Figure 9 on page 16). It is important to note that the transmit signal amplitude can be affected by magnetics insertion loss as well as stray capacitance in the front-end design. Therefore, it is important to quantify these additional possible sources of attenuation and adjust the value of the RDAC resistor accordingly to compensate.

A 1% change in RDAC current results in a 1% change in transmit amplitude at the TD+/- outputs. Increasing the value of the RDAC resistor results in a proportional decrease in transmit amplitude, and vice - versa.

LOW POWER MODES

The BCM5221 supports two low power modes of operation as discussed in the data sheet: Manual Low Power Mode, and Automatic Power Down Mode.

Manual Low Power mode (LOW_PWR pin = 1) configures the device such that all circuitry, with the exception of the Energy Detect block, is powered down. This mode results in maximum device current consumption of approximately 10mA. This Energy Detect circuit asserts the ENERGY_DET output when receive energy is detected at the RD+/- wire side inputs. Specifically, if energy of at least 300 mV pk-pk differential is present for at least 1.3 ms, the ENERGY_DET pin asserts. REF_CLK must be present for the Energy Detection mode to function properly.

In order to remove the PHY from the Energy Detect Low Power mode, the LOWPWR pin must be set to a logic zero. you do not need to generate a hardware reset. REF_CLK must be active and stable.

Automatic Power Down Mode is enabled by setting bit 5 of the Shadow Register 1Ah. When this mode is enabled, the BCM5221 remains inactive and will not transmit anything onto the wire until it detects energy (at least 300mV differential) at it's RD+/- inputs. Once energy is detected, the BCM5221 will automatically power up operate normally. Note that the use of this feature should be restricted to implementations and environments where the Link partner is a known entity. For example, if both ends of the link happen to be in Automatic Power Down mode, the link will never activate.

It is important to note that in order to successfully enter either of the Low Power modes, REF_CLK must continue for a least two full clock cycles after LOWPWR is switched. This is to ensure that low power mode is properly latched in. REF_CLK can then be deactivated, if needed.

DUAL FUNCTION PINS

The BCM5221 includes several dual purpose pins that combine input and output functions. The input function for these pins is latched into the device at power-on / reset. These pins assume the output function during normal device operation.

PHYAD4/CK25. Physical Address input which, along with the other 4 PHYAD pins, sets a unique address for this device to allow MDIO access. The CK25 output is a buffered version of REF_CLK for general use.

PHYAD3/PAUSE. Physical Address input which, along with the other 4 PHYAD pins, sets a unique address for this device to allow MDIO access. The PAUSE output is an active low indication of the Flow Control capability of the far-end link partner (logic 0 = link partner supports PAUSE, logic 1 = link partner does not support PAUSE). The state of this output is determined by the result of auto-negotiation.

PHYAD2/ACT_LED#. Physical Address input which, along with the other 4 PHYAD pins, sets a unique address for this device to allow MDIO access. The ACT_LED# output is an active low indication of packet activity (transmit and receive) through the BCM5221 (logic 0 = activity, logic 1 = idle). If the use of this LED output is required, Broadcom recommends that PHYAD2 be strapped high since the LED output polarity is active low.

PHYAD1/COL_LED#. Physical Address input that, along with the other 4 PHYAD pins, sets a unique address for this device to allow MDIO access. The COL_LED# output is an active low indication of collision and only meaningful during half duplex operation (logic 0 = collision, logic 1 = no collision). If the use of this LED output is required, Broadcom recommends that PHYAD1 be strapped high because the LED output polarity is active low.

PHYAD0/FDX_LED#. Physical Address input which, along with the other 4 PHYAD pins, sets a unique address for this device to allow MDIO access. The FDX_LED# output is an active low indication of the current duplex state of the BCM5221 (logic 0 = Full Duplex, logic 1 = Half Duplex). If the use of this LED output is required, Broadcom recommends that PHYAD0 be strapped high because the LED output polarity is active low.

SPDLED#/ADV_PAUSE#. Active LED output that indicates the current operating speed of the BCM5221 (logic 0 = 100 MBps, logic 1 = 10 Mbps). The ADV_PAUSE# active low input allows the local MAC to directly indicate to the BCM5221 it's ability to support flow control. A logic 0 will set bit 10 in register 04h. A logic 1 clears bit 10 in register 04h.

100BASE-FX

The BCM5221 supports 100BASE-FX operation via the SD+/-, RD+/-, and TX+/- pins. The connection diagrams in Figure 3 on page 6 illustrate the proper termination and level shifting required to interface the BCM5221 to a 3.3V fiber transceiver.

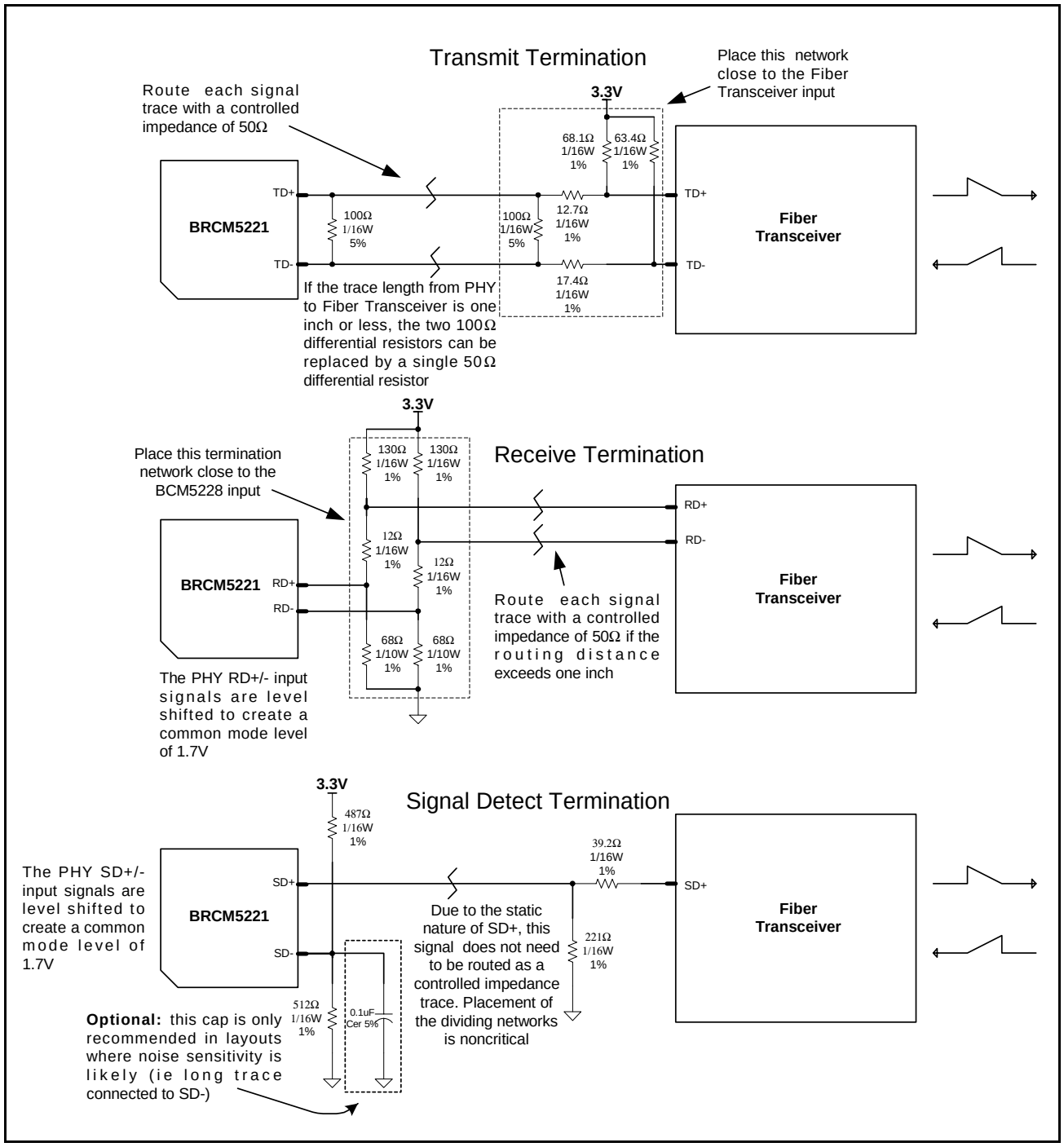

Figure 3: BCM5221 3.3V 100BASE-FX Interface

Figure 3 illustrates only the termination scheme for the 100BASE-FX interface. Refer to the fiber transceiver manufacturer's guidelines for transceiver power supply connection and filtering.

The TD+/- and RD+/- signal traces between PHY and the fiber transceiver should each be routed with a characteristic impedance of 50Ω (100Ω differential) to match the termination network impedance given in Figure 3.

The SD+/- traces do not require special impedance considerations due to the static nature of signal detect. Note that the actual potential of the 3.3V rail connected to the SD- voltage divider should match the 3.3V potential as measured on the fiber transceiver power pins (VDD as measured at the transceiver power pins may be less than nominal if series inductive filtering is used, which may be recommended by the fiber transceiver manufacturer).

Configuring the BCM5221 100Base-FX operation is accomplished simply by connecting the SD+ input to a 100Base-FX compliant transceiver and by setting the potential of the SD- pin as shown in Figure 3. There is no way to configure for 100Base-FX operation via software.

Hewlett Packard (http://www.hp.com/HP-COMP/fiber/sg/) and Siemens (http://w2.siemens.de/semiconductor/products/37/37651.htm) both manufacture high quality 100BASE-FX transceivers.

SD+/-. Assuming the use of a 3.3V fiber transceiver, take care to level shift the SD+ signal from the fiber transceiver to the BCM5221 properly. Because the SD signal from the transceiver is essentially static, there is no need to treat the SD+ trace as a transmission line. A simple level shifter is required and its placement relative to either the BCM5221 or the fiber optic transceiver is non-critical. As with any interface, trace lengths should be kept to a minimum wherever possible. The SD- input of the BCM5221 requires an external bias of 1.7V to ensure that the differential SD+/- input functions properly.

RD+/- . Because the RD+/- inputs of the BCM5221 are internally biased, and because typical 3.3V fiber transceivers normally source PECL with a Vbb (center of the voltage swing) of approximately 2.0V, level shifting is required. Additionally, if the system layout requires that the RD+/- trace lengths are more than approximately one inch, take care to set up the termination to account for transmission line effects as well (as indicated in Figure 3).

TD+/- . The BCM5221 employs current-sink outputs to transmit the 100Base-FX signaling to the fiber transceiver so a special level shifting and impedance matching termination network must be implemented. The slight mismatch in the final voltage divider for the TD+ versus TD- ensures that the TD+/- input of the fiber transceiver will not switch due to noise that might be present when the BCM5221 is quiet.

SERIAL 10M (7-WIRE INTERFACE)

The BCM5221 will interface to most MicroProcessors via serial 10M across the MII (also referred to as 7-Wire interface). This mode can only be enabled via the MDIO interface by writing a 1 to bit 1 of register 1Eh.

Figure 4 on page 8 illustrates the connection between the BCM5221 and a typical µP. Note that this figure represents connection with the more popular Motorola µPs (such as the MPC850, 860, etc).

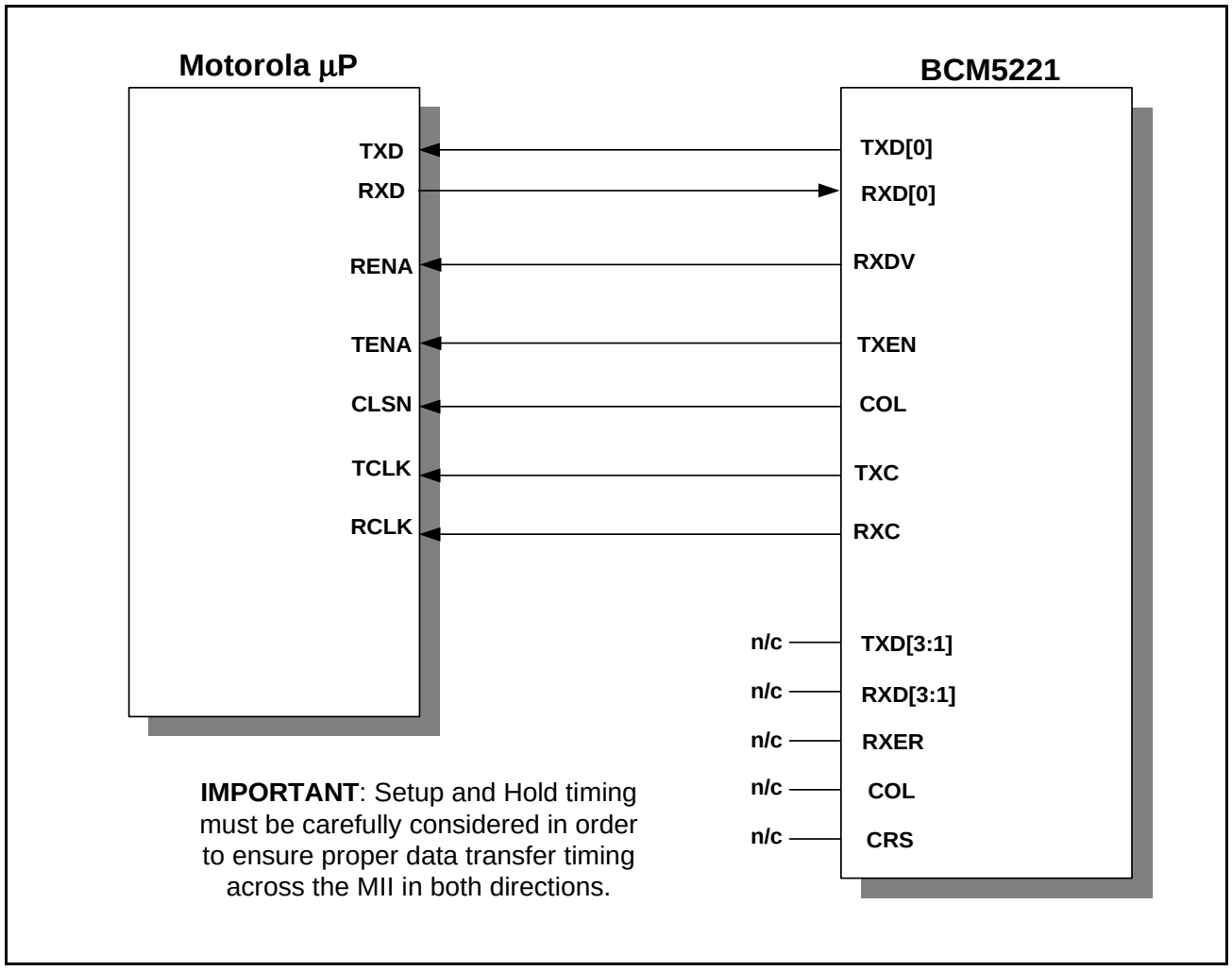

Figure 4: BCM5221 Serial 10 (7-Wire) Interface

AUTO-MDI/MDIX CROSSOVER

In most 10/100Base-TX connections, one end of the link is configured as an MDI (Medium Dependent Interface) crossover so that each transceiver's transmitter is connected to the other's receiver. This allows the end user to install straight-through cables. However, there are many instances where cross-over cables are required and this has caused significant confusion and downtime in the field. The BCM5221 contains the ability to perform Auto-MDI/MDIX crossover on chip, thus eliminating the need for crossover cables or cross-wired (MDIX) ports.

During auto-negotiation and 10/100BASE-TX operation, the BCM5221 normally transmits on TD± and receives on RD±. When connected via a straight-through cable to another device that does not perform the Auto-MDI/MDIX crossover, the BCM5221 automatically switches its transmitter to RD± and its receiver to TD± to communicate with the remote device. If two devices are connected that both have Auto-MDI/MDIX crossover capability, then a random algorithm determines which end performs the crossover function.

The Auto-MDI/MDIX crossover feature is a function of auto-negotiation. If the BCM5221 is configured not to perform Auto-Negotiation, the feature does not work, and a specific cable is required to ensure the Transmitter at one end of the cable is connected with the Receiver at the other end of the cable. This feature is enabled by default, but can be disabled by setting

bit 11 in Register 1Ch to a 1. During operation, the MDI state can be determined by reading bit 13 of Register 1Ch, as indicated in the BCM5221 data sheet. Additionally, a manual MDI swap can be forced by setting or clearing bit 12 of Register 1Ch.

The Auto-MDI/MDIX feature is implemented in the BCM5221 in accordance with the IEEE 802.3ab specification. The Automatic MDI/MDI-X state machine facilitates switching between the receiving pair and the transmitting pair respectively, prior to the auto-negotiation mode of operation so that Fast Link Pulses (FLPs) can be transmitted and received in compliance with Clause 28 of the auto-negotiation specification. The final state of the crossover circuit is determined by an algorithm that controls the switching function between the two pairs (transmit and receive). The algorithm uses an 11-bit Linear Feedback Shift Register (LFSR) to create a pseudo-random sequence with which the BCM5221 determines its initial configuration. In the BCM5221, care is taken to ensure the LFSR is seeded with a unique value during reset. This determines the initial state of MDI or MDIX.

Per the specification, a sample timer is implemented in a manner that allows the BCM5221 to detect either valid Link Pulses or a Valid Link. If after 62+/-2 ms the receiver is unable to detect a valid Link Pulse or a valid Link, the LFSR is advanced, switching the pairs. Additionally, an asynchronous timer is used in the unlikely event where the two PHYs have identical reference clocks and reset circuits. When this timer expires, it resets the state machine to the MDI State and restarts the sample timer. This timer is free running and has no impact on the LFSR.

Auto-MDI/MDIX operates only on the transmit and receive data pairs (swapping them if required). It does not operate on the individual wires within a given pair and therefore cannot correct for possible polarity swap issues. However, the 10BASE-T transceiver within the BCM5221 includes polarity detection and correction to ensure proper functionality should a polarity problem exist in the wiring. Note that 100Base-TX signaling is NOT sensitive to polarity and therefore does not strictly require polarity detection and correction.

Specific magnetics and cable termination issues must be considered when using the BCM5221 in Auto-MDI/MDIX mode. See the following section for further detail.

MAGNETICS

Most applications requires single channel magnetics to support implementations based on one or more BCM5221 devices. In some applications, Quad channel magnetics may be more practical.

In any case, note that one important restriction in pairing magnetics with the BCM5221 relates to the ordering of isolation transformer and common mode choke in the transmit signal path (and receive signal path when Auto-MDI/MDIX is enabled). The transmit output signal from the BCM5221 must be connected to the isolation transformer first, followed by the common mode choke (as depicted in Figure 5). If any common mode choke is placed between the transmit output pins and the isolation transformer, potentially severe signal distortion results while operating in 10Base-T and auto-negotiation modes.

The following list includes recommended Single and Quad channel magnetics components from various vendors for use with the BCM5221 (and BCM5220). The use of these magnetics is recommended regardless of whether Auto-MDI/MDIX is enabled.

Bel. S558-5999-W2 (Single) S558-5999-Q9 (Quad - for use with single height or stacked RJ connectors)

Pulse Engineering. H1102 (single) H1164 (Quad)

Halo. TG110-S050N2 (single)

Figure 5 on page 10 illustrates specific magnetics interconnect and differential cable termination requirements for applications that use Auto-MDI/MDIX.

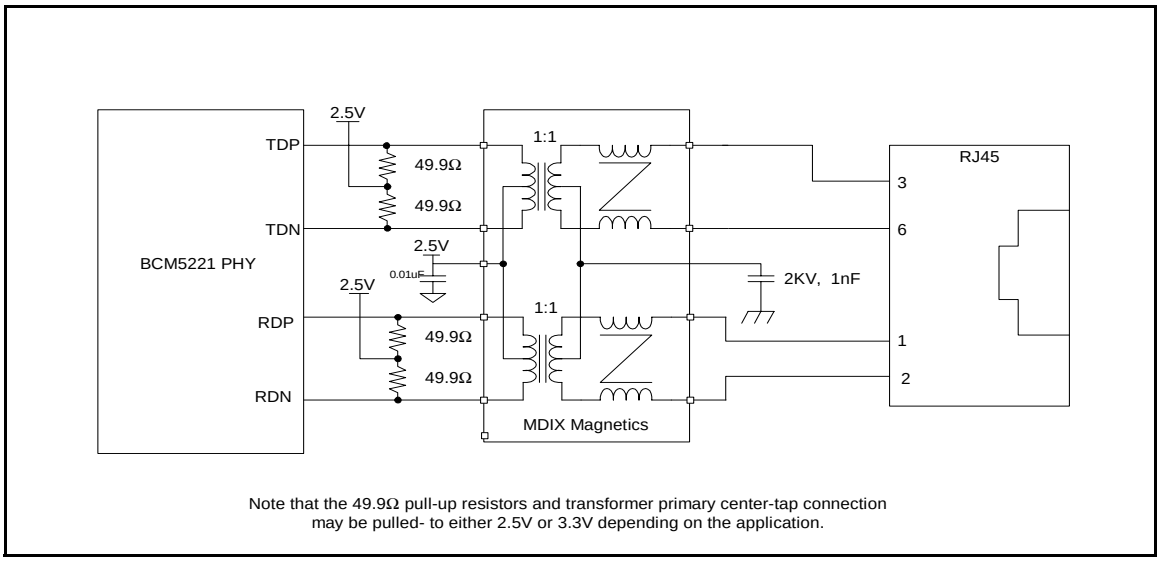

Figure 5: Magnetics Connection and Differential Cable Termination Requirements

MEDIA CONVERSION

This section describes the ability of the BCM5221 to act as a Media Convertor (100Base-TX <> 100Base-FX). The BCM5221 includes internal receive channel FIFOs to allow the data to cross over the clock boundaries without any requirement for external buffering or clock multiplexing.

Figure 6 on page 11 illustrates how to implement glueless media conversion using two BCM5221 devices. Note that Auto-negotiation should be disabled for both of the BCM5221 devices. Additionally, half-duplex operation between the two 5221 devices is not supported. Media Conversion must be implemented in full-duplex. Note that this does not preclude the use of a BCM5221 media converter in a half-duplex system.

The following pin strapping is required for Media Conversion. Pull-up and pull-down values of 4.7 KΩ are recommended.

100BASE-TX PHY:

- LINKLED#/MEDIA_CONV# (pin 35) must be pulled low
- MII_EN (pin 18) must be pulled low
- ANEN (pin 38) must be pulled low
- F100 (pin 37) must be pulled high or left unconnected
- FDX (pin 39) must be pulled high
- SD+ and SD- (pins 21 and 19) must be pulled low or left unconnected

100BASE-FX PHY:

- LINKLED#/MEDIA_CONV# (pin 35) must be pulled low
- MII_EN (pin 18) must be pulled low
- ANEN (pin 38) must be pulled low
- F100 (pin 37) must be pulled high or left unconnected
- FDX (pin 39) must be pulled high
- SD+ and SD- (pins 21 and 19) must be connected as specified in the 100BASE-FX section of this application note.

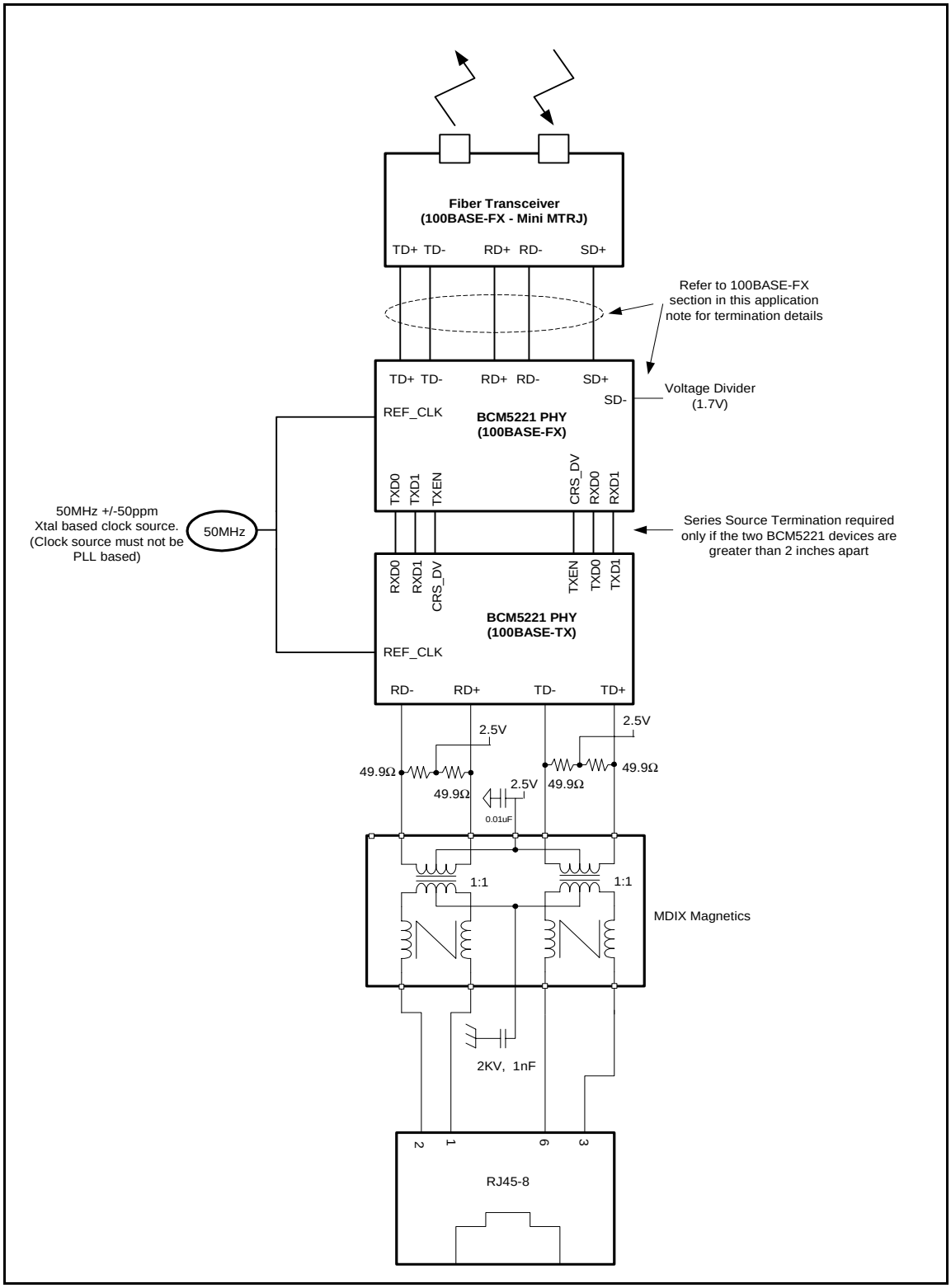

Figure 6: Media Conversion Connection Example

CABLE LENGTH MONITORING CAPABILITY

The DSP nature of the 10/100 receiver within the BCM5221 allows real-time access to equalizer states that provide cable length estimate information.

Specifically, bits [14:12] in Shadow Register 1Bh provide a +/- 10 meter length estimate of the CAT 5 cable connected to the receiver inputs of the 5221 (assuming of course that the far end station is operational). This estimate is accessed by simply reading the aforementioned bits. This provides the user with an easily accessed and powerful diagnostic tool for determining potential problems within the cable plant and/or associated connectors. See Table 1 for decode.

Table 1: Cable Length Estimate

Register 1Bh 14, 13, 12	***Cable Length in Meters***
000	<20
001	20 to <40
010	40 to <60
011	60 to <80
100	80 to <100
010	100 to <120
100	120 to <140
010	>140

JTAG CONSIDERATIONS

The BCM5221 device incorporates JTAG as a shared function with several device input control and output LED functions. This pin sharing should be carefully considered if the use of JTAG is required. This pin sharing approach provides JTAG functionality within the feature-rich BCM5221.

JTAG test mode is only enabled when the active high JTAG_EN input is pulled high. When JTAG_EN is enabled, the following pins become the JTAG test interface for the BCM5221.

Table 2: JTAG Signals

JTAG Signal	***Type***	***BCM5221 KPB***	***BCM5221 KPT***	***Description***
JTAG_EN	I_{PD}	A2	64	JTAG Enable. Active high. When this signal is high, causes the BCM5221 to enter JTAG test mode which enables TRST#, TCK, TMS, TDI and TDO signals. For normal operation leave this pin unconnected.
TRST#	I_{PU}	F7	38	Test Reset. This pin becomes JTAG TRST#. This is an asynchronous active low reset input to JTAG TAP controller. This signal is multiplexed with ANEN signal input.
TCK	I_{PU}	F6	37	JTAG test clock input. This signal is multiplexed with F100 signal.
TMS	I/O_{PU}	G8	36	Test Mode Select input. This signal is multiplexed with SPD_LED# and ADV_PAUSE#.

Table 2: JTAG Signals (Cont.)

JTAG Signal	Type	BCM5221 KPB	BCM5221 KPT	Description
TDI	I/O_{PU}	H8	35	Test Data Input. This signal is multiplexed with LNKLED# and MEDIA_CONV# signals.
TDO	I/O_{PU}	H7	33	Test Data Output. This signal is multiplexed with RCVLED#, ACTLED# and MDIX_DIS signals.
I_{PD} = Input with internal pull-down. I_{PU} = Input with internal pull-up. I/O_{PD} = Input/Output with internal pull-down. I/O_{PU} = Input/Output with internal pull-up.				

JTAG FUNCTIONAL DESCRIPTION

The JTAG_EN signal should be set to a high logic level to enable JTAG function since JTAG signals are multiplexed with other signals during normal operation. Once enabled, TCK, TRST#, TMS, TDI and TDO provide JTAG functionality. Please refer to the following schematics to connect JTAG signals and JTAG compatible devices to JTAG chain.

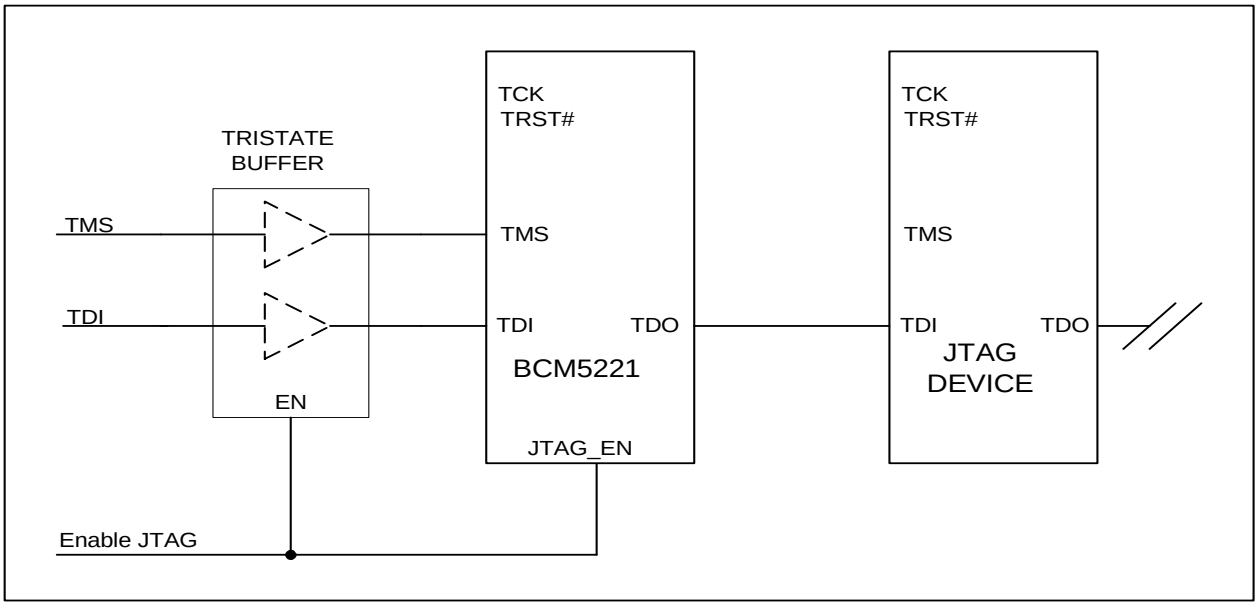

Figure 7: JTAG Chain Schematics

Setting JTAG_EN to a high level causes the BCM5221 to enter JTAG mode. You must connect the JTAG TDI and TMS input signals to the BCM5221 TDI and TMS input signals through tri-state buffers as shown in the above schematics because these inputs are multiplexed with other output signals during normal operation.

ELIMINATING TRI-STATE BUFFER REQUIREMENT

Preferred Method. If the design does not require LNKLED# and SPD_LED# signals, it is possible to connect the JTAG TDI and TMS signals directly to the TDI and TMS pins of the BCM5221. Eliminating the TDI tri-state buffers is accomplished by the following two writes.

1 Enable shadow register by writing a 1to bit 7 of MII register 1Fh.

2 Write a 1 to bit 3 of MII shadow register 1Ah.

After the 1 is written to bit 3 of MII shadow register 1Ah, set the JTAG_EN signal high to enable JTAG operation.

Alternative Method. After a normal reset, the BCM5221 JTAG signal pins for TDI and TMS are used to source LNKLED# and SPDLED# signals. At this point if the JTAG_EN signal is set high without first completing the above two writes, then there is a potential contention between JTAG signals and the BCM5221 signals driving the same pins. However, even if the Preferred Method is not followed, analysis has shown that the inherent current limiting capability of Broadcom LED output buffers is such that there will be no reliability impact as long as the above two writes are executed within 5 seconds of JTAG_EN being set high.

SUPPLY PINS AND POWER PLANES

This section describes the power pins and recommended power plane partitioning for the BCM5221 as well as detailed descriptions of each type of power supply pin.

A solid power supply plane is always recommended for each supply required by the application. If the design calls for both 2.5V and 3.3V supples, then dedicated board layers should be provided for each supply. Fragmenting, segmenting, or otherwise interrupting a power supply plane is not recommended.

The BCM5221 is essentially a 2.5V device with on-chip regulators, making it suitable for 3.3V applications. To clarify the purpose of the power pin types, each type is listed and defined below (See Figure 1 on page 2).

OVDD. This pin supplies power to the digital input and output buffer stages of the BCM5221. By connecting OVDD to a 3.3V power rail, all of the 3.3V tolerant digital inputs accepts either CMOS or TTL input signaling or static levels. If the system design allows for all input signaling to be limited to a maximum swing of 2.5V, the OVDD pin can be connected to the 2.5V rail.

REGAVDD and REGDVDD. These voltage regulator input pins should be connected to the 3.3V system power rail only if the device is to be powered from a single 3.3V supply (See Figure 1). These pins should be left unconnected in applications where the BCM5221 is powered by 2.5V.

DVDD. In 3.3V applications, these pins serve as connection points for the internal digital core circuitry to allow for external supply filtering. In 2.5V applications, these pins must be connected to an external 2.5V supply to supply power to the core.

AVDD. In 3.3V applications, these pins serve as connection points for the internal analog circuitry to allow for external supply filtering. In 2.5V applications, these pins must be connected to an external 2.5V supply to power the analog circuits.

BIASVDD. This pin, which supplies power to internal bias circuitry, should always be connected to the AVDD pins.

MULTI-PORT DESIGNS

For applications requiring two or three ports (such as uplinks or router designs), multiple BCM5221 PHYs can be implemented.

For BCM5221 multi-port applications, Broadcom recommends that VDD and GND are implemented via uninterrupted power and ground planes for the entire system with the exception of chassis ground.

See Figure 8 on page 15 for a simplified illustration of a BCM5221 multi-port power plane layout recommendation.

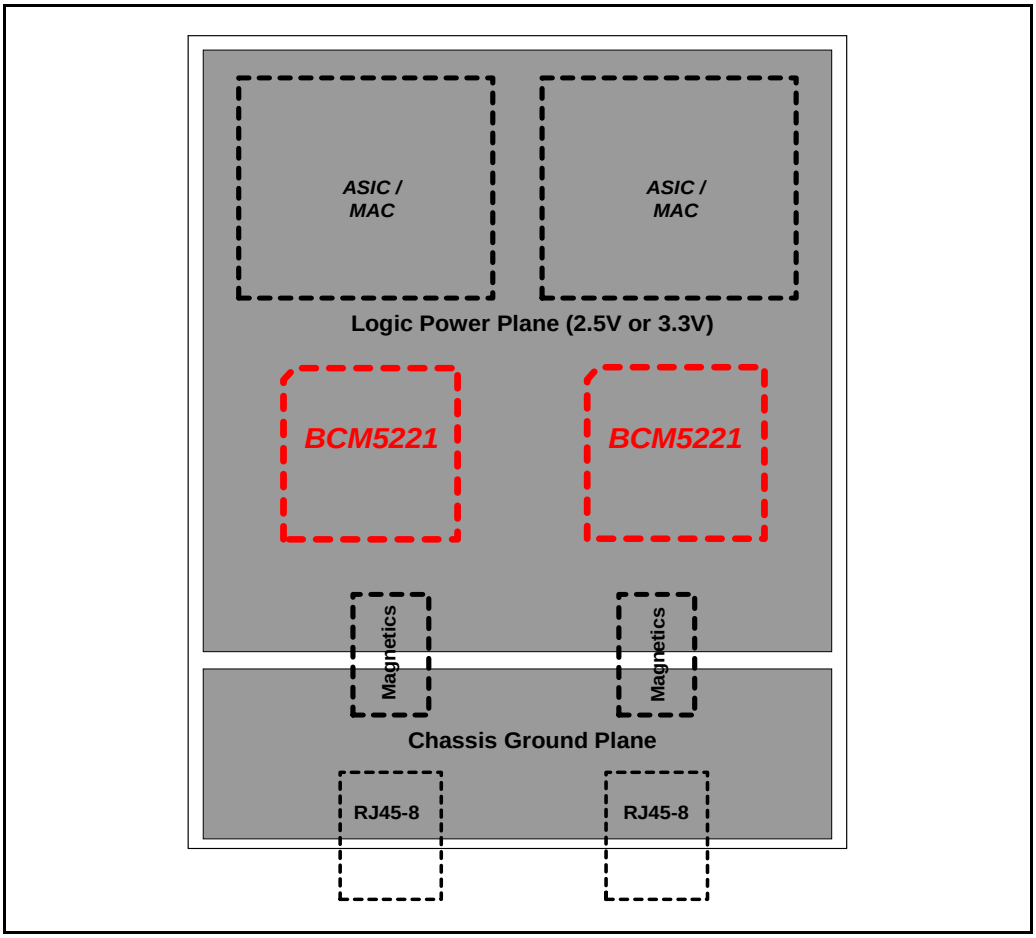

Figure 8: Multiport Power Plane Example

10/100 TWISTED PAIR MII TO MDI

Figure 9 on page 16 represents a typical 10/100 twisted pair DTE implementations, MII to MDI inclusive, for the BCM5221. This example assumes the use of 2.5V VDD for the system, with the digital interface running at 3.3V.

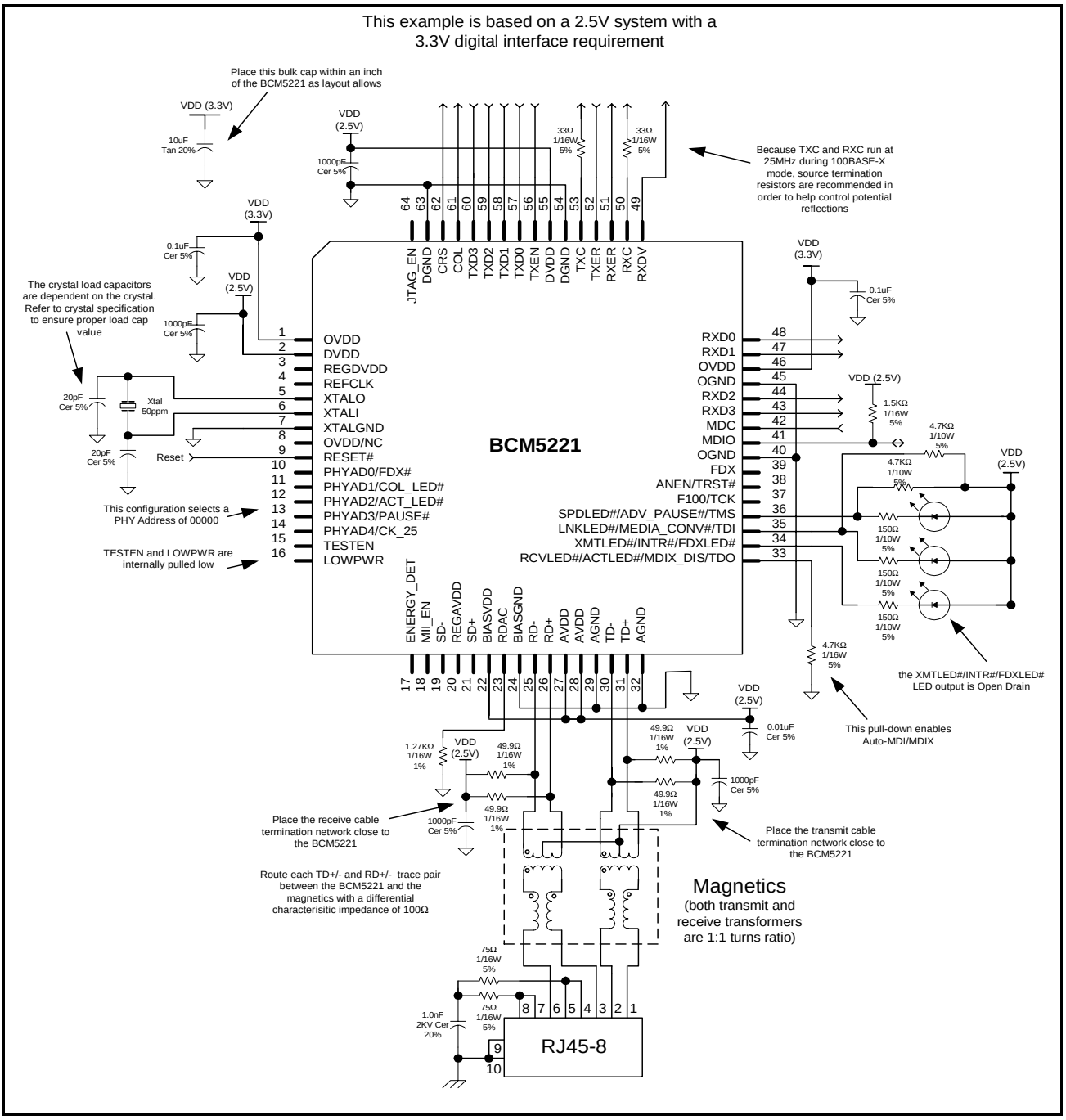

Figure 9: BCM5221 Typical Twisted pair Connection (MII to MDI)

GENERAL LAYOUT NOTES

When determining component placement and routing for a BCM5221 based design, the following recommendations help optimize system design and performance.

Analog Related Passive Component Placement. Relative component placement across the analog side of the BCM5221 (pins 17 through 32) is critical and should be addressed with the following priorities in mind:

- Power supply filter components should be placed first and located closest to the PHY (highest priority).
- Transmit termination resistors should be placed as close as possible to the TD+/- pins of the PHY.
- Receive termination network should be placed as close as possible to the RD+/- pins of the PHY.

TD+/- Trace Routing. When routing the TD+/- signal traces from the PHY to the 1:1 transformer, the traces should be routed adjacent to a ground plane for controlled characteristic impedance. Broadcom recommends that the TD+ and TD- signal traces be routed with matched length (as short as possible), and with a characteristic differential impedance of 100Ω.

100Base-TX and 10Base-T Signaling. The BCM5221 incorporates a unique transmit drive architecture that sinks current instead of sourcing current. In 100Base-TX mode, 40 mA is always pulled down through the transmit transformer's primary winding (via the center tap connection to VDD) and is steered in one direction of the other, depending on the state of the transmit DAC. This generates a true differential 2V nominal pk-pk voltage swing that is centered around the VDD center tap potential of the transmit transformer.

When configured for 10BASE-T operation, the transmit DAC operates in class AB mode. This implementation conserves device power by reducing the total transmit current required to generate the IEEE compliant Manchester encoded signaling. In order to ensure that the transmit signal retains optimal integrity, it is recommended that the controlled impedance transmit path from the PHY to the magnetics be kept as short and direct as possible with minimum vias, and with properly placed termination.

RD+/- Trace Routing. The RD+ and RD- traces, which connect the receive transformer to the PHY, should be routed with a differential characteristic impedance of 100Ω and should be routed adjacent to a ground plane. Again, matched trace length is important.

Reference Clock. If the design requires a low cost crystal, minimize trace length from the crystal to the XTALI and XTALO pins of the BCM5221. This will help minimize stray capacitance and noise pick-up that might otherwise affect the reference clock integrity. In a worst case scenario, too much parasitic capacitance and/or inductance in the crystal traces could cause the crystal to suffer from start-up problems and/or instability.

When using a single-ended reference clock, it is usually best to series terminate at the clock source to ensure optimal signal integrity at the input to the BCM5221.

Magnetics to RJ45-8. Broadcom recommends that properly grounded (usually to the chassis ground) shielded RJ45-8 media connectors are used to control EMI emissions.

When routing the transmit and receive pairs between magnetics and the RJ45-8, it is recommended that an inner layer or layers be used. The outer layers (top and bottom) can then be dedicated to chassis ground in the area between the magnetics and the RJ45-8. This will help isolate the sensitive analog signals from external noise sources, as well as help reduce EMI emissions. See Figure 9 on page 16.

Chassis Ground. When planning the placement of chassis ground in the layout, it is always beneficial to consider placing at least two component pads (1206 size) across the void between chassis ground and system ground (see Figure 9 on page 16). These component pads may be stuffed with a variety of components to reduce EMI emissions. Installing OΩ resistors, high R value resistors, capacitors, or leaving these pads unpopulated are options to be considered. These options can provide substantial flexibility when attempting to control EMI emissions.

Board Layer Allocation. Figure 10 on page 19 illustrates one option for board layer allocation. The figure gives an example based on a single VDD and single Ground plane. Of course some applications will require a second VDD plane in order to accommodate a second power rail.

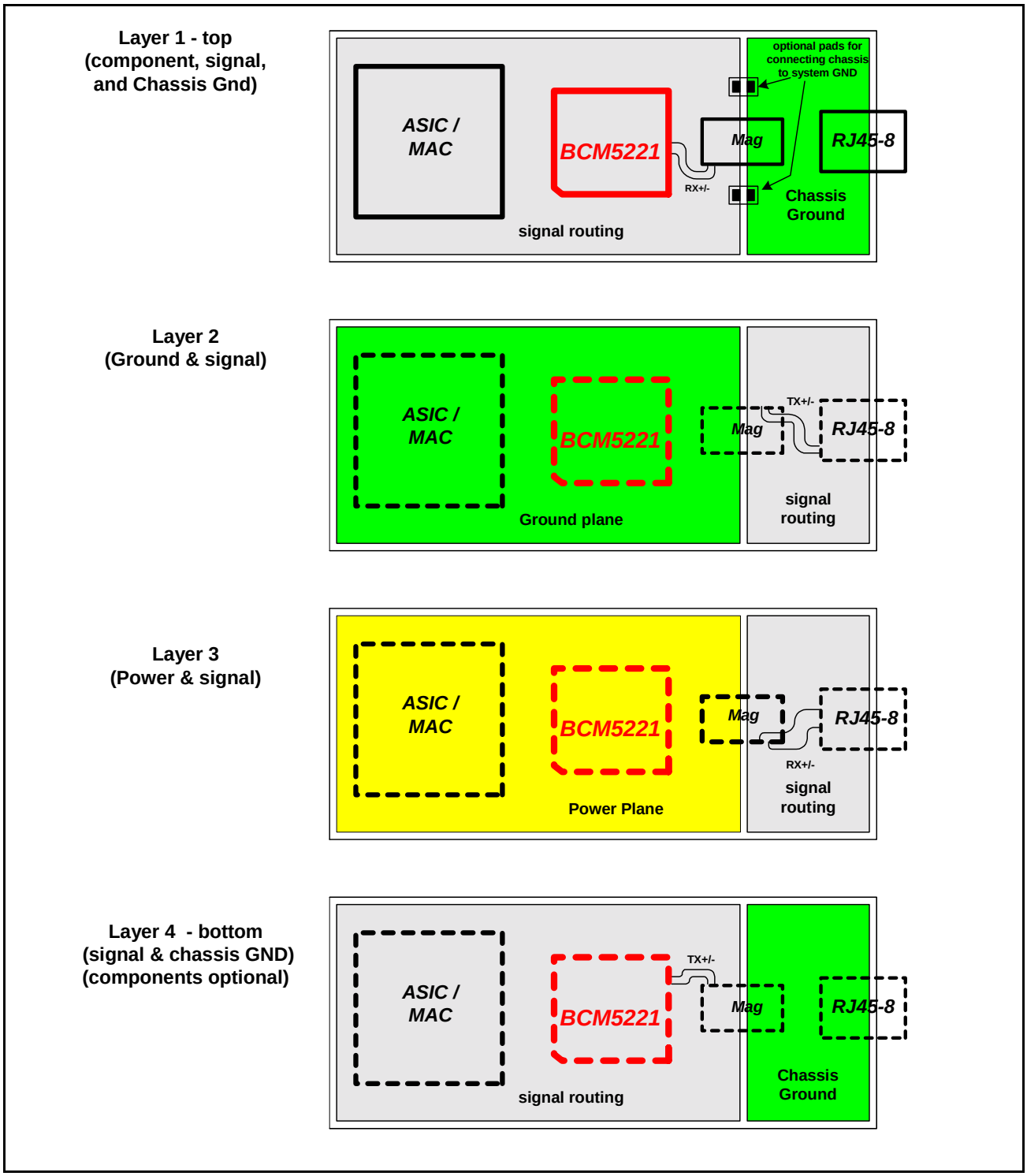

Figure 10: Typical Layer Allocation (BCM5221)

Power Supply Filter Component Placement. Power supply filter component placement is illustrated in Figure 10 and Figure 11. Use these general placement guidelines to ensure optimal performance.

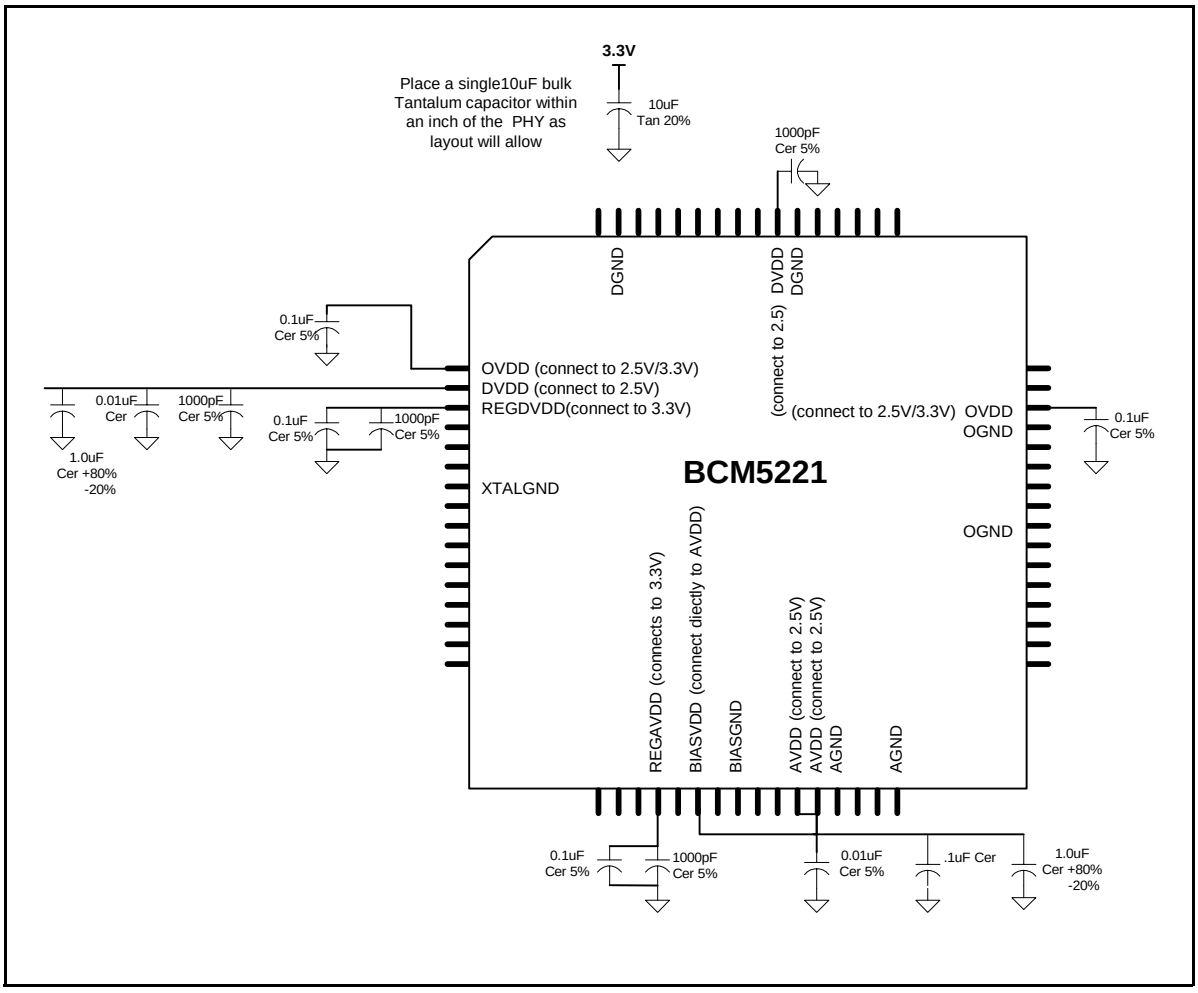

Figure 11: BCM5221 Relative Placement of Filter Components

General Layout Recommendations. The following general layout recommendations help ensure a robust overall system design:

- Keep all trace lengths to a minimum, especially for the more sensitive signal traces between the PHY and RJ45-8.
- Each signal trace routed between the PHY and the RJ45-8 should be controlled impedance of 50Ω (100Ω differential).
- Refrain from routing traces with right-angle corners. Always chamfer trace corners as gradually as possible.
- Route differential pairs such that the + and - signals are matched in length.
- Route all MII signal traces with a target characteristic impedance of 68Ω.
- Always attempt to route noisy digital traces away from sensitive power supply pins and associated filtering such as AVDD.
- If any two traces must cross each other, even though it would have to be on separate layers, always cross them at 90 degrees to minimize potential crosstalk.
- Always place power supply filter components as close as possible to the recommended pins (see Figure 8 on page 15) in order to maximize the filtering effects. If a filter component cannot be directly connected to a given power pin with a very short and fat etch, do not connect it via copper trace. Instead make the connection directly to the associated planes with vias.
- Refrain from routing any signals (analog or digital) over non-contiguous power or ground planes as this causes interrup-

tions in the controlled impedance and results in reflections and a possible increase in EMI emissions.

- Leave the outer edges of the pcb (approximately 200 mils) voided on all layers to minimize fringe effects that could otherwise contribute to EMI emissions.
- Other than the chassis ground area, keep the system ground plane as a single uninterrupted plane of maximum area to create a low impedance path for all return currents. This will also help control EMI emissions.
- Connect all power and ground pins directly to their respective planes via large and/or multiple vias. Avoid routing traces for power and ground pin connections.

THERMAL INFORMATION

This section includes basic thermal information pertaining to the BCM522KPB and BCM5221KPT package types. Table 3 and Table 4 provide a comparison of Theta-J_A versus Airflow.

Table 3: BCM5221KPB Theta-J_A vs. Airflow

64 FPBGA Package	*AIR FLOW (feet per minute)*					
	0	*100*	*200*	*400*	*500*	*600*
Theta-J_A (C/W)	35.15	25.57	22.99	20.88	20.35	20.3
Power Dissipation (W)	TBD	TBD	TBD	TBD	TBD	TBD

Theta-J_C for this package is given as 21.23 C/W. Additionally, the BCM5221KPB is designed for and rated for a maximum Junction Temperature of 125C.

Table 4: BCM5221KPT Theta-J_A vs. Airflow

64 PQFP Package	*AIR FLOW (feet per minute)*					
	0	*100*	*200*	*400*	*500*	*600*
Theta-J_A (C/W)	TBD	TBD	TBD	TBD	TBD	TBD
Power Dissipation (W)	TBD	TBD	TBD	TBD	TBD	TBD

Theta-J_C for this package is given as TBD. Additionally, the BCM5221KPT is designed for and rated for a maximum Junction Temperature of 125C.

BCM5221 vs. BCM5220

The BCM5220 differs from the BCM5221 as follows:

- The BCM5220 does not support Auto-MDI/MDIX
- The BCM5220 does not support Cable quality Monitoring
- The BCM5220 does not provide JTAG support

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