BCM5214

10/100BASE-TX Quad-Φ™ Transceiver

GENERAL DESCRIPTION

The BCM5214 is a 0.35 micron CMOS die shrink of the BCM5208 Quad transceiver packaged in a 128-pin MQFP package. The BCM5214 is a single-chip Quad 10/100BASE-TX transceiver targeted at Fast Ethernet switches. The device contains four full-duplex 10BASE-T/100BASE-TX Fast Ethernet transceivers, each of which performs all of the physical layer interface functions for 10BASE-T Ethernet on CAT 3, 4 or 5 unshielded twisted pair (UTP) cable and 100BASE-TX Fast Ethernet on CAT 5 UTP cable.

The BCM5214 is a highly integrated solution combining digital adaptive equalizers, ADCs, phase locked loops, line drivers, encoders, decoders and all the required support circuitry into a single monolithic CMOS chip. It complies fully with the IEEE 802.3 specification, including the Auto-Negotiation subsections.

The BCM5214 supports the low pin count, industry standard, Reduced Media Independent Interface (RMII). The BCM5214 also supports a much lower pin count Serial Media Independent Interface (SMII).

The effective use of digital technology in the BCM5214 design results in robust performance over a broad range of operating scenarios. Problems inherent to mixed-signal implementations, such as analog offset and on-chip noise, are eliminated by employing field proven digital adaptive equalization and digital clock recovery techniques.

FEATURES

- 10BASE-T/100BASE-TX IEEE 802.3 Compliant
- Single-Chip Quad Physical Interface — MAC to Magnetics
- Reduced Media Independent Interface (RMII)
- Serial Media Independent Interface (SMII)
- Fully Integrated Digital Adaptive Equalizers
- 125-MHz Clock Generator and Timing Recovery
- On-Chip Multimode Transmit Waveshaping
- Edge-Rate Control to Eliminate External Filters
- Integrated Baseline Wander Correction
- Full-Duplex Support
- IEEE 802.3-Compliant Auto-Negotiation
- Shared MII Management Interface up to 12.5 Mbps
- Multiple Programmable Serial or Parallel LED Modes
- Interrupt Output Capability
- Loopback Mode for Diagnostics
- IEEE 1149.1 (JTAG) and NAND-Chain ICT support
- Low-Power Single-Supply 3.3 Volt CMOS Technology
- 128-Pin MQFP

APPLICATIONS

- Fast Ethernet Switches
- Multi-Port Adapter Cards

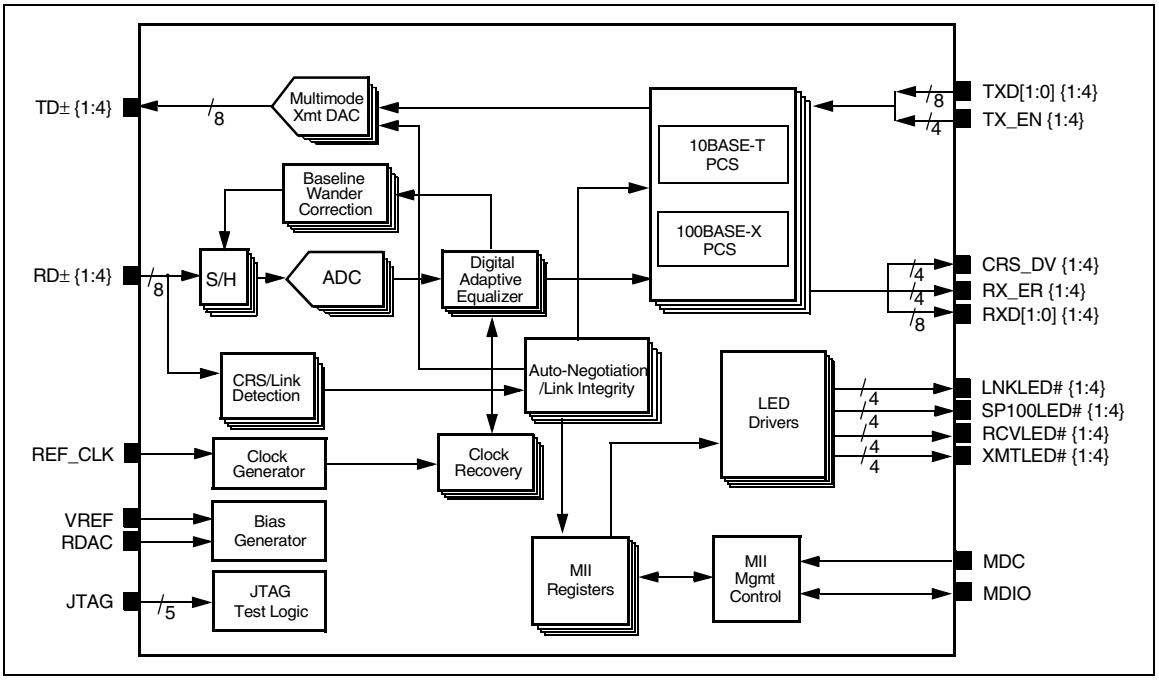


Figure 1: Functional Block Diagram

16215 Alton Parkway • P.O. Box 57013 • Irvine, California 92619-7013 • Phone: 949-450-8700 • Fax: 949-450-8710

Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, California 92619-7013

REVISION HISTORY

REVISION #	*DATE*	*CHANGE DESCRIPTION*
0.1	9/10/99	Initial Release
0.2	9/20/99	Corrected “variable” error.
DS03-405	3/9/00	Cover Page: Removed bullet “Compatible with 3.3V...” from Features list Table 5 on page 8: Under LED heading, changed Pin 80 and 66 from ‘O’ to ‘I/O_{pu}’ Table 5 on page 8: In Receive Activity LED description, removed the word ‘mode’. Table 5 on page 8: Removed pins 1, 17, 22, and 39 from ‘AVDD’ and added them to new row ‘NC’ Figure 2 on page 13: In Pin Diagram, changed pin 1-AVDD to NC, pin 5 AGND to AVDD, pin 17-AVDD to NC, pin 22-AVDD to NC and pin 38-AVDD to NC. Pin 67, INTR{3} changed to {4} and FDXLED{3} changed to {4}. Table 32 on page 40: Added row, to read “CRS_DV Delay....” Table 33 on page 41: Removed row SRX Hold. Changed SRX Setup to read SRX Delay. Figure 7 on page 42: Removed SRX_SETUP reference and changed SRX_HOLD to read SRX_DELAY Added Figure 9 on page 44 and Table 38 on page 43: LED Timing (Serial Mode). Added Figure 10 on page 44 and Table 39 on page 44: LED Timing (Low Cost Serial Mode). Table 41 on page 47: Changed IVDD to read OVDD. Table 42 on page 47: Removed IVDD row. Page 38-46: Added several timing specification values.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Section 1: Functional Description

OVERVIEW

The BCM5214 is a single-chip device containing four independent Fast Ethernet transceivers. Each performs all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full- or half-duplex Ethernet on CAT 3, 4 or 5 cable.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, Auto-Negotiation and RMII and SMII management functions. The BCM5214 can be connected to a MAC through the RMII on one side and connects directly to the network media on the other side through isolation transformers. The BCM5214 is compliant with the IEEE 802.3 standard.

ENCODER / DECODER

In 100BASE-TX and 100BASE-FX modes, the BCM5214 transmits and receives a continuous data stream on twisted pair. When the RMII transmit enable is asserted, data from the transmit data pins is encoded into 5-bit code-groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1 on page 3. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following baseline wander correction, adaptive equalization, and clock recovery, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into five-bit code groups.

The five-bit code groups are decoded into four-bit data nibbles, as shown in Table 1. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the RMII or SMII interface. When an invalid code group is detected in the data stream, the BCM5214 asserts the RMII RX_ER signal or RX_ER bit in SMII mode. The chip also asserts RX_ER for several other error conditions that improperly terminate the data stream. While RX_ER is asserted, the receive data pins are driven with a four-bit code indicating the type of error detected.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the Link Fail state where only idle codes are transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the Link Pass state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD+/- pins for the presence of valid link pulses.

CARRIER SENSE

In RMII mode, the carrier sense and receive data valid signals are multiplexed on the same pin. The carrier sense is asserted asynchronously on the CRS_DV pin as soon as valid activity is detected in the receive data stream. Loss of carrier results in the deassertion of CRS_DV synchronous to the cycle of REF_CLK that presents the first di-bit of a nibble onto RXD. IF the PHY has additional bits to present on RXD following the initial deassertion of CRS_DV, then the PHY asserts CRS_DV on cycles of REF_CLK that present the second di-bit of each nibble and deassert CRS_DV on cycles of REF_CLK that present the first di-bit of each nibble. If carrier sense is asserted and a valid SSD is not detected immediately, then RX_ER is asserted. A value of 2h (2 hex) is driven on the receive data pins to indicate false carrier sense.

In SMII mode, CRS is synchronous with REF_CLK. See Table 2 on page 5 for other bit definitions.

AUTO-NEGOTIATION

The BCM5214 can negotiate its mode of operation over the twisted pair link using the Auto-Negotiation mechanism defined in the IEEE 802.3 specification. Auto-Negotiation can be enabled or disabled by hardware or software control. When the Auto-Negotiation function is enabled, the BCM5214 automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5214 can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full and/or half-duplex. Each transceiver negotiates independently with its link partner, and chooses the highest level of operation available for its own link.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes inter-symbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5214 achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization and decision feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 140 meters on CAT 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5214 achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self - adapting to any quality of cable or cable length. Due to transmit pre-equalization in 10BASE-T mode, the adaptive equalizer is bypassed in this mode of operation.

ADC

Each receive channel has its own 125-MHz, analog-to-digital converter (ADC). The ADC samples the incoming data on the receive channel and produces an output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low-offset, high-power supply noise rejection, fast settling time, and low bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clocks are locked to the 50-MHz clock input while the receive clocks are locked to the incoming data streams. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating modes. The input data streams are sampled by the recovered clock from each port and fed synchronously to the respective digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5214 automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error. The baseline wander correction circuit is not required, and is therefore bypassed, in 10BASE-T operating mode.

Table 1: 4B5B Encoding

NAME	4B CODE	5B CODE	MEANING
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000*	11111	Idle
J	0101*	11000	Start-of-Stream Delimiter, Part 1
K	0101*	10001	Start-of-Stream Delimiter, Part 2
T	0000*	01101	End-of-Stream Delimiter, Part 1
R	0000*	00111	End-of-Stream Delimiter, Part 2
H	1000	00100	Transmit Error (used to force signalling errors)
V	0111	00000	Invalid Code
V	0111	00001	Invalid Code
V	0111	00010	Invalid Code
V	0111	00011	Invalid Code
V	0111	00101	Invalid Code
V	0111	00110	Invalid Code
V	0111	01000	Invalid Code
V	0111	01100	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code

Notes:
** Treated as invalid code (mapped to 0111) when received in data field.*

MULTIMODE TRANSMIT DAC

The multimode transmit digital to analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode, and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components, thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC utilizes a current drive output that is well balanced and produces very low noise transmit signals.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted pair cable. The data is scrambled by *exclusive ORing* the NRZ signal with the output of an 11-bit-wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by *exclusive ORing* it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver does not attempt to decode the data stream unless the descrambler is locked. When locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724µs, it becomes unlocked, and the receive decoder will be disabled. If the receiver is put into Token Ring mode (see bit 10, reg. 1Bh), the descrambler monitors the receiver for 5792 µs before unlocking. The descrambler is always forced into the unlocked state when a link failure condition is detected. Stream cipher scrambling/descrambling is not used in 10BASE-T mode.

RMII INTERFACE

The interface in the BCM5214 is based on the low pin count (Reduced) Media Independent Interface (RMII) developed by the RMII Consortium. A copy of the specification can be found on the Consortium web site at: http://www.rmii-consort.com.

The purpose of this interface is to provide a low-cost alternative to the IEEE 802.3u[2] MII interface. It is capable of supporting 10 and 100 Mbit data rates with a single clock, using independent two-bit-wide transmit and receive paths.

A single synchronous reference clock of 50 MHz is used as a timing reference for all transmitters and receivers. By doubling the clock frequency relative to the MII, four pins are saved in the data path, which uses two lines into each transmitter and two lines out of each receiver relative to four lines in each direction in the MII interface. Because Start of Packet and End of Packet timing information is preserved across the interface, the MAC is able to derive the COL signal from the receive and transmit data delimiters, saving another pin.

Transmit and receive clocks are eliminated as well. All data transfers are synchronous with REF_CLK. This poses less of a challenge for the transmitter than it does for the receiver, which is required to buffer output data in a FIFO until an edge of the REF_CLK is suitably aligned. The received data bits and the RX_DV signal are passed through the FIFO; the CRS_DV bit is not. It is asserted for the time the wire is receiving a frame. If the remote transmitter is idle and no data need be passed from the receiver, status information can be made available by setting Bit 1 of Register 10h. Out-of-Band Signaling will consist of two di-bit pairs immediately following the last di-bit pair of a received packet. The two di-bit pairs consist of (Full-duplex, Link Speed — msb, lsb) and (RX_ER, FIFO Error — msb,lsb).

SMII INTERFACE

The Serial MII Interface is an alternative to the RMII interface. The objective is to reduce the number of pins required to interconnect the MAC and the PHY. This is accomplished by clocking data and control signals in and out of each PHY on a pair of pins at a rate of 125 MHz. The SMII mode is selected by pulling the SMII_EN pin high.

Data and control signals passing from the MAC to the PHY use the serial transmit (STX) line; data and control signals passing from the PHY to the MAC use the serial receive (SRX) line. All bit transfers are synchronous with clock (SCLK) at 125 MHz; frame sync is provided by a fourth line (SYNC), asserted at the beginning of each frame, which occurs every ten cycles of SCLK. Each PHY is provided with an STX and an SRX pair. Pins TXD[0]{x} and RXD[0]{x}, where *x* is the port number of the specific PHY, are used to perform the STX and SRX functions on the BCM5214.

This chip has a single SCLK and SYNC input, which is common to all PHYs. Pins REF_CLK and SSYNC are used for these functions on the BCM5214.

Receive data and control information are passed from the PHY to the MAC in ten-bit frames. In 100 Mbps mode, each frame represents a new byte of data. In 10 Mbit mode, each byte of data is repeated ten times; the MAC can sample any one of every ten frames. Because the timing of data coming from a remote transmitter is not synchronized with the local SCLK or SYNC lines and may contain errors in frequency, a FIFO capable of storing 28 bits is provided in each receive path. The received data bits and the RX_DV signal are passed through the FIFO; the CRS bit is not. It is asserted for the time the wire is receiving a frame. If the remote transmitter is idle and no data needs to be passed from the receiver, status information becomes available.

Transmit data and control information are passed from the MAC to the PHY in ten-bit frames, as in the receive path. In 100 Mbit mode, each frame represents a new byte of data. In 10 Mbit mode, each byte of data is repeated ten times; the PHY can transmit any one of every ten frames.

Table 2: SMII SRX Line Description

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
x	0	RX_ER from previous frame	Speed 0 = 10MBit 1 = 100MBit	Duplex 0 = Half 1 = Full	Link 0 = Down 1 = Up	Jabber 0 = OK 1 = Error	Upper Nibble 0 = Invalid 1 = Valid	False Carrier Detected	1
x	1	One Data Byte							

CRS refers to Carrier Sense, and RX_DV refers to Receive Data Valid. When RX_DV is 1, RXD7-0 convey packet data; when RX_DV is 0, RXD7-0 convey RX_ER and PHY status.

Table 3: SMII STX Line Description

TX_ER	TX_EN	TXD7-0
x	0	x
x	1	One Data Byte

TX_ER refers to Transmit Error, and TX_EN refers to Transmit Enable. TXD7– 0 convey packet data.

INTERRUPT MODE

The BCM5214 can be programmed to provide an interrupt from each of the four transceivers. The interrupt feature is disabled by default. Do the following to enable interrupt capability:

1 SER_LED_EN#, pin 66 should be high during reset or clear serial LED mode by clearing MII Register 1Bh, bit 4 in port 2, to a 0 (default).

2 Disable FDXLED function by clearing MII Register 1Ah, bit 15 to a 0.

3 Enable interrupt function by setting MII Register 1Ah, bit 14 to a 1.

The FDXLED# pins will then become INTR# pins.

The status of each interrupt source is also reflected in Register 1Ah, bits 1, 2 and 3. The sources of interrupt are changes in link, speed or full-duplex status. If any type of interrupt occurs, the Interrupt Status bit, Register 1Ah, bit 0, is set.

In addition, each transceiver has its own register controlling the interrupt function. If the interrupt enable bit is set to 0, no status bits are set and no interrupts are generated. If the interrupt enable bit is set to 1, the following conditions apply:

- If mask status bits are to 0 and the interrupt mask is set to 1, status bits will be set but no interrupts generated.
- If mask status bits are set to 0 and the interrupt mask is set to 0, status bits and interrupts will be available.
- If mask status bits are set to 1 and the interrupt mask is set to 0, no status bits and no interrupts will be available.

Changes from active to inactive or vice versa will cause an interrupt. Setting Register 1Ah, bit 8 high will mask all interrupts, regardless of the settings of the individual mask bits.

LEDS

The BCM5214 supports two types of serial LED modes: Serial LED mode and Low Cost Serial LED mode.

SERIAL LED MODE

The BCM5208R is configured for serial LED operation when the SERIAL_LED_EN# pin is sampled at hard reset or when the serial led enable of slice 2 (of 4) is enabled by setting MII register 1Bh, bit 4. Connect the pin to ground, through a 4.7 KΩ resistor to select the mode. In this mode, the BCM5208R sources a serial data stream, the associated clock, and a framing signal, as follows:

- **Serial Data Stream**, SER_SDO# — An active low bit stream comprised of contiguous 24 bit frames.
- **Serial Data Clock**, SER_SCLK — SER_SDO# is clocked out on the falling edge of SER_SCLK, which runs at about 1 MHz.
- **Framing Pulse**, SFRAME — Logic high pulse occurring once every 24 SER_SDO# bit times. SFRAME goes high coincident with bit zero of port 1.

The BCM5208R incorporates three options for providing LED and Interrupt information from the Serial LED bit stream. When Serial LED Mode is enabled (SERIAL_LED_EN# pin tied low), and no further action is taken, the default Normal mode is selected. You can set Bits 14 and 15 in register 1Ah to select the other modes as defined in Table 4 below.

Note

When the Serial LED mode is enabled by software (Reg. 1Bh, bit 4 of slice 2), all other parallel LEDs are inactive (off). When Serial LED mode is enabled by hardware (SERIAL_LED_EN# pin), all other parallel LEDs are active. To enable or disable parallel LEDs while in Serial LED mode, set or reset Reg. 1Bh, bit 4 of slice 3.

Table 4: Serial LED Mode Bit Framing

OPTION	REG 1Ah	Serial Bit 5	Serial Bit 4	Serial Bit 3	Serial Bit 2	Serial Bit 1	Serial Bit 0
Normal	Bit14 = 0 Bit15 = 0	FDX	COL	Speed100	Link	Transmit	Receive
Interrupt	Bit14 = 1 Bit15 = 0	FDX	Global Interrupt	Speed100	Link	Slice Interrupt	Activity
Full-Duplex	Bit14 = 0 Bit15 = 1	FDX	COL	Speed100	Link	FDX	Activity

A Global Interrupt indicates an interrupt from any of the six PHY slices as if they were ORed together. A Slice Interrupt is provided on a per-PHY basis. See the register bit descriptions for register 1Ah for more information about interrupt handling.

Low Cost Serial LED Mode

The BCM5214 also supports a low cost serial LED mode. This serial mode can be enabled only by hardware. The low cost serial LED mode is enabled when LNKLED#{3}, pin 80 (LC_SER_LED_EN#) is held low during power-on reset. When enabled, RCVLED#{1}, pin 99, sources the serial clock (LC_SER_SCLK) and RCVLED#{3}, pin 82, sources the active low serial data (LC_SER_SDO#}.

The LEDs are shifted out on the LC_SER_SDO# in the following order: ActivityLED{1}, ActivityLED{2}, ActivityLED{3}, ActivityLED{4}, LinkLED{1}, LinkLED{2}, LinkLED{3}, LinkLED{4}, FullduplexLED{1}, FullduplexLED{2}, FullduplexLED{3}, FullduplexLED{4}, SpeedLED{1}, SpeedLED{2}, SpeedLED{3}, and SpeedLED{4}.

LED Test

The BCM5208R incorporates several register control bits that you can use to force all external LEDs on, to test the LEDs themselves. To have software control the LEDs, the BCM5208R ANEN input pin must be high (or left floating). The following register writes the result in the forced assertion of all LED outputs independent of valid link. These apply to both serial and parallel LED modes:

- Write 403Ch to Register 18h (this forces LNKLED# on).
- Write 00AAh to Register 1Bh (this forces both ACTLED# and FDXLED# on).
- Write 2000h to Register 00h (this forces SPDLED# on while disabling Auto-Negotiation).

Section 2: Hardware Signal Definition Table

Table 5: Pin Definitions

PIN #	PIN LABEL	TYPE	DESCRIPTION
MEDIA CONNECTIONS			
2, 3	RD+ {1}, RD- {1}	I_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
16, 15	RD+ {2}, RD- {2}		
23, 24	RD+ {3}, RD- {3}		
37, 36	RD+ {4}, RD- {4}		
7, 8	TD+ {1}, TD- {1}	O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
11, 10	TD+ {2}, TD- {2}		
28, 29	TD+ {3}, TD- {3}		
32, 31	TD+ {4}, TD- {4}		
RMII INTERFACE			
106	REF_CLK	I	**Reference Clock Input.** These pins must be driven with a continuous 50-MHz clock in the RMII application and 125 MHz in the SMII application. They provide timing for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. Accuracy shall be +/- 50 ppm, with a duty cycle between 35% and 65% inclusive.
84	SSYNC	I_{PD}	**SMII SYNC.** In SMII mode, this pin provides a free running sync pulse occurring 1 of every 10 clock cycles. In RMII mode, this pin is NC (No Connect).
117, 116, 53, 52	CRS_DV {1:4}	O_{3S}	**Carrier Sense/Receive Data Valid.** CRS_DV shall be asserted by the PHY when the medium is non-idle. The data on RXD[1:0] is considered valid once CRS_DV is asserted. During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity. CRS_DV is not synchronized with respect to REF_CLK.
120, 88	TXD[1:0] {1}	I_{PD}	**Transmit Data Input.** TXD[1:0] dibit wide data is input on these pins for transmission by the PHY. The data is synchronous with REF_CLK. TXD[1] is the most significant bit. Values other than “00” on TXD[1:0] while TX_EN is deasserted are ignored by the PHY.
108, 87	TXD[1:0] {2}		
61, 86	TXD[1:0] {3}		
48, 85	TXD[1:0] {4}		
122, 109, 60, 47	TX_EN {1:4}	I_{PD}	**Transmit Enable.** Active high. Indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. TX_EN is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented to the RMII. TX_EN transitions synchronously with respect to REF_CLK.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias.
Bus Naming Convention: Pin label followed by [MSB:LSB] followed by {Port #}.

Table 5: Pin Definitions (Cont.)

PIN #	PIN LABEL	TYPE	DESCRIPTION
114, 115	RXD[1:0] {1}	O_{3S}	**Receive Data Outputs.** RXD[1:0] data is output synchronous with REF_CLK. RXD[1] is the most significant bit.
94, 95	RXD[1:0] {2}		
75, 74	RXD[1:0] {3}		
56, 54	RXD[1:0] {4}		
113, 112, 58 57	RX_ER {1:4}	O_{3S}	**Receive Error Detected.** Active high. RX_ER is asserted for one or more REF_CLK periods to indicate that an error was detected somewhere in the frame presently being transferred from the PHY. RX_ER transitions synchronously with respect to REF_CLK.
45	MDIO	I/O_{PU}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
44	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies up to 12.5 MHz are supported.
46	RESET#	I_{PU}	**Reset.** Active Low. Resets the BCM5214. Pin not included in NAND chain.
MODE			
123, 124, 125, 118, 119	PHYAD [4:0]	I_{PD}	**PHY ADdress Selects.** These inputs set the base address for MII management PHY addresses. Also serve as test control inputs along with TESTEN to select the NAND-chain test mode.
121	F100	I_{PU}	**10/100 Mode Select.** When high and ANEN is low, all transceivers will be forced to 100BASE-X operation. When low and ANEN is low, all transceivers will be forced to 10BASE-T operation. When ANEN is high, F100 has no effect on the operation.
39	ANEN	I_{PU}	**Auto-Negotiation Enable.** Active high. When pulled high, Auto-Negotiation will begin immediately after reset. When low, Auto-Negotiation is disabled after reset. Auto-Negotiation is always under software control (Register 0, bit 12).
126	FDXEN	I_{PD}	**Full-Duplex Mode Enable.** The FDXEN pin is logically ORed with an MII control bit to generate an internal full-duplex enable signal. When FDXEN is high, the BCM5214 may operate in full-duplex mode as determined by Auto-Negotiation or software. When FDXEN is low, the internal control bit (Register 0, bit 8) will determine the full-duplex operating mode. Initial value of the internal control bit is zero.
127	TESTEN	I_{PD}	**Test Enable.** Active high test control input used along with PHYAD[4:0] to select the NAND-chain test mode. This test mode is latched when TESTEN is pulsed high, then low, with PHYAD[4:0]=10111. This pin is not included in the NAND chain and must be pulled low or left unconnected during normal operation.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias.
Bus Naming Convention: Pin label followed by [MSB:LSB] followed by {Port #}.

Table 5: Pin Definitions (Cont.)

PIN #	PIN LABEL	TYPE	DESCRIPTION
50,49	NANDMD[1:0]	I_{PD}	**NAND Mode.** Active-high test control inputs used along with TESTEN and PHYAD[4:2] to select NAND-chain test mode. This test mode is latched when TESTEN is pulsed high then low, with PHYAD[4:2]=101 and NANDMD[1:0]=11. This pin is not included in the NAND-chain and must be pulled low or left unconnected during normal operation.
128	DLLTEST	I_{PU}	This pin must be left unconnected during normal operation.
42	ER0	I_{PU}	**Transmit DAC Edge Rate Control.** This pin control the slew rate of each of the transmit DACs. The 10-90% rise time is set by the value on ER0 as follows: 0 = 1 ns and 1 = 4 ns.
43	TXER_EN#	I_{PU}	**TXER Enable.** This pin selects the direction (input enable) of TXER/ SP100LED# pins. When TXER_EN# is low, it selects the input direction or TXER. When TXER_EN# is high, it selects output direction or SP100LED#.
104	SMII_EN	I_{PD}	**SMII Enable.** This pin selects between the RMII and SMII interfaces. An active high will select the SMII interface, while an active low or open pin will select the RMII interface.
BIAS			
19	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of each of the transmit DACs. A resistor of 1.24 KΩ ±1% must be connected between the RDAC pin and AGND.
20	VREF	B	**Voltage Reference.** Low-impedance bias pin driven by the internal band-gap voltage reference. This pin must be left unconnected during normal operation.
LED			
101	LNKLED# {1}	O	**Link Integrity LED.** Active low. This output signal indicates the link status of the PHY. LNKLED is driven low when the link to the PHY is good. Serial LED mode is enabled by “pull-down” of pin 66 during reset. When the Serial LED mode is enabled, pin 91 becomes the Serial LED mode frame signal. Low cost serial LED mode is enabled by “pull-down” of pin 80 during reset.
91	LNKLED# {2} SFRAME		
80	LNKLED# {3} LC_SER_LED_EN#	I/O_{PU}	
66	LNKLED# {4} SER_LED_EN#		
102, 92, 79, 65	SP100LED# {1:4} TXER {1:4}	I/O	**Speed 100 LED.** Driven low when operating in 100BASE-X modes and high when operating in 10BASE-T modes. **TXER.** This pin will become an active high input TXER signal if TXER_EN# is driven low during reset.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias.
Bus Naming Convention: Pin label followed by [MSB:LSB] followed by {Port #}.

Table 5: Pin Definitions (Cont.)

PIN #	PIN LABEL	TYPE	DESCRIPTION
100	XMTLED# {1} INTR# {1} FDXLED# {1}	O_{OD}	**Transmit Activity LED.** Active low output. The transmit activity LED is driven low for approximately 80 ms each time there is transmit activity while in the link pass state. When INTR mode is enabled, the pin becomes an interrupt output. When FDX LED mode is enabled, the pin becomes FDXLED output. When the Serial LED mode is enabled, pin 90 becomes the Serial LED mode data output signal.
90	XMTLED# {2} INTR# {2} FDXLED# {2} SER_SDO#		
81	XMTLED# {3} INTR# {3} FDXLED# {3}		
67	XMTLED# {4} INTR# {4} FDXLED# {4}		
99	RCVLED# {1} ACTLED# {1} LC_SER_SCLK	O_{OD}	**Receive Activity LED.** Active low output. The receive activity LED is driven low for approximately 80ms each time there is receive activity while in the link pass state. When in either INTR or FDXLED modes, this pin becomes ACTLED output for either receive or transmit activity. When the Serial LED is enabled, pin 89 becomes the Serial LED mode clock signal. When the low cost serial LED is enabled, pin 99 becomes Low cost serial LED mode clock signal and pin 82 becomes the data output signal.
89	RCVLED# {2} ACTLED# {2} SER_SCLK		
82	RCVLED# {3} ACTLED# {3} LC_SER_SDO#		
68	RCVLED# {4} ACTLED# {4}		
JTAG			
63	TDI	I_{PU}	**Test Data Input.** Single control input to the JTAG TAP controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.
73	TMS	I_{PU}	**Test Mode Select.** Serial data input to the JTAG TAP controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
72	TCK	I_{PU}	**Test Clock.** Clock input used to synchronize the JTAG TAP control and data transfers. If unused, may be left unconnected.
62	TDO	O_{3S}	**Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias.
Bus Naming Convention: Pin label followed by [MSB:LSB] followed by {Port #}.

Table 5: Pin Definitions (Cont.)

PIN #	PIN LABEL	TYPE	DESCRIPTION
71	TRST#	I_{PU}	**Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. Must be held low during power-up to insure the TAP Controller initializes to the test-logic-reset state. May be pulled low continuously when JTAG functions are not used.
POWER			
105	PLLVDD		**Phase Locked Loop VDD.**
107	PLLGND		**Phase Locked Loop GND.**
18	BIASVDD		**Bias VDD.**
21	BIASGND		**Bias GND.**
5, 13, 26, 34,	AVDD		**Analog VDD.**
4, 6, 9, 12, 14, 25, 27, 30, 33, 35	AGND		**Analog GND.**
77, 83, 97	DVDD		**Digital Core VDD.**
78, 96	DGND		**Digital Core GND.**
51, 59, 69, 76, 98, 110	OVDD		**Digital Periphery (Output Buffer) VDD.**
41 55, 70, 93, 103, 111	OGND		**Digital Periphery (Output Buffer) GND.**
1, 17 22, 38 40, 64	NC		**No Connect Pins.**

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias.
Bus Naming Convention: Pin label followed by [MSB:LSB] followed by {Port #}.

Section 3: Pinout Diagram

Figure 2 provides the pinout diagram for the BCM5214.

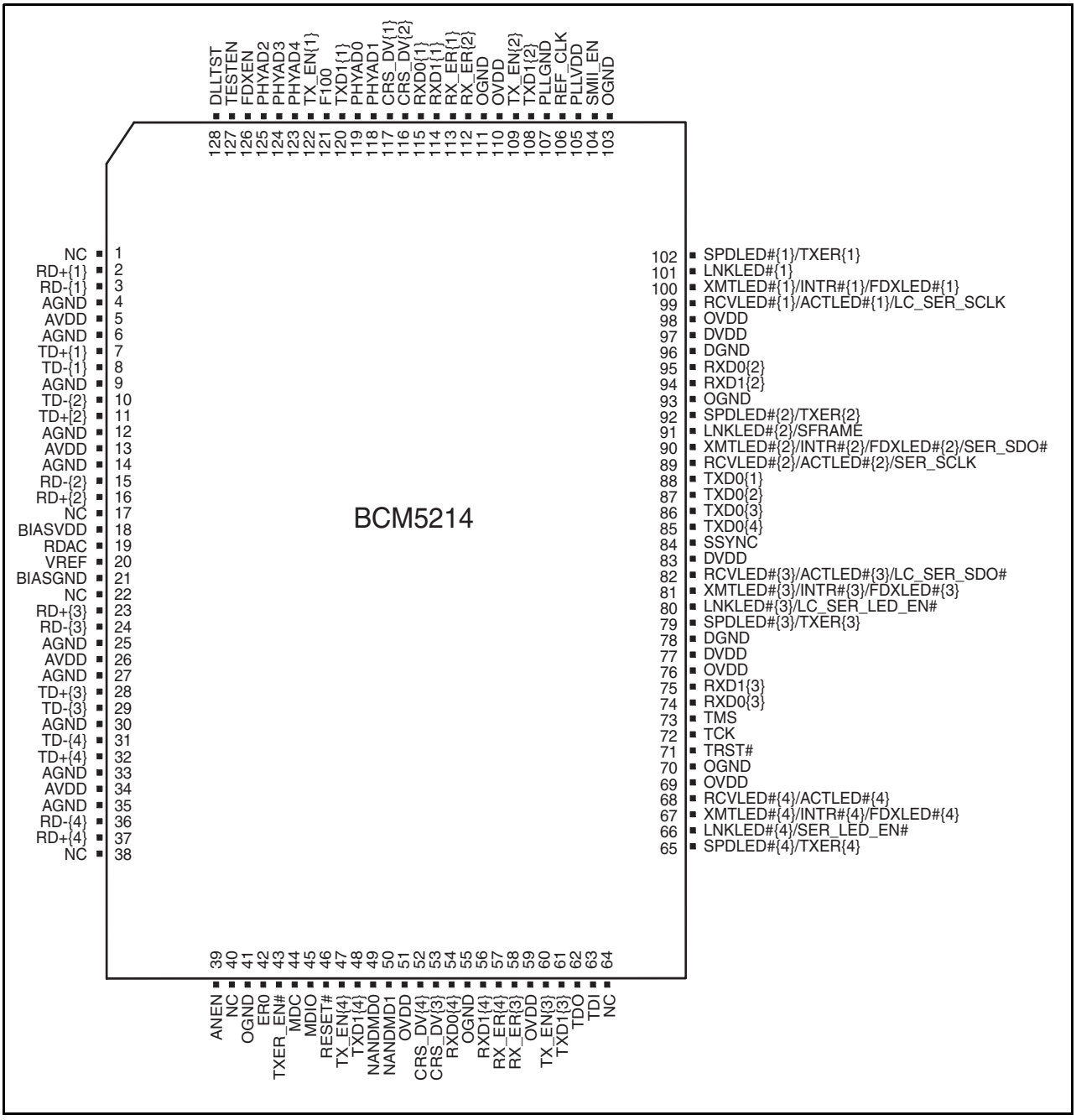


Figure 2: BCM5214 Pin Diagram

Section 4: Operational Description

RESETTING THE BCM5214

There are two ways to reset each transceiver in the BCM5214. A hardware reset pin is provided, which resets all internal nodes inside the chip to a known state. The reset pulse must be asserted for at least 400 ns. Hardware reset should always be applied to a BCM5214 after power-up.

Each transceiver in the BCM5214 also has an individual software reset capability. To perform software reset, a 1 must be written to bit 15 of the transceiver's MII Control Register (see MII Register Definitions on page 19). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a 0 is written to the MII Control Register reset bit.

Two pins are sampled during hardware reset:

- LC_SER_LED_EN# (Pin 80)
- SER_LED_EN# (Pin 66)

A software reset will not cause the pins to be sampled.

ISOLATE MODE

Each transceiver in the BCM5214 can be isolated from the RMII. When a transceiver is put into isolate mode, all RMII inputs (TXD[1:0] and TX_EN) are ignored, and all RMII outputs (CRS_DV, RX_ER, and RXD[1:0]) are set at high impedance. Only the MII management pins (MDC, MDIO, MDC2, MDIO2) operate normally. Upon resetting the chip, the isolate mode is off. Writing a 1 to bit 10 of the MII Control Register puts the transceiver into isolate mode. Writing a 0 to the same bit removes it from isolate mode.

LOOPBACK MODE

The loopback mode allows in-circuit testing of the BCM5214 chip. All packets sent in through the TXD pins are looped back internally to the RXD pins, and are not sent out to the cable. Incoming packets on the cable are ignored.

The loopback mode can be entered by writing a 1 to bit 14 of the MII Control Register. To resume normal operation, bit 14 of the MII Control Register must be 0. For 100BASE-TX loopback to work properly, AuxControl register (18hex), bit 14 must be set to force internal link on and 100BASE-X AuxControl register (10hex), bit 13 must be set to disable the transmitter.

Several function bypass modes are also supported, which provide different combinations of feedback paths during loopback testing. These bypass modes include: bypass scrambler, bypass MLT3 encoder and bypass 4B5B encoder.

FULL-DUPLEX MODE

The BCM5214 supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. By default, each transceiver in the BCM5214 powers up in half-duplex mode.

When Auto-Negotiation is disabled, full-duplex operation can be enabled either by a pin (FDXEN) or by an RMII register bit (Register “0”’ bit 8).

When Auto-Negotiation is enabled, full-duplex capability is advertised by default but can be overridden by a write to the Auto-Negotiation Advertisement Register (04h).

10BASE-T MODE

The same magnetics module is used to interface the twisted-pair cable in 10BASE-T mode and in 100BASE-TX mode. The data will be two-level Manchester coded instead of three-level MLT3 and no scrambling/descrambling or 4B5B coding is performed.

PHY ADDRESS

Each transceiver in the BCM5214 will have a unique PHY address for MII management. The PHY address is determined by the using the base address, which is input on the PHYAD[4:0] pins. The following shows the addressing of the eight PHYs.

PHY0 = PHYAD + 0, PHY1 = PHYAD + 1,... PHY7 = PHYAD + 7

Every time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

Section 5: Register Summary

MII Management Interface: Register Programming

The BCM5208R fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written to and read from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5208R at a rate of 0 – 12.5 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. Every RMII read or write instruction frame contains the following fields:

Table 6: MII Management Frame Format

OPERATION	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE	DIRECTION
READ	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	driven to BCM5208R driven by BCM5208R
WRITE	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	driven to BCM5208R

Preamble (PRE). 32 consecutive 1 bits must be sent through the MDIO pin to the BCM5208R to signal the beginning of an RMII instruction. Fewer than 32 1 bits cause the remainder of the instruction to be ignored.

Start of Frame (ST). A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP). A READ instruction is indicated by 10, while a WRITE instruction is indicated by 01.

PHY Address (PHYAD). A five-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips. The BCM5208R supports a complete address space with PHYAD[4:0] inputpins used as the base address for selecting one of the eight transceivers.

Register Address (REGAD). A five-bit Register Address follows, with the MSB transmitted first. The register map of the BCM5214, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA). The next two bit times are used to avoid contention on the MDIO pin when a Read operation is performed. For a write operation, 10 must be sent to the BCM5208R chip during these two bit times. For a Read operation, the MDIO pin must be placed into high-impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

Data. The last 16 bits of the frame are the actual data bits. For a write operation, these bits are sent to the BCM5214, whereas for a read operation, these bits are driven by the BCM5214. In either case, the MSB is transmitted first.

When writing to the BCM5214, the data field bits must be stable 10 ns before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM5214, the data field bits are valid after the rising-edge of MDC until the next rising-edge of MDC.

Idle. A high impedance state of the MDIO line. All tri-state drivers are disabled and the PHYs pull-up resistor pulls the MDIO line to logic 1. Note that at least one or more clocked idle states are required between frames.

Following are two examples of MII write and read instructions:

- In order to put a transceiver with PHY address 00001 into Loopback mode, the following MII write instruction must be issued: 1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000 1...
- In order to determine if a PHY is in the link pass state, the following MII read instruction must be issued: 1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ 1...

For the MII read operation, the BCM5208R will drive the MDIO line during the TA and Data fields (the last 17 bit times). A final 65th clock pulse must be sent to close the transaction and cause a write operation to take place.

MII REGISTER MAP SUMMARY

Table 7 contains the MII register summary for each port of the BCM5214. The register addresses are specified in hex form, and the name of register bits have been abbreviated. When writing to the reserved bits, always write a “0” value, and when reading from these bits, ignore the output value. Never write any value to an undefined register address. The reset value of the registers are shown in the INIT column.

Table 7: MII Register Map Summary

ADDR	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
00h	CONTROL	Soft Reset	Loopback	Force100	AutoNeg Enable	Power Down	Isolate	Restart AutoNeg	Full Duplex	Collision Test	Reserved							3000h
01h	STATUS	T4 Capable	TX FDX Capable	TX Capable	10BT FDX Capable	10BT Capable	Reserved				MF pream suppress	AutoNeg Complete	Remote Fault	AutoNeg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
02h	PHYID HIGH	0	0					0	0	0	1	0	0	0	0	0	0	0040h
03h	PHYID LOW	0	1	1	0	0	0	Model # 1	0	1	0	0	0	Revision # 0	0	0	0	6280h
04h	AUTONEG ADVERTISE	Next Page	Reserved	Remote Fault	Reserved Technologies		Pause	Adv T4	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	Advertised Selector Field [4:0] 0	0	0	0	1	01E1h
05h	LINK PARTNER ABILITY	LP Next Page	LP Acknowledge	LP Remote Fault	Reserved Technologies		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0] 0	0	0	0	0	0000h
06h	AUTONEG EXPANSION	Reserved											Par Det Fault	LP Next Pg Able	Next Pg Able	Page Recvd	LP Auto Neg Able	0000h
07h	NEXT PAGE	Next Page	Reserved	Message Page	Acknowledge 2	Toggle	Message/Unformatted Code Field											2001h
08h	LP NEXT PAGE	Next Page	Reserved	Message Page	Acknowledge 2	Toggle	Message/Unformatted Code Field											0000h
10h	100BASE-X AUX CONTROL	Reserved		Trans Disable	Reserved		Bypass 4B5B Enc/Dec	Bypass Scram/ Descram	Bypass NRZI Enc/Dec	Bypass Rcv Sym Alignment	BASEline Wander Disable	FEF Enable	Reserved		Extended RMII FIFOs	RMII Out of Band	Reserved	
11h	100BASE-X AUX STATUS	Reserved				RMII Over Under Run	FXMode	Locked	Current 100 Link Status	Current Remote Fault	Reserved	False Carrier Detected	Bad ESD Detected	RCV Error Detected	XMT Error Detected	Lock Error Detected	MLT3 Error Detected	
12h	100BASE-X RCV ERROR COUNTER	Receive Error Counter																0000h
13h	100BASE-X FALSE CARRIER COUNTER	RMII Over-run/Under-run Counter									False Carrier Sense Counter							0000h

Table 7: MII Register Map Summary (Cont.)

ADDR	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
14h	100BASE-X DISCONNECT COUNTER	RMII/ SMII Fastrxd	RMII/SMII Slowrxd	Reserved						Reserved								0000h
15h	RESERVED	Reserved																
16h	RESERVED	Reserved																
17h	PTEST	Reserved																0000h
18h	AUXILIARY CONTROL/ STATUS	Jabber Disable	Force Link	Reserved						HSQ	LSQ	Edge Rate [1:0]		AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	003xh
19h	AUXILIARY STATUS SUMMARY	AutoNeg Complete	AutoNeg Complete Ack	AutoNeg Ack Detect	AutoNeg Ability Detect	AutoNeg Pause	AutoNeg HCD			AutoNeg Pardet Fault	LP Remote Fault	LP Page Rcvd	LP AutoNeg Able	SP100 Indicator	Link Status	Internal AutoNeg Enabled	Jabber Detect	0000h
1Ah	INTERRUPT	FDX LED Enable	INTR Enable	Reserved		FDX Mask	SPD Mask	Link Mask	INTR Mask	Reserved				FDX Change	SPD Change	Link Change	INTR Status	0F00h
1Bh	AUX MODE2 REGISTER	Reserved					Token Ring Mode			Block 10BT Echo Mode	Traffic Meter LED Mode	Activity LED Force On	Serial LED Enable	Reserved	Activity/ Link LED Enable	Qual Parallel Detect Mode	Reserved	008Ah
1Ch	10BASE-T AUX. ERROR & GENERAL STATUS	Reserved					Manchstr Code Err (BT)	EOF Err (BT)	Polarity Err (BT)	0	Revision # 0	1	Reserved	AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	00xxh
1Dh	AUXILIARY MODE	Reserved		PHY Enable	Reserved								Activity LED Force Inactive	Link LED Force Inactive	Reserved	Block TXEN Mode	Reserved	x000h
1Eh	AUXILIARY MULTI-PHY	HCD TX FDX	HC T4	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart AutoNeg	AutoNeg Complete	Complete ACK	ACK Detect	Ability Detect	Super Isolate	Reserved			0000h
1Fh	BROADCOM TEST	Reserved - Do Not Write																

MII CONTROL REGISTER

Table 8: MII Control Register (Address 00d, 00h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Soft Reset	R/W (SC)	1 = PHY reset 0 = Normal operation	0
14	Loopback	R/W	1 = Loopback mode 0 = Normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation enable 0 = Auto-Negotiation disable	1
11	Power Down	RO	0 = Normal operation	0
10	Isolate	R/W	1 = Electrically isolate PHY from RMII/SMII 0 = Normal operation	0
9	Restart Auto-Negotiation	R/W (SC)	1 = Restart Auto-Negotiation process 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half-duplex	0
7	Reserved	RO	Ignore when Read	0
6:0	Reserved	RO	Ignore when Read	0

Notes:
R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High,
LL & LH Clear after read operation.

Soft Reset. To reset the BCM5208R by software control, a 1 must be written to bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and need not be cleared using a second MII write. Writes to other Control Register bits have no effect until the reset process is completed, which requires approximately 1 µs. Writing a 0 to this bit has no effect. Because this bit is self-clearing, after a few cycles from a write operation, it returns a 0 when read.

Loopback. The BCM5208R can be placed into loopback mode by writing a 1 to bit 14 of the Control Register. The loopback mode can be cleared by writing a 0 to bit 14 of the control register, or by resetting the chip. When this bit is read, it can return a 1 when the chip is in software-controlled loopback mode; otherwise it returns a 0. For the 100BASE-TX to operate properly, register 18hex (AuxControl), bit 14 must be set to force the internal link on and register 10hex (100BASE-X AuxControl), bit 13 must be set to disable the transmitter.

Forced Speed Selection. If Auto-Negotiation is enabled, this bit has no effect on the speed selection. However, if Auto-Negotiation is disabled by software control, the operating speed of the BCM5208R can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a 1 to this bit forces 100BASE-X operation, while writing a 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection, including both hardware and software control, use bit 8 of the Auxiliary Control Register.

Auto-Negotiation Enable. Auto-Negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic 0, Auto-Negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of 0, Auto-Negotiation is disabled by software control. When Auto-Negotiation is disabled in this manner, writing a 1 to the same bit of the Control Register or resetting the chip will re-enable Auto-Negotiation. Writing to this bit has no effect when Auto-Negotiation has been disabled by hardware control. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

Power Down. The BCM5208R does not implement a low power mode.

Isolate. Each individual PHY may be isolated from its Media Independent Interface by writing a 1 to bit 10 of the Control Register. All RMII outputs are tri-stated and all RMII inputs are ignored. Because the MII management interface is still active, the isolate mode can be cleared by writing a 0 to bit 10 of the control register, or by resetting the chip. When this bit is read, it will return a 1 when the chip is in isolate mode; otherwise it will return a 0.

Restart Auto-Negotiation. Bit 9 of the Control Register is a self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the Auto-Negotiation state machine. For this bit to have an effect, Auto-Negotiation must be enabled. Writing a 1 to this bit restarts the Auto-Negotiation, while writing a 0 to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY Register.

Duplex Mode. By default, the BCM5208R powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a 1 to bit 8 of the Control Register while Auto-Negotiation is disabled. Half-duplex mode can be resumed by writing a 0 to bit 8 of the control register, or by resetting the chip.

Reserved Bits. All reserved MII register bits must be written as 0 at all times. Ignore the BCM5208R output when these bits are read.

MII STATUS REGISTER

Table 9: MII Status Register (Address 01d, 01h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore when read	0
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	0
4	Remote Fault	RO LH	1 = Far-end fault condition detected 0 = No far-end fault condition detected	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable 0 = Not Auto-Negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link Pass state) 0 = Link is down (Link Fail state)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0

Table 9: MII Status Register (Address 01d, 01h) (Cont.)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
0	Extended Capability	RO	1 = Extended register capable	1

Notes:
R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High,
LL & LH Clear after read operation.

100BASE-T4 Capability. The BCM5208R is not capable of 100BASE-T4 operation, and returns a 0 when bit 15 of the status register is read.

100BASE-X Full-Duplex Capability. The BCM5208R is capable of 100BASE-X full-duplex operation, and returns a 1 when bit 14 of the Status Register is read.

100BASE-X Half-Duplex Capability. The BCM5208R is capable of 100BASE-X half-duplex operation, and returns a 1 when bit 13 of the Status Register is read.

10BASE-T Full-Duplex Capability. The BCM5208R is capable of 10BASE-T full-duplex operation, and returns a 1 when bit 12 of the Status Register is read.

10BASE-T Half-Duplex Capability. The BCM5208R is capable of 10BASE-T half-duplex operation, and returns a 1 when bit 11 of the Status Register is read.

Reserved Bits. Ignore the BCM5208R output when these bits are read.

MF Preamble Suppression. This bit is the only writeable bit in the Status Register. Setting this bit to a "1" allows subsequent RMII management frames to be accepted with or without the standard preamble pattern. When Preamble Suppression is enabled, only two preamble bits are required between successive Management Commands, instead of the normal 32.

Auto-Negotiation Complete. Bit 5 of the Status Register returns a 1 if the Auto-Negotiation process has been completed and the contents of registers 4, 5 and 6 are valid.

Remote Fault. The PHY returns a 1 in bit 4 of the Status Register when its link partner has signalled a far-end fault condition. When a far-end fault occurs, the bit is latched at 1 and remains so until the register is read and the remote fault condition has been cleared; this only applies to the FX mode of operation.

Auto-Negotiation Capability. The BCM5208R is capable of performing IEEE Auto-Negotiation, and returns a 1 when bit 4 of the Status Register is read, regardless of whether the Auto-Negotiation function has been disabled.

Link Status. The BCM5208R returns a 1 on bit 2 of the Status Register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the Link Pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the Link Pass state has been entered again.

Jabber Detect. 10BASE-T operation only. The BCM5208R returns a 1 on bit 1 of the Status Register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability. The BCM5208R supports extended capability registers, and returns a 1 when bit 0 of the Status Register is read. Several extended registers have been implemented in the BCM5208R, and their bit functions are defined later in this section.

PHY Identifier Registers

Table 10: PHY Identifier Registers (Addresses 02d and 03d, 02h and 03h)

BIT	NAME	R/W	DESCRIPTION	VALUE
15:0	MII Address 00010	RO	PHYID HIGH	0040h
15:0	MII Address 00011	RO	PHYID LOW	61F0h

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24-bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5214 part, 1Fh, and Broadcom Revision number, 00h, is placed into two MII Registers. The translation from OUI, Model Number and Revision Number to PHY Identifier Register occurs as follows:

PHYID HIGH [15:0] = OUI[21:6]

PHYID LOW [15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

Note that the two most significant bits of the OUI are not represented (OUI[23:22]).

The table above shows the result of concatenating these values in order to form the MII Identifier Registers PHYID HIGH and PHYID LOW.

Auto-Negotiation Advertisement Register

Table 11: Auto-Negotiation Advertisement Register (Address 04d, 04h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Next Page	R/W	1 = Next Page Ability enabled 0 = Next Page Ability disabled	0
14	Reserved	RO	Ignore when Read	
13	Reserved	R/W	Ignore when Read	0
12:11	Reserved Technologies	RO	Ignore when Read	
10	Advertise Pause Capability	R/W	1 = Pause Operation for full-duplex	0
9	Advertise 100BASE-T4	R/W	0 = Do Not Advertise T4 Capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X full-duplex 0 = Do Not Advertise 100BASE-X full-duplex	0
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex 0 = Do Not Advertise 10BASE-T full-duplex	0
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	R/W	Indicates 802.3	00001

Next Page. The BCM5208R supports Next Page capability.

Reserved Bits. Ignore output when read.

Remote Fault. Writing a 1 to bit 13 of the Advertisement Register causes a Remote Fault indicator to be sent to the Link Partner during Auto-Negotiation. Writing a 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

Reserved Technologies Bits. Ignore output when read.

Pause Operation for Full-Duplex Links. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

Advertisement Bits. Bits 9:5 of the Advertisement Register allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM5208R. By writing a 1 to any of the bits, the corresponding ability will be transmitted to the Link Partner. Writing a 0 to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset.

Selector Field. Bits 4:0 of the Advertisement register contain the value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 12: Auto-Negotiation Link Partner Ability Register (Address 05d, 05h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Next Page	RO	1 = Link partner has next page ability 0 = Link partner does not have next page ability	0
14	Acknowledge	RO	1 = Link partner has received link code word 0 = Link partner has not received link code word	0
13	Remote Fault	RO	1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault	0
12:11	Reserved Technologies	RO	Ignore when Read	–
10	LP Pause	RO	1 = Link partner pause capable	0
9	100BASE-T4 capability	RO	1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable	0
8	100BASE-TX Full Duplex capability	RO	1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable	0
7	100BASE-TX capability	RO	1 = Link partner is 100BASE-TX capable 0 = Link partner is not 100BASE-TX capable	0
6	10BASE-T Full Duplex capability	RO	1 = Link partner is 10BASE-T full duplex capable 0 = Link partner is not 10BASE-T full duplex capable	0
5	10BASE-T capability	RO	1 = Link partner is 10BASE-T capable 0 = Link partner is not 10BASE-T capable	0
4:0	Selector Field	RO	Link partner protocol selector field	00000

Note that the values contained in the Auto-Negotiation Link Partner Ability Register are only guaranteed to be valid after Auto-Negotiation is successfully completed, as indicated by bit 5 of the MII Status Register.

Next Page. Bit 15 of the Link Partner Ability Register returns a value of 1 when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit.

Acknowledge. Bit 14 of the Link Partner Ability Register is used by Auto-Negotiation to indicate that a device has successfully received its Link Partner's Link Code Word.

Remote Fault. Bit 13 of the Link Partner Ability Register returns a value of 1 when the Link Partner signals that a remote fault has occurred. The BCM5208R copies the value to this register and does not act upon it.

Reserved Bits. Ignore when read.

Pause. Indicates that the link partner pause bit is set.

Advertisement Bits. Bits 9:5 of the Link Partner Ability Register reflect the abilities of the Link Partner. A 1 on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time Auto-Negotiation is restarted or the BCM5214 is reset.

Selector Field. Bits 4:0 of the Link Partner Ability Register reflect the value of the Link Partner's selector field. These bits are cleared any time Auto-Negotiation is restarted or the chip is reset.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 13: Auto-Negotiation Expansion Register (Address 06d, 06h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:5	Reserved	RO	Ignore when Read	
4	Parallel Detection Fault	RO LH	1 = Parallel Detection fault. 0 = No Parallel Detection fault	0
3	Link Partner Next Page Able	RO	1 = Link Partner has Next Page capability 0 = Link Partner does not have Next Page	0
2	Next Page Able	RO		0
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto-Negotiation Able	RO LH	1 = Link Partner has Auto-Negotiation capability 0 = Link Partner does not have Auto-Negotiation	0
Notes: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High,* LL & LH Clear after read operation.				

Reserved Bits. Ignore when read.

Parallel Detection Fault. Bit 4 of the Auto-Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto-Negotiation state machine. For further details, refer to the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Able. Bit 3 of the Auto-Negotiation Expansion Register returns a 1 when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Next Page Able.

Page Received. Bit 1 of the Auto-Negotiation Expansion Register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

Link Partner Auto-Negotiation Able. Bit 0 of the Auto-Negotiation Expansion Register returns a 1 when the Link Partner is known to have Auto-Negotiation capability. Before any Auto-Negotiation information is exchanged, or if the Link Partner does not comply with IEEE Auto-Negotiation, the bit returns a value of 0.

AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

Table 14: Next Page Transmit Register (Address 07d, 07h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Next Page	R/W	1 = Additional Next Page(s) will follow 0 = Last page	0
14	Reserved	R/W	Ignore when read	0
13	Message Page	R/W	1= Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	0
10:0	Message/Unformatted Code Field	R/W		1

Next Page. Indicates whether this is the last Next Page to be transmitted.

Message Page. Differentiates a Message Page from an Unformatted Page.

Acknowledge 2. Indicates that a device has the ability to comply with the message.

Toggle. Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An eleven-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An eleven-bit-wide field, which may contain an arbitrary value.

AUTO-NEGOTIATION LINK PARTNER (LP) NEXT PAGE TRANSMIT REGISTER

Table 15: Next Page Transmit Register (Address 08d, 08h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Next Page	RO	1 = Additional Next Page(s) will follow 0 = Last page	0
14	Reserved	RO	Ignore when read	0
13	Message Page	RO	1= Message page 0 = Unformatted page	0
12	Acknowledge 2	RO	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	0
10:0	Message/Unformatted Code Field	RO		0

Next Page. Indicates whether this is the last Next Page.

Message Page. Differentiates a Message Page from an Unformatted Page.

Acknowledge 2. Indicates that Link Partner has the ability to comply with the message.

Toggle. Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An eleven-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An eleven-bit-wide field, which may contain an arbitrary value.

100BASE-X AUXILIARY CONTROL REGISTER

Table 16: 100BASE-X Auxiliary Control Register (Address 16d, 10h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:14	Reserved		Ignore when read	
13	Transmit Disable	R/W	1 = Transmitter disabled in PHY 0 = Normal operation	0
12:11	Reserved	RO	Ignore when read	0
10	Bypass 4B5B Encoder/ Decoder	R/W	1 = Transmit and receive 5B codes over RMII pins 0 = Normal RMII interface	0
9	Bypass Scrambler/ Descrambler	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass NRZI Encoder/ Decoder	R/W	1 = NRZI encoder and decoder are disabled 0 = NRZI encoder and decoder are enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = BASEline wander correction disabled 0 = BASEline wander correction enabled	0
5	FEF Enable	R/W	1 = Far End Fault enabled 0 = Far End Fault disabled	0
4:3	Reserved	R/W	Write as 0, ignore when read	
2	Extended RMII FIFO Enable	R/W	1 = Extended FIFO mode, 0 = Normal FIFO mode	0
1	RMII Out-of-Band Enable	R/W	1 = Enabled, 0 = Disabled	0
0	Reserved	R/W	Write as 0, ignore when read	0

Reserved Bits. Ignore when read.

Transmit Disable. The transmitter may be disabled by writing a 1 to bit 13 of MII Register 10h. The transmitter output (TD±) is forced into a high impedance state.

Bypass 4B5B Encoder/Decoder. The 4B5B encoder and decoder can bypassed by writing a 1 to bit 10 of MII Register 10h. The transmitter sends 5B codes from the TXER and TXD[3:0] pins directly to the scrambler. TXEN must be active and frame encapsulation (insertion of J/K and T/R codes) are not performed. The receiver places de-scrambled and aligned 5B codes onto the RXER and RXD[3:0] pins. CRS is still asserted when a valid frame is received.

Bypass Scrambler/Descrambler. The stream cipher function can be disabled by writing a 1 to bit 9 of MII register 10h. The stream cipher function may be re-enabled by writing a 0 to this bit.

Bypass NRZI Encoder/Decoder. The NRZI encoder and decoder can be bypassed by writing a 1 to bit 8 of MII Register 10h, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) can be re-enabled by writing a 0 to this bit.

Bypass Receive Symbol Alignment. Receive symbol alignment can be bypassed by writing a 1 to bit 7 of MII Register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes are placed directly on the RXER and RXD[3:0] pins.

Baseline Wander Correction Disable. The baseline wander correction circuit can be disabled by writing a "1" to bit 6 of MII register 10h. The BCM5214 corrects for baseline wander on the receive data signal when this bit is cleared.

FEF Enable. Controls the Far End Fault mechanism associated with 100BASE-FX operation. A 1 enables the FEF function and a 0 disables it.

Extended RMII FIFO Enable. Controls the extended RMII FIFO mechanism.

RMII Out-of-Band Enable. Controls the RMII out-of band mechanism within the RMII receive logic.

Reserved Bits. The Reserved bits of the 100BASE-X Auxiliary Control Register must be written as 0 at all times. Ignore the BCM5214 outputs when these bits are read.

100BASE-X AUXILIARY STATUS REGISTER

Table 17: 100BASE-X Auxiliary Status Register (Address 17d, 11h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:12	Reserved	RO	Ignore when read	0
11	RMII Overrun/Underrun Detected	RO	1 = Error detected 0 = No error	0
10	FX Mode	RO	1 = 100BASE-FX mode 0 = 100BASE-TX or 10BASE-T mode	SD± PINS
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7	Remote Fault	RO	1 = Remote fault detected 0 = No remote fault detected	0
6	Reserved	RO	Ignore when read	0
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 =No false carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = No ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Notes:
R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High,
LL & LH Clear after read operation.

RMII Overrun/Underrun Error. The PHY returns a 1 in bit 11, when the RMII receive FIFO encounters an overrun or underrun condition.

FX Mode. Returns a value derived from the SD± input pins. Returns 1 when the SD± pins are driven with a valid differential signal level. Returns 0 when both SD+ and SD- are simultaneously driven low.

Locked. The PHY returns a 1 in bit 9 when the de-scrambler is locked to the incoming data stream. Otherwise it returns a 0.

Current 100BASE-X Link Status. The PHY returns a 1 in bit 8 when the 100BASE-X link status is good. Otherwise it returns a 0.

Remote Fault. The PHY returns a 1 while its link partner is signalling a far-end fault condition. Otherwise it returns a 0.

False Carrier Detected. The PHY returns a 1 in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise it returns a 0.

Bad ESD Detected. The PHY returns a 1 in bit 4 if an End of Stream Delimiter error has been detected since the last time this register was read. Otherwise it returns a 0.

Receive Error Detected. The PHY returns a 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise it returns a 0.

Transmit Error Detected. The PHY returns a 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise it returns a 0.

Lock Error Detected. The PHY returns a 1 in bit 1if the de-scrambler has lost lock since the last time this register was read. Otherwise it returns a 0.

MLT3 Code Error Detected. The PHY returns a 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise it returns a 0.

100BASE-X Receive Error Counter

Table 18: 100BASE-X Receive Error Counter (Address 18d, 012h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:0	Receive Error Counter	R/W	Number of Non-Collision packets with Receive Errors since last Read	0000h

This counter increments each time the BCM5214 receives a non-collision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting Receive Errors until cleared.

100BASE-X False Carrier Sense Counter

Table 19: 100BASE-X False Carrier Sense Counter (Address 19d, 13h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	RMII Over-run/Under-run Counter	R/W	Number of RMII Over-runs/Under-runs since last Read	00
7:0	False Carrier Sense Counter	R/W	Number of False Carrier Sense events since last Read	00h

The RMII counter increments each time the BCM5214 detects an over-run or under-run of the RMII FIFOs. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting over-run/under-run Errors until cleared.

The False Carrier Sense counter increments each time the BCM5214 detects a false carrier on the receive input. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting False Carrier Sense Errors until cleared.

100BASE-X Disconnect Counter

Table 20: 100BASE-X Disconnect Counter (Address 20d, 14h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	RMII/SMII Fast RXD	RO	1 = In extended FIFO mode, detect fast receive data 0 = Normal	0
14	RMII/SMII Slow RXD	RO	1 = In extended FIFO mode, detect slow receive data 0 = Normal	0
13:0	Reserved	RO	Write as 0, ignore when read	0

RMII/SMII Fast RXD. Extended FIFO operation only. Bit 15 of the Disconnect counter register indicates the FIFO state machine has detected fast receive data relative to the REF_CLK input.

RMII/SMII Slow RXD. Extended FIFO operation only. Bit 14 of the Disconnect counter register indicates the FIFO state machine has detected slow receive data relative to the REF_CLK input.

AUXILIARY CONTROL/STATUS REGISTER

Table 21: Auxiliary Control/Status Register (Address 24d, 18h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Jabber Disable	R/W	1= Jabber function disabled in PHY 0 = Jabber function enabled in PHY	0
14	Link Disable	R/W	1= Link Integrity test disabled in PHY 0 = Link Integrity test is enabled in PHY	0
13:8	Reserved	RO	Ignore when read	000000
7:6	HSQ : LSQ	R/W	These two bits define the Squelch Mode of the 10BASE-T Carrier Sense mechanism: 00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Not allowed	00
5:4	Edge_Rate [1:0]	R/W	00 = 1 ns 01 = 2 ns 10 = 3 ns 11 = 4 ns	11
3	Auto-Negotiation Indicator	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

Jabber Disable. 10BASE-T operation only. Bit 15 of the Auxiliary Control Register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a 1 to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

Link Disable. Writing a 1 to bit 14 of the Auxiliary Control Register allows the user to disable the Link Integrity state machines, and place the BCM5208R into forced Link Pass status. Writing a 0 to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

HSQ and LSQ. Extend or decrease the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high- and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5208R to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Edge Rate. Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode. These bits are logically ANDed with the ER[1:0] input pins to produce the internal edge-rate controls (Edge_Rate[1] AND ER[1], Edge_Rate[0] AND ER[0]).

Auto-negotiation Indicator. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5208R. A combination of a 1in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 3 of the Auxiliary Control Register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 0 when one of following two cases is true:

- The ANEN pin is low AND the F100 pin is low, OR:
- Bit 12 of the Control Register has been written “0” AND bit 13 of the Control Register has been written “0”. When bit 8 of the Auxiliary Control Register is “0”, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. Bit 1 of the Auxiliary Control Register is a read-only bit that shows the true current operation speed of the BCM5208R. A 1bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208R is always operating at 10BASE-T speed.

Full-Duplex Indication. Bit 0 of the Auxiliary Control Register is a read-only bit that returns a 1 when the BCM5208R is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY STATUS SUMMARY REGISTER

Table 22: Auxiliary Status Summary Register (Address 25d, 19h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed	0
14	Auto-Negotiation Complete Acknowledge	RO LH	1 = Auto-Negotiation completed acknowledge state	0
13	Auto-Negotiation Acknowledge Detected	RO LH	1 = Auto-Negotiation acknowledge detected	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-Negotiation for link partner ability	0
11	Auto-Negotiation Pause	RO	BCM5214 & link partner Pause Operation bit set	0
10:8	Auto-Negotiation HCD	RO	000 = No Highest Common Denominator 001 = 10BASE-T 010 = 10BASE-T full-duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX full-duplex 11x = Undefined	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel Detection fault	0
6	Link Partner Remote Fault	RO		
5	Link Partner Page Received	RO LH	1 = New Page has been received	0
4	Link Partner Auto-Negotiation Able	RO	1 = Link Partner is Auto-Negotiation capable	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	0
2	Link Status	RO LL	1 = Link is Up (link pass state)	0

Table 22: Auxiliary Status Summary Register (Address 25d, 19h) (Cont.)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
1	Auto-Negotiation Enabled	RO	1 = Auto-Negotiation enabled.	1
0	Jabber Detect	RO LL	1 = Jabber condition detected.	0
Notes: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High,* LL & LH Clear after read operation.				

The Auxiliary Status Summary Register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bits can be found associated with their primary register descriptions.

INTERRUPT REGISTER

Table 23: Interrupt Register (Address 26d, 1Ah)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	FDX LED Enable	R/W	Full-duplex LED Enable	SERIAL_LED_EN#
14	INTR Enable	R/W	Interrupt Enable	0
13:12	Reserved	RO	Ignore when read	0
11	FDX Mask	R/W	Full-duplex Interrupt Mask	1
10	SPD Mask	R/W	SPEED Interrupt Mask	1
9	LINK Mask	R/W	LINK Interrupt Mask	1
8	INTR Mask	R/W	Master Interrupt Mask	1
7:4	Reserved	RO	Ignore when read	0
3	FDX Change	RO LH	Duplex Change Interrupt	0
2	SPD Change	RO LH	Speed Change Interrupt	0
1	LINK Change	RO LH	Link Change Interrupt	0
0	INTR Status	RO LH	Interrupt Status	0
Notes: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.*				

FDX LED Enable. Setting this bit enables the FDX LED mode. Bits 14 and 15 of this register are mutually exclusive. Only one can be set at a time. When FDXLED mode is enabled, FDXLED# becomes FDX LED and ACTLED# becomes activity LED. When both FDXLED mode and Interrupt enable are disabled, FDXLED# becomes XMTLED# and ACTLED# becomes RCVLED#. The default state of this bit reflects the state of the SERIAL_LED_EN# pin.

Interrupt Enable. Setting this bit enables Interrupt Mode. Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time. When Interrupt Mode is enabled, FDXLED# becomes INTR#.

FDX Mask. When this bit is set, changes in duplex mode will not generate an interrupt.

SPD Mask. When this bit is set, changes in operating speed will not generate an interrupt.

Link Mask. When this bit is set, changes in Link status do not generate an interrupt.

Interrupt Mask. Master Interrupt Mask. When this bit is set, no interrupts are generated, regardless of the state of the other MASK bits.

FDX Change. A 1 indicates a change of duplex status since last register read. Register read clears the bit.

SPD Change. A 1 indicates a change of speed status since last register read. Register read clears the bit.

Link Change. A 1 indicates a change of link status since last register read. Register read clears the bit.

Interrupt Status. Represents status of the INTR# pin. A 1 indicates that the interrupt mask is off and that one or more of the change bits are set. Register read clears the bit.

AUXILIARY MODE 2 REGISTER

Table 24: Auxiliary Mode 2 Register (Address 27d, 1Bh)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:11	Reserved	RO	Ignore when read	0
10	Extended Packet Mode	R/W	1 = Enable, 0 = Disable	0
9:8	Reserved	RO	Ignore when read	0
7	Block 10BT Echo Mode	R/W	1 = Enable, 0 = Disable	1
6	Traffic Meter LED Mode	R/W	1 = Enable, 0 = Disable	0
5	Activity LED Force On	R/W	1 = ON, 0 = Normal operation	0
4	Serial LED Mode	R/W	1 = Enable, 0 = Disable	$\overline{\text{SERIAL\_LED\_EN\#}}$
3	Reserved	R/W	Write as 1, Ignore when read	1
2	Activity/Link LED Mode	R/W	1 = Enable, 0 = Disable	0
1	Qual Parallel Detect Mode	R/W	1 = Enable, 0 = Disable	1
0	Reserved	RO	Ignore when read	0

Notes:
R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.

Extended Packet Mode. When enabled, the 100BASE-X unlock timer changes to allow long packets.

Block 10BT Echo Mode. When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal does not echo onto the RXDV pin. The TXEN echos onto the CRS pin and the CRS deassertion directly follows the TXEN deassertion.

Traffic Meter LED Mode. When enabled, the Activity LEDs (ACTLED# and FDXLED# if full-duplex LED and interrupt LED modes are not enabled) do not blink based on the internal LED clock (approximately 80ms on time). Instead, they blink based on the rate of Receive and Transmit activity. Each time a Receive or Transmit operation occurs, the LED turns on for a minimum of 5ms. During light traffic, the LED blinks at a low rate, while during heavier traffic the LEDs remains on.

Activity LED Force on. When asserted, the Activity LEDs (ACTLED# and FDXLED# if full-duplex LED and interrupt LED modes are not enabled) are turned on. This bit has a higher priority than the Activity LED force Inactive, bit 4, register 1Dh.

Serial LED Mode. This bit is only valid in port 2. When enabled, the values of the 4 slices LED outputs are serially shifted out on the second slices' LED outputs. The sequence of serial output bits is as follows: Receive, Transmit, Link, Speed, Global Interrupt, Full-Duplex. If the interrupts are not enabled for the particular slice, then the sequence is as follows: Receive, Transmit, Link, Speed, Collision, Full-Duplex. The values of these bits can vary due to the different LED modes available. The default state of this bit reflects the opposite state of the SER_LED_EN#, pin 66.

Activity/Link Led Mode. When enabled, the ACTLED# output goes active upon acquiring link and pulses during Receive or Transmit activity.

Qualified Parallel Detect Mode. This bit allows the Auto-Negotiation/Parallel Detection process to be qualified with information in the Advertisement register.

If this bit is not set, the local BCM5214 device is enabled to Auto-Negotiate, and the far-end device is a 10BASE-T or 100BASE-X non-Auto-Negotiating legacy type, the local device Auto-Negotiate/Parallel Detects the far-end device, regardless of the contents of its Advertisement register (04h).

If this bit is set, the local device compares the link speed detected to the contents of its Advertisement register. If the particular link speed is enabled in the Advertisement register, the local device asserts link. If the link speed is disabled in this register, then the local device does not assert link and continues monitoring for a matching capability link speed.

10BASE-T Auxiliary Error & General Status Register

Table 25: 10BASE-T Auxiliary Error & General Status Register (Address 28d, 1Ch)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:11	Reserved	RO	Ignore when read	
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T)	0
9	End Of Frame Error	RO	1 = EOF detection error (10BASE-T)	0
8	Polarity Inversion	RO	1 = Channel Polarity Inverted 0 = Channel Polarity Correct	0
7:5	Revision	RO	Revision Number	001
4	Reserved	RO	Ignore when read	0
3	Auto-Negotiation Indication	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

All error bits in the Auxiliary Error Status Register are read-only and are latched high. When certain types of errors occur in the BCM5208R, one or more corresponding error bits become 1. They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RX_ER output pin at the time the error occurs.

Manchester Code Error. Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

End of Frame Error. Indicates that the End Of Frame (EOF) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

Polarity. Reflects the Polarity status of the receive channel pair. The BCM5208R is capable of automatically inverting the polarity of the receive channel. No data errors are reported to indicate that the automatic polarity inversion is occurring. Instead, this bit returns a 1 whenever the polarity of the receive channel is inverted.

Revision. Read-only bits that return the revision number of the BCM5208R. The current revision is 001.

Auto-negotiation Indication. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the

BCM5208R. A combination of a 1 in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 15 of the Auxiliary Mode Register returns a 0. At all other times, it returns a 1.

Force 100/10 Indication. A read-only bit that returns a value of 0 when one of following two cases is true:

- The ANEN pin is low AND the F100 pin is low, or
- Bit 12 of the Control Register has been written 0 AND bit 13 of the Control Register has been written 0.

When bit 8 of the Auxiliary Control Register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. A read-only bit that shows the true current operation speed of the BCM5208R. A 1 bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208R is always operating at 10BASE-T speed.

Full-Duplex Indication. A read-only bit that returns a 1 when the BCM5208R is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY MODE REGISTER

Table 26: Auxiliary Mode Register (Address 29d, 1Dh)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	Reserved	RO	Ignore when read	0
14	Reserved	RO	Ignore when read	0
13	PHY Enable	R/W	1 = PHY enabled in segmentation mode 0 = PHY disabled in segmentation mode	0
12	Reserved	RO	Ignore when read	0
11:5	Reserved	RO	Ignore when read	0
4	Activity LED Disable	R/W	1 = Disable XMT/RCV Activity LED outputs 0 = Enable XMT/RCV Activity LED outputs	0
3	Link LED Disable	R/W	1 = Disable Link LED output 0 = Enable Link LED output	0
2	Reserved	RO	Ignore when read	0
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0
0	Reserved	RO	Ignore when read	0

PHY Enable. Applicable only when Segmentation Enable is active**.** When set to a 1, this PHY is connected to the RMII interface specified in the Segmentation Control Register. When 0, this PHY is disconnected from the selected RMII interface.

Activity LED Disable. When set to 1, disables the ACTLED# output pin. When 0, ACTLED# output pin is enabled.

Link LED Disable. When set to 1, disables the Link LED output pin. When 0, Link LED output is enabled.

Block TXEN Mode. When this mode is enabled, short IPGs of 1, 2, 3 or 4 TXC cycles all result in the insertion of two IDLEs before the beginning of the next packet's JK symbols.

AUXILIARY MULTIPLE PHY REGISTER

Table 27: Auxiliary Multiple PHY Register (Address 30d, 1Eh)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15	HCD_TX_FDX	RO	1 = Auto-Negotiation result is 100BASE-TX full-duplex	0
14	HCD_T4	RO	1 = Auto-Negotiation result is 100BASE-T4	0
13	HCD_TX	RO	1 = Auto-Negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-Negotiation result is 10BASE-T full-duplex	0
11	HCD_10BASE-T	RO	1 = Auto-Negotiation result is 10BASE-T	0
10:9	Reserved	RO	Ignore when read	0
8	Restart Auto-Negotiation	R/W (SC)	1 = Restart Auto-Negotiation process 0 = No effect	0
7	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process Completed 0 = Auto-Negotiation process not Completed	0
6	Acknowledge Complete	RO	1 = Auto-Negotiation Acknowledge Completed	0
5	Acknowledge Detected	RO	1 = Auto-Negotiation Acknowledge Detected	0
4	Ability Detect	RO	1 = Auto-Negotiation waiting for LP Ability	0
3	Super Isolate	R/W	1 = Super Isolate mode 0 = Normal Operation	0
2	Reserved	RO	Ignore when read	0
1	Reserved	R/W	Write as 0, Ignore when read	0
0	Reserved	R/W	Write as 0, Ignore when read	0

HCD Bits. Bits 15:11 of the Auxiliary Multiple PHY Register are five read-only bits that report the Highest Common Denominator (HCD) result of the Auto-Negotiation process. Immediately upon entering the Link Pass state after each reset or Restart Auto-Negotiation, only one of these five bits is 1. The Link Pass state is identified by a 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time Auto-Negotiation is restarted or the BCM5214 is reset. Note that for their intended application, these bits will uniquely identify the HCD only after the first Link Pass after reset or restart of Auto-Negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the Link Partner is different, more than one of the above bits may be active.

Restart Auto-Negotiation. A self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, Auto-Negotiation must be enabled. Writing a 1 to this bit restarts Auto-Negotiation. Since the bit is self-clearing (SC), it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Control Register.

Auto-negotiation Complete. This read-only bit returns a 1 after the Auto-Negotiation process has been completed. It remains 1 until the Auto-Negotiation process is restarted, a Link Fault occurs, or the chip is reset. If Auto-Negotiation is disabled or the process is still in progress, the bit returns a 0.

Acknowledge Complete. This read-only bit returns a 1 after the Acknowledgment exchange portion of the Auto-Negotiation process has been completed and the Arbitrator state machine has exited the Complete Acknowledge state. It remains this value until the Auto-Negotiation process is restarted, a Link Fault occurs, Auto-Negotiation is disabled, or the BCM5214 is reset.

Acknowledge Detected. This read-only bit is set to 1 when the Arbitrator state machine exits the Acknowledged Detect state. It remains high until the Auto-Negotiation process is restarted, or the BCM5214 is reset.

Ability Detect. This read-only bit returns a 1 when the Auto-Negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the Auto-Negotiation process begins, and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns a 0 any time the Auto-Negotiation state machine is not in the Ability Detect state.

Super Isolate. Writing a 1 to this bit places the BCM5208R into the Super Isolate mode. Similar to the Isolate mode, all RMII inputs are ignored, and all RMII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5208R to coexist with another PHY on the same printed circuit board, with only one being activated at any time.

BROADCOM TEST REGISTER

Table 28: Broadcom Test (Address 31d, 1Fh)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
Reserved — Do Not Write				

Reserved Bits. The Broadcom test register bits are reserved and should never be written.

Section 6: Timing and AC Characteristics

All RMII Interface pins comply with IEEE 802.3u timing specifications (See "RMII Interface" on page 4). All digital output timing specified at C_L = 30 pF.

Output rise/fall times measured between 10% and 90% of the output signal swing. Input rise/fall times measured between V_{IL} max. and V_{IH} min. Output signal transitions referenced to the midpoint of the output signal swing. Input signal transitions referenced to the midpoint between V_{IL} max. and V_{IH} min.

Table 29: Clock Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
REF_CLK Cycle Time (50-MHz Operation)	CK_CYCLE		20		ns
REF_CLK Cycle Time (125-MHz Operation)	CK_CYCLE		8		ns
REF_CLK High/Low Time			20		
REF_CLK High/Low Time (50-MHz Operation)	CK_HI CK_LO	7	10	13	ns
REF_CLK High/Low Time (125-MHz Operation)	CK_HI CK_LO		4		ns
REF_CLK Rise/Fall Time					
REF_CLK Rise/Fall Time (50-MHz Operation)	CK_EDGE			2	ns
REF_CLK Rise/Fall Time (125-MHz Operation)	CK_EDGE			1	ns

Table 30: Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Reset Pulse Length with stable REF_CLK Input	RESET_LEN	400			ns
Activity after end of Reset	RESET_WAIT	100			µs
RESET Rise/Fall Time	RESET_EDGE			10	ns

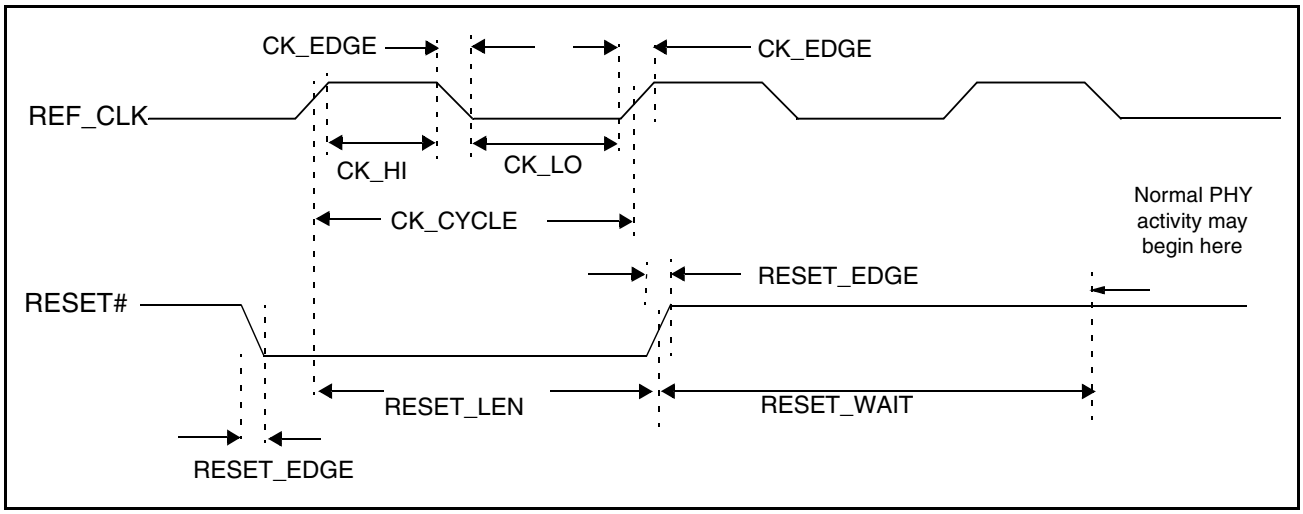


Figure 3: Clock and Reset Timing

Table 31: RMII Transmit Timing

PARAMETER	SYMBOL	Min	TYP	MAX	UNIT
REF_CLK Cycle Time			20		ns
TXEN, TXD[1:0] Setup Time to REF_CLK rising	TXEN_SETUP	4			ns
TXEN, TXD[1:0] Hold Time from REF_CLK rising	TXEN_HOLD	2			ns
TD± after TXEN Assert	TXEN_TDATA				ns
TXD to TD± Steady State Delay	TXD_TDATA				ns

Notes:
1. TXD[1:0] provides valid data for each REF_CLK period while TX_EN is asserted.
2. Because the REF_CLK frequency is ten times the data rate in 10Mbps mode, the value on TXD[1:0] is valid so that TXD[1:0] can be sampled every tenth cycle, regardless of the starting cycle within the group and yield the correct frame data.

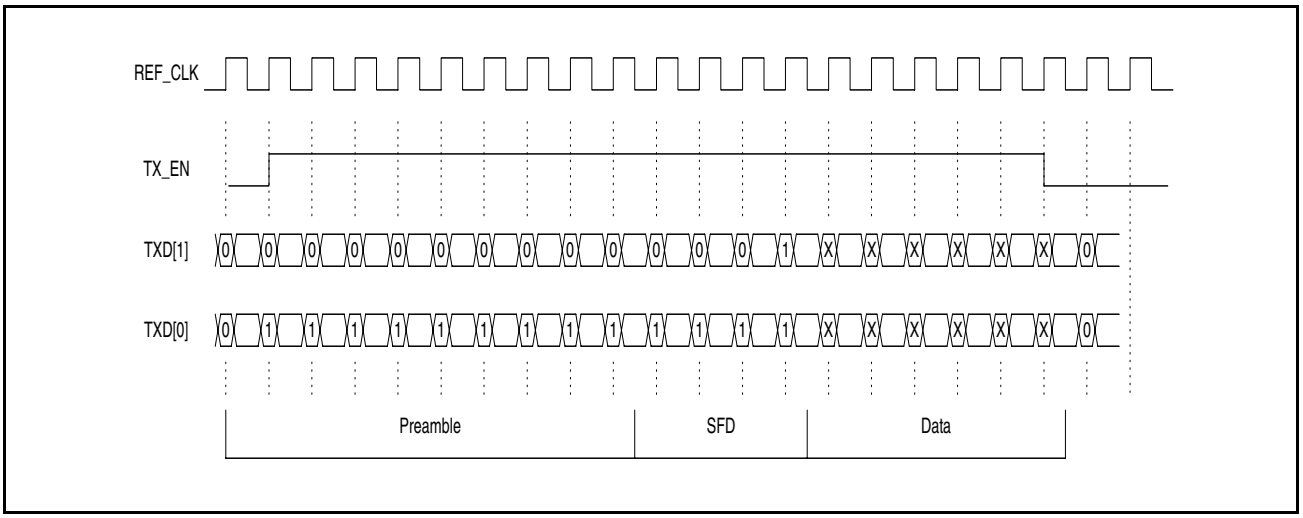


Figure 4: RMII Transmit Packet Timing

Table 32: RMII Receive Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
REF_CLK Cycle Time			20		ns
RXD [1:0] Output delay to REF_CLK Rising		2		16	ns
CRS_DV, RX_ER Delay from REF_CLK Rising		2		16	ns
CRS_DV Assert after RD±	RX_CRS_DV				ns
CRS_DV Deassert after RD±	RX_CRS_DV				ns
CRS_DV Deassert after RD±	RX_CRS_DV_EOP				ns
RD± to CRS_DV Steady State Delay	RX_RXD				ns

Notes:
1. Because the REF_CLK frequency is ten times the data rate in 10Mbps mode, the value on RXD[1:0] is valid so that RXD[1:0] may be sampled every tenth cycle, regardless of the starting cycle within the group and yield the correct frame data.
2. The receiver accounts for differences between the local REF_CLK and the recovered clock through use of sufficient elasticity buffering.
3. The output delay is with a load of 25PF which will accommodate a pcb trace length of over 12 inches.

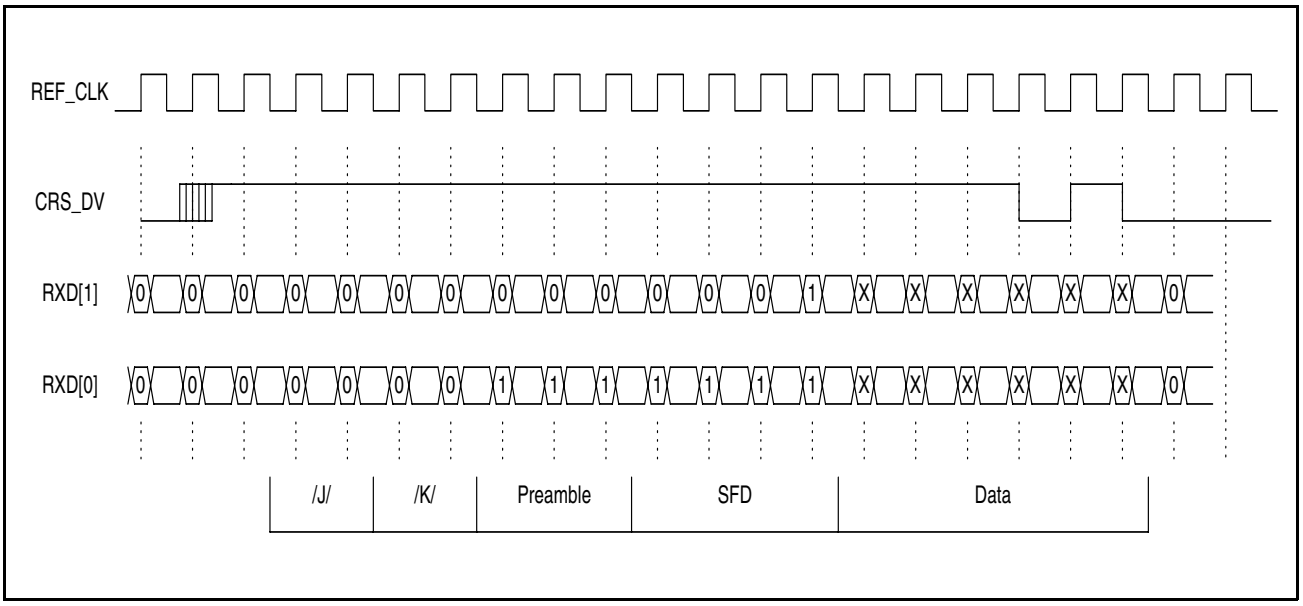


Figure 5: RMII Receive Packet Timing

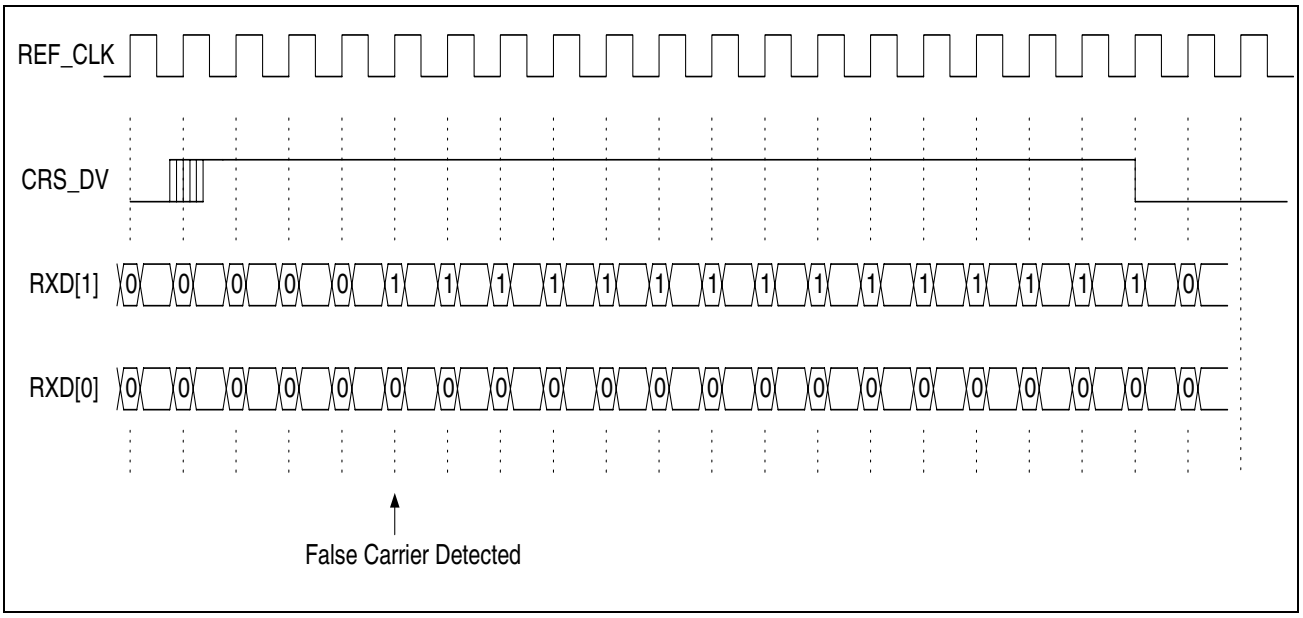


Figure 6: RMII Receive Packet with False Carrier

Table 33: SMII Receive Data Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
SRX Delay	SRX_DELAY	2		5	ns

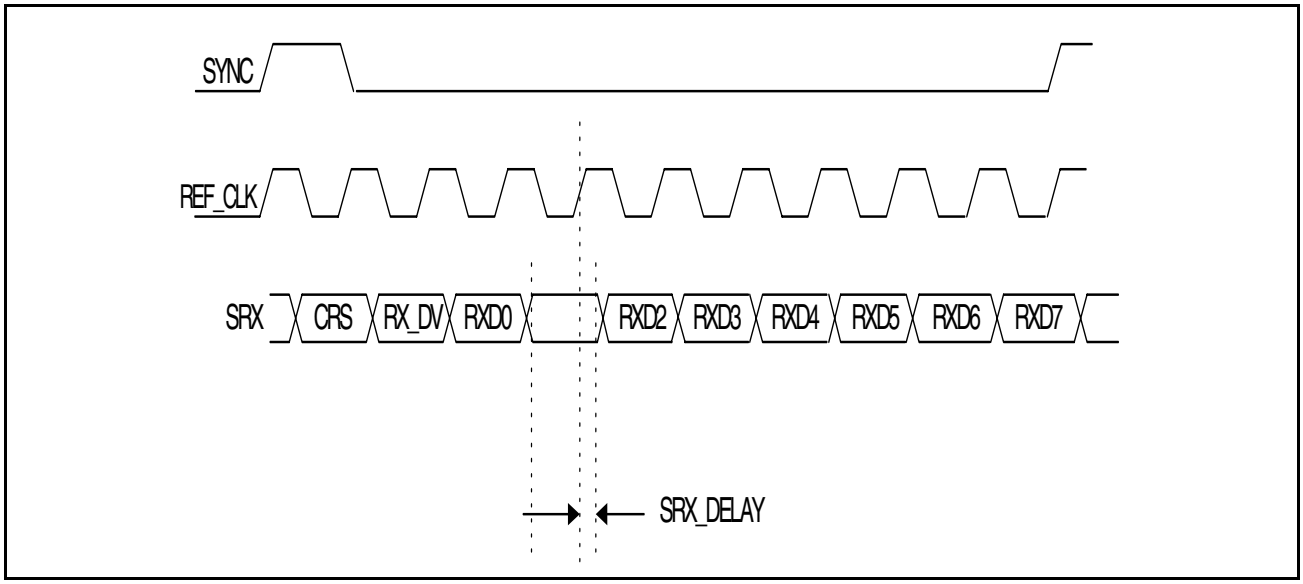


Figure 7: SMII Receive Data Timing

Table 34: SMII Transmit Data Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
STX Setup	STX_SETUP	1.5			ns
STX Hold	STX_HOLD	1.0			ns

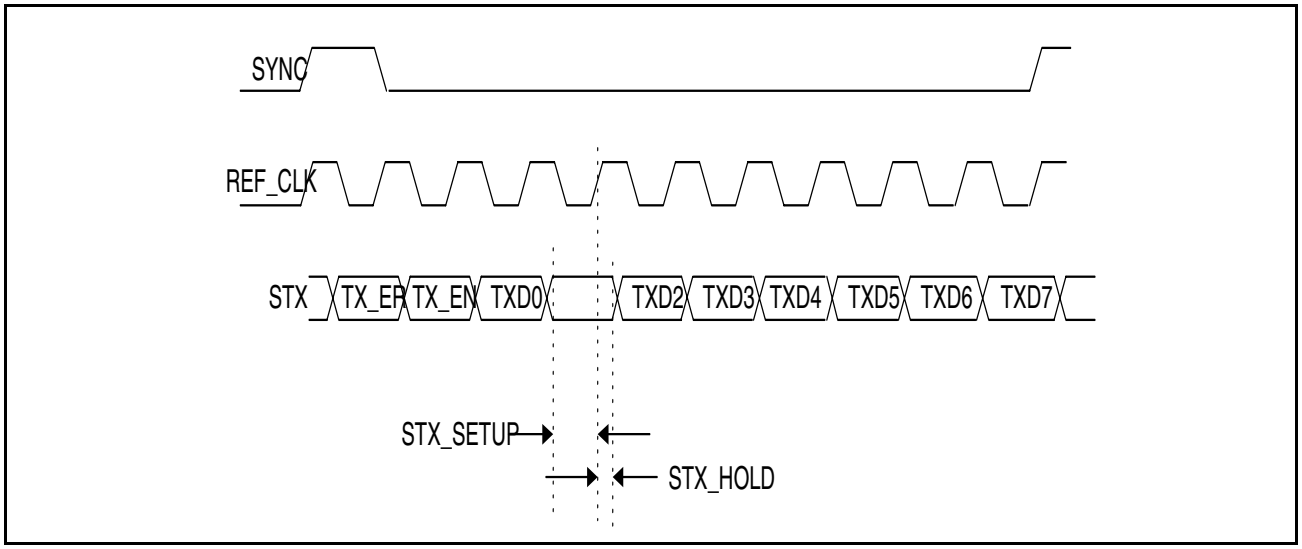


Figure 8: SMII Transmit Data Timing

Table 35: Loopback Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
TXD to RXD Steady State Propagation Delay			160		ns
LPBK Setup Time to TXEN					ns
LPBK Hold Time from TXEN					ns

Table 36: Auto-Negotiation Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Link Test Pulse Width			100		ns
FLP Burst Interval			16		ms
Clock Pulse to Clock Pulse			123		us
Clock Pulse to Data Pulse (Data = 1)			62.5		us

Table 37: LED Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
LED On Time (ACTLED)			80		ms
LED Off Time (ACTLED)			80		ms

Table 38: LED Timing (Serial Mode)

PARAMETER	SYMBOL	Min	TYP	MAX	UNIT
Shift Clock	SCLK		1		MHz
LED Serial Mode Data Set-Up	SDO_SETUP		200		ns
LED Serial Mode Data Hold	SDO_HOLD		200		ns
LED Frame Pulse Set-Up	SFRM_SETUP		200		ns
LED Frame Pulse Hold	SFRM_HOLD		200		ns

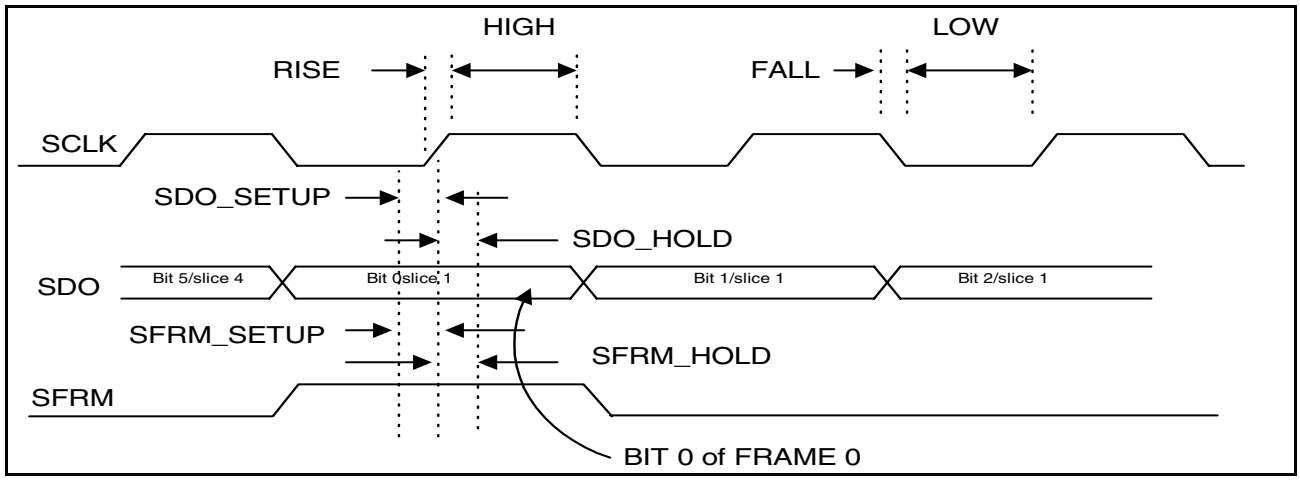


Figure 9: LED Timing (Serial Mode)

Table 39: LED Timing (Low Cost Serial Mode)

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
Shift Clock (LC Ser SCLK)	T_{cy}		80		ns
Data Set-up (LC ser SDO#)	T_S	20			ns
Data Hold	T_H	20			ns
Refresh	T_{REF}		5.2		ms

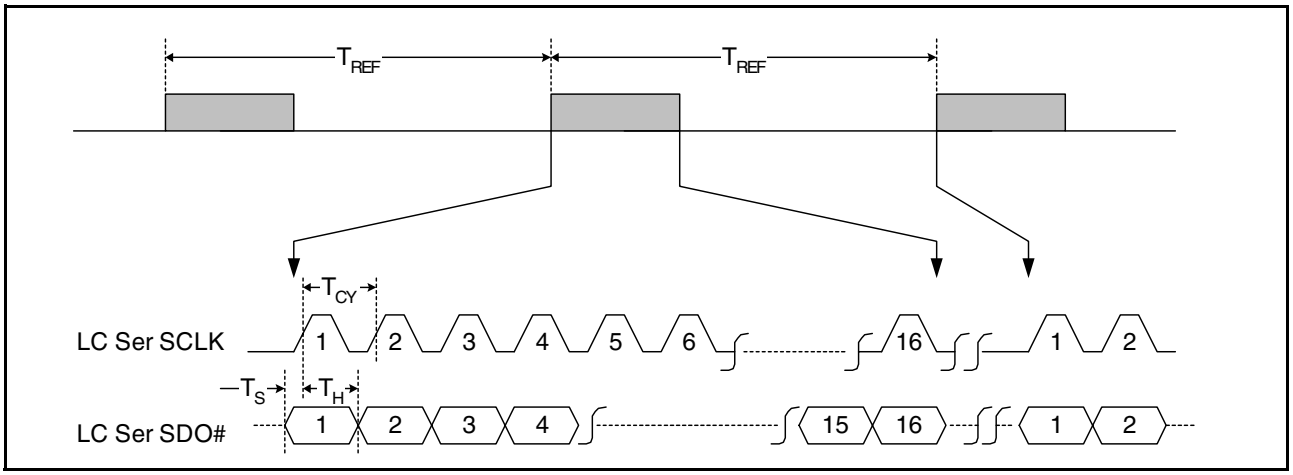


Figure 10: LED Timing (Low Cost Serial Mode)

Table 40: MII Management Data Interface Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
MDC Cycle Time		80			ns
MDC High/Low		30			ns
MDC Rise/Fall Time				10	ns
MDIO Input Setup Time to MDC rising		10			ns
MDIO Input Hold Time from MDC rising		10			ns
MDIO Output Delay from MDC rising				50	ns

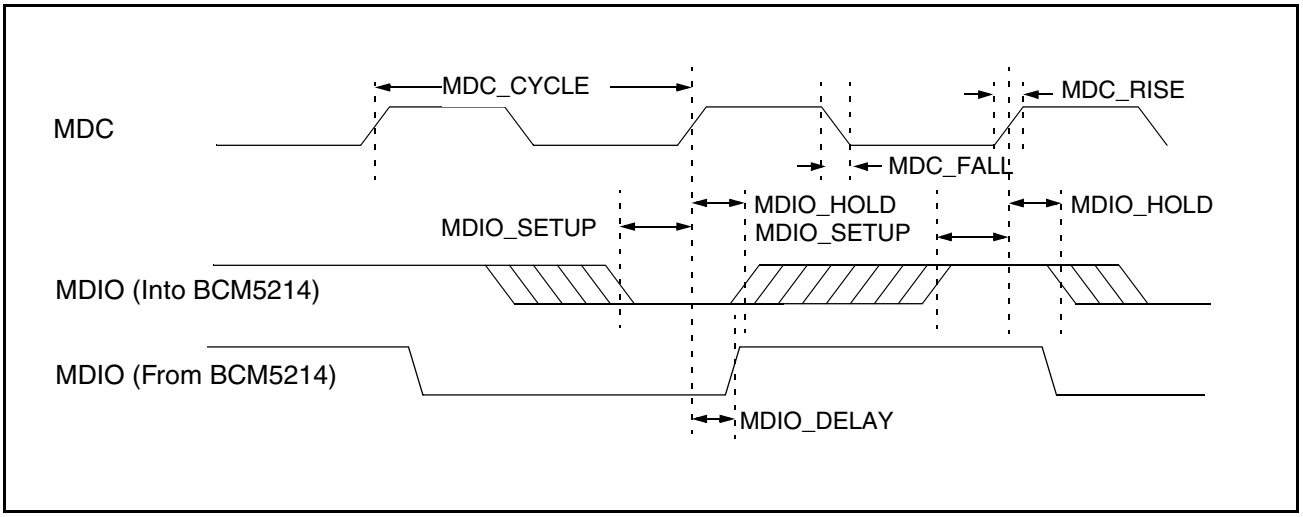


Figure 11: Management Interface Timing

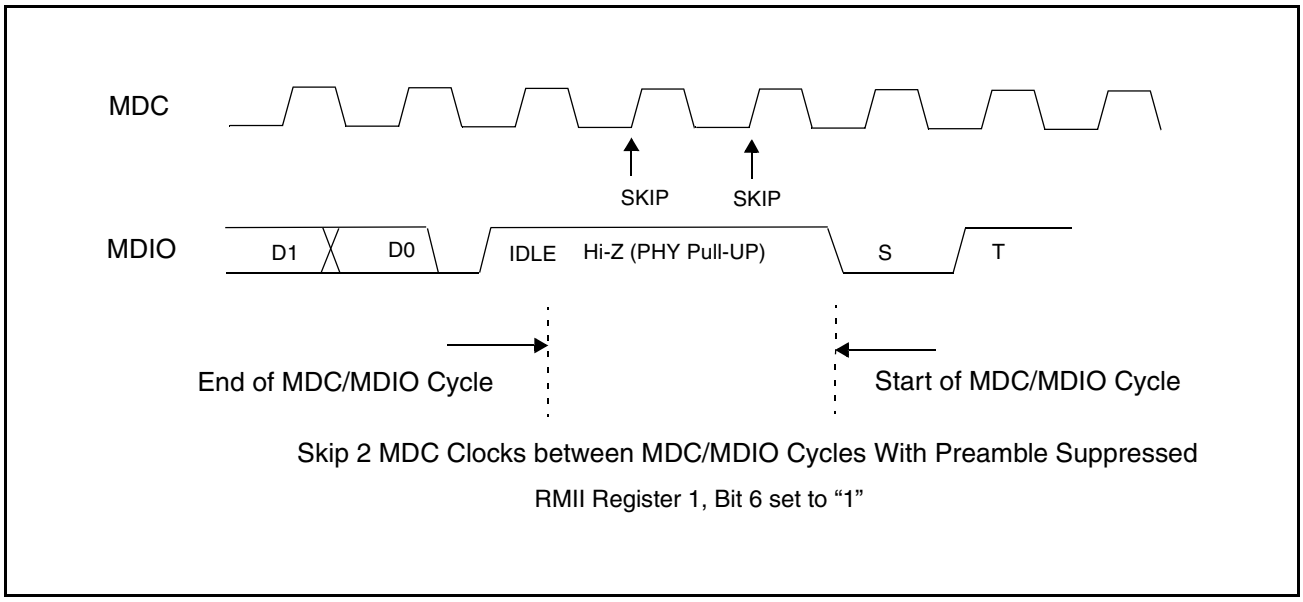


Figure 12: Management Interface Timing (with Preamble Suppression On)

Section 7: Electrical Characteristics

Table 41: Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITs
V_{DD}	Supply Voltage	GND – 0.3	3.6	V
V_I	Input Voltage	GND – 0.3	OVDD + 0.3	V
I_I	Input Current		±10	mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge		1000	V

Note:
These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

Table 42: Recommended Operating Conditions

SYM	PARAMETER	PINS	OPERATING MODES	MIN	MAX	UNITS
V_{DD}	Supply Voltage	AVDD, DVDD, OVDD		3.135	3.465	V
V_{IH}	High-Level Input Voltage	All Digital Inputs		2.0		V
V_{IL}	Low-Level Input Voltage	All Digital Inputs			0.8	V
V_{ICM}	Common Mode Input Voltage	RD± {1:4}	100BASE-TX	1.60	1.80	V
T_A	Ambient Operating Temperature			0	70	°C

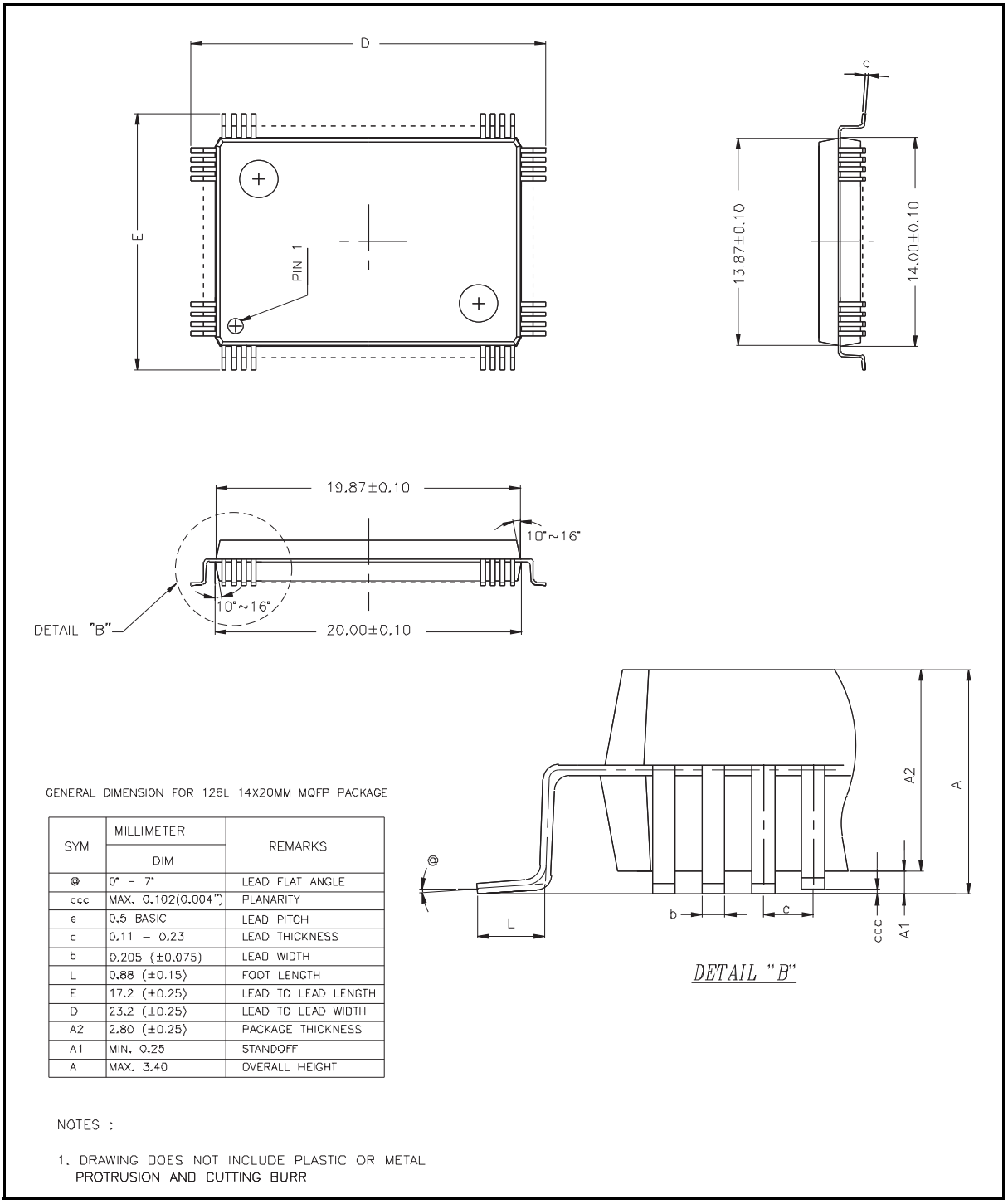
Table 43: Electrical Characteristics

SYM	PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Total Supply Current	AVDD, DVDD, OVDD	100BASE-TX		615		mA
V_{OH}	High-Level Output Voltage	All Digital Outputs Except LED Outputs	I_{OH} = –10 mA	2.4			V
		All LED Outputs	I_{OH} = –15 mA	2.4			V
		TD± {1:4}	driving loaded magnetics module			V_{DD} + 1.5	V
V_{OL}	Low-Level Output Voltage	All Digital Outputs	I_{OL} = 8 mA			0.4	V
		TD± {1:4}	driving loaded magnetics module	V_{DD} -1.5			V

Table 43: Electrical Characteristics (Cont.)

SYM	PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
I_I	Input Current	Digital Inputs w/ Pull-Up Resistors	V_I = DVDD			+100	µA
			V_I = DGND			-200	µA
		Digital Inputs w/ Pull-Down Resistors	V_I = DVDD			+200	µA
			V_I = DGND			-100	µA
		All other Digital Inputs	DGND ≤ V_I ≤ OVDD			±100	µA
I_{OZ}	High-Impedance Output Current	All Three-state Outputs	DGND ≤ V_O ≤ OVDD				µA
		All Open-drain Outputs	V_O = OVDD				µA
V_{BIAS}	Bias Voltage	VREF, RDAC		1.18		1.30	V

Section 8: Mechanical Information



GENERAL DIMENSION FOR 128L 14X20MM MQFP PACKAGE

SYM	MILLIMETER DIM	REMARKS
θ	0° – 7°	LEAD FLAT ANGLE
ccc	MAX. 0.102(0.004")	PLANARITY
e	0.5 BASIC	LEAD PITCH
c	0.11 – 0.23	LEAD THICKNESS
b	0.205 (±0.075)	LEAD WIDTH
L	0.88 (±0.15)	FOOT LENGTH
E	17.2 (±0.25)	LEAD TO LEAD LENGTH
D	23.2 (±0.25)	LEAD TO LEAD WIDTH
A2	2.80 (±0.25)	PACKAGE THICKNESS
A1	MIN. 0.25	STANDOFF
A	MAX. 3.40	OVERALL HEIGHT

NOTES :

1. DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION AND CUTTING BURR

Figure 13: 128-Pin MQFP Package

Section 9: Ordering Information

PART NUMBER	PACKAGE	AMBIENT TEMPERATURE
BCM5214	128 MQFP	0° to 70° C 32° to 158° F

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, California 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710