BCM5208R

10/100BASE-TX Quad-Φ™ Transceiver

GENERAL DESCRIPTION

The BCM5208R is a 0.35 micron CMOS die shrink of the BCM5208 Quad transceiver. The BCM5208R is a single-chip Quad 10/100BASE-TX transceiver targeted at Fast Ethernet switches. The device contains four full-duplex 10BASE-T/100BASE-TX Fast Ethernet transceivers, each of which performs all of the physical layer interface functions for 10BASE-T Ethernet on CAT 3, 4 or 5 unshielded twisted pair (UTP) cable and 100BASE-TX Fast Ethernet on CAT 5 UTP cable.

The BCM5208R is a highly integrated solution combining digital adaptive equalizers, ADCs, phase locked loops, line drivers, encoders, decoders and all the required support circuitry into a single monolithic CMOS chip. It complies fully with the IEEE 802.3u specification, including the Media Independent Interface (MII) and Auto-Negotiation subsections, providing compatibility with all industry standard Fast Ethernet Media Access Controller (MAC).

The effective use of digital technology in the BCM5208R design results in robust performance over a broad range of operating scenarios. Problems inherent to mixed-signal implementations, such as analog offset and on-chip noise, are eliminated by employing field-proven digital adaptive equalization and digital clock recovery techniques.

FEATURES

- Drop-in replacement for BCM5208 in 10BASE-T/100 BASE-TX applications
- 10BASE-T/100BASE-TX IEEE 802.3u Compliant
- Single-Chip Quad Physical Interface - MII to Magnetics
- Media Independent Interface (MII) for each Port
- Fully Integrated Digital Adaptive Equalizers
- 125-MHz Clock Generator and Timing Recovery
- On-Chip Multimode Transmit Waveshaping
- Edge-Rate Control to eliminate External Filters
- Integrated Baseline Wander Correction
- Full-Duplex Support
- IEEE 802.3u-Compliant Auto-Negotiation
- Shared MII Management Interface up to 12.5 Mbps
- Multiple Programmable Serial or Parallel LED Modes
- Interrupt Output Capability
- Loopback Mode for Diagnostics
- IEEE 1149.1 (JTAG) and NAND-Chain ICT support
- Low-Power Single-Supply 3.3 Volt CMOS Technology
- Compatibility with 3.3 Volt and 5.0 Volt I/O
- 208-Pin PQFP

APPLICATIONS

- Fast Ethernet Switches
- Multi-Port Adapter Cards

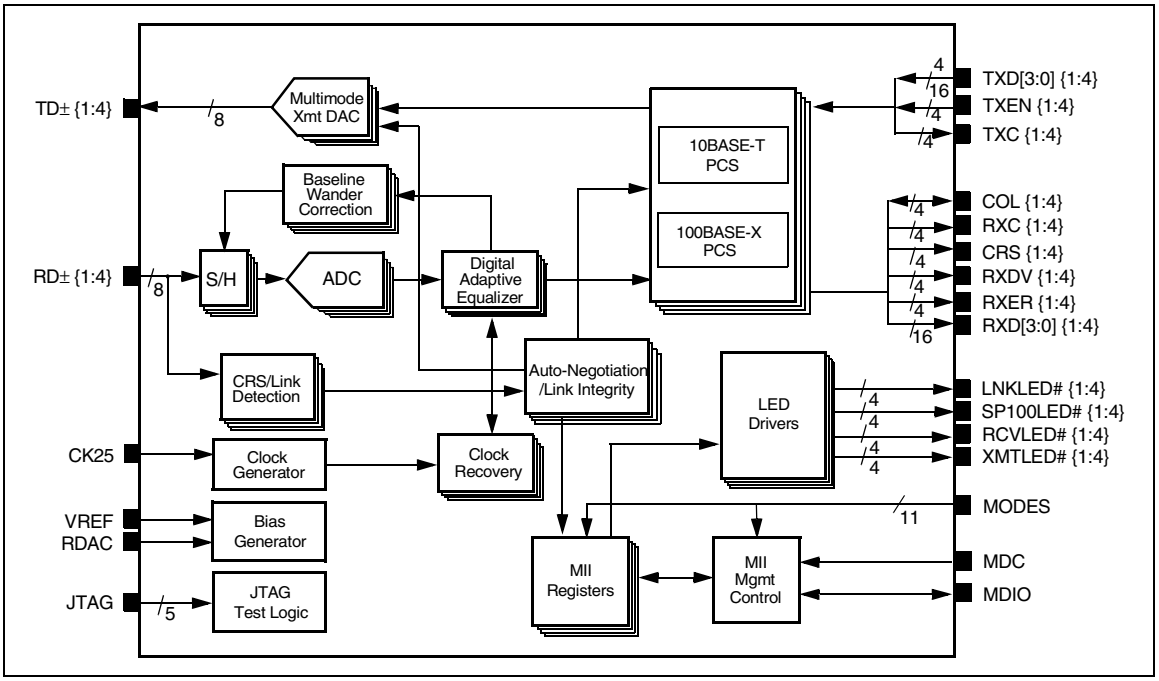

Figure 1: Functional Block Diagram

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REVISION HISTORY

REVISION #	DATE	CHANGE DESCRIPTION
01	7/30/99	Initial Release
02	2/14/00	Page 5 and 9: Hardware enabling of the serial LED mode requires LNKLED {1}, pin 203 and LNKLED#{4}, pin 159 to be low during power-on reset. Page 6, Table 3: Serial LED Mode bit framing, bit 4 is normal and full-duplex option would output COL status instead of “1”. Page 9: Low cost serial LED mode is enabled by ‘pull down’ of pin 178 instead of 198. Page 17: Added the requirement of 65th clock pulse on MDC for proper MDIO operation. Page 35: Included a note to explain FDX LED Enable default mode. Page 36: Included teo notes to explain the default values of bit 7, 4, 3, and bit 1 of register 1BH. Page 48: Added Low cost Serial LED mode timing diagram and table.

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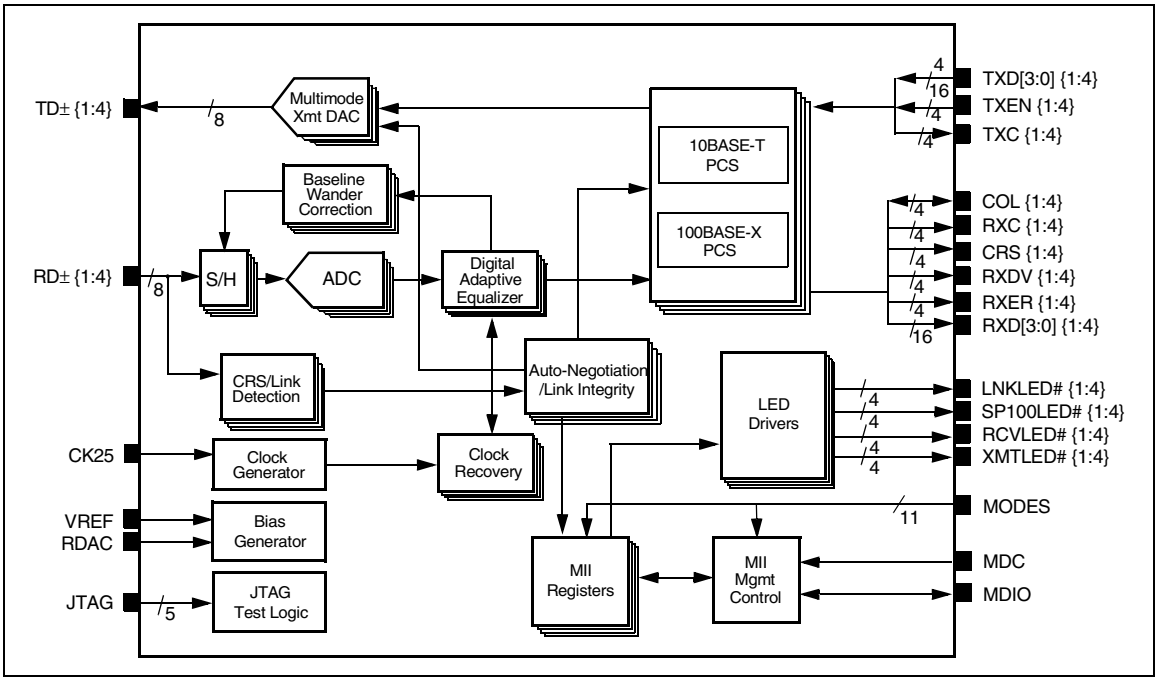

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TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES

LIST OF TABLES

LIST OF TABLES

Section 1: Functional Description

Overview

The BCM5208R is a single-chip device containing four independent Fast Ethernet transceivers. Each performs all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full- or half-duplex Ethernet on CAT 3, 4 or 5 cable.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor functions, Auto-Negotiation, and MII management functions. The BCM5208R can be connected to a MAC through the MII on one side and connects directly to the network media on the other side through isolation transformers for UTP modes. The BCM5208R is fully compliant with the IEEE 802.3 and 802.3u standards.

Encoder / Decoder

In 100BASE-TX mode, the BCM5208R transmits and receives a continuous data stream on twisted pair cable. When the MII transmit enable is asserted, nibble wide (4-bit) data from the transmit data pins is encoded into 5-bit code-groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1 on page 3. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following baseline wander correction, adaptive equalization, and clock recovery in TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

The 5-bit code groups are decoded into 4-bit data nibbles, as shown in Table 1. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM5208R asserts the MII RXER signal. The chip also asserts RXER for several other error conditions that improperly terminate the data stream. While RXER is asserted, the receive data pins will be driven with a 4-bit code indicating the type of error detected. The error codes are listed in Table 2.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

Link Monitor

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the “Link Fail” state where only idle codes will be transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the “Link Pass” state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD+/- pins for the presence of valid link pulses.

CARRIER SENSE

In 100BASE-X modes, carrier sense is asserted asynchronously on the CRS pin as soon as activity is detected in the receive data stream. RXDV is asserted as soon as a valid start-of-stream delimiter (SSD) is detected. Carrier sense and RXDV are deasserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. If carrier sense is asserted and a valid SSD is not detected immediately, then RXER is asserted in place of RXDV. A value of Eh (E hex) is driven on the receive data pins to indicate false carrier sense.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RD+/- input pins.

In half-duplex DTE mode, the BCM5208R additionally asserts carrier sense while transmit enable is asserted and the link monitor is in the “Pass” state. In full-duplex mode, CRS is only asserted for receive activity.

COLLISION DETECTION

In half-duplex mode, collision detect is asserted on the COL pin whenever carrier sense is asserted while transmission is in progress. Collision detect is never asserted in full-duplex mode.

AUTO-NEGOTIATION

The BCM5208R contains the ability to negotiate its mode of operation over the twisted pair link using the Auto-Negotiation mechanism defined in the IEEE 802.3u specification. Auto-Negotiation can be enabled or disabled by hardware or software control. When the Auto-Negotiation function is enabled, the BCM5208R automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5208R can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full and/or half-duplex. Each transceiver negotiates independently with its link partner, and chooses the highest level of operation available for its own link.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes interzonal interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5208R achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization and decision feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on CAT 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5208R achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self adapting to any quality of cable or cable length. In 10BASE-T operation the adaptive equalizer is bypassed.

ADC

Each receive channel has its own 6-bit, 125-MHz analog-to-digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low offset, high power supply noise rejection, fast settling time, and low bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clocks are locked to the 25-MHz clock input while the receive clocks are locked to the incoming data streams. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with different operating modes. The input data streams are sampled by the recovered clock from each port and fed synchronously to the respective digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5208R automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error. The baseline wander correction circuit is not required, andis therefore bypassed, in 10BASE-T mode.

Table 1: 4B5B Encoding

Name	*4B Code*	*5B Code*	*Meaning*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000*	11111	Idle
J	0101*	11000	Start-of-Stream Delimiter, Part 1
K	0101*	10001	Start-of-Stream Delimiter, Part 2
T	0000*	01101	End-of-Stream Delimiter, Part 1
R	0000*	00111	End-of-Stream Delimiter, Part 2
H	1000	00100	Transmit Error (used to force signalling errors)
V	0111	00000	Invalid Code
V	0111	00001	Invalid Code

Table 1: 4B5B Encoding (Cont.)

Name	4B Code	5B Code	Meaning
V	0111	00010	Invalid Code
V	0111	00011	Invalid Code
V	0111	00101	Invalid Code
V	0111	00110	Invalid Code
V	0111	01000	Invalid Code
V	0111	01100	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code
* Treated as invalid code (mapped to 0111) when received in data field.			

Table 2: Receive Error Encoding

Error type	RXD[3:0]
Stream cipher error—descrambler lost lock	0010
Link failure	0011
Premature end of stream	0110
Invalid code	0111
Transmit error	1000
False carrier sense	1110

MULTIMODE TRANSMIT DAC

The multimode transmit digital-to-analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components, thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC utilizes a current drive output that is well balanced and produces very low noise transmit signals.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted pair cable. The data is scrambled by *exclusive ORing* the NRZ signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by *exclusive ORing* it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler will “lock” to the scrambler state after detecting a sufficient number of consecutive idle code groups. The receiver will not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler will continuously monitor the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724µs, it will become unlocked, and the receive decoder will be disabled. The descrambler will always be forced into the unlocked state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 10BASE-T mode.

MII MANAGEMENT

Each transceiver within the BCM5208R contains an independent set of MII management registers. They share a single MDC/MDIO serial interface, Each transceiver has a unique address and must be accessed individually. The common base address for the group of four individual transceivers is defined by configuring the three external PHYAD address input pins.

INTERRUPT MODE

The BCM5208R can be programmed to provide an interrupt output from each of the four transceivers. The interrupt feature is disabled by default. When the interrupt capability is enabled by setting MII register 1Ah, bit 14, the XMTLED# pin becomes the INTR# pin and the RCVLED# pin becomes an activity pin named ACTLED#. The INTR# pins are open-drain and may be wire-ORed together. The status of each interrupt source is also reflected in Register 1Ah, bits 1, 2 and 3. The sources of interrupt are change in link, speed or full-duplex status. If any type of interrupt occurs, the Interrupt Status bit, Register 1Ah, bit 0, will be set.

In addition, each transceiver has its own register controlling the interrupt function.

If the interrupt enable bit is set to 0, no status bits will be set and no interrupts will be generated. If the interrupt enable bit is set to 1, the following conditions apply:

- If mask status bits are set to 0 and the interrupt mask is set to 1, status bits will be set but no interrupts generated.
- If mask status bits are set to 0 and the interrupt mask is set to 0, status bits and interrupts will be available.
- If mask status bits are set to 1 and the interrupt mask is set to 0, no status bits and no interrupts will be available.

Changes from “active” to “inactive” or vice versa will cause an interrupt. Setting Register 1Ah, bit 8 high will mask all interrupts, regardless of the settings of the individual mask bits.

LED MODES

The BCM5208R supports two types of Serial LED modes; Serial LED Mode and Low Cost Serial LED mode.

SERIAL LED MODES

Serial LED mode in the BCM5208R supports several modes for providing LED and interrupt information as a serial bit stream. The LED data is presented on a single pin, with a second pin providing a shift clock and a third providing framing. When the Serial LED mode is enabled, pin 182 (Ser SCLK) becomes the bit clock output, pin 183 (Ser SDO#) becomes the data output and pin 184 (Ser SFRM) provides the framing pulse.

After the Serial LED mode is enabled, several options for bit format become available. If no action is taken, bits are shifted out as shown in the top line of the table below. If the INTR bit (bit 14 of MII Register 1Ah) is set, data is shifted out as shown in the Interrupt row of the table. If the FDXLED bit (bit 15 of MII Register 1Ah) is set, data is shifted out as shown in the full-duplex row of the table.

In each mode, 24 bits comprise a frame. Bits are shifted in the order shown in the table below, with the bits in column marked BIT 0 leaving the chip first and the bits in column BIT 5 leaving the chip later in time. The sequence repeats four times between frame pulses to provide data for each PHY in the quad device. Bits are numbered from 0 to 5; frames are numbered from 1 to 4. Therefore, bit 0 of PHY 1 is the first bit out of the frame, and bit 5 of PHY 4 is the 24th bit out of the frame.

Data is shifted out on the falling edge of the shift clock, which is approximately 1 MHz. Data is valid on the rising edge of the shift clock. The framing pulse (Ser SFRM) is high during the bit 0 time of frame1. For timing information, see Table 37 on page 48.

Serial LED mode can be enabled in the hardware by holding LNKLED#{1}, pin 203 and LNKLED#{4}, pin 159 low during power-on reset.

Table 3: Serial LED Mode Bit Framing

Option	*MII REG 1Ah*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Normal	Bit 14 =0 Bit 15 =0	FDX	COL	Speed	Link	Transmit	Receive
Interrupt	Bit 14 =1 Bit 15 =0	FDX	Global Interrupt	Speed	Link	Slice Interrupt	Activity
Full-Duplex	Bit 14 =0 Bit 15 =1	FDX	COL	Speed	Link	FDX	Activity
A Global Interrupt indicates an interrupt from any of the four slices ORed together; a Slice Interrupt is from one of the four-PHYs.							

LOW COST SERIAL LED MODE

The BCM5208R also supports a low-cost serial LED mode. This serial mode can be enabled only by hardware. The low-cost serial LED mode is enabled when LNKLED#{3}, pin 178 (LC_SER_LED_EN#) is held low during power-on reset. When enabled, RCVLED#{1}, pin 201, sources the serial clock (LC Ser SCLK) and RCVLED#{3}, pin 180, sources the active low serial data (LC Ser SDO#}.

The LEDs are shifted out on the LC Ser SDO# in the following order: ActivityLED{1}, ActivityLED{2}, ActivityLED{3}, ActivityLED{4}, LinkLED{1}, LinkLED{2}, LinkLED{3}, LinkLED{4}, FullduplexLED{1}, FullduplexLED{2}, FullduplexLED{3}, FullduplexLED{4}, SpeedLED{1}, SpeedLED{2}, SpeedLED{3}, and SpeedLED{4}.

Section 2: Hardware Signal Definition Table

Table 4 provides the pin descriptions for the BCM5208R.

Table 4: Pin Descriptions

Pin	*Pin Label*	*Type*	*Description*
MEDIA CONNECTIONS			
60, 61	RD+ {1},RD- {1}	I_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
75, 74	RD+ {2},RD- {2}		
82, 83	RD+ {3},RD- {3}		
97, 96	RD+ {4},RD- {4}		
65, 66	TD+ {1},TD- {1}	O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
70, 69	TD+ {2},TD- {2}		
87, 88	TD+ {3},TD- {3}		
92, 91	TD+ {4},TD- {4}		
CLOCK			
6	CK25	I	**25 MHz Reference Clock Input.** This pin must be driven with a continuous 25 MHz clock in all operating modes.
MII INTERFACE			
27, 12, 145, 130	TXC {1:4}	O_{3S}	**Transmit Clock.** Delivers a 25-MHz output in 100BASE-X mode and a 2.5-MHz in 10BASE-T mode output.
33, 34, 35, 36	TXD[3:0] {1}	I_{PD}	**Transmit Data Input.** Nibble-wide transmit data is input on these pins synchronously to TXC. TXD[3] is the most significant bit.
208, 1, 9, 10	TXD[3:0] {2}		
150, 149, 148, 147	TXD[3:0] {3}		
124, 123, 122, 121	TXD[3:0] {4}		
37,11, 146,120	TXEN {1:4}	I_{PD}	**Transmit Enable.** Active high. Indicates that the data nibble is valid on TXD[3:0].
17, 190, 172, 140	RXC {1:4}	O_{3S}	**Receive Clock.** 25-MHz output in 100BASE-X mode and 2.5-MHz output in 10BASE-T mode. This clock is recovered from the incoming data on the cable inputs. RXC is a continuously running output clock resynchronized at the start of each incoming packet. This synchronization may result in an elongated period during one cycle when RXDV is low.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
19, 20, 21, 23	RXD[3:0] {1}	O_{3S}	**Receive Data Outputs.** Nibble-wide receive data is driven out of these pins synchronously to RXC. RXD[3] is the most significant bit.
192,193, 194, 195	RXD[3:0] {2}		
170,169, 168, 167	RXD[3:0] {3}		
138, 137, 136, 134	RXD[3:0] {4}		
24,196, 166, 133	RXDV {1:4}	O_{3S}	**Receive Data Valid.** Active high. Indicates that a receive frame is in progress, and that the data stream present on the RXD output pins is valid.
18, 191, 171, 139	RXER {1:4}	O_{3S}	**Receive Error Detected.** Active high. Indicates that there has been an error during a receive frame.
26, 206, 157, 131	CRS {1:4}	O_{3S}	**Carrier Sense.** Active high. Indicates traffic on link. In 100BASE-X modes, CRS is asserted when a non-idle condition is detected in the receive data stream and deasserted when idle or a valid end of stream delimiter is detected. In 10BASE-T mode, CRS is asserted when a valid preamble is detected and deasserted when end-of-file or an idle condition is detected. In DTE mode, CRS is also asserted during transmission of packets. CRS is an asynchronous output signal.
25, 205, 151, 132	COL {1:4}	I/O_{PD}	**Collision Detect.** In half-duplex modes, active high output indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous output signal.
118	MDIO	I/O_{PD}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
117	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies up to 12.5 MHz are supported.
119	RESET#	I_{PU}	**Reset.** Active Low. Resets the BCM5208R. Pin not included in NAND chain.
MODE			
38, 39, 40	PHYAD [4:2]	I_{PD}	**PHY Address Selects.** These inputs set the three MSBs for the MII management PHY addresses. The two LSBs, PHYAD [1:0], are internally wired to each of the four ports: PHYAD [00] = Port 1,..., PHYAD [11] = Port 4. Also serve as test control inputs along with TESTEN and NANDMD[1:0] to select the NAND-chain test mode.
42	FDXEN	I_{PD}	**Full-Duplex Mode Enable.** This pin's function applies only to DTE mode when Auto-Negotiation is disabled. The FDXEN pin is logically ORed with the MII Control register bit 8 to generate an internal full-duplex enable signal. When Auto-Negotiation is enabled, the FDXEN is ignored.

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Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
104	F100	I_{PU}	**Force 100BASE-X Operation.** When F100 is high and ANEN is low, all transceivers will be forced to 100BASE-X operation. When F100 is low and ANEN is low, all transceivers are forced to 10BASE-T operation. When ANEN is high, F100 has no effect on operation.
105	ANEN	I_{PU}	**Auto-Negotiation Enable.** When pulled high, Auto-Negotiation begins immediately after reset. When low, Auto-Negotiation is disabled after reset. Auto-Negotiation is always under software control (Register "0", bit 12).
116, 115	ER[1:0]	I_{PU}	**Transmit DAC Edge Rate Control.** These pins control the slew rate of each of the transmit DACs. The 10-90% rise time is set by the value on ER[1:0] as follows: 00 = 1 ns; 01 = 2 ns; 10 = 3 ns; 11 = 4 ns.
43	TESTEN	I_{PD}	**Test Enable.** Active-high test control input used along with NANDMD[1:0] and PHYAD[4:2] to select the NAND-chain test mode. This test mode is latched when TESTEN is pulsed high then low, with PHYA[4:2]=101 and NANDMD[1:0] = 11. This pin is not included in the NAND chain and must be pulled low or left unconnected during normal operation.
54, 53	NANDMD[1:0]	I_{PD}	**NAND Mode.** Active-high test control inputs used along with TESTEN and PHYA[4:2] to select the NAND-chain test mode. Both inputs must be driven high during latching of the test-mode. Must be pulled low or left unconnected during normal operation.
BIAS			
78	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of each of the transmit DACs. A resistor of 1.24 KΩ ±1% must be connected between the RDAC pin and AGND.
79	VREF	B	**Voltage Reference.** Low-impedance bias pin driven by the internal bandgap voltage reference. This pin must be left unconnected during normal operation.
LED			
203	LNKLED# {1}	O	**Link Integrity LED.** Active low. This output signal indicates the link status of the PHY. LNKLED is driven low when the link to the PHY is good. Serial LED mode is enabled by "pull-down" of pin 203, LNK LED#{1}, and pin 159, SER LED_EN#{2}, during reset. When the Serial LED mode is enabled, pin 184 becomes the Serial LED mode frame signal. Low cost serial LED mode is enabled by "pull-down" of pin 178 during reset.
184	LNKLED# {2} Ser SFRM		
178	LNKLED# {3} LC_SER_LED_EN#		
159	LNKLED# {4} SER_LED_EN#		
204, 185, 177, 158	SP100LED# {1:4}	O	**Speed 100 LED.** Driven low when operating in 100BASE-X modes and high when operating in 10BASE-T modes.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
202	XMTLED# {1} INTR# {1} FDXLED# {1}	O_{OD}	**Transmit Activity LED.** Active low output. The transmit activity LED is driven low for approximately 80ms each time there is transmit activity while in the link pass state. When INTR mode is enabled, the pin becomes an interrupt output. When FDX LED mode is enabled, the pin becomes FDXLED output. When the Serial LED mode is enabled, pin 183 becomes the Serial LED mode data output signal.
183	XMTLED# {2} INTR# {2} FDXLED# {2} Ser SDO#		
179	XMTLED# {3} INTR# {3} FDXLED# {3}		
160	XMTLED# {4} INTR# {4} FDXLED# {4}		
201	RCVLED# {1} ACTLED# {1} LC Ser SCLK	O_{OD}	**Receive Activity LED.** Active low output. The receive activity LED is driven low for approximately 80ms each time there is receive activity while in the link pass state. When in either INTR or FDXLED modes, this pin becomes ACTLED output for either receive or transmit activity. When the Serial LED mode is enabled, pin 182 becomes the Serial LED mode clock signal. When the low cost serial LED mode is enabled, pin 201 becomes Low cost serial LED mode clock signal and pin 180 becomes the data output signal.
182	RCVLED# {2} ACTLED# {2} Ser SCLK		
180	RCVLED# {3} ACTLED# {3} LC Ser SDO#		
161	RCVLED# {4} ACTLED# {4}		
JTAG			
99	TDI	I_{PU}	**Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
100	TDO	O_{3S}	**Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise.
101	TMS	I_{PU}	**Test Mode Select.** Single control input to the JTAG TAP Controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.
102	TCK	I_{PU}	**Test Clock.** Clock input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
103	TRST#	I_{PU}	**Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. Must be held low during power-up to insure the TAP Controller initializes to the test-logic-reset state. May be pulled low continuously when JTAG functions are not used.
44	DLLTEST	I_{PU}	**DLL Bypass Test Enable.** This pin is for factory testing only, and must be connected to DVDD or left floating.
POWER			
181	IVDD		**Input VDD.** +5.0V or +3.3V. If any of the inputs are driven to 5.0V, this pin must be connected to the 5.0V supply. If none of the inputs are driven above 3.3V, this pin can be connected to the 3.3V supply.
7	PLLVDD		Phase Locked Loop VDD
8	PLLGND		Phase Locked Loop GND
77	BIASVDD		Bias VDD
80	BIASGND		Bias GND
63, 72, 85, 94	AVDD		Analog VDD
62, 64, 67, 68, 71, 73, 84, 86, 89, 90, 93, 95	AGND		Analog GND
175, 198	DVDD		Digital Core VDD
176, 197	DGND		Digital Core GND
13, 129, 144,162, 173,200	OVDD		Digital Periphery (Output Buffer) VDD
3, 14, 22, 29, 50, 107, 128, 135,143, 154, 163, 174, 188, 199	OGND		Digital Periphery (Output Buffer) GND

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Section 3: Pinout Diagram

Figure 2 provides the pinout diagram for the BCM5208R.

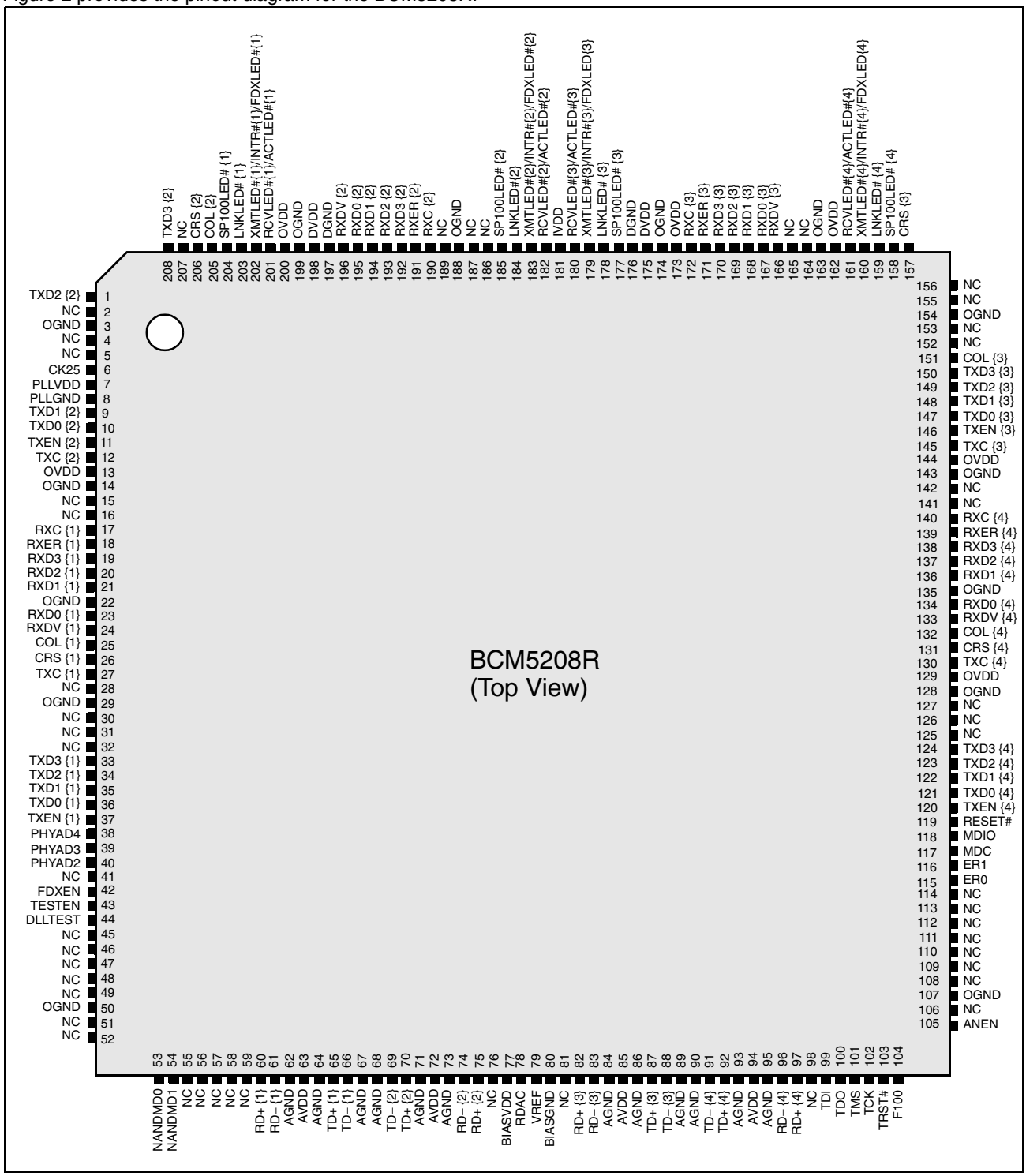


Figure 2: Pinout Diagram

BCM5208R AND BCM5208 COMPATIBILITY

The BCM5208R and BCM5208 are both packaged using a 208-pin PQFP. Common signals to both devices use the same pin configuration. Therefore, it is possible to use the BCM5208R in designs that use the BCM5208, if the following items are taken into consideration.

FUNCTIONS NOT SUPPORTED

The following functions are not supported in the BCM5208R:

- FX mode
- Repeater mode

SIGNALS NOT SUPPORTED

The following BCM5208 input signals are not supported in the BCM5208R:

- SD+/- {1:4} (100BASE-FX Signal Detect)
- RPTR (Repeater Mode Enable)
- TXJAM {1:4} (Transmit Jam)
- TXER {1:4} (Transmit Error)
- RXEN {1:4} (Receiver Enable)
- CIMEN (Carrier Integrity Monitor Enable)

ADDITIONAL FUNCTION SUPPORTED

- Next Page function is supported through MII register 07h and 08h.

POWER AND GROUND PINS

The BCM5208R uses fewer power and ground pins for DVDD, OVDD, AVDD, DGND, OGND, and AGND. However, the power and ground pins used by the BCM5208R are in the same locations as those used by the BCM5208.

USING A BCM5208R IN PLACE OF A BCM5208

If your design uses a BCM5208, you can use a BCM5208R in its place. Signals that are not supported by the BCM5208R do not affect other functions that are supported by the BCM5208, since these signals are not connected internally to the device. However, care should be taken when using a BCM5208R in place of a BCM5208 to ensure that unsupported signals connected from the circuit board to the device do not expect the device to function in a certain manner.

See Figure 3 on page 14, which shows the signals not supported in the BCM5208R and their locations.

Figure 3 provides the pinout compatibility diagram for the BCM5208 and BCM5208R. The pin signals shown with a strike-through represent the BCM5208-only signals.

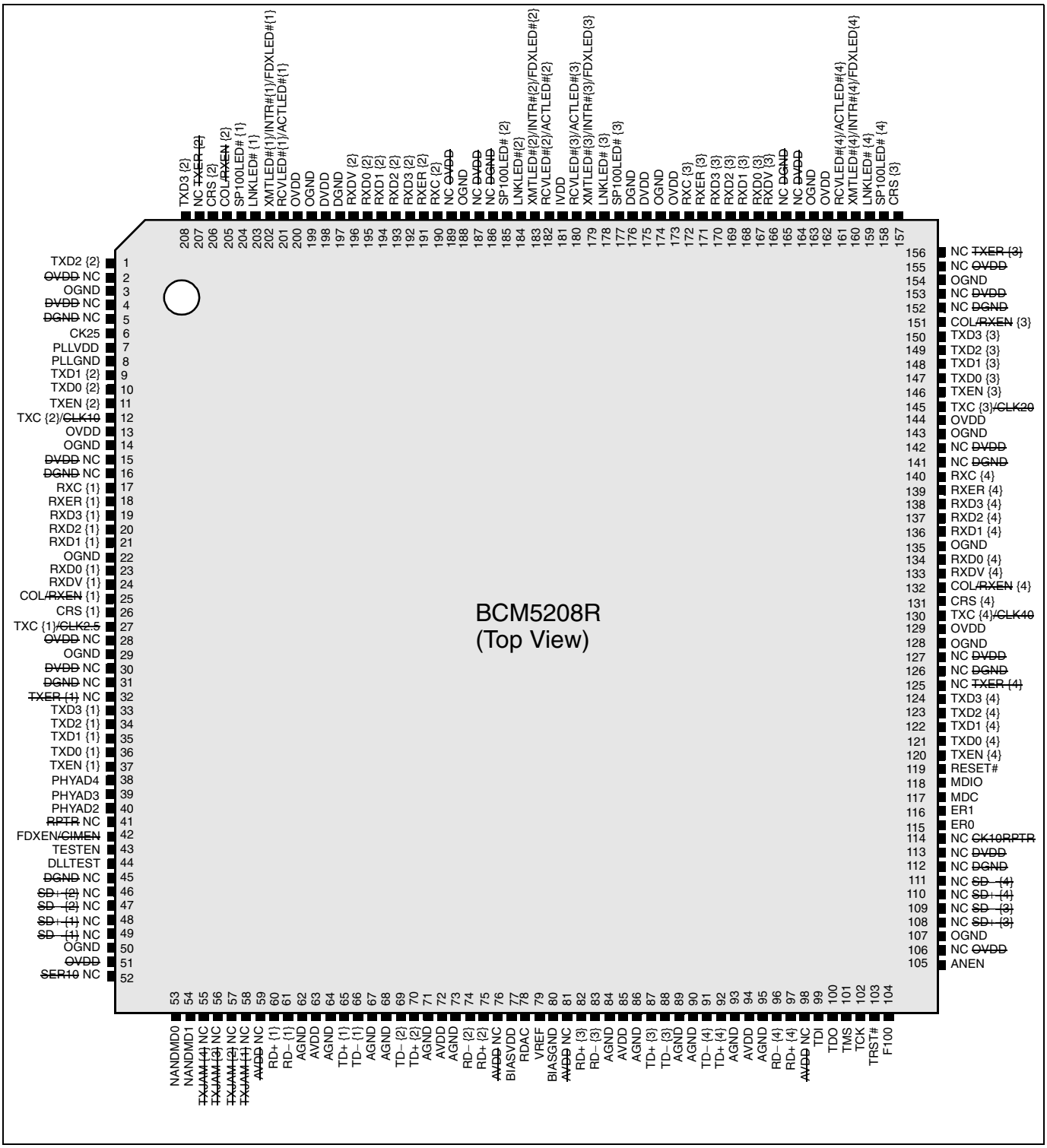


Figure 3: BCM5208/5208R Pinout Compatibility Diagram

Section 4: Operational Description

RESETTING THE BCM5208R

There are two ways to reset each transceiver in the BCM5208R. A hardware reset pin has been provided that resets all internal nodes inside the chip to a known state. The reset pulse must be asserted for at least 400 ns. Hardware reset should always be applied to a BCM5208R after power-up.

Each transceiver in the BCM5208R also has an individual software reset capability. To perform software reset, a 1 must be written to bit 15 of the transceiver's MII Control Register (see MII Register Definitions). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a 0 is written to the MII Control Register reset bit.

ISOLATE MODE

Each transceiver in the BCM5208R can be isolated from the MII. When a transceiver is put into isolate mode, all MII inputs (TXD[3:0] and TXEN) are ignored, and all MII outputs (TXC, COL, CRS, RXC, RXDV, RXER, and RXD[3:0]) are set at high impedance. Only the MII management pins (MDC, MDIO) operate normally. Upon resetting the chip, the isolate mode is off. Writing a "1" to bit 10 of the MII Control Register puts the transceiver into isolate mode. Writing a "0" to the same bit removes it from isolate mode.

LOOPBACK MODE

The loopback mode allows in-circuit testing of the BCM5208R chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. Incoming packets on the cable are ignored. Because of this, the COL pin is not normally activated during loopback mode. To test that the COL pin is actually working, the BCM5208R can be placed into collision test mode. This mode is enabled by writing a 1 to bit 7 of the MII Control Register. Asserting TXEN causes the COL output to go high, and deasserting TXEN causes the COL output to go low.

The loopback mode can be entered by writing a 1 to bit 14 of the MII Control Register. To resume normal operation, bit 14 of the MII Control Register must be 0.

Several function bypass modes are also supported, which can provide a number of different combinations of feedback paths during loopback testing. These bypass modes include bypass scrambler, bypass MLT3 encoder, and bypass 4B5B encoder.

FULL-DUPLEX MODE

The BCM5208R supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. The COL signal is never activated while in full-duplex mode. By default, each transceiver in the BCM5208R powers up in half-duplex mode.

When Auto-Negotiation is disabled, full-duplex operation can be enabled either by a pin (FDXEN) or by an MII register bit (Register "0" bit 8).

When Auto-Negotiation is enabled in DTE mode, full-duplex capability is advertised by default but can be overridden by a write to the Auto-Negotiation Advertisement Register (04h).

10BASE-T MODE

The same magnetics module is used to interface the twisted-pair cable in 10BASE-T mode and in 100BASE-TX mode. The data will be two-level Manchester coded instead of three-level MLT3 and no scrambling/descrambling or 4B5B coding is performed. Data and clock rates are decreased by a factor of 10, with the MII interface operating at 2.5 MHz.

PHY ADDRESS

Each transceiver in the BCM5208R has a unique PHY address for MII management. The addresses are set through the PHY address pins. The pins are latched at the trailing end of reset. Transceiver 1 has the address AAA00, where AAA = PHYAD[4:2]. Transceivers 2-4 have addresses AAA01, AAA10 and AAA11, respectively. Each time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

Section 5: Register Summary

MII Management Interface: Register Programming

The BCM5208R fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written to and read from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5208R at a rate of 0–12.5 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. See Table 5 for the fields in every MII read or write instruction frame.

Table 5: MII Management Frame Format

OPERATION	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE	DIRECTION
READ	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5208R Driven by BCM5208R
WRITE	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5208R

Preamble (PRE). Thirty two consecutive 1 bits must be sent through the MDIO pin to the BCM5208R to signal the beginning of an MII instruction. Fewer than thirty-two 1 bits will cause the remainder of the instruction to be ignored.

Start of Frame (ST). A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP). A READ instruction is indicated by 10, while a WRITE instruction is indicated by 01.

PHY Address (PHYAD). A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips. The BCM5208R supports the full 32-PHY address space with PHYAD[4:2] input-pin controlled and PHYAD[1:0] internally decoded to select one of the four transceivers.

Register Address (REGAD). A 5-bit Register Address follows, with the MSB transmitted first. The register map of the BCM5208R, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA). The next two bit times are used to avoid contention on the MDIO pin when a read operation is performed. For a write operation, 10 must be sent to the BCM5208R chip during these two bit times. For a read operation, the MDIO pin must be placed into High-Impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

Data. The last 16 bits of the frame are the actual data bits. For a Write operation, these bits are sent to the BCM5208R, whereas, for a Read operation, these bits are driven by the BCM5208R. In either case, the MSB is transmitted first.

When writing to the BCM5208R, the data field bits must be stable for 10 ns before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM5208R, the data field bits are valid after the rising-edge of MDC until the next rising-edge of MDC.

Idle. A high impedance state of the MDIO line. All tri-state drivers are disabled and the PHY's pull-up resistor pulls the MDIO line to logic 1. Note: At least one or more clocked idle states are required between frames.

Following are two examples of MII write and read instructions:

To put a transceiver with PHY address 00001 into Loopback mode, the following MII write instruction must be issued:

1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000 1...

To determine whether a PHY is in the link pass state, the following MII read instruction must be issued:

1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ 1...

For the MII read operation, the BCM5208R drives the MDIO line during the TA and Data fields (the last 17 bit times).

A final 65th clock pulse must be sent to close the transaction and to cause a write operation.

MII REGISTER MAP SUMMARY

Table 6 contains the MII register summary for each port of the BCM5208R. The register addresses are specified in hex form, and the name of register bits have been abbreviated. When writing to the reserved bits, always write a 0 value, and when reading from these bits, ignore the output value. Never write any value to an undefined register address. The reset value of the registers are shown in the INIT column.

Table 6: MII Register Map Summary

Addr	*Name*	*15*	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*INIT*
00h	**CONTROL**	Soft Reset	Loopback	Force10 0	AutoNeg Enable	Power Down	Isolate	Restart AutoNeg	Full Duplex	Collision Test	Reserved							3000h
01h	**STATUS**	T4 Capable (0)	TX FDX Capable	TX Capable	10BT FDX Capable	10BT Capable	Reserved				MF pream suppress	AutoNeg Complete	Reserved	AutoNeg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
02h	**PHYID HIGH**	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0040h
03h	**PHYID LOW**	0	1	1	0	0	0	Model # 0	1	0	0	1	1	Revision # 1	0	1	0	613Bh
04h	**AUTONEG ADVERTISE**	Next Page 0	Reserved	Remote Fault	Reserved Technologies		Pause	Adv T4 (0)	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	Advertised Selector Field [4:0] 0	0	0	0	1	01E1h
05h	**LINK PARTNER ABILITY**	LP Next Page	LP Acknowlg	LP Remote Fault	Reserved Technologies		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0]					0004h
06h	**AUTONEG EXPANSION**	Reserved											ParDet Fault	LP Next Pg Able	Next Pg Able	Page Recvd	LP Auto Neg Able	0004h
07h	**NEXT PAGE**	Next Page	Reserved	Message Page	Acknowledge2		Toggle	Message / Unformatted Code field										2001h
08h	**LP NEXT PAGE**	LP Next Page	Reserved	Message Page	Acknowledge2		Toggle	Message / Unformatted Code field										0000h
10h	**100BASE-X AUX CONTROL**	Reserved		Trans Disable	Reserved		Bypass 4B5B enc/dec	Bypass Scram/ Descram	Bypass NRZI enc/dec	Bypass rcv sym alignment	Baseline Wander cor Disable	Reserved						
11h	**100BASE-X AUX STATUS**	Reserved						Locked	Current 100 Link Status	Reserved		False Carrier Detected	Bad ESD Detected	RCV Error Detected	XMT Error Detected	Lock Error Detected	MLT3 Error Detected	
12h	**100BASE-X RCV ERROR COUNTER**	Reserved								Receive Error Counter								0000h
13h	**100BASE-X FALSE CARRIER COUNTER**	Reserved								False Carrier Sense Counter								0000h

Note 1: Reg 11h: Only bit 6 is qualified with TX Link. Other bits may be set in non-TX operation.

Table 6: MII Register Map Summary (Cont.)

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
14h	**Reserved**	Reserved																
15h	**Reserved**	Reserved																
16h	**Reserved**	Reserved																
17h	**PTEST**	Reserved - Write as Zero																0000h
18h	**AUXILIARY CONTROL/ STATUS**	Jabber Disable	Force Link	Reserved					TXDAC Power Mode	HSQ	LSQ	Edge Rate [1:0]		AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	003xh
19h	**AUXILIARY STATUS SUMMARY**	AutoNeg Complete	AutoNeg FLP-Link Good-Chk	AutoNeg Ack Detect	AutoNeg Ability Detect	AutoNeg Pause	AutoNeg HCD			AutoNeg ParDet Fault	LP Remote Fault	LP Page Rcvd	LP AutoNeg Able	SP100 Indicator	Link Status	Internal AutoNeg Enabled	Jabber Detect	0000h
1Ah	**INTERRUPT**	FDX LED Enable	INTR Enable	Reserved		FDX Mask	SPD Mask	Link Mask	INTR Mask	Reserved				FDX Change	SPD Change	Link Change	INTR Status	0F00h
1Bh	**AUXILLIARY MODE 2**	Reserved								Block 10BASE T Echo Mode	Traffic Meter LED Mode	Activity LED Force ON	Serial LED Mode	SQE Disable Mode	Reserved	Qual Parallel Detect Mode	Reserved	FF00h
1Ch	**10BASE-T AUX. ERROR & GENERAL STATUS**	Reserved					Manchstr Code Err (10BT)	EOF Err (10BT)	Polarity Err (10BT)	0	Revision # 0	1	Reserved	AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	00xxh
1Dh	**AUXILIARY MODE**	Reserved											Activity LEDs Force Inactive	Link LED Force Inactive	Reserved	Block TXEN Mode	Reserved	x000h
1Eh	**AUXILIARY MULTI-PHY**	HCD TX FDX	HCD T4 (0)	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart AutoNeg	AutoNeg Complete	FLP-Link Good-Chk	ACK Detect	Ability Detect	Super Isolate	Reserved		RXER Code Mode	0000h
1Fh	**BROADCOM Test**	Reserved - Do Not Write																

Note 2: Bit 0 is qualified with TX Link.

MII CONTROL REGISTER

The MII control register bit descriptions are shown in Table 7.

Table 7: MII Control Register (Address 00d, 00h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Reset	R/W (S/C)	1 = PHY reset 0= normal operation	0
14	Loopback	R/W	1 = loopback mode 0 = normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-Negotiation Enable	R/W	1 = auto-negotiation enable 0 = auto-negotiation disable	1
11	Power Down	RO	0 = normal operation	0
10	Isolate	R/W	1 = electrically isolate PHY from MII 0 = normal operation	0
9	Restart Auto-Negotiation	R/W (S/C)	1 = restart Auto-Negotiation 0 = normal operation	0
8	Duplex Mode	R/W	1 = full-duplex 0 = half-duplex	0
7	Collision Test Enable	R/W	1 = collision test mode enable 0 = collision test mode disable	0
6:0	Reserved	RO	Ignore when Read	0

Note: *R/W = Read/Write, RO = Read Only, SC = Self Clear*

Reset. To reset the BCM5208R by software control, a “1” must be written to bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and does not need to be cleared using a second MII write. Writes to other control register bits have no effect until the reset process is completed, which requires approximately 1 µs. Writing a 0 to this bit has no effect. Because this bit is self-clearing, after a few cycles from a write operation, it returns a 0 when read.

Loopback. The BCM5208R can be placed into loopback mode by writing a 1 to bit 14 of the Control Register. The loopback mode can be cleared by writing a 0 to bit 14 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in software-controlled loopback mode, otherwise it returns a 0.

Forced Speed Selection. If Auto-Negotiation is enabled, this bit has no effect on the speed selection. However, if Auto-Negotiation is disabled by software control, the operating speed of the BCM5208R can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a 1 to this bit forces 100BASE-X operation, while writing a 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection, including both hardware and software control, use bit 8 of the Auxiliary Control Register.

Auto-Negotiation Enable. Auto-Negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic 0, Auto-Negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of 0, Auto-Negotiation is disabled by software control. When Auto-Negotiation is disabled in this manner, writing a 1 to the same bit of the Control Register or resetting the chip re-enables Auto-Negotiation. Writing to this bit has no effect when Auto-Negotiation has been disabled by hardware control. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

Power Down. The BCM5208R does not implement a low power mode.

Isolate. Each individual PHY can be isolated from its Media Independent Interface by writing a 1 to bit 10 of the Control Register. All MII outputs are tri-stated and all MII inputs are ignored. Because the MII management interface is still active, the isolate mode can be cleared by writing a 0 to bit 10 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in isolate mode, otherwise it returns a 0.

Restart Auto-Negotiation. Bit 9 of the Control Register is a self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the Auto-Negotiation state machine. For this bit to have an effect, Auto-Negotiation must be enabled. Writing a 1 to this bit restarts the Auto-Negotiation, while writing a 0 to this bit has no effect. Because the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY Register.

Duplex Mode. By default, the BCM5208R powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a 1 to bit 8 of the Control Register while Auto-Negotiation is disabled. Half-duplex mode can be resumed by writing a 0 to bit 8 of the control register, or by resetting the chip.

Collision Test. The COL pin can be tested during loopback by activating the Collision Test mode. While in this mode, asserting TXEN causes the COL output to go high within 512 bit times. Deasserting TXEN causes the COL output to go low within 4 bit times. Writing a 1 to bit 7 of the Control Register enables the Collision Test mode. Writing a 0 to this bit or resetting the chip disables the Collision Test mode. When this bit is read, it returns a 1 when the Collision Test mode has been enabled, otherwise it returns a 0. This bit should only be set while in loopback test mode.

Reserved Bits. All reserved MII register bits must be written as 0 at all times. Ignore the BCM5208R output when these bits are read.

MII STATUS REGISTER

The MII status register bit descriptions are shown in Table 8.

Table 8: MII Status Register (Address 01d, 01h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore when read	0
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	0
4	Reserved	RO	Write as “0”, Ignore when read	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable 0 = Not Auto-Negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link Pass state) 0 = Link is down (Link Fail state)	0

Table 8: MII Status Register (Address 01d, 01h) (Cont.)

Bit	Name	R/W	Description	Default
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)*

100BASE-T4 Capability. The BCM5208R is not capable of 100BASE-T4 operation, and returns a 0 when bit 15 of the status register is read.

100BASE-X Full-Duplex Capability. The BCM5208R is capable of 100BASE-X full-duplex operation, and returns a 1 when bit 14 of the Status Register is read.

100BASE-X Half-Duplex Capability. The BCM5208R is capable of 100BASE-X half-duplex operation, and returns a 1 when bit 13 of the Status Register is read.

10BASE-T Full-Duplex Capability. The BCM5208R is capable of 10BASE-T full-duplex operation, and returns a 1 when bit 12 of the Status Register is read.

10BASE-T Half-Duplex Capability. The BCM5208R is capable of 10BASE-T half-duplex operation, and returns a 1 when bit 11 of the Status Register is read.

Reserved Bits. Ignore the BCM5208R output when these bits are read.

MF Preamble Suppression. This bit is the only writable bit in the Status Register. Setting this bit to a “1” allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When Preamble Suppression is enabled, only 2 preamble bits are required between successive Management Commands, instead of the normal 32.

Auto-Negotiation Complete. Bit 5 of the Status Register returns a 1 if the Auto-Negotiation process has been completed and the contents of registers 4, 5 and 6 are valid.

Auto-Negotiation Capability. The BCM5208R is capable of performing IEEE Auto-Negotiation, and will return a 1 when bit 4 of the Status Register is read, regardless of whether or not the Auto-Negotiation function has been disabled.

Link Status. The BCM5208R returns a 1 on bit 2 of the Status Register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the Link Pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the Link Pass state has been entered again.

Jabber Detect. 10BASE-T operation only. The BCM5208R returns a 1 on bit 1 of the Status Register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability. The BCM5208R supports extended capability registers, and returns a 1 when bit 0 of the Status Register is read. Several extended registers have been implemented in the BCM5208R, and their bit functions are defined later in this section.

PHY IDENTIFIER REGISTERS

The physical indentifier registers bit descriptions are shown in Table 9.

Table 9: PHY Indentifier Registers (Address 02d, 02h, 03d, and 03h)

Bit	*Name*	*R/W*	*Description*	*Value*
15:0	MII Address 00010	RO	PHYID HIGH	0040h
15:0	MII Address 00011	RO	PHYID LOW	613Bh
Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*				

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24 bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5208R part, 13h, and Broadcom Revision number, 01h, is placed into two MII Registers. The translation from OUI, Model Number and Revision Number to PHY Identifier Register occurs as follows:

- PHYID HIGH [15:0] = OUI[21:6]
- PHYID LOW [15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

The two most significant bits of the OUI are not represented (OUI[23:22]).

Table 9 shows the result of concatenating these values in order to form the MII Identifier Registers PHYID HIGH and PHYID LOW.

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 10 shows the auto-negotiation advertisement register bit descriptions.

Table 10: Auto-Negotiation Advertisement Register (Address 04d and 04h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Next Page Ability enabled 0 = Next Page Ability disabled	0
14	Reserved	RO	Ignore when read	
13	Remote Fault	R/W	1 = Transmit Remote Fault	0
12:11	Reserved Technologies	RO	Ignore when read	
10	Advertise Pause Capability	R/W	1 = Pause Operation for full-duplex	0
9	Advertise 100BASE-T4	R/W	0 = Do not advertise T4 capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X full-duplex 0 = Do not advertise 100BASE-X full-duplex	1
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex 0 = Do not advertise 10BASE-T full-duplex	1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	RO	Fixed value: indicates 802.3	00001
Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*				

Next Page. The BCM5208R supports Next Page Capability.

Remote Fault. Writing a 1 to bit 13 of the Advertisement Register sends a Remote Fault indicator to the Link Partner during Auto-Negotiation. Writing a 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

Reserved Bits. Ignore output when read.

Pause Operation for Full-Duplex Links. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

Advertisement Bits. Bits 9:5 of the Advertisement Register allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM5208R. By writing a 1 to any of the bits, the corresponding ability is transmitted to the Link Partner. Writing a 0 to any bit suppresses the corresponding ability from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset. Even though bit 9, Advertise 100BASE-T4 is writable, it should never be set because the BCM5208R is incapable of the T4 operation.

Selector Field. Bits 4:0 of the Advertisement register contain the fixed value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 11 shows the auto-negotiation link partner ability register bit descriptions.

Table 11: Auto-Negotiation Link Partner Ability Register (Address 05d, 05h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	LP Next Page	RO	Link Partner next page bit	0
14	LP Acknowledge	RO	Link Partner acknowledge bit	0
13	LP Remote Fault	RO	Link Partner remote fault indicator	0
12:11	Reserved Technologies	RO	Ignore when read	000
10	LP Advertise Pause	RO	Link Partner has Pause Capability	0
9	LP Advertise 100BASE-T4	RO	Link Partner has 100BASE-T4 capability	0
8	LP Advertise 100BASE-X FDX	RO	Link Partner has 100BASE-X FDX capability	0
7	LP Advertise 100BASE-X	RO	Link Partner has 100BASE-X capability	0
6	LP Advertise 10BASE-T FDX	RO	Link Partner has 10BASE-T FDX capability	0
5	LP Advertise 10BASE-T	RO	Link Partner has 10BASE-T capability	0
4:0	Link Partner Selector Field	RO	Link Partner selector field	00000

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

The values contained in the Auto-Negotiation Link Partner Ability Register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 5 of the MII Status Register.

Next Page. Bit 15 of the Link Partner Ability Register returns a value of 1 when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit.

Acknowledge. Bit 14 of the Link Partner Ability Register is used by Auto-Negotiation to indicate that a device has successfully received its Link Partner's Link Code Word.

Remote Fault. Bit 13 of the Link Partner Ability Register returns a value of 1 when the Link Partner signals that a remote fault has occurred. The BCM5208R simply copies the value to this register and does not act upon it.

Reserved Bits. Ignore when Read.

Pause. Indicates that the link partner pause bit is set.

Advertisement Bits. Bits 9:5 of the Link Partner Ability Register reflect the abilities of the Link Partner. A 1 on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time Auto-Negotiation is restarted or the BCM5208R is reset.

Selector Field. Bits 4:0 of the Link Partner Ability Register reflect the value of the Link Partner's selector field. These bits are cleared any time Auto-Negotiation is restarted or the chip is reset.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 12 shows the auto-negotiation expansion register bit descriptions.

Table 12: Auto-Negotiation Expansion Register (Address 06d and 06h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	RO	Ignore when Read	
4	Parallel Detection Fault	RO LH	1 = Parallel Detection fault 0 = No Parallel Detection fault	0
3	Link Partner Next Page Able	RO	1 = Link Partner has Next Page capability 0 = Link Partner does not have Next Page	0
2	Next Page Able	RO	1 = Next Page Able	1
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto-Negotiation Able	RO LH	1 = Link Partner has Auto-Negotiation capability 0 = Link Partner does not have Auto-Negotiation	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)*

Parallel Detection Fault. Bit 4 of the Auto-Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto-Negotiation state machine. For further details, please refer to the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Able. Bit 3 of the Auto-Negotiation Expansion Register returns a 1 when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Page Received. Bit 1 of the Auto-Negotiation Expansion Register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

Link Partner Auto-Negotiation Able. Bit 0 of the Auto-Negotiation Expansion Register returns a 1 when the Link Partner is known to have Auto-Negotiation capability. Before any Auto-Negotiation information is exchanged, or if the Link Partner does not comply with IEEE Auto-Negotiation, the bit returns a value of 0.

AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

Table 13 shows the auto-negotiation Next Page Transmit register bit descriptions.

Table 13: Next Page Transmit Register (Address 07d, 07h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Additional Next Page(s) will follow 0 = Last page	0
14	Reserved	R/W	Ignore when Read	0
13	Message Page	R/W	1= Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	0
10:0	Message/Unformatted Code Field	R/W		1

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Next Page. Indicates whether this is the last Next Page to be transmitted.

Message Page. Differentiates a Message Page from an Unformatted Page.

Acknowledge 2. Indicates that a device has the ability to comply with the message.

Toggle. Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field, which may contain an arbitrary value.

AUTO-NEGOTIATION LINK PARTNER (LP) NEXT PAGE TRANSMIT REGISTER

Table 14 shows the auto-negotiation link partner register bit descriptions.

Table 14: Next Page Transmit Register (Address 08d, 08h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	RO	1 = Additional Next Page(s) will follow 0 = Last page	0
14	Reserved	RO	Ignore when read	0
13	Message Page	RO	1= Message page 0 = Unformatted page	0
12	Acknowledge 2	RO	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	0
10:0	Message/Unformatted Code Field	RO		0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Next Page. Indicates whether this is the last Next Page.

Message Page. Differentiates a Message Page from an Unformatted Page.

Acknowledge 2. Indicates that Link Partner has the ability to comply with the message.

Toggle. Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field, which may contain an arbitrary value.

100BASE-X Auxiliary Control Register

The 100BASE-X auxiliary control register bit descriptions are shown in Table 15.

Table 15: 100BASE-X Auxiliary Control Register (Address 16d, 10h)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Write as 0, ignore when read	0
13	Transmit Disable	R/W	1 = transmitter disabled in PHY 0 = normal operation	0
12:11	Reserved	R/W	Write as 0, ignore when read	0
10	Bypass 4B5B Encoder/Decoder	R/W	1 = Transmit and receive 5B codes over MII pins 0 = Normal MII interface	0
9	Bypass Scrambler/Descrambler	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass NRZI Encoder/Decoder	R/W	1 = NRZI encoder and decoder is disabled 0 = NRZI encoder and decoder is enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = Baseline wander correction disabled 0 = Baseline wander correction enabled	0
5:0	Reserved	R/W	Write as 000000; ignore when read	000000

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Transmit Disable. The transmitter can be disabled by writing a 1 to bit 13 of MII Register 10h. When the transmitter is disabled, in the TX mode, the transmitter output (TD±) is forced into MLT3 zero value. The transmitter is enabled at reset, as well as when a 0 is written to this bit.

Bypass 4B5B Encoder/Decoder. The 4B5B encoder and decoder may be bypassed by writing a “1” to bit 10 of MII Register 10h. The transmitter sends 5B codes from the TXER and TXD[3:0] pins directly to the scrambler. TXEN is ignored and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places de-scrambled and aligned 5B codes onto the RXER and RXD[3:0] pins. CRS is still asserted when a valid frame is received.

Bypass Scrambler/Descrambler. The stream cipher function can be disabled by writing a 1 to bit 9 of MII register 10h. The stream cipher function can be re-enabled by writing a 0 to this bit.

Bypass NRZI Encoder/Decoder. The NRZI encoder and decoder can be bypassed by writing a 1 to bit 8 of the MII Register 10h, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) can be re-enabled by writing a 0 to this bit.

Bypass Receive Symbol Alignment. Receive symbol alignment can be bypassed by writing a 1 to bit 7 of MII Register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes are placed directly on the RXER and RXD[3:0] pins.

Baseline Wander Correction Disable. The baseline wander correction circuit can be disabled by writing a 1 to bit 6 of MII register 10h. The BCM5208R corrects for baseline wander on the receive data signal when this bit is cleared.

Reserved Bits. The Reserved bits of the 100BASE-X Auxiliary Control Register must be written as 0 at all times. Ignore the BCM5208R outputs when these bits are read.

100BASE-X AUXILIARY STATUS REGISTER

See Table 16 for an explanation of the bit descriptions for the 100BASE-X auxiliary status register.

Table 16: 100BASE-X Auxiliary Status Register (Address 17d, 11h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:10	Reserved	RO	Ignore when read	000000
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7:6	Reserved	RO	Ignore on Read	00
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 =No false carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = No ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 =No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)*

Locked. The PHY returns a 1 in bit 9 when the de-scrambler is locked to the incoming data stream. Otherwise it returns a 0.

Current 100BASE-X Link Status. The PHY returns a 1 in bit 8 when the 100BASE-X link status is good. Otherwise it returns a 0.

False Carrier Detected. The PHY returns a 1 in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise it returns a 0.

Bad ESD Detected. The PHY returns a 1 in bit 4 if an end of stream delimiter error has been detected since the last time this register was read. Otherwise it returns a 0.

Receive Error Detected. The PHY returns a 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise it returns a 0.

Transmit Error Detected. The PHY returns a 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise it returns a 0.

Lock Error Detected. The PHY returns a 1 in bit 1 if the de-scrambler has lost lock since the last time this register was read. Otherwise it returns a 0.

MLT3 Code Error Detected. The PHY returns a 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise it returns a 0.

100BASE-X Receive Error Counter

The 100BASE-X receive error counter increments each time the BCM5208R receives a non-collision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting Receive Errors until cleared. See Table 17 for the bit descriptions.

Table 17: 100BASE-X Receive Error Counter (Address 18d, 012h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as “00h”; ignore when read	00h
7:0	Receive Error Counter	R/W	Number of Non-Collision packets with Receive Errors since last read	00h

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

100BASE-X False Carrier Sense Counter

The 100BASE-X false carrier sense counter increments each time the BCM5208R detects a false carrier on the receive input. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting False Carrier Sense Errors until cleared. See Table 18 for the bit descriptions.

Table 18: 100BASE-X False Carrier Sense Counter (Address 19d, 13h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as “00h”, ignore when read	00h
7:0	False Carrier Sense Counter	R/W	Number of False Carrier Sense events since last read	00h

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

AUXILIARY CONTROL/STATUS REGISTER

Table 19 shows the auxiliary control/status register bit descriptions.

Table 19: Auxiliary Control/Status Register (Address 24d, 18h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Jabber Disable	R/W	1= Jabber function disabled in PHY 0 = Jabber function enabled in PHY	0
14	Link Disable	R/W	1= Link Integrity test disabled in PHY 0 = Link Integrity test is enabled in PHY	0
13:8	Reserved	RO	Ignore when read	000000
7:6	HSQ : LSQ	R/W	These two bits define the Squelch Mode of the 10BASE-T Carrier Sense mechanism: 00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Not allowed	00
5:4	Edge Rate [1:0]	R/W	00 = 1 ns 01 = 2 ns 10 = 3 ns 11 = 4 ns	11
3	Auto-Negotiation Indicator	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Jabber Disable. 10BASE-T operation only. Bit 15 of the Auxiliary Control Register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a 1 to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

Link Disable. Writing a 1 to bit 14 of the Auxiliary Control Register allows the user to disable the Link Integrity state machines and place the BCM5208R into forced Link Pass status. Writing a 0 to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

Test Mode. Active-high test mode control bit. Must be written with 0 for normal operation.

HSQ and LSQ. Extend or decrease the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high- and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5208R to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high

level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Edge Rate. Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode. These bits are logically ANDed with the ER[1:0] input pins to produce the internal edge-rate controls (Edge_Rate[1] AND ER[1], Edge_Rate[0] AND ER[0]).

Auto-Negotiation Indicator. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5208R. A combination of a 1 in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 3 of the Auxiliary Control Register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 0 when one of following cases is true:

- The ANEN pin is low AND the F100 pin is low.
- Bit 12 of the Control Register has been written 0 AND bit 13 of the Control Register has been written 0. When bit 8 of the Auxiliary Control Register is 0, the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. Bit 1 of the Auxiliary Control Register is a read-only bit that shows the true current operation speed of the BCM5208R. A 1 bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208R is always operating at 10BASE-T speed.

Full-Duplex Indication. Bit 0 of the Auxiliary Control Register is a read-only bit that returns a 1 when the BCM5208R is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY STATUS SUMMARY REGISTER

The auxiliary status summary register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bitsare included with their primary register descriptions in this document. Bits 10:8, the Auto-Negotiation HCD, are only set for full Auto-Negotiation process, and not for either Parallel Detection or forced-speed modes. Table 20 shows the bit descriptions.

Table 20: Auxiliary Status Summary Register (Address 25d, 19h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed	0
14	Auto-Negotiation Flp-Link Good-Check	RO LH	1 = Auto-Negotiation FLP-Link Good Check	0
13	Auto-Negotiation Acknowl-edge Detected	RO LH	1 = Auto-Negotiation acknowledge detected	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-Negotiation for link partner ability	0
11	Auto-Negotiation Pause	RO	BCM5208R and link partner Pause Operation bit set	0
10:8	Auto-Negotiation HCD	RO	000 = No Highest Common Denominator 001 = 10BASE-T 010 = 10BASE-T full-duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX full-duplex 11x = Undefined	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel Detection fault	0
6	Link Partner Remote Fault	RO		
5	Link Partner Page Received	RO LH	1 = New Page has been received	0
4	Link Partner Auto-Negotiation Able	RO	1 = Link Partner is Auto-Negotiation capable	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	0
2	Link Status	RO LL	1 = Link is up (link pass state)	0
1	Auto-Negotiation Enabled	RO	1 = Auto-Negotiation enabled	1
0	Jabber Detect	RO LL	1 = Jabber condition detected	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

INTERRUPT REGISTER

Table 21 shows the bit descriptions for the interrupt register.

Table 21: Interrupt Register (Address 26d, 1Ah)

Bit	*Name*	*R/W*	*DESCRIPTION*	*Default*
15	FDX LED Enable	R/W	Full-Duplex LED Enable	0, see Note A
14	INTR Enable	R/W	Interrupt Enable	0
13:12	Reserved	RO		0
11	FDX Mask	R/W	Full-Duplex Interrupt Mask	1
10	SPD Mask	R/W	SPEED Interrupt Mask	1
9	LINK Mask	R/W	LINK Interrupt Mask	1
8	INTR Mask	R/W	Master Interrupt Mask	1
7:4	Reserved	RO		0
3	FDX Change	RO LH	Duplex Change Interrupt	0
2	SPD Change	RO LH	Speed Change Interrupt	0
1	LINK Change	RO LH	Link Change Interrupt	0
0	INTR Status	RO LH	Interrupt Status	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Note A: *This bit defaults to a '1' only when LNKLED#{1} is pulled down and LNKLED#{4} is pulled up during power-on reset.*

FDX LED Enable. Setting this bit enables the FDX LED mode. Bits 14 and 15 of this register are mutually exclusive. Only one can be set at a time. When FDXLED mode is enabled, XMTLED# becomes FDXLED# and RCVLED# becomes ACTLED#.

Interrupt Enable. Setting this bit enables Interrupt Mode. Bits 14 and 15 of this register are mutually exclusive. Only one can be set at a time. When Interrupt Mode is enabled, XMTLED# becomes INTR# and RCVLED# becomes ACTLED#. If both bits 14 and 15 are set at the same time, the FDXLED# overrides the INTR# output, even though the interrupt's FDX, SPD, and LINK change status bits will behave as in normal interrupt operation.

FDX Mask. When this bit is set, changes in duplex mode do not generate an interrupt.

SPD Mask. When this bit is set, changes in operating speed do not generate an interrupt.

Link Mask. When this bit is set, changes in link status do not generate an interrupt.

Interrupt Mask. Master Interrupt Mask. When this bit is set, no interrupts are generated, regardless of the state of the other MASK bits.

FDX Change. A 1 indicates a change of duplex status since the last register read. A register read clears the bit.

SPD Change. A 1 indicates a change of speed status since the last register read. A register read clears the bit.

Link Change. A 1 indicates a change of link status since the last register read. A register read clears the bit.

Interrupt Status. Represents status of the INTR# pin. A 1 indicates that the interrupt mask is off and that one or more of the change bits are set. A register read clears the bit.

AUXILIARY MODE 2 REGISTER

The bit descriptions for auxiliary mode 2 register are shown in Table 22.

Table 22: Auxiliary Mode 2 (Address 27d, 1Bh)

Bit	*Name*	*R/W*	*DESCRIPTION*	*Default*
15:8	Reserved	RO	Ignore when read	FFh
7	Block 10BASE-T Echo Mode	R/W	1=10BASE-T half-duplex TXEN does not echo onto RXDV 0=10BASE-T half-duplex TXEN echoes onto RXDV	0, see Note B
6	Traffic Meter LED Mode	R/W	1=Traffic Meter LED Mode ON 0=Traffic Meter LED Mode OFF	0
5	Activity LED Force ON	R/W	1=Activity LEDs forced ON 0=Activity LEDs not forced	0
4	Serial LED Mode	R/W	1=Serial LED Mode enabled 0=Serial LED Mode disabled	0, see Note C
3	SQE Disable Mode	R/W	1=SQE not transmitted in 10BASE-T half-duplex 0=SQE transmitted in 10BASE-T half-duplex	0, see Note B
2	Reserved	RO	Ignore when read	0
1	Qual Parallel Detect Mode	R/W	1=Parallel Detect Qualification Mode ON 0=Parallel Detect Qualification Mode OFF	0, see Note B
0	Reserved	RO	Ignore when read	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Note B: *This bit defaults to a "1" if LNKLED#{1} is pulled low during power-on reset.*

Note C: *This bit defaults to a "1" if both LNKLED#{1} and LNKLED#{4} are pulled low during power-on reset.*

Block 10BASE-T Echo Mode. Default 0. When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal will not echo onto the RXDV pin. The TXEN will echo onto the CRS pin, and the CRS deassertion directly follow the TXEN deassertion.

Traffic Meter LED Mode. Default is 0. When asserted, the Receive and Transmit (Activity) LEDs (XMTLED# and RCV-LED# pins) do not blink based on the internal LED-CLK (approximately 80ms ON time). Instead, they blink based on the rate of Receive and Transmit activity. Each time a Receive or a Transmit operation occurs, the respective LED turns on for a minimum of 5ms. With light traffic, the LEDs blink at a low rate. During medium to heavy traffic (packets within 5ms of each other), the LEDs remain on.

Activity LED Force On. Default is 0. When asserted, the Receive and Transmit (Activity) LEDs (XMTLED# and RCV-LED# pins) are turned on. When 0, they have no effect on the Activity LEDs. The Activity Force ON bit has higher priority than Activity LED Force Inactive, bit 4, Register 1Dh.

Serial LED Mode. Default is 0. When asserted, the 4 slices' LED outputs will be serially shifted out on the 2nd slices' LED outputs.

The sequence of outputs for the different Serial modes are: FDX, Global Interrupt, Speed, Link, Slice Interrupt, Activity when the Interrupt mode is set; FDX, '1', Speed, Link, FDX, Activity when the FDXLED mode is set and, FDX, '1', Speed, Link, Transmit, Receive when neither Interrupt nor FDXLED modes are selected. When this bit is 0, the four LED outputs per slice are operated in parallel. See Table 3 on page 6 for more details.

SQE Disable Mode. Default is 0. When asserted, disables SQE pulses when operating in 10BASE-T half-duplex mode.

Qualified Parallel Detect Mode. This bit allows the Auto-Negotiation/Parallel Detection process to be qualified with information in the Advertisement Register. Default value is 0.

If this bit is not set, and the local BCM5208R device is enabled to Auto-Negotiate and the far-end device is a 10BASE-T or 100BASE-TX non-Auto-Negotiating legacy type, the local device Auto-Negotiate/Parallel detects the far-end device, regardless of the contents of its Advertisement Register, 04h.

If this bit is set, the local device compares the link speed detected to the contents of its Advertisement Register. If the particular link speed is enabled in the Advertisement register, the local device asserts link. If the link speed is disabled in this register, then the local device does not assert link and continues monitoring for a matching capability link speed.

10BASE-T Auxiliary Error and General Status Register

The bit descriptions for the 10BASE-T auxiliary error and general status register are shown in Table 23.

All error bits in the auxiliary error status register are read-only and are latched high. When certain types of errors occur in the BCM5208R, one or more corresponding error bits become "1". They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RXER output pin at the time the error occurs.

Table 23: 10BASE-T Auxiliary Error and General Status Register (Address 28d, 1Ch)

Bit	*Name*	*R/W*	*Description*	*Default*
15:11	Reserved	RO	Ignore when read	x
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T)	0
9	EOF Error	RO	1 = EOF detection error (10BASE-T)	0
8	Polarity Inversion	RO	1 = Channel Polarity Inverted 0 = Channel Polarity Correct	0
7:5	Revision	RO	Revision Number	001
4	Reserved	RO	Ignore when read	0
3	Auto-Negotiation Indication	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Manchester Code Error. Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

EOF Error. Indicates that the EOF (end of frame) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

Polarity. Reflects the Polarity status of the receive channel pair. The BCM5208R can automatically invert the polarity of the receive channel. No data errors are reported to indicate that the automatic polarity inversion is occurring. Instead, this bit returns a 1 whenever the polarity of the receive channel is inverted.

Revision. Read-only bits that return the revision number of the BCM5208R. The current revision is labelled 001.

Auto-Negotiation Indication. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5208R. A combination of a 1 in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 15 of the Auxiliary Mode Register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 0 when one of following cases is true:

- The ANEN pin is low AND the F100 pin is low.
- Bit 12 of the Control Register has been written 0 AND bit 13 of the Control Register has been written 0.

When bit 8 of the Auxiliary Control Register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. A read-only bit that shows the true current operation speed of the BCM5208R. A 1 bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208R is always operating at 10BASE-T speed.

Full-Duplex Indication. A read-only bit that returns a 1 when the BCM5208R is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY MODE REGISTER

The bit descriptions for the auxiliary mode register are shown in Table 24.

Table 24: Auxiliary Mode Register (Address 29d, 1Dh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	R/W	Write as “000h”, ignore when read	000h
4	Activity LEDs Force Inactive		1 = Disable XMT/RCV Activity LED outputs 0 = Allow XMT/RCV Activity LED outputs	0
3	Link LED Force Inactive		1 = Disable Link LED output 0 = Allow Link LED output	0
2	Reserved	RO		0
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0
0	Reserved	RO		0
Note: *Default is 00 for all PHYs if RPTR pin is high during reset*				

Activity LEDs Force Inactive. When set to 1, the XMTLED# and RCVLED# output pins are forced into their inactive state regardless of the mode (normal, FDX, Interrupt, or Serial) these outputs are configured to. When 0, XMTLED# and RCVLED# output pins are enabled.

Link LED Force Inactive. When set to 1, the Link LED output pin is forced into its inactive state. When 0, Link LED output is enabled.

Block TXEN Mode. When this mode is enabled, short IPGs of 1, 2, 3 or 4 TXC cycles all result in the insertion of two IDLEs before the beginning of the next packet's JK symbols.

AUXILIARY MULTIPLE PHY REGISTER

The bit descriptions for the auxiliary multiple PHY register are shown in Table 25.

Table 25: Auxiliary Multiple PHY Register (Address 30d, 1Eh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	HCD_TX_FDX	RO	1 = Auto-Negotiation result is 100BASE-TX full-duplex	0
14	HCD_T4	RO	0 = BCM5208R does not support 100BASE-T4 ability	0
13	HCD_TX	RO	1 = Auto-Negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-Negotiation result is 10BASE-T full-duplex	0
11	HCD_10BASE-T	RO	1 = Auto-Negotiation result is 10BASE-T	0
10:9	Reserved	RO	Ignore when read	0
8	Restart Auto-Negotiation	R/W (SC)	1 = Restart Auto-Negotiation process 0 = (No effect)	0
7	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process Completed 0 = Auto-Negotiation process not Completed	0
6	FLP-Link Good-Check	RO	1 = Auto-Negotiation FLP-Link Good-Check	0
5	Acknowledge Detected	RO	1 = Auto-Negotiation Acknowledge Detected	0
4	Ability Detect	RO	1 = Auto-Negotiation waiting for LP Ability	0
3	Super Isolate	R/W	1 = Super Isolate mode 0 = Normal Operation	0
2:1	Reserved	R/W	Write as "00", ignore when read	00
0	RXER Code Mode	R/W	1 = Enable RXER Code Mode 0 = Disable RXER Code Mode	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

HCD Bits. Bits 15:11 of the Auxiliary Multiple PHY Register are five read-only bits that report the Highest Common Denominator (HCD) result of the Auto-Negotiation process. Immediately upon entering the Link Pass state after each reset or Restart Auto-Negotiation, only one of these five bits is 1. The Link Pass state is identified by a 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time Auto-Negotiation is restarted or the BCM5208R is reset. Note that for their intended application, these bits uniquely identify the HCD only after the first Link Pass after reset or restart of Auto-Negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the Link Partner is different, more than one of the above bits may be active. These bits are only set for full Auto-Negotiation hand-shake, and not for Parallel Detection of Forced speed modes. Note that bit 14, HCD_T4, is never set in the BCM5208R.

Restart Auto-Negotiation. A self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, Auto-Negotiation must be enabled. Writing a 1 to this bit restarts Auto-Negotiation. Since the bit is self-clearing, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Control Register.

Auto-Negotiation Complete. This read-only bit returns a 1 after the Auto-Negotiation process has been completed. It remains 1 until the Auto-Negotiation process is restarted, a Link Fault occurs, or the chip is reset. If Auto-Negotiation is disabled or the process is still in progress, the bit returns a 0.

FLP-Link Good-Check. This read-only bit returns a 1 when the Auto-Negotiation arbitrator state machine has entered the FLP-link Good-Check state. It remains this value until the Auto-Negotiation process is restarted, a Link Fault occurs, Auto-Negotiation is disabled, or the BCM5208R is reset.

Acknowledge Detected. This read-only bit is set to 1 when the Arbitrator state machine exits the Acknowledged Detect state. It remains high until the Auto-Negotiation process is restarted, or the BCM5208R is reset.

Ability Detect. This read-only bit returns a 1 when the Auto-Negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the Auto-Negotiation process begins, and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns a 0 any time the Auto-Negotiation state machine is not in the Ability Detect state.

Super Isolate. Writing a 1 to this bit places the BCM5208R into the Super Isolate mode. Similar to the Isolate mode, all MII inputs are ignored, and all MII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5208R to coexist with another PHY on the same adapter card, with only one being activated at any time.

RXER Code Mode. Writing a 1 to bit 0 of the Auxiliary Mode Register enables the RXER Code mode during 10BASE-T operation. In this mode, when a receive data error occurs, indicated by pins RXDV=1 and RXER=1, the RXD[3:0] bus contains a non-zero 4-bit encoded value indicating the type of error. This feature provides the user with more detailed information regarding the status of the system. Writing a 0 to this bit or resetting the chip restores normal operation.

Note that this mode does not disrupt normal communication with the MAC layer, and can safely be used at all times. Also, please note that the RXER Code mode is not available in 10BASE-T Serial mode. In 100BASE-X operation, the RXER code mode is always active. See Table 2 on page 4 for more information.

BROADCOM TEST REGISTER

The Broadcom test register bits are reserved and should never be written.

Table 26: Broadcom Test (Address 31d, 1Fh)

Bit	*Name*	*R/W*	*DESCRIPTION*	*Default*
Reserved—Do Not Write				

Section 6: Timing and AC Characteristics

All MII Interface pins comply with IEEE 802.3u timing specifications (See Reconciliation Sub-layer and Media Independent Interface in IEEE 802.3u timing specifications). All digital output timing is specified at C_L = 30 pF.

Output rise/fall times are measured between 10% and 90% of the output signal swing. Input rise/fall times are measured between V_{IL} max. and V_{IH} min. Output signal transitions are referenced to the midpoint of the output signal swing. Input signal transitions are referenced to the midpoint between V_{IL} max. and V_{IH} min. See Table 27 and Table 28 for timing parameters. See Figure 4 on page 41 for an illustration of clock and reset timing.

Table 27: Clock Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
CK25 Cycle Time	CK_CYCLE	39.998	40	40.002	ns
CK25 High/Low Time	CK_HI CK_LO	18	20	22	ns
CK25 Rise/Fall Time	CK_EDGE	–	–	4	ns

Table 28: Reset Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Reset Pulse Length with stable CK25 Input	RESET_LEN	400	–	–	ns
Activity after end of Reset	RESET_WAIT	100	–	–	µs
RESET Rise/Fall Time	RESET_EDGE	–	–	10	ns

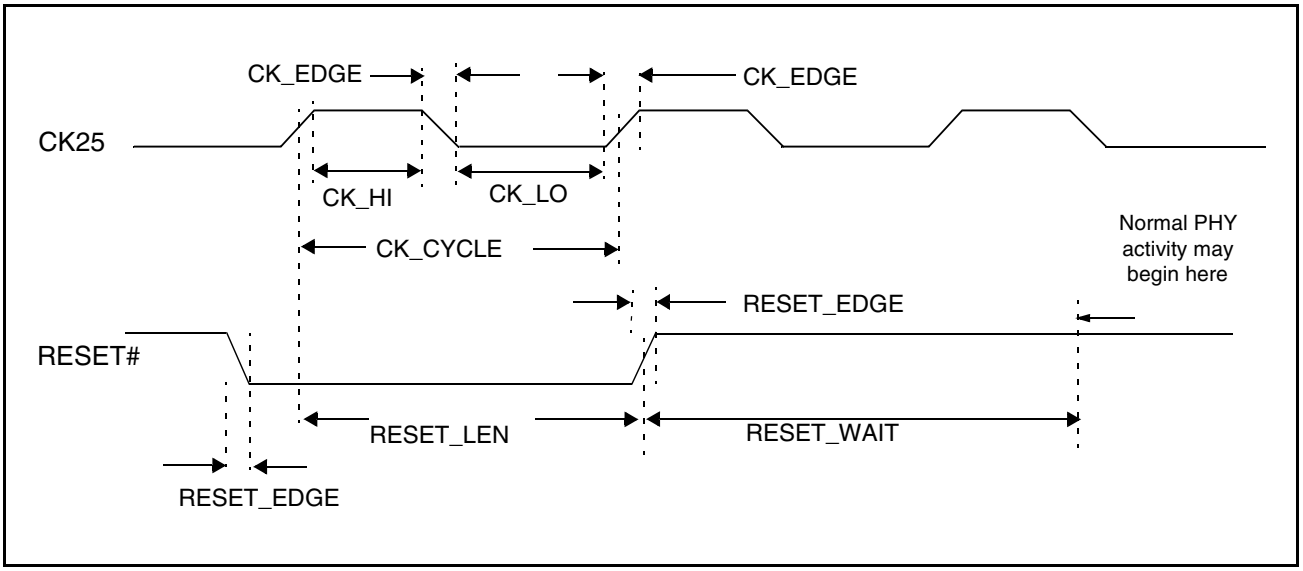


Figure 4: Clock and Reset Timing

Table 29 provides the parameters for 100BASE-X transmit timing. Figure 5 on page 42 illustrates 100BASE-TX transmit start of packet timing and Figure 6 on page 43 shows the 100BASE-TX transmit end of packet timing.

Table 29: 100BASE-X Transmit Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
TXC Cycle Time			40		ns
TXC High/Low Time		16	20	24	ns
TXC Rise/Fall Time		2	–	5	ns
TXEN, TXER, TXD[3:0] Setup Time to TXC rising	TXEN_SETUP	12	–		ns
TXEN, TXER, TXD[3:0] Hold Time from TXC rising	TXEN_HOLD	0	–	–	ns
TD± after TXEN Assert	TXEN_TDATA	60	–	80	ns
TXD to TD± Steady State Delay	TXD_TDATA	60	–	80	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	–	30	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	–	30	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL	–	–	30	ns
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP	–	–	30	ns
TXEN, TXER, TXD[3:0] Setup Time to CK25 rising		2	–	--	ns
TXEN, TXER, TXD[3:0] Hold Time from CK25 rising		10	–	–	ns

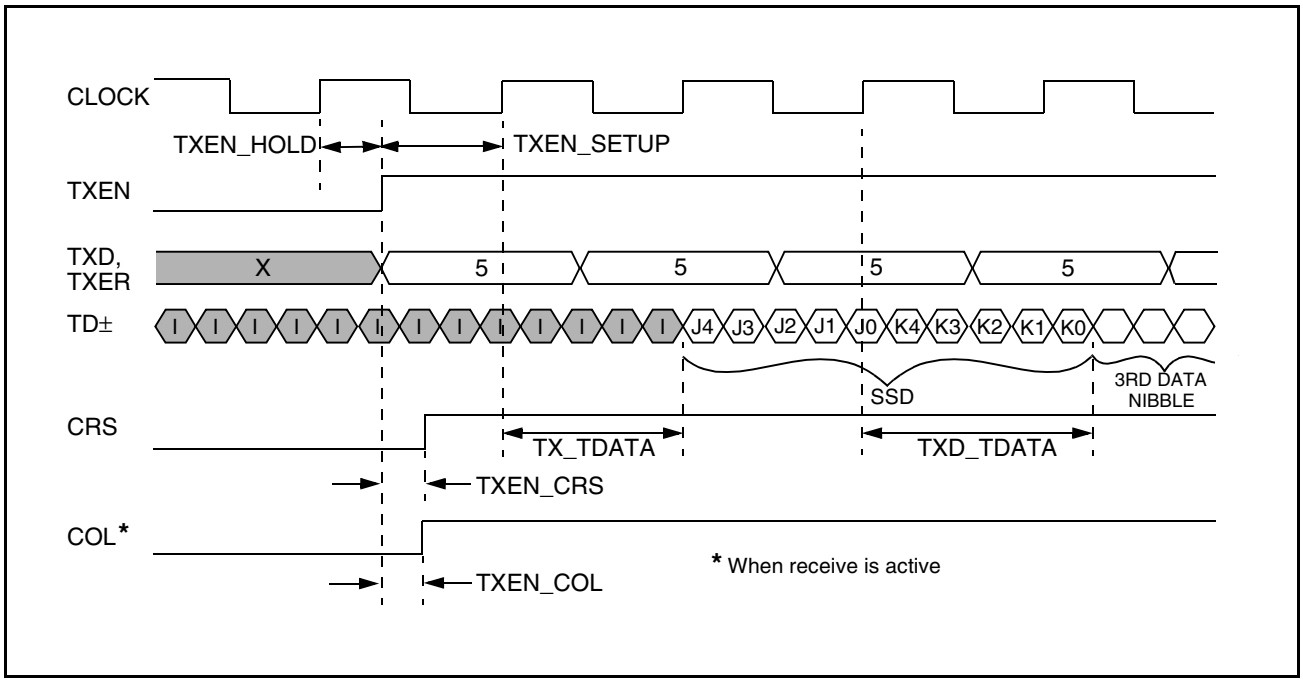


Figure 5: Transmit Start of Packet Timing (100BASE-TX)

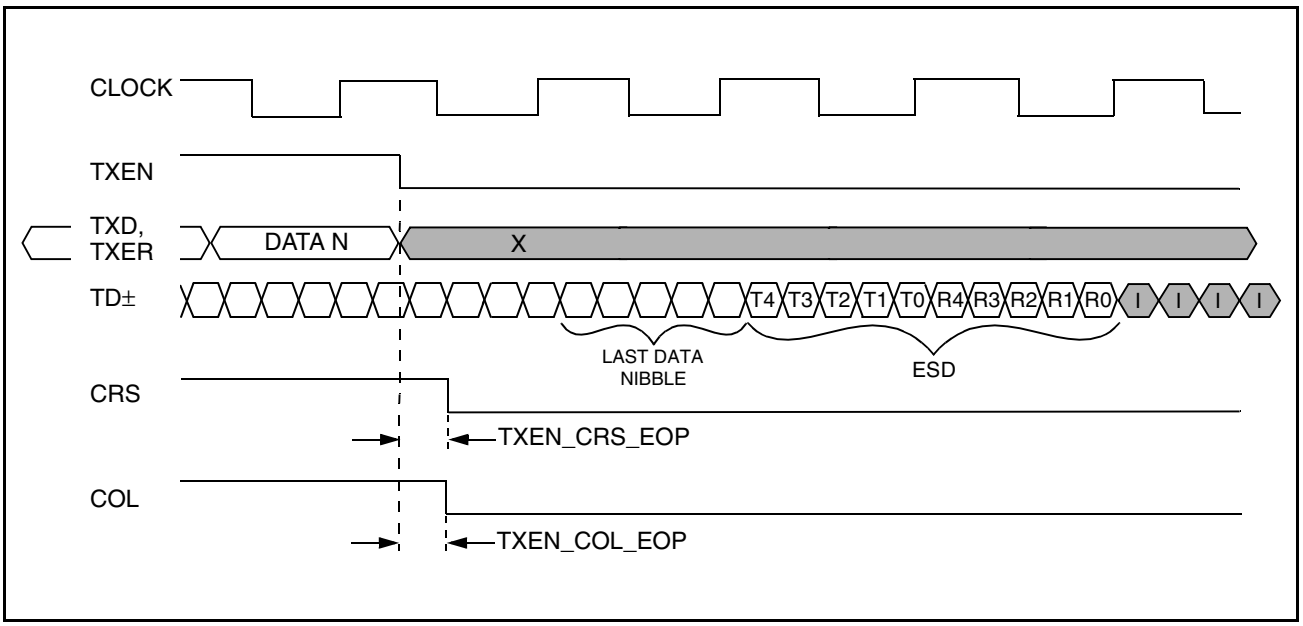


Figure 6: Transmit End of Packet Timing (100 Base-TX)

Table 30 provides the parameters for 10BASE-T transmit timing.

Table 30: 10BASE-T Transmit Timing—Parallel Mode

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
TXC Cycle Time (10BASE-T)	TXC_CYCLE	395	400	405	ns
TXC High/Low Time (10BASE-T)		197.5	200	202.5	ns
TXC Rise/Fall Time		2		5	ns
TXEN, TXD[3:0] valid after TXC Rising	TXEN_VALID			25	ns
TXEN, TXD[3:0] Hold after to TXC Rising	TXEN_HOLD_DTE	75			ns
TD+/- after TXEN Assert	TXEN_TDATA	–	400	450	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	50	100	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	770	1200	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL				
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP				
Idle on Twisted Pair after TXEN De-Assert	TX_QUIET	––	460	500	ns

On the foloowing pages, Table 31 provides the parameters for 100BASE-X receive timing. Figure 7 illustrates 100BASE-TX receive start of packet timing and Figure 8 shows 100BASE-TX receive end of packet timing. Figure 9 shows 100BASE-TX receive packet premature end. Figure 10 illustrates link failure or stream cipher error during receive packet. False carrier sense timing is shown in Figure 11.

Table 31: 100BASE-X Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
RXC Cycle Time		39.5	40	40.5	ns
RXC High/Low Time (RXDV Asserted)		18	20	22	ns
RXC High Time (RXDV Deasserted)		18	20	54	ns
RXC Low Time (RXDV Deasserted)		18	20	38	ns
RXC Rise/Fall Time		2	–	5	ns
RXDV, RXER, RXD[3:0] Delay from RXC Falling		-3	–	3	ns
CRS Deassert from RXC Falling (Valid EOP Only)		-3	–	3	ns
CRS Assert after RD±	RX_CRS	90	–	120	ns
CRS Deassert after RD± (Valid EOP)	RX_CRS_EOP	130	–	160	ns
CRS Deassert after RD± (premature end)	RX_CRS_IDLE	170	–	200	ns
RXDV Assert after RD±	RX_RXDV	130	–	160	ns
RXDV Deassert after RD±	RX_RXDV_EOP	130	–	160	ns
RXDV Assert after CRS		35	–	45	ns
RD± to RXD Steady State Delay	RX_RXD	150	–	180	ns
COL Assert after RD± (while TX)	RX_COL	90	–	120	ns
COL Deassert after RD± (Valid EOP)	RX_COL_EOP	130	–	160	ns
COL Deassert after RD± (Premature End)	RX_COL_IDLE	170	–	200	ns
RXEN high to RXC, RXDV, RXER, RXD[3:0] Delay		0		50	ns
RXC, RXDV, RXER, RXD[3:0] High-Z from RXEN Low		20		70	ns

Note: *RXC minimum high and low times are guaranteed when RXEN is asserted or deasserted. The MII port will always tristate while RXC is low.*

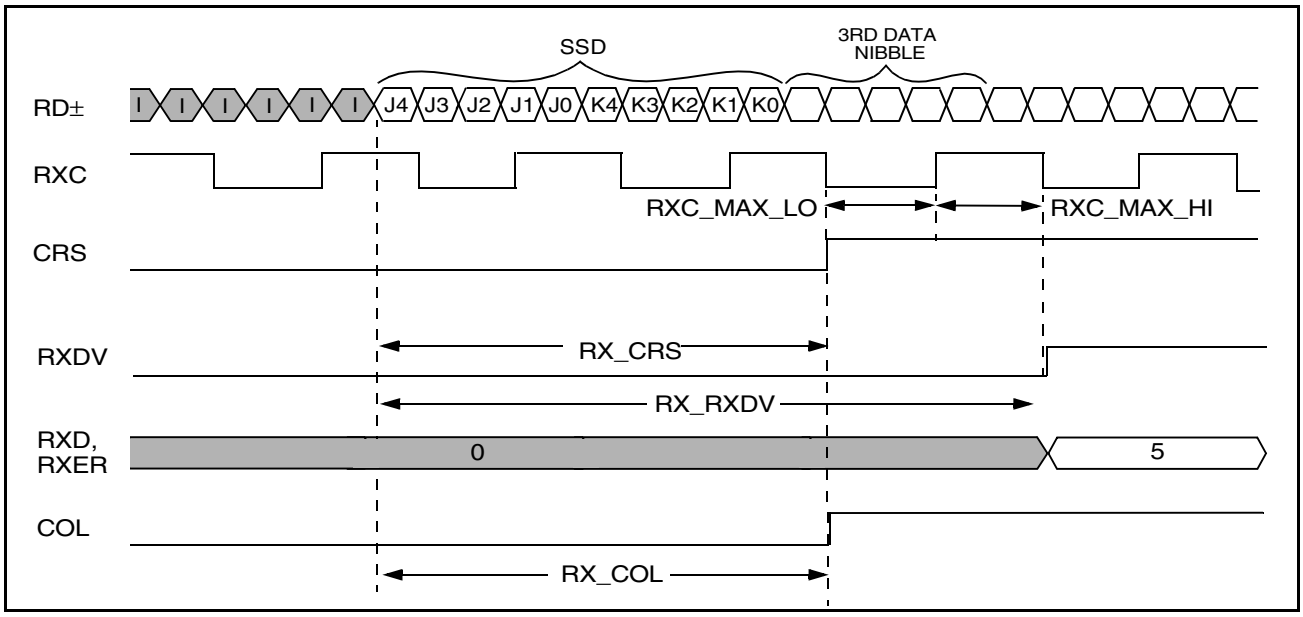


Figure 7: Receive Start of Packet Timing (100BASE-TX)

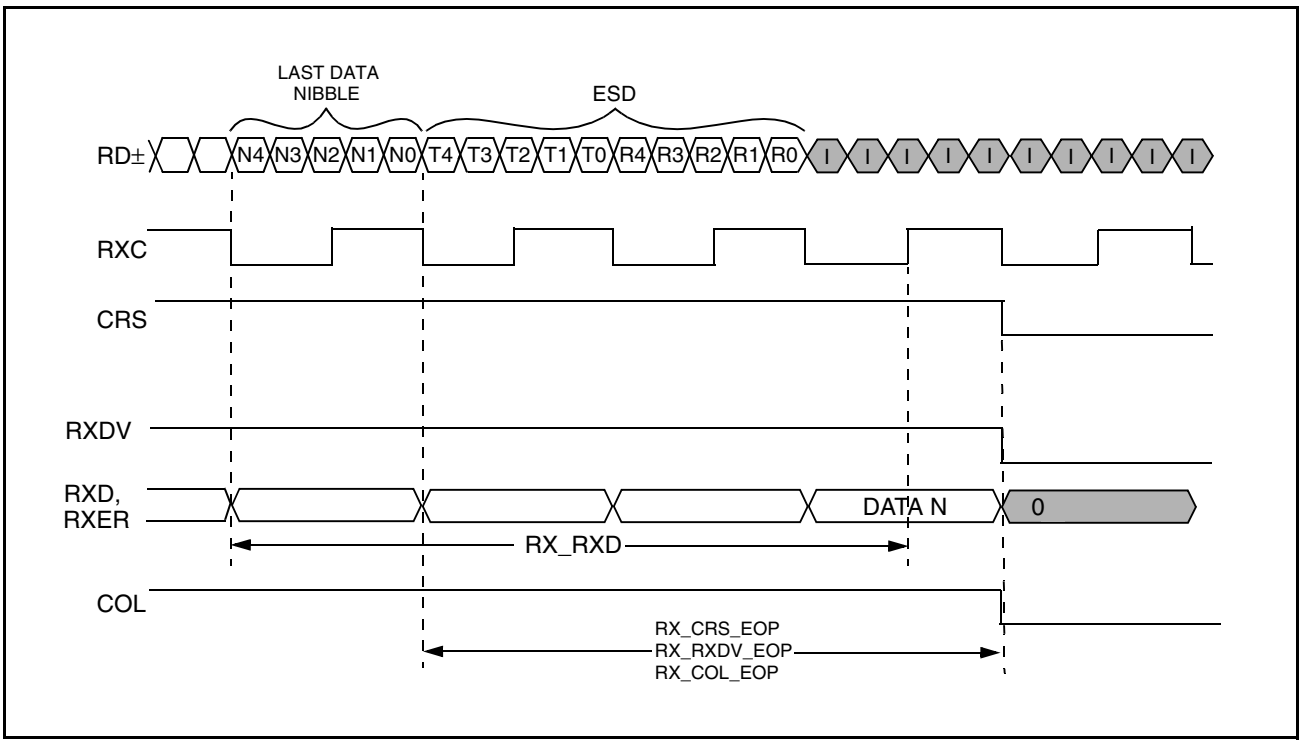


Figure 8: Receive End of Packet Timing (100BASE-TX)

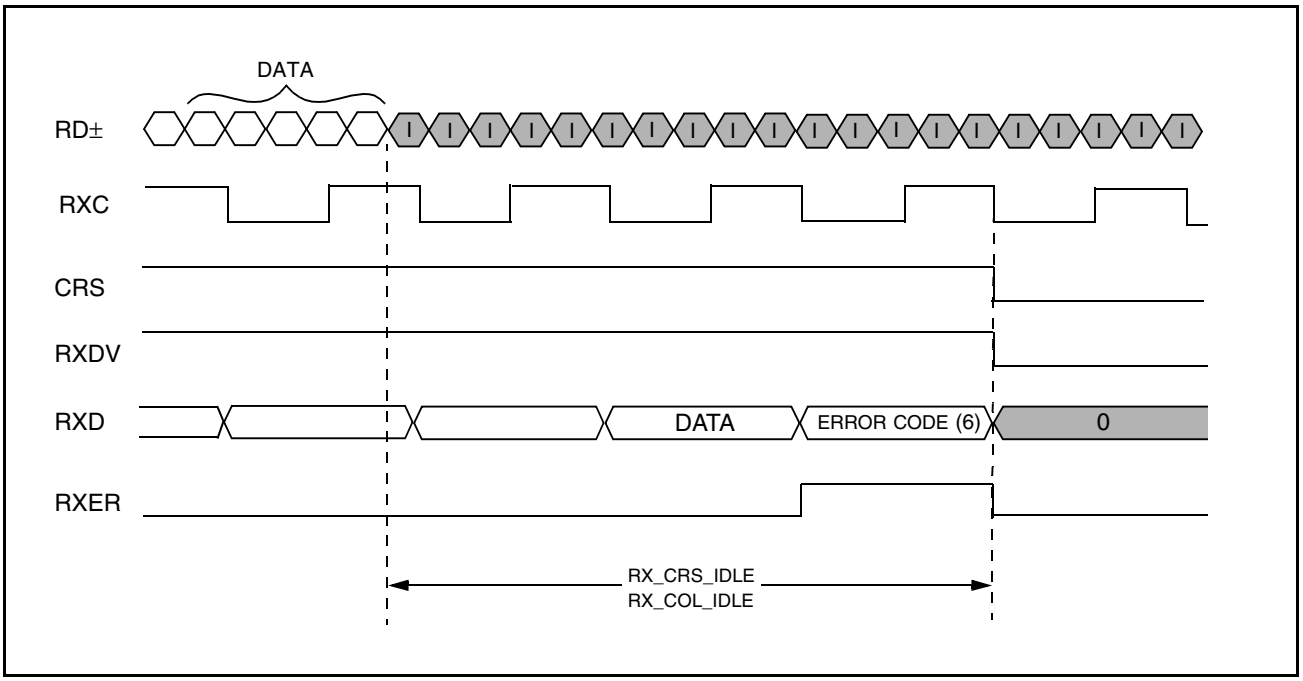


Figure 9: Receive Packet Premature End (100BASE-TX)

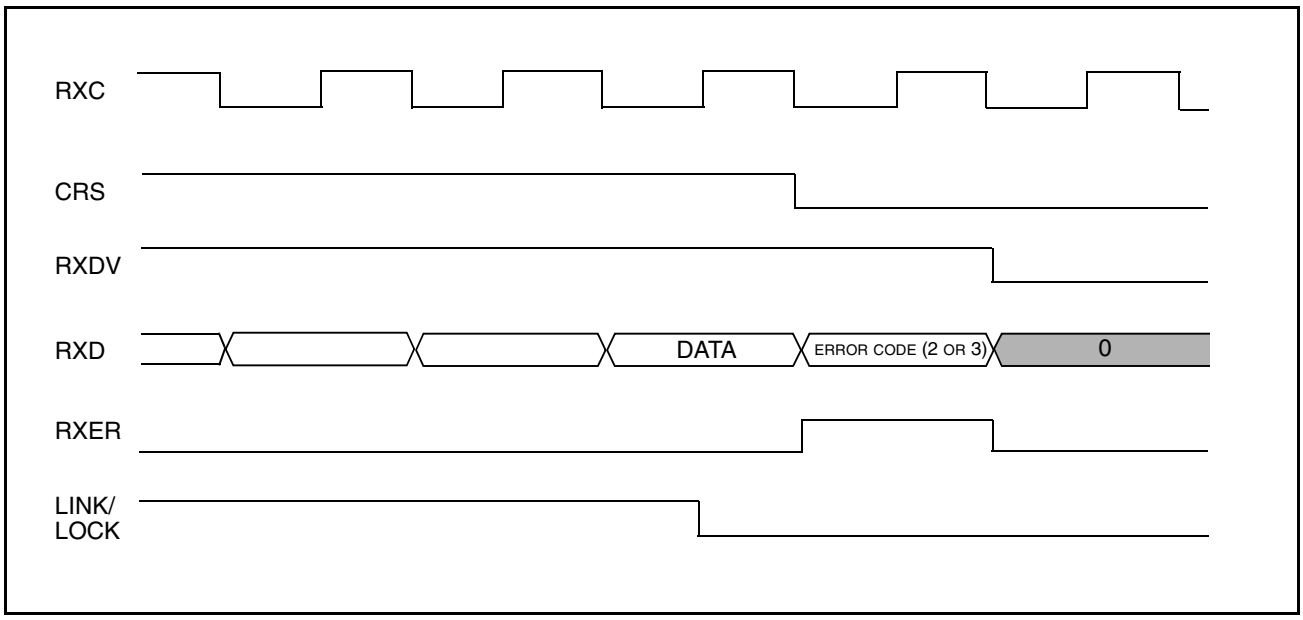


Figure 10: Link Failure or Stream Cipher Error During Receive Packet

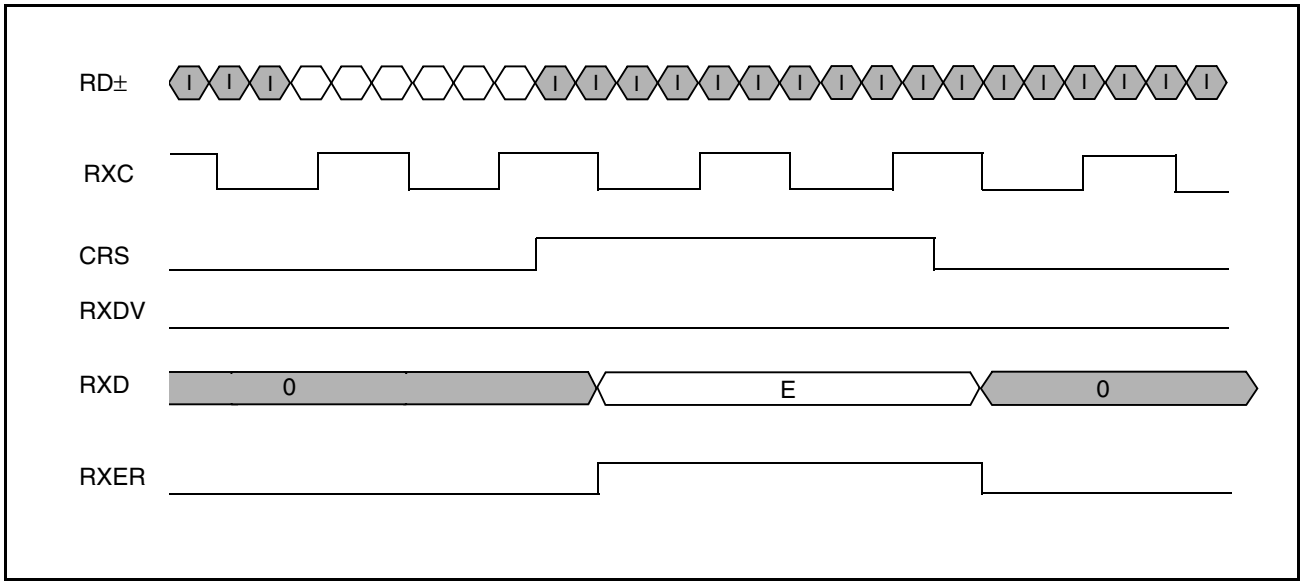


Figure 11: False Carrier Sense Timing (100BASE-TX)

Table 32 provides the parameters for 10BASE-T receive timing. 10BASE-T collision timing parameters are shown in Table 33.

Table 32: 10BASE-T Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
RXC Cycle Time	RXC_CYCLE	370.0	400	430.0	ns
RXC High/Low Time		150.5	200	240.5	ns
CRS Assert after First Rising Edge of Preamble with Positive Start-of-Idle	RX_CRS_BT	100	150	250	ns
CRS Assert after First Falling Edge of Preamble with Negative Start-of-Idle	RX_CRS_BT	100	150	250	ns
RXC Valid after CRS Assert	RXC_VALID	–	–	2000	ns
RXDV Assert after Receive Analog Data	RX_RXDV	–	1900	2300	ns
RXDV Deassert after Receive Analog EOP Ends	RX_NOT_RXDV	–	510	560	ns
CRS Deassert after Receive Analog EOP Ends	RX_NOT_RXDV	–	510	560	ns
Note: *Positive Start of Idle contains four "1" data samples, which implies correct polarity, and Negative Start-of-Idle contains four "0" data samples, which implies reversed polarity. Refer to IEEE 802.3, Clause 14, Figure 14-10.*					

Table 33: 10BASE-T Collision Timing

Parameter	Symbol	Min	Typ	Max	Unit
COL Assert after First Rising Edge of Preamble with Positive Start-of-Idle	RX_COL	–	250	300	ns
COL Assert after First Falling Edge of Preamble with Negative Start-of-Idle	RX_COL	–	250	300	ns
COL Deassert after TXEN Deassert (While Receiving)	TXEN_NOT_COL	–	440	490	ns
COL Assert after TXEN Assert (While Receiving)	TXEN_COL	–	50	100	ns
COL Deassert after Receive Analog Ends (While Transmitting)	RX_NOT_COL	–	400	450	ns

Table 34, Table 35, Table 36 and Table 37 provide the parameters for loopback timing, auto-negotiation, and LED timing. Figure 12 illustrates serial mode LED timing.

Table 34: Loopback Timing

Parameter	Symbol	Min	Typ	Max	Unit
TXD to RXD Steady State Propagation Delay		–	160	–	ns
LPBK Setup Time to TXEN		500	–	–	ns
LPBK Hold Time from TXEN		200	–	–	ns

Table 35: Auto-Negotiation Timing

Parameter	Symbol	Min	Typ	Max	Unit
Link Test Pulse Width		–	100	–	ns
FLP Burst Interval		5.7	16	22.3	ms
Clock Pulse to Clock Pulse		111	123	139	us
Clock Pulse to Data Pulse (Data = 1)		55.5	62.5	69.5	us

Table 36: LED Timing (Parallel Mode)

Parameter	Symbol	Min	Typ	Max	Unit
LED On Time (XMTLED, RCVLED)		–	80	–	ms
LED Off Time (XMTLED, RCVLED)		–	80	–	ms

Table 37: LED Timing (Serial Mode)

Parameter	Symbol	Min	Typ	Max	Unit
Shift Clock	SCLK		1		MHz
LED Serial Mode Data Set-Up	SDO_SETUP		200		ns
LED Serial Mode Data Hold	SDO_HOLD		200		ns
LED Frame Pulse Set-Up	SFRM_SETUP		200		ns
LED Frame Pulse Hold	SFRM_HOLD		200		ns

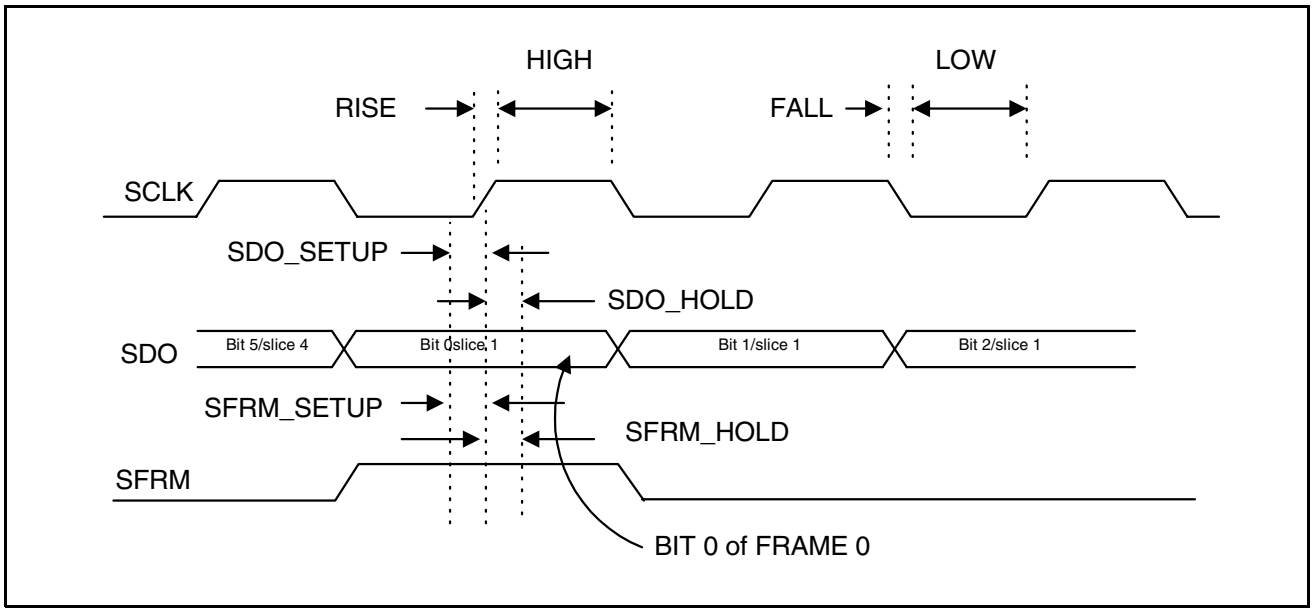


Figure 12: LED Timing (Serial Mode)

Table 38: LED Timing (Low Cost Serial Mode)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Shift Clock (LC Ser SCLK)	T_{cy}		80		ns
Data Set-up (LC ser SDO#)	T_S	20			ns
Data Hold	T_H	20			ns
Refresh	T_{REF}		5.2		ms

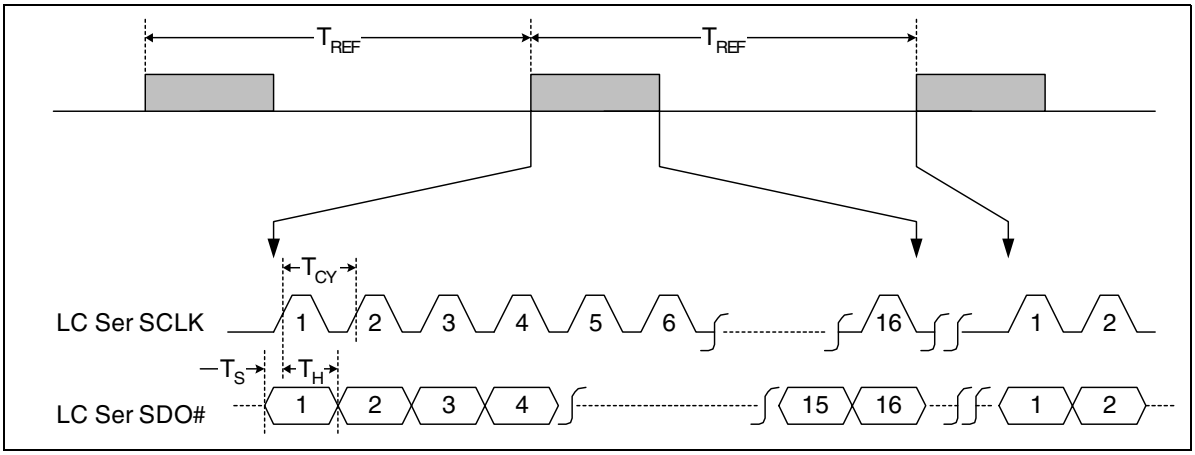


Figure 13: LED Timing (Low Cost Serial Mode)

Management data interface timing parameters are described in Table 39. Figure 14 and Figure 15 illustrate two types of management interface timing.

Table 39: Management Data Interface Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
MDC Cycle Time		80	-	-	ns
MDC High/Low		30	-	-	ns
MDC Rise/Fall Time		-	-	10	ns
MDIO Input Setup Time from MDC rising		10	-	-	ns
MDIO Input Hold Time from MDC rising		10	-	-	ns
MDIO Output Delay from MDC rising		0	-	50	ns

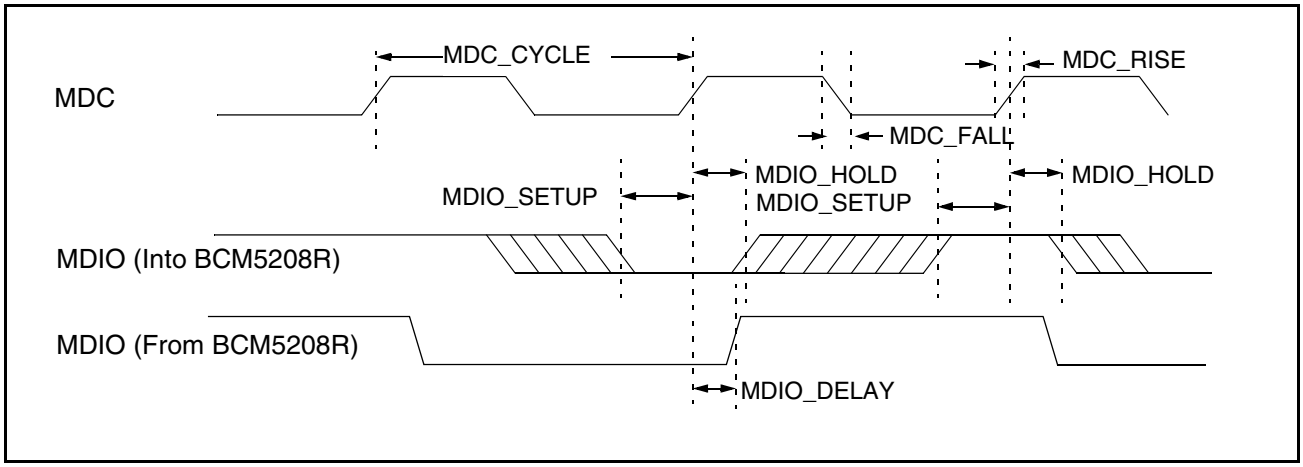
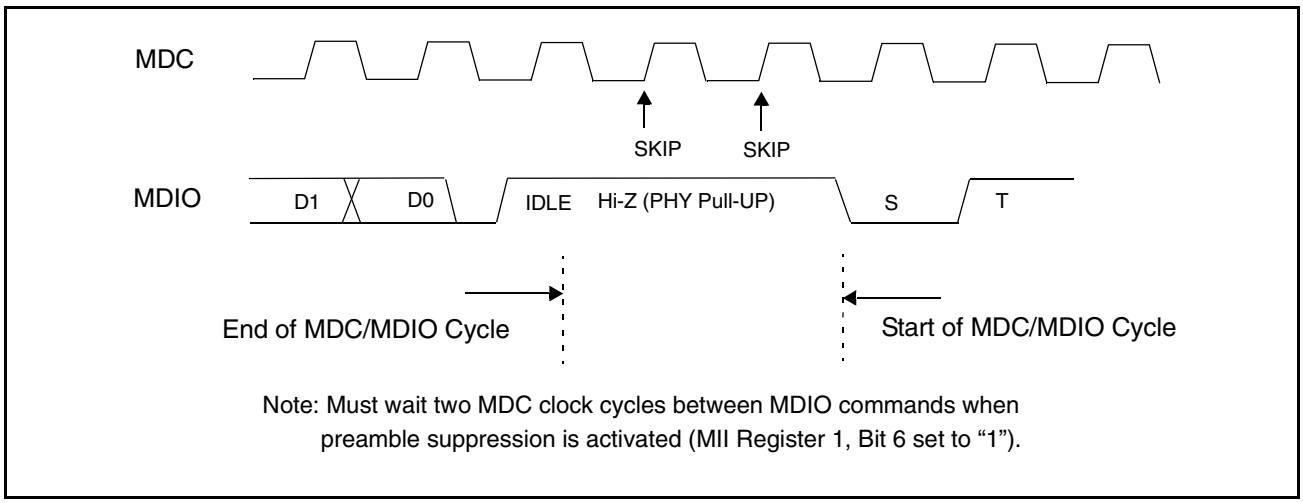


Figure 14: Management Interface Timing



Note: Must wait two MDC clock cycles between MDIO commands when preamble suppression is activated (MII Register 1, Bit 6 set to “1”).

Figure 15: Management Interface Timing (with Preamble Suppression On)

Section 7: Electrical Characteristics

This section covers the electrical characteristics of the BCM5208R.

Table 40 covers the absolute maximum ratings for the BCM5208R. The recommended operating conditions are shown in Table 41. Table 42 gives the electrical characteristics of the BCM5208R.

Table 40: Absolute Maximum Ratings

Symbol	*Parameter*	*Min*	*Max*	*Units*
V_{DD}	Supply Voltage	3.00	3.60	V
V_I	Input Voltage	GND – 0.3	IVDD + 0.3	V
I_I	Input Current			mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge		1000	V

Note: *These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.*

Table 41: Recommended Operating Conditions

Symbol	*Parameter*	*Pins*	*Operating Mode*	*Min*	*Max*	*Units*
V_{DD}	Supply Voltage	AVDD, DVDD, OVDD		3.135	3.465	V
		IVDD		3.135	5.25	V
V_{IH}	High-Level Input Voltage	All Digital Inputs		2.0		V
V_{IL}	Low-Level Input Voltage	All Digital Inputs			0.8	V
V_{IDIFF}	Differential Input Voltage	RD± {1:4}	100BASE-TX	700		mV
V_{ICM}	Common Mode Input Voltage	RD± {1:4}	100BASE-TX	1.55	1.95	V
T_A	Ambient Operating Temperature			0	70	°C

Table 42: Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Min	Typ	Max	Units
I_{DD}	Total Supply Current	AVDD, DVDD, OVDD, IVDD	100BASE-TX		612	650	mA
V_{OH}	High-Level Output Voltage	All LED Outputs	I_{OH} = –15 mA	2.4			V
		All Digital Outputs, Except LED Outputs	I_{OH} = –10 mA	2.4			V
		TD± {1:4}	Driving Loaded Magnetics Module			VDD + 1.5	V
V_{OL}	Low-Level Output Voltage	All Digital Outputs	I_{OL} = 8 mA			0.4	V
		TD± {1:4}	driving loaded magnetics module	VDD – 1.5			V
I_I	Input Current	Digital Inputs with Pull-Up Resistors	V_I = IVDD			+100	µA
			V_I = DGND			-200	µA
		Digital Inputs with Pull-Down Resistors	V_I = IVDD			+200	µA
			V_I = DGND			-100	µA
		All Other Digital Inputs	DGND ≤ V_I ≤ IVDD			±100	µA
I_{OZ}	High-Impedance Output Current	All Three-state Outputs	DGND ≤ V_O ≤ OVDD				µA
		All Open-Drain Outputs	V_O = OVDD				µA
V_{BIAS}	Bias Voltage	VREF, RDAC		1.18		1.30	V

Section 8: Application Examples

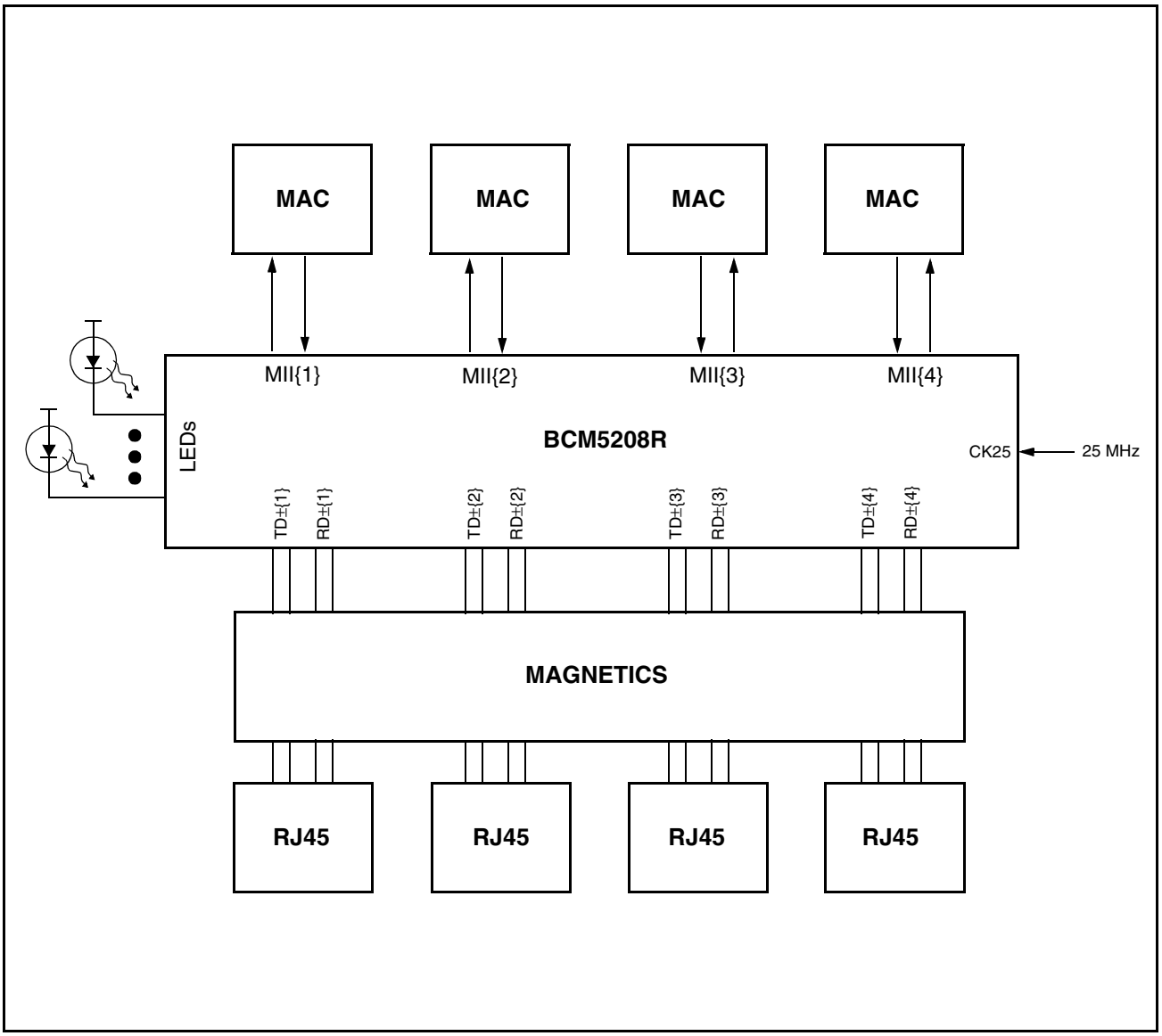
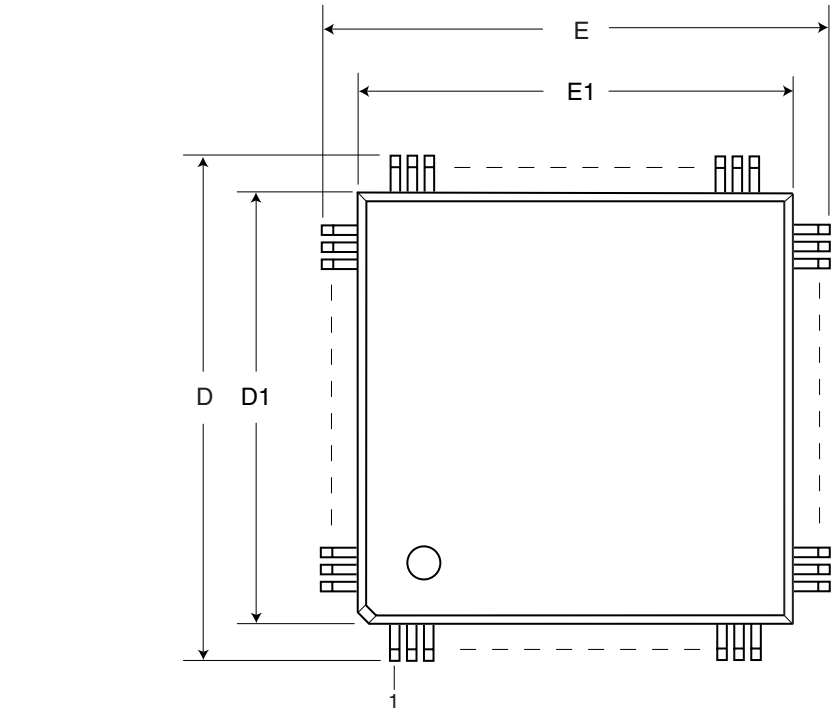
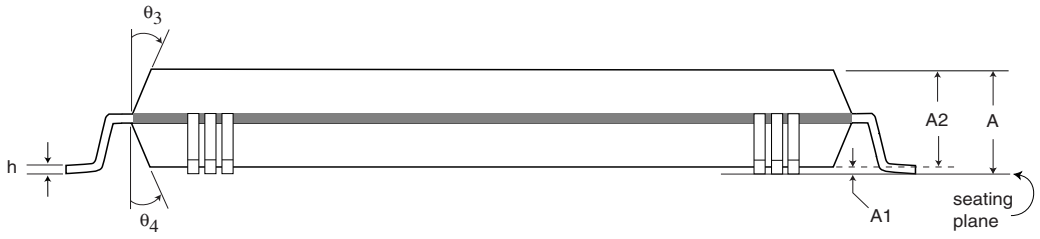


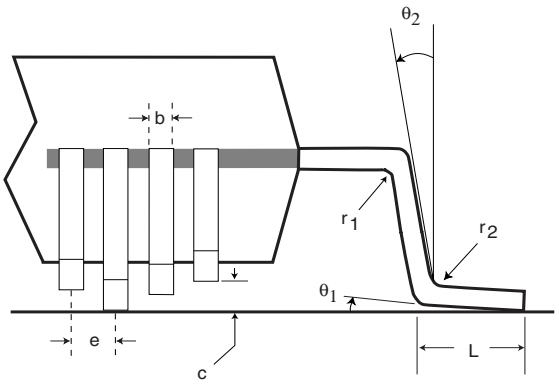
Figure 16: Switch Application





Symbol	Millimeter		
	Min	Nom	Max
A	—	—	4.10
A1	0.25	0.37	0.50
A2	3.39	3.49	3.59
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
L	0.30	0.60	0.75
b	0.15	0.22	0.30
h	0.13		0.23
e	0.50 BSC		
c	—	0.08	0.102
r_1	—	0.20	—
r_2	—	0.30	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	10°	—
θ_4	—	10°	—

208-pin detail



Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

Figure 17: 208-Pin PQFP

Section 9: Ordering Information

Table 43: Ordering Information

Part Number	Package	Ambient Temperature
BCM5208R KPF	208-PQFP	0° to 70° C (32° to 158° F)

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, California 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710

Section 1: Functional Description

Overview

The BCM5208R is a single-chip device containing four independent Fast Ethernet transceivers. Each performs all the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full- or half-duplex Ethernet on CAT 3, 4 or 5 cable.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor functions, Auto-Negotiation, and MII management functions. The BCM5208R can be connected to a MAC through the MII on one side and connects directly to the network media on the other side through isolation transformers for UTP modes. The BCM5208R is fully compliant with the IEEE 802.3 and 802.3u standards.

Encoder / Decoder

In 100BASE-TX mode, the BCM5208R transmits and receives a continuous data stream on twisted pair cable. When the MII transmit enable is asserted, nibble wide (4-bit) data from the transmit data pins is encoded into 5-bit code-groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1 on page 3. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable.

Following baseline wander correction, adaptive equalization, and clock recovery in TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

The 5-bit code groups are decoded into 4-bit data nibbles, as shown in Table 1. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM5208R asserts the MII RXER signal. The chip also asserts RXER for several other error conditions that improperly terminate the data stream. While RXER is asserted, the receive data pins will be driven with a 4-bit code indicating the type of error detected. The error codes are listed in Table 2.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

Link Monitor

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the “Link Fail” state where only idle codes will be transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the “Link Pass” state and the transmit and receive functions are enabled.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD+/- pins for the presence of valid link pulses.

CARRIER SENSE

In 100BASE-X modes, carrier sense is asserted asynchronously on the CRS pin as soon as activity is detected in the receive data stream. RXDV is asserted as soon as a valid start-of-stream delimiter (SSD) is detected. Carrier sense and RXDV are deasserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. If carrier sense is asserted and a valid SSD is not detected immediately, then RXER is asserted in place of RXDV. A value of Eh (E hex) is driven on the receive data pins to indicate false carrier sense.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RD+/- input pins.

In half-duplex DTE mode, the BCM5208R additionally asserts carrier sense while transmit enable is asserted and the link monitor is in the “Pass” state. In full-duplex mode, CRS is only asserted for receive activity.

COLLISION DETECTION

In half-duplex mode, collision detect is asserted on the COL pin whenever carrier sense is asserted while transmission is in progress. Collision detect is never asserted in full-duplex mode.

AUTO-NEGOTIATION

The BCM5208R contains the ability to negotiate its mode of operation over the twisted pair link using the Auto-Negotiation mechanism defined in the IEEE 802.3u specification. Auto-Negotiation can be enabled or disabled by hardware or software control. When the Auto-Negotiation function is enabled, the BCM5208R automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5208R can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full and/or half-duplex. Each transceiver negotiates independently with its link partner, and chooses the highest level of operation available for its own link.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes interzonal interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5208R achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization and decision feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on CAT 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5208R achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self adapting to any quality of cable or cable length. In 10BASE-T operation the adaptive equalizer is bypassed.

ADC

Each receive channel has its own 6-bit, 125-MHz analog-to-digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low offset, high power supply noise rejection, fast settling time, and low bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clocks are locked to the 25-MHz clock input while the receive clocks are locked to the incoming data streams. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with different operating modes. The input data streams are sampled by the recovered clock from each port and fed synchronously to the respective digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5208R automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error. The baseline wander correction circuit is not required, andis therefore bypassed, in 10BASE-T mode.

Table 1: 4B5B Encoding

Name	*4B Code*	*5B Code*	*Meaning*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000*	11111	Idle
J	0101*	11000	Start-of-Stream Delimiter, Part 1
K	0101*	10001	Start-of-Stream Delimiter, Part 2
T	0000*	01101	End-of-Stream Delimiter, Part 1
R	0000*	00111	End-of-Stream Delimiter, Part 2
H	1000	00100	Transmit Error (used to force signalling errors)
V	0111	00000	Invalid Code
V	0111	00001	Invalid Code

Table 1: 4B5B Encoding (Cont.)

Name	4B Code	5B Code	Meaning
V	0111	00010	Invalid Code
V	0111	00011	Invalid Code
V	0111	00101	Invalid Code
V	0111	00110	Invalid Code
V	0111	01000	Invalid Code
V	0111	01100	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code
* Treated as invalid code (mapped to 0111) when received in data field.			

Table 2: Receive Error Encoding

Error type	RXD[3:0]
Stream cipher error—descrambler lost lock	0010
Link failure	0011
Premature end of stream	0110
Invalid code	0111
Transmit error	1000
False carrier sense	1110

MULTIMODE TRANSMIT DAC

The multimode transmit digital-to-analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components, thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode. The transmit DAC utilizes a current drive output that is well balanced and produces very low noise transmit signals.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted pair cable. The data is scrambled by *exclusive ORing* the NRZ signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by *exclusive ORing* it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler will “lock” to the scrambler state after detecting a sufficient number of consecutive idle code groups. The receiver will not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler will continuously monitor the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724µs, it will become unlocked, and the receive decoder will be disabled. The descrambler will always be forced into the unlocked state when a link failure condition is detected.

Stream cipher scrambling/descrambling is not used in 10BASE-T mode.

MII MANAGEMENT

Each transceiver within the BCM5208R contains an independent set of MII management registers. They share a single MDC/MDIO serial interface, Each transceiver has a unique address and must be accessed individually. The common base address for the group of four individual transceivers is defined by configuring the three external PHYAD address input pins.

INTERRUPT MODE

The BCM5208R can be programmed to provide an interrupt output from each of the four transceivers. The interrupt feature is disabled by default. When the interrupt capability is enabled by setting MII register 1Ah, bit 14, the XMTLED# pin becomes the INTR# pin and the RCVLED# pin becomes an activity pin named ACTLED#. The INTR# pins are open-drain and may be wire-ORed together. The status of each interrupt source is also reflected in Register 1Ah, bits 1, 2 and 3. The sources of interrupt are change in link, speed or full-duplex status. If any type of interrupt occurs, the Interrupt Status bit, Register 1Ah, bit 0, will be set.

In addition, each transceiver has its own register controlling the interrupt function.

If the interrupt enable bit is set to 0, no status bits will be set and no interrupts will be generated. If the interrupt enable bit is set to 1, the following conditions apply:

- If mask status bits are set to 0 and the interrupt mask is set to 1, status bits will be set but no interrupts generated.
- If mask status bits are set to 0 and the interrupt mask is set to 0, status bits and interrupts will be available.
- If mask status bits are set to 1 and the interrupt mask is set to 0, no status bits and no interrupts will be available.

Changes from “active” to “inactive” or vice versa will cause an interrupt. Setting Register 1Ah, bit 8 high will mask all interrupts, regardless of the settings of the individual mask bits.

LED MODES

The BCM5208R supports two types of Serial LED modes; Serial LED Mode and Low Cost Serial LED mode.

SERIAL LED MODES

Serial LED mode in the BCM5208R supports several modes for providing LED and interrupt information as a serial bit stream. The LED data is presented on a single pin, with a second pin providing a shift clock and a third providing framing. When the Serial LED mode is enabled, pin 182 (Ser SCLK) becomes the bit clock output, pin 183 (Ser SDO#) becomes the data output and pin 184 (Ser SFRM) provides the framing pulse.

After the Serial LED mode is enabled, several options for bit format become available. If no action is taken, bits are shifted out as shown in the top line of the table below. If the INTR bit (bit 14 of MII Register 1Ah) is set, data is shifted out as shown in the Interrupt row of the table. If the FDXLED bit (bit 15 of MII Register 1Ah) is set, data is shifted out as shown in the full-duplex row of the table.

In each mode, 24 bits comprise a frame. Bits are shifted in the order shown in the table below, with the bits in column marked BIT 0 leaving the chip first and the bits in column BIT 5 leaving the chip later in time. The sequence repeats four times between frame pulses to provide data for each PHY in the quad device. Bits are numbered from 0 to 5; frames are numbered from 1 to 4. Therefore, bit 0 of PHY 1 is the first bit out of the frame, and bit 5 of PHY 4 is the 24th bit out of the frame.

Data is shifted out on the falling edge of the shift clock, which is approximately 1 MHz. Data is valid on the rising edge of the shift clock. The framing pulse (Ser SFRM) is high during the bit 0 time of frame1. For timing information, see Table 37 on page 48.

Serial LED mode can be enabled in the hardware by holding LNKLED#{1}, pin 203 and LNKLED#{4}, pin 159 low during power-on reset.

Table 3: Serial LED Mode Bit Framing

Option	*MII REG 1Ah*	*Bit 5*	*Bit 4*	*Bit 3*	*Bit 2*	*Bit 1*	*Bit 0*
Normal	Bit 14 =0 Bit 15 =0	FDX	COL	Speed	Link	Transmit	Receive
Interrupt	Bit 14 =1 Bit 15 =0	FDX	Global Interrupt	Speed	Link	Slice Interrupt	Activity
Full-Duplex	Bit 14 =0 Bit 15 =1	FDX	COL	Speed	Link	FDX	Activity
A Global Interrupt indicates an interrupt from any of the four slices ORed together; a Slice Interrupt is from one of the four-PHYs.							

LOW COST SERIAL LED MODE

The BCM5208R also supports a low-cost serial LED mode. This serial mode can be enabled only by hardware. The low-cost serial LED mode is enabled when LNKLED#{3}, pin 178 (LC_SER_LED_EN#) is held low during power-on reset. When enabled, RCVLED#{1}, pin 201, sources the serial clock (LC Ser SCLK) and RCVLED#{3}, pin 180, sources the active low serial data (LC Ser SDO#}.

The LEDs are shifted out on the LC Ser SDO# in the following order: ActivityLED{1}, ActivityLED{2}, ActivityLED{3}, ActivityLED{4}, LinkLED{1}, LinkLED{2}, LinkLED{3}, LinkLED{4}, FullduplexLED{1}, FullduplexLED{2}, FullduplexLED{3}, FullduplexLED{4}, SpeedLED{1}, SpeedLED{2}, SpeedLED{3}, and SpeedLED{4}.

Section 2: Hardware Signal Definition Table

Table 4 provides the pin descriptions for the BCM5208R.

Table 4: Pin Descriptions

Pin	*Pin Label*	*Type*	*Description*
MEDIA CONNECTIONS			
60, 61	RD+ {1},RD- {1}	I_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
75, 74	RD+ {2},RD- {2}		
82, 83	RD+ {3},RD- {3}		
97, 96	RD+ {4},RD- {4}		
65, 66	TD+ {1},TD- {1}	O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
70, 69	TD+ {2},TD- {2}		
87, 88	TD+ {3},TD- {3}		
92, 91	TD+ {4},TD- {4}		
CLOCK			
6	CK25	I	**25 MHz Reference Clock Input.** This pin must be driven with a continuous 25 MHz clock in all operating modes.
MII INTERFACE			
27, 12, 145, 130	TXC {1:4}	O_{3S}	**Transmit Clock.** Delivers a 25-MHz output in 100BASE-X mode and a 2.5-MHz in 10BASE-T mode output.
33, 34, 35, 36	TXD[3:0] {1}	I_{PD}	**Transmit Data Input.** Nibble-wide transmit data is input on these pins synchronously to TXC. TXD[3] is the most significant bit.
208, 1, 9, 10	TXD[3:0] {2}		
150, 149, 148, 147	TXD[3:0] {3}		
124, 123, 122, 121	TXD[3:0] {4}		
37,11, 146,120	TXEN {1:4}	I_{PD}	**Transmit Enable.** Active high. Indicates that the data nibble is valid on TXD[3:0].
17, 190, 172, 140	RXC {1:4}	O_{3S}	**Receive Clock.** 25-MHz output in 100BASE-X mode and 2.5-MHz output in 10BASE-T mode. This clock is recovered from the incoming data on the cable inputs. RXC is a continuously running output clock resynchronized at the start of each incoming packet. This synchronization may result in an elongated period during one cycle when RXDV is low.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
19, 20, 21, 23	RXD[3:0] {1}	O_{3S}	**Receive Data Outputs.** Nibble-wide receive data is driven out of these pins synchronously to RXC. RXD[3] is the most significant bit.
192,193, 194, 195	RXD[3:0] {2}		
170,169, 168, 167	RXD[3:0] {3}		
138, 137, 136, 134	RXD[3:0] {4}		
24,196, 166, 133	RXDV {1:4}	O_{3S}	**Receive Data Valid.** Active high. Indicates that a receive frame is in progress, and that the data stream present on the RXD output pins is valid.
18, 191, 171, 139	RXER {1:4}	O_{3S}	**Receive Error Detected.** Active high. Indicates that there has been an error during a receive frame.
26, 206, 157, 131	CRS {1:4}	O_{3S}	**Carrier Sense.** Active high. Indicates traffic on link. In 100BASE-X modes, CRS is asserted when a non-idle condition is detected in the receive data stream and deasserted when idle or a valid end of stream delimiter is detected. In 10BASE-T mode, CRS is asserted when a valid preamble is detected and deasserted when end-of-file or an idle condition is detected. In DTE mode, CRS is also asserted during transmission of packets. CRS is an asynchronous output signal.
25, 205, 151, 132	COL {1:4}	I/O_{PD}	**Collision Detect.** In half-duplex modes, active high output indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous output signal.
118	MDIO	I/O_{PD}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
117	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies up to 12.5 MHz are supported.
119	RESET#	I_{PU}	**Reset.** Active Low. Resets the BCM5208R. Pin not included in NAND chain.
MODE			
38, 39, 40	PHYAD [4:2]	I_{PD}	**PHY Address Selects.** These inputs set the three MSBs for the MII management PHY addresses. The two LSBs, PHYAD [1:0], are internally wired to each of the four ports: PHYAD [00] = Port 1,..., PHYAD [11] = Port 4. Also serve as test control inputs along with TESTEN and NANDMD[1:0] to select the NAND-chain test mode.
42	FDXEN	I_{PD}	**Full-Duplex Mode Enable.** This pin's function applies only to DTE mode when Auto-Negotiation is disabled. The FDXEN pin is logically ORed with the MII Control register bit 8 to generate an internal full-duplex enable signal. When Auto-Negotiation is enabled, the FDXEN is ignored.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
104	F100	I_{PU}	**Force 100BASE-X Operation.** When F100 is high and ANEN is low, all transceivers will be forced to 100BASE-X operation. When F100 is low and ANEN is low, all transceivers are forced to 10BASE-T operation. When ANEN is high, F100 has no effect on operation.
105	ANEN	I_{PU}	**Auto-Negotiation Enable.** When pulled high, Auto-Negotiation begins immediately after reset. When low, Auto-Negotiation is disabled after reset. Auto-Negotiation is always under software control (Register "0", bit 12).
116, 115	ER[1:0]	I_{PU}	**Transmit DAC Edge Rate Control.** These pins control the slew rate of each of the transmit DACs. The 10-90% rise time is set by the value on ER[1:0] as follows: 00 = 1 ns; 01 = 2 ns; 10 = 3 ns; 11 = 4 ns.
43	TESTEN	I_{PD}	**Test Enable.** Active-high test control input used along with NANDMD[1:0] and PHYAD[4:2] to select the NAND-chain test mode. This test mode is latched when TESTEN is pulsed high then low, with PHYA[4:2]=101 and NANDMD[1:0] = 11. This pin is not included in the NAND chain and must be pulled low or left unconnected during normal operation.
54, 53	NANDMD[1:0]	I_{PD}	**NAND Mode.** Active-high test control inputs used along with TESTEN and PHYA[4:2] to select the NAND-chain test mode. Both inputs must be driven high during latching of the test-mode. Must be pulled low or left unconnected during normal operation.
BIAS			
78	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of each of the transmit DACs. A resistor of 1.24 KΩ ±1% must be connected between the RDAC pin and AGND.
79	VREF	B	**Voltage Reference.** Low-impedance bias pin driven by the internal bandgap voltage reference. This pin must be left unconnected during normal operation.
LED			
203	LNKLED# {1}	O	**Link Integrity LED.** Active low. This output signal indicates the link status of the PHY. LNKLED is driven low when the link to the PHY is good. Serial LED mode is enabled by "pull-down" of pin 203, LNK LED#{1}, and pin 159, SER LED_EN#{2}, during reset. When the Serial LED mode is enabled, pin 184 becomes the Serial LED mode frame signal. Low cost serial LED mode is enabled by "pull-down" of pin 178 during reset.
184	LNKLED# {2} Ser SFRM		
178	LNKLED# {3} LC_SER_LED_EN#		
159	LNKLED# {4} SER_LED_EN#		
204, 185, 177, 158	SP100LED# {1:4}	O	**Speed 100 LED.** Driven low when operating in 100BASE-X modes and high when operating in 10BASE-T modes.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
202	XMTLED# {1} INTR# {1} FDXLED# {1}	O_{OD}	**Transmit Activity LED.** Active low output. The transmit activity LED is driven low for approximately 80ms each time there is transmit activity while in the link pass state. When INTR mode is enabled, the pin becomes an interrupt output. When FDX LED mode is enabled, the pin becomes FDXLED output. When the Serial LED mode is enabled, pin 183 becomes the Serial LED mode data output signal.
183	XMTLED# {2} INTR# {2} FDXLED# {2} Ser SDO#		
179	XMTLED# {3} INTR# {3} FDXLED# {3}		
160	XMTLED# {4} INTR# {4} FDXLED# {4}		
201	RCVLED# {1} ACTLED# {1} LC Ser SCLK	O_{OD}	**Receive Activity LED.** Active low output. The receive activity LED is driven low for approximately 80ms each time there is receive activity while in the link pass state. When in either INTR or FDXLED modes, this pin becomes ACTLED output for either receive or transmit activity. When the Serial LED mode is enabled, pin 182 becomes the Serial LED mode clock signal. When the low cost serial LED mode is enabled, pin 201 becomes Low cost serial LED mode clock signal and pin 180 becomes the data output signal.
182	RCVLED# {2} ACTLED# {2} Ser SCLK		
180	RCVLED# {3} ACTLED# {3} LC Ser SDO#		
161	RCVLED# {4} ACTLED# {4}		
JTAG			
99	TDI	I_{PU}	**Test Data Input.** Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
100	TDO	O_{3S}	**Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise.
101	TMS	I_{PU}	**Test Mode Select.** Single control input to the JTAG TAP Controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.
102	TCK	I_{PU}	**Test Clock.** Clock input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Table 4: Pin Descriptions (Cont.)

Pin	Pin Label	Type	Description
103	TRST#	I_{PU}	**Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. Must be held low during power-up to insure the TAP Controller initializes to the test-logic-reset state. May be pulled low continuously when JTAG functions are not used.
44	DLLTEST	I_{PU}	**DLL Bypass Test Enable.** This pin is for factory testing only, and must be connected to DVDD or left floating.
POWER			
181	IVDD		**Input VDD.** +5.0V or +3.3V. If any of the inputs are driven to 5.0V, this pin must be connected to the 5.0V supply. If none of the inputs are driven above 3.3V, this pin can be connected to the 3.3V supply.
7	PLLVDD		Phase Locked Loop VDD
8	PLLGND		Phase Locked Loop GND
77	BIASVDD		Bias VDD
80	BIASGND		Bias GND
63, 72, 85, 94	AVDD		Analog VDD
62, 64, 67, 68, 71, 73, 84, 86, 89, 90, 93, 95	AGND		Analog GND
175, 198	DVDD		Digital Core VDD
176, 197	DGND		Digital Core GND
13, 129, 144,162, 173,200	OVDD		Digital Periphery (Output Buffer) VDD
3, 14, 22, 29, 50, 107, 128, 135,143, 154, 163, 174, 188, 199	OGND		Digital Periphery (Output Buffer) GND

Note: # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = Bias. Bus Naming Convention: pin label followed by [MSB:LSB] followed by {Port #}.

Section 3: Pinout Diagram

Figure 2 provides the pinout diagram for the BCM5208R.

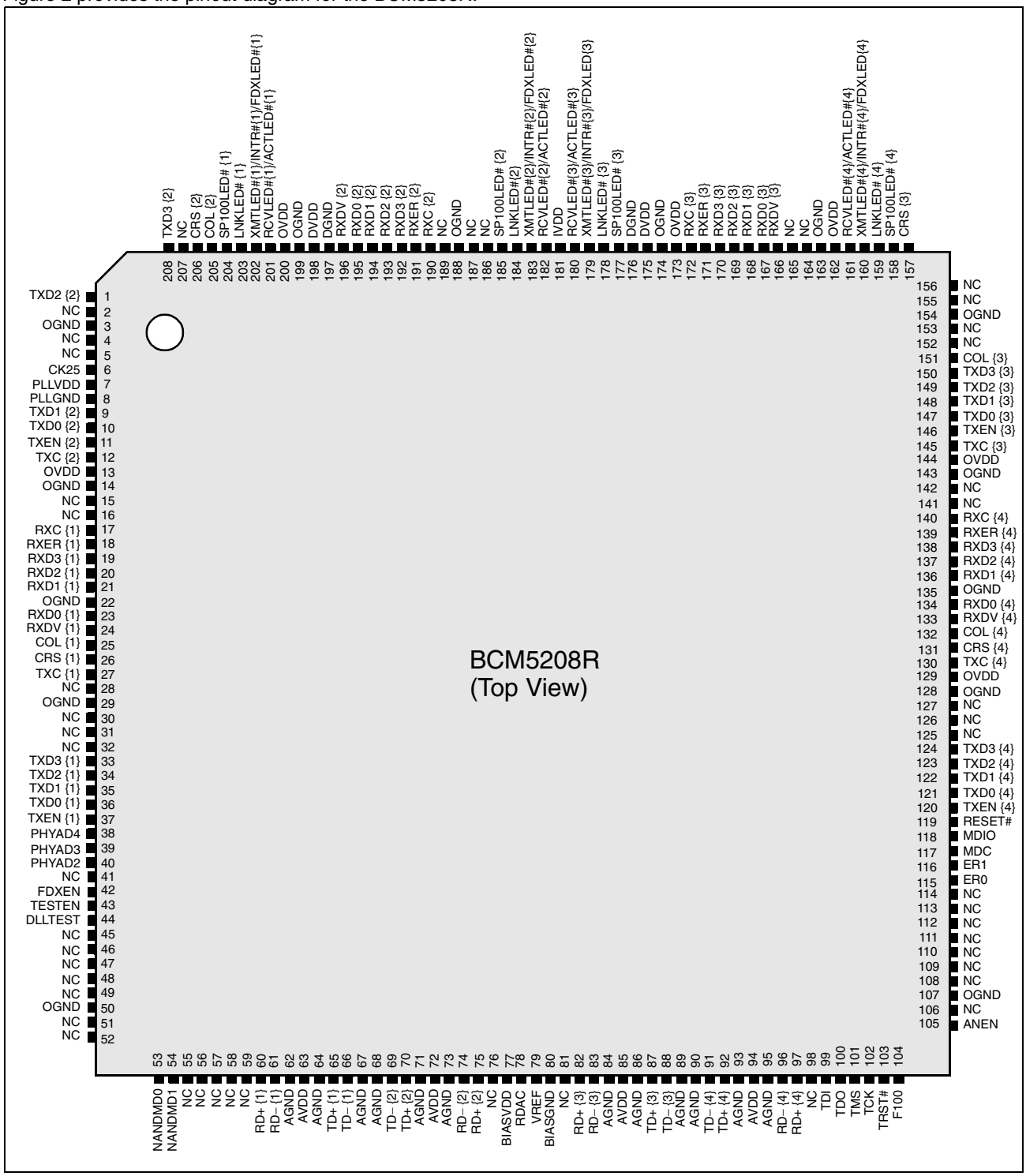


Figure 2: Pinout Diagram

BCM5208R AND BCM5208 COMPATIBILITY

The BCM5208R and BCM5208 are both packaged using a 208-pin PQFP. Common signals to both devices use the same pin configuration. Therefore, it is possible to use the BCM5208R in designs that use the BCM5208, if the following items are taken into consideration.

FUNCTIONS NOT SUPPORTED

The following functions are not supported in the BCM5208R:

- FX mode
- Repeater mode

SIGNALS NOT SUPPORTED

The following BCM5208 input signals are not supported in the BCM5208R:

- SD+/- {1:4} (100BASE-FX Signal Detect)
- RPTR (Repeater Mode Enable)
- TXJAM {1:4} (Transmit Jam)
- TXER {1:4} (Transmit Error)
- RXEN {1:4} (Receiver Enable)
- CIMEN (Carrier Integrity Monitor Enable)

ADDITIONAL FUNCTION SUPPORTED

- Next Page function is supported through MII register 07h and 08h.

POWER AND GROUND PINS

The BCM5208R uses fewer power and ground pins for DVDD, OVDD, AVDD, DGND, OGND, and AGND. However, the power and ground pins used by the BCM5208R are in the same locations as those used by the BCM5208.

USING A BCM5208R IN PLACE OF A BCM5208

If your design uses a BCM5208, you can use a BCM5208R in its place. Signals that are not supported by the BCM5208R do not affect other functions that are supported by the BCM5208, since these signals are not connected internally to the device. However, care should be taken when using a BCM5208R in place of a BCM5208 to ensure that unsupported signals connected from the circuit board to the device do not expect the device to function in a certain manner.

See Figure 3 on page 14, which shows the signals not supported in the BCM5208R and their locations.

Figure 3 provides the pinout compatibility diagram for the BCM5208 and BCM5208R. The pin signals shown with a strike-through represent the BCM5208-only signals.

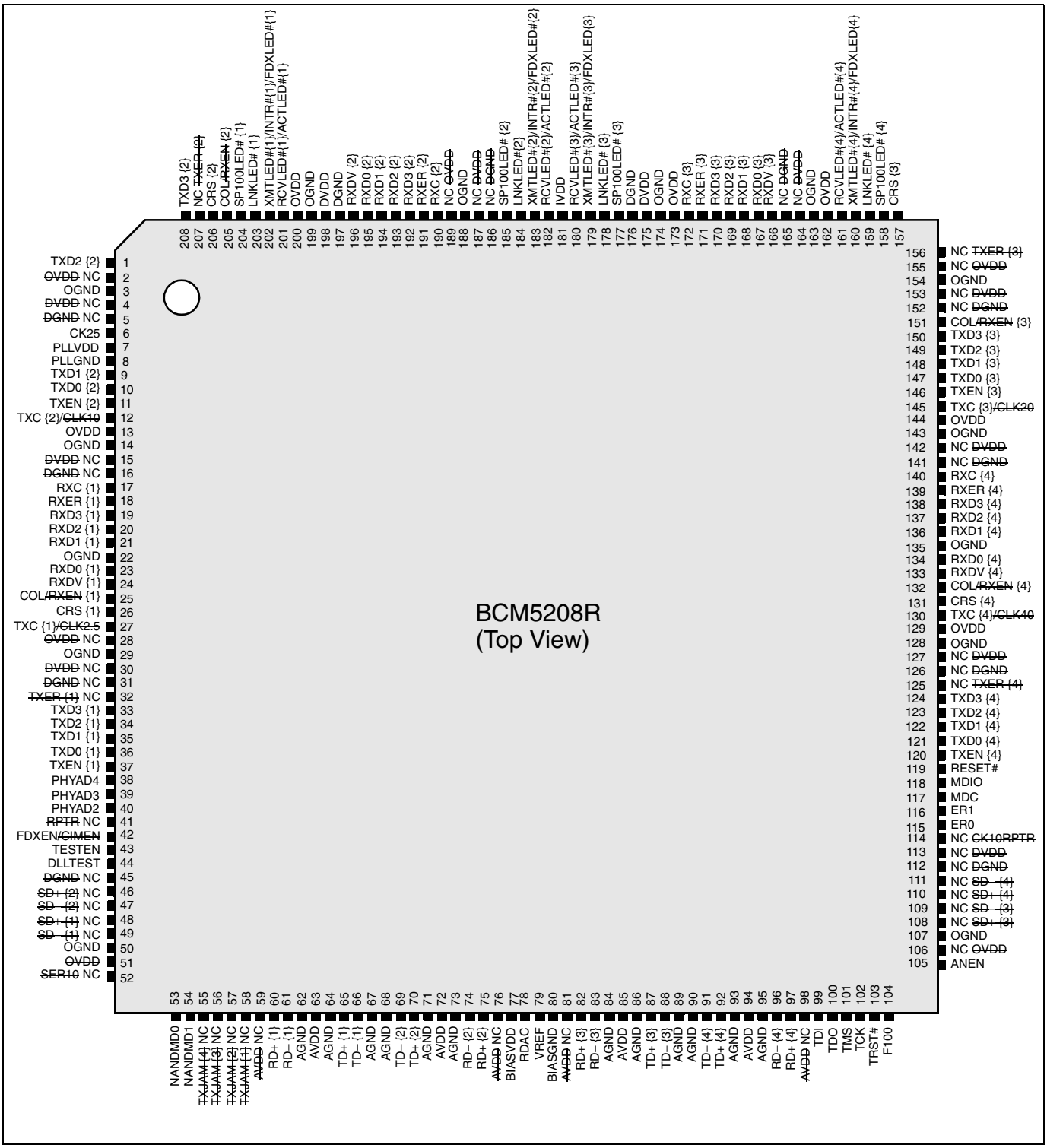


Figure 3: BCM5208/5208R Pinout Compatibility Diagram

Section 4: Operational Description

RESETTING THE BCM5208R

There are two ways to reset each transceiver in the BCM5208R. A hardware reset pin has been provided that resets all internal nodes inside the chip to a known state. The reset pulse must be asserted for at least 400 ns. Hardware reset should always be applied to a BCM5208R after power-up.

Each transceiver in the BCM5208R also has an individual software reset capability. To perform software reset, a 1 must be written to bit 15 of the transceiver's MII Control Register (see MII Register Definitions). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a 0 is written to the MII Control Register reset bit.

ISOLATE MODE

Each transceiver in the BCM5208R can be isolated from the MII. When a transceiver is put into isolate mode, all MII inputs (TXD[3:0] and TXEN) are ignored, and all MII outputs (TXC, COL, CRS, RXC, RXDV, RXER, and RXD[3:0]) are set at high impedance. Only the MII management pins (MDC, MDIO) operate normally. Upon resetting the chip, the isolate mode is off. Writing a "1" to bit 10 of the MII Control Register puts the transceiver into isolate mode. Writing a "0" to the same bit removes it from isolate mode.

LOOPBACK MODE

The loopback mode allows in-circuit testing of the BCM5208R chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. Incoming packets on the cable are ignored. Because of this, the COL pin is not normally activated during loopback mode. To test that the COL pin is actually working, the BCM5208R can be placed into collision test mode. This mode is enabled by writing a 1 to bit 7 of the MII Control Register. Asserting TXEN causes the COL output to go high, and deasserting TXEN causes the COL output to go low.

The loopback mode can be entered by writing a 1 to bit 14 of the MII Control Register. To resume normal operation, bit 14 of the MII Control Register must be 0.

Several function bypass modes are also supported, which can provide a number of different combinations of feedback paths during loopback testing. These bypass modes include bypass scrambler, bypass MLT3 encoder, and bypass 4B5B encoder.

FULL-DUPLEX MODE

The BCM5208R supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable. The COL signal is never activated while in full-duplex mode. By default, each transceiver in the BCM5208R powers up in half-duplex mode.

When Auto-Negotiation is disabled, full-duplex operation can be enabled either by a pin (FDXEN) or by an MII register bit (Register "0" bit 8).

When Auto-Negotiation is enabled in DTE mode, full-duplex capability is advertised by default but can be overridden by a write to the Auto-Negotiation Advertisement Register (04h).

10BASE-T MODE

The same magnetics module is used to interface the twisted-pair cable in 10BASE-T mode and in 100BASE-TX mode. The data will be two-level Manchester coded instead of three-level MLT3 and no scrambling/descrambling or 4B5B coding is performed. Data and clock rates are decreased by a factor of 10, with the MII interface operating at 2.5 MHz.

PHY ADDRESS

Each transceiver in the BCM5208R has a unique PHY address for MII management. The addresses are set through the PHY address pins. The pins are latched at the trailing end of reset. Transceiver 1 has the address AAA00, where AAA = PHYAD[4:2]. Transceivers 2-4 have addresses AAA01, AAA10 and AAA11, respectively. Each time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

Section 5: Register Summary

MII Management Interface: Register Programming

The BCM5208R fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written to and read from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5208R at a rate of 0–12.5 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. See Table 5 for the fields in every MII read or write instruction frame.

Table 5: MII Management Frame Format

OPERATION	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE	DIRECTION
READ	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5208R Driven by BCM5208R
WRITE	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5208R

Preamble (PRE). Thirty two consecutive 1 bits must be sent through the MDIO pin to the BCM5208R to signal the beginning of an MII instruction. Fewer than thirty-two 1 bits will cause the remainder of the instruction to be ignored.

Start of Frame (ST). A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP). A READ instruction is indicated by 10, while a WRITE instruction is indicated by 01.

PHY Address (PHYAD). A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips. The BCM5208R supports the full 32-PHY address space with PHYAD[4:2] input-pin controlled and PHYAD[1:0] internally decoded to select one of the four transceivers.

Register Address (REGAD). A 5-bit Register Address follows, with the MSB transmitted first. The register map of the BCM5208R, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA). The next two bit times are used to avoid contention on the MDIO pin when a read operation is performed. For a write operation, 10 must be sent to the BCM5208R chip during these two bit times. For a read operation, the MDIO pin must be placed into High-Impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

Data. The last 16 bits of the frame are the actual data bits. For a Write operation, these bits are sent to the BCM5208R, whereas, for a Read operation, these bits are driven by the BCM5208R. In either case, the MSB is transmitted first.

When writing to the BCM5208R, the data field bits must be stable for 10 ns before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM5208R, the data field bits are valid after the rising-edge of MDC until the next rising-edge of MDC.

Idle. A high impedance state of the MDIO line. All tri-state drivers are disabled and the PHY's pull-up resistor pulls the MDIO line to logic 1. Note: At least one or more clocked idle states are required between frames.

Following are two examples of MII write and read instructions:

To put a transceiver with PHY address 00001 into Loopback mode, the following MII write instruction must be issued:

1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000 1...

To determine whether a PHY is in the link pass state, the following MII read instruction must be issued:

1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ 1...

For the MII read operation, the BCM5208R drives the MDIO line during the TA and Data fields (the last 17 bit times).

A final 65th clock pulse must be sent to close the transaction and to cause a write operation.

MII REGISTER MAP SUMMARY

Table 6 contains the MII register summary for each port of the BCM5208R. The register addresses are specified in hex form, and the name of register bits have been abbreviated. When writing to the reserved bits, always write a 0 value, and when reading from these bits, ignore the output value. Never write any value to an undefined register address. The reset value of the registers are shown in the INIT column.

Table 6: MII Register Map Summary

Addr	*Name*	*15*	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*	*INIT*
00h	**CONTROL**	Soft Reset	Loopback	Force10 0	AutoNeg Enable	Power Down	Isolate	Restart AutoNeg	Full Duplex	Collision Test	Reserved							3000h
01h	**STATUS**	T4 Capable (0)	TX FDX Capable	TX Capable	10BT FDX Capable	10BT Capable	Reserved				MF pream suppress	AutoNeg Complete	Reserved	AutoNeg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
02h	**PHYID HIGH**	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0040h
03h	**PHYID LOW**	0	1	1	0	0	0	Model # 0	1	0	0	1	1	Revision # 1	0	1	0	613Bh
04h	**AUTONEG ADVERTISE**	Next Page 0	Reserved	Remote Fault	Reserved Technologies		Pause	Adv T4 (0)	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	Advertised Selector Field [4:0] 0	0	0	0	1	01E1h
05h	**LINK PARTNER ABILITY**	LP Next Page	LP Acknowlg	LP Remote Fault	Reserved Technologies		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0]					0004h
06h	**AUTONEG EXPANSION**	Reserved											ParDet Fault	LP Next Pg Able	Next Pg Able	Page Recvd	LP Auto Neg Able	0004h
07h	**NEXT PAGE**	Next Page	Reserved	Message Page	Acknowledge2		Toggle	Message / Unformatted Code field										2001h
08h	**LP NEXT PAGE**	LP Next Page	Reserved	Message Page	Acknowledge2		Toggle	Message / Unformatted Code field										0000h
10h	**100BASE-X AUX CONTROL**	Reserved		Trans Disable	Reserved		Bypass 4B5B enc/dec	Bypass Scram/ Descram	Bypass NRZI enc/dec	Bypass rcv sym alignment	Baseline Wander cor Disable	Reserved						
11h	**100BASE-X AUX STATUS**	Reserved						Locked	Current 100 Link Status	Reserved		False Carrier Detected	Bad ESD Detected	RCV Error Detected	XMT Error Detected	Lock Error Detected	MLT3 Error Detected	
12h	**100BASE-X RCV ERROR COUNTER**	Reserved								Receive Error Counter								0000h
13h	**100BASE-X FALSE CARRIER COUNTER**	Reserved								False Carrier Sense Counter								0000h

Note 1: Reg 11h: Only bit 6 is qualified with TX Link. Other bits may be set in non-TX operation.

Table 6: MII Register Map Summary (Cont.)

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
14h	**Reserved**	Reserved																
15h	**Reserved**	Reserved																
16h	**Reserved**	Reserved																
17h	**PTEST**	Reserved - Write as Zero																0000h
18h	**AUXILIARY CONTROL/ STATUS**	Jabber Disable	Force Link	Reserved					TXDAC Power Mode	HSQ	LSQ	Edge Rate [1:0]		AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	003xh
19h	**AUXILIARY STATUS SUMMARY**	AutoNeg Complete	AutoNeg FLP-Link Good-Chk	AutoNeg Ack Detect	AutoNeg Ability Detect	AutoNeg Pause	AutoNeg HCD			AutoNeg ParDet Fault	LP Remote Fault	LP Page Rcvd	LP AutoNeg Able	SP100 Indicator	Link Status	Internal AutoNeg Enabled	Jabber Detect	0000h
1Ah	**INTERRUPT**	FDX LED Enable	INTR Enable	Reserved		FDX Mask	SPD Mask	Link Mask	INTR Mask	Reserved				FDX Change	SPD Change	Link Change	INTR Status	0F00h
1Bh	**AUXILLIARY MODE 2**	Reserved								Block 10BASE T Echo Mode	Traffic Meter LED Mode	Activity LED Force ON	Serial LED Mode	SQE Disable Mode	Reserved	Qual Parallel Detect Mode	Reserved	FF00h
1Ch	**10BASE-T AUX. ERROR & GENERAL STATUS**	Reserved					Manchstr Code Err (10BT)	EOF Err (10BT)	Polarity Err (10BT)	0	Revision # 0	1	Reserved	AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	00xxh
1Dh	**AUXILIARY MODE**	Reserved											Activity LEDs Force Inactive	Link LED Force Inactive	Reserved	Block TXEN Mode	Reserved	x000h
1Eh	**AUXILIARY MULTI-PHY**	HCD TX FDX	HCD T4 (0)	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart AutoNeg	AutoNeg Complete	FLP-Link Good-Chk	ACK Detect	Ability Detect	Super Isolate	Reserved		RXER Code Mode	0000h
1Fh	**BROADCOM Test**	Reserved - Do Not Write																

Note 2: Bit 0 is qualified with TX Link.

MII CONTROL REGISTER

The MII control register bit descriptions are shown in Table 7.

Table 7: MII Control Register (Address 00d, 00h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Reset	R/W (S/C)	1 = PHY reset 0= normal operation	0
14	Loopback	R/W	1 = loopback mode 0 = normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbps 0 = 10 Mbps	1
12	Auto-Negotiation Enable	R/W	1 = auto-negotiation enable 0 = auto-negotiation disable	1
11	Power Down	RO	0 = normal operation	0
10	Isolate	R/W	1 = electrically isolate PHY from MII 0 = normal operation	0
9	Restart Auto-Negotiation	R/W (S/C)	1 = restart Auto-Negotiation 0 = normal operation	0
8	Duplex Mode	R/W	1 = full-duplex 0 = half-duplex	0
7	Collision Test Enable	R/W	1 = collision test mode enable 0 = collision test mode disable	0
6:0	Reserved	RO	Ignore when Read	0

Note: *R/W = Read/Write, RO = Read Only, SC = Self Clear*

Reset. To reset the BCM5208R by software control, a “1” must be written to bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and does not need to be cleared using a second MII write. Writes to other control register bits have no effect until the reset process is completed, which requires approximately 1 µs. Writing a 0 to this bit has no effect. Because this bit is self-clearing, after a few cycles from a write operation, it returns a 0 when read.

Loopback. The BCM5208R can be placed into loopback mode by writing a 1 to bit 14 of the Control Register. The loopback mode can be cleared by writing a 0 to bit 14 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in software-controlled loopback mode, otherwise it returns a 0.

Forced Speed Selection. If Auto-Negotiation is enabled, this bit has no effect on the speed selection. However, if Auto-Negotiation is disabled by software control, the operating speed of the BCM5208R can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a 1 to this bit forces 100BASE-X operation, while writing a 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. To read the overall state of forced speed selection, including both hardware and software control, use bit 8 of the Auxiliary Control Register.

Auto-Negotiation Enable. Auto-Negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic 0, Auto-Negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of 0, Auto-Negotiation is disabled by software control. When Auto-Negotiation is disabled in this manner, writing a 1 to the same bit of the Control Register or resetting the chip re-enables Auto-Negotiation. Writing to this bit has no effect when Auto-Negotiation has been disabled by hardware control. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

Power Down. The BCM5208R does not implement a low power mode.

Isolate. Each individual PHY can be isolated from its Media Independent Interface by writing a 1 to bit 10 of the Control Register. All MII outputs are tri-stated and all MII inputs are ignored. Because the MII management interface is still active, the isolate mode can be cleared by writing a 0 to bit 10 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in isolate mode, otherwise it returns a 0.

Restart Auto-Negotiation. Bit 9 of the Control Register is a self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the Auto-Negotiation state machine. For this bit to have an effect, Auto-Negotiation must be enabled. Writing a 1 to this bit restarts the Auto-Negotiation, while writing a 0 to this bit has no effect. Because the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY Register.

Duplex Mode. By default, the BCM5208R powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a 1 to bit 8 of the Control Register while Auto-Negotiation is disabled. Half-duplex mode can be resumed by writing a 0 to bit 8 of the control register, or by resetting the chip.

Collision Test. The COL pin can be tested during loopback by activating the Collision Test mode. While in this mode, asserting TXEN causes the COL output to go high within 512 bit times. Deasserting TXEN causes the COL output to go low within 4 bit times. Writing a 1 to bit 7 of the Control Register enables the Collision Test mode. Writing a 0 to this bit or resetting the chip disables the Collision Test mode. When this bit is read, it returns a 1 when the Collision Test mode has been enabled, otherwise it returns a 0. This bit should only be set while in loopback test mode.

Reserved Bits. All reserved MII register bits must be written as 0 at all times. Ignore the BCM5208R output when these bits are read.

MII STATUS REGISTER

The MII status register bit descriptions are shown in Table 8.

Table 8: MII Status Register (Address 01d, 01h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore when read	0
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	0
4	Reserved	RO	Write as “0”, Ignore when read	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable 0 = Not Auto-Negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link Pass state) 0 = Link is down (Link Fail state)	0

Table 8: MII Status Register (Address 01d, 01h) (Cont.)

Bit	Name	R/W	Description	Default
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)*

100BASE-T4 Capability. The BCM5208R is not capable of 100BASE-T4 operation, and returns a 0 when bit 15 of the status register is read.

100BASE-X Full-Duplex Capability. The BCM5208R is capable of 100BASE-X full-duplex operation, and returns a 1 when bit 14 of the Status Register is read.

100BASE-X Half-Duplex Capability. The BCM5208R is capable of 100BASE-X half-duplex operation, and returns a 1 when bit 13 of the Status Register is read.

10BASE-T Full-Duplex Capability. The BCM5208R is capable of 10BASE-T full-duplex operation, and returns a 1 when bit 12 of the Status Register is read.

10BASE-T Half-Duplex Capability. The BCM5208R is capable of 10BASE-T half-duplex operation, and returns a 1 when bit 11 of the Status Register is read.

Reserved Bits. Ignore the BCM5208R output when these bits are read.

MF Preamble Suppression. This bit is the only writable bit in the Status Register. Setting this bit to a “1” allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When Preamble Suppression is enabled, only 2 preamble bits are required between successive Management Commands, instead of the normal 32.

Auto-Negotiation Complete. Bit 5 of the Status Register returns a 1 if the Auto-Negotiation process has been completed and the contents of registers 4, 5 and 6 are valid.

Auto-Negotiation Capability. The BCM5208R is capable of performing IEEE Auto-Negotiation, and will return a 1 when bit 4 of the Status Register is read, regardless of whether or not the Auto-Negotiation function has been disabled.

Link Status. The BCM5208R returns a 1 on bit 2 of the Status Register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the Link Pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the Link Pass state has been entered again.

Jabber Detect. 10BASE-T operation only. The BCM5208R returns a 1 on bit 1 of the Status Register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability. The BCM5208R supports extended capability registers, and returns a 1 when bit 0 of the Status Register is read. Several extended registers have been implemented in the BCM5208R, and their bit functions are defined later in this section.

PHY IDENTIFIER REGISTERS

The physical indentifier registers bit descriptions are shown in Table 9.

Table 9: PHY Indentifier Registers (Address 02d, 02h, 03d, and 03h)

Bit	*Name*	*R/W*	*Description*	*Value*
15:0	MII Address 00010	RO	PHYID HIGH	0040h
15:0	MII Address 00011	RO	PHYID LOW	613Bh
Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*				

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24 bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5208R part, 13h, and Broadcom Revision number, 01h, is placed into two MII Registers. The translation from OUI, Model Number and Revision Number to PHY Identifier Register occurs as follows:

- PHYID HIGH [15:0] = OUI[21:6]
- PHYID LOW [15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

The two most significant bits of the OUI are not represented (OUI[23:22]).

Table 9 shows the result of concatenating these values in order to form the MII Identifier Registers PHYID HIGH and PHYID LOW.

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 10 shows the auto-negotiation advertisement register bit descriptions.

Table 10: Auto-Negotiation Advertisement Register (Address 04d and 04h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Next Page Ability enabled 0 = Next Page Ability disabled	0
14	Reserved	RO	Ignore when read	
13	Remote Fault	R/W	1 = Transmit Remote Fault	0
12:11	Reserved Technologies	RO	Ignore when read	
10	Advertise Pause Capability	R/W	1 = Pause Operation for full-duplex	0
9	Advertise 100BASE-T4	R/W	0 = Do not advertise T4 capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X full-duplex 0 = Do not advertise 100BASE-X full-duplex	1
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex 0 = Do not advertise 10BASE-T full-duplex	1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	RO	Fixed value: indicates 802.3	00001
Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*				

Next Page. The BCM5208R supports Next Page Capability.

Remote Fault. Writing a 1 to bit 13 of the Advertisement Register sends a Remote Fault indicator to the Link Partner during Auto-Negotiation. Writing a 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else 0 if no write has been completed since the last chip reset.

Reserved Bits. Ignore output when read.

Pause Operation for Full-Duplex Links. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

Advertisement Bits. Bits 9:5 of the Advertisement Register allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM5208R. By writing a 1 to any of the bits, the corresponding ability is transmitted to the Link Partner. Writing a 0 to any bit suppresses the corresponding ability from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset. Even though bit 9, Advertise 100BASE-T4 is writable, it should never be set because the BCM5208R is incapable of the T4 operation.

Selector Field. Bits 4:0 of the Advertisement register contain the fixed value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 11 shows the auto-negotiation link partner ability register bit descriptions.

Table 11: Auto-Negotiation Link Partner Ability Register (Address 05d, 05h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	LP Next Page	RO	Link Partner next page bit	0
14	LP Acknowledge	RO	Link Partner acknowledge bit	0
13	LP Remote Fault	RO	Link Partner remote fault indicator	0
12:11	Reserved Technologies	RO	Ignore when read	000
10	LP Advertise Pause	RO	Link Partner has Pause Capability	0
9	LP Advertise 100BASE-T4	RO	Link Partner has 100BASE-T4 capability	0
8	LP Advertise 100BASE-X FDX	RO	Link Partner has 100BASE-X FDX capability	0
7	LP Advertise 100BASE-X	RO	Link Partner has 100BASE-X capability	0
6	LP Advertise 10BASE-T FDX	RO	Link Partner has 10BASE-T FDX capability	0
5	LP Advertise 10BASE-T	RO	Link Partner has 10BASE-T capability	0
4:0	Link Partner Selector Field	RO	Link Partner selector field	00000

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

The values contained in the Auto-Negotiation Link Partner Ability Register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 5 of the MII Status Register.

Next Page. Bit 15 of the Link Partner Ability Register returns a value of 1 when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit.

Acknowledge. Bit 14 of the Link Partner Ability Register is used by Auto-Negotiation to indicate that a device has successfully received its Link Partner's Link Code Word.

Remote Fault. Bit 13 of the Link Partner Ability Register returns a value of 1 when the Link Partner signals that a remote fault has occurred. The BCM5208R simply copies the value to this register and does not act upon it.

Reserved Bits. Ignore when Read.

Pause. Indicates that the link partner pause bit is set.

Advertisement Bits. Bits 9:5 of the Link Partner Ability Register reflect the abilities of the Link Partner. A 1 on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time Auto-Negotiation is restarted or the BCM5208R is reset.

Selector Field. Bits 4:0 of the Link Partner Ability Register reflect the value of the Link Partner's selector field. These bits are cleared any time Auto-Negotiation is restarted or the chip is reset.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 12 shows the auto-negotiation expansion register bit descriptions.

Table 12: Auto-Negotiation Expansion Register (Address 06d and 06h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	RO	Ignore when Read	
4	Parallel Detection Fault	RO LH	1 = Parallel Detection fault 0 = No Parallel Detection fault	0
3	Link Partner Next Page Able	RO	1 = Link Partner has Next Page capability 0 = Link Partner does not have Next Page	0
2	Next Page Able	RO	1 = Next Page Able	1
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto-Negotiation Able	RO LH	1 = Link Partner has Auto-Negotiation capability 0 = Link Partner does not have Auto-Negotiation	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)*

Parallel Detection Fault. Bit 4 of the Auto-Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto-Negotiation state machine. For further details, please refer to the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Able. Bit 3 of the Auto-Negotiation Expansion Register returns a 1 when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Page Received. Bit 1 of the Auto-Negotiation Expansion Register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

Link Partner Auto-Negotiation Able. Bit 0 of the Auto-Negotiation Expansion Register returns a 1 when the Link Partner is known to have Auto-Negotiation capability. Before any Auto-Negotiation information is exchanged, or if the Link Partner does not comply with IEEE Auto-Negotiation, the bit returns a value of 0.

AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

Table 13 shows the auto-negotiation Next Page Transmit register bit descriptions.

Table 13: Next Page Transmit Register (Address 07d, 07h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	R/W	1 = Additional Next Page(s) will follow 0 = Last page	0
14	Reserved	R/W	Ignore when Read	0
13	Message Page	R/W	1= Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	0
10:0	Message/Unformatted Code Field	R/W		1

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Next Page. Indicates whether this is the last Next Page to be transmitted.

Message Page. Differentiates a Message Page from an Unformatted Page.

Acknowledge 2. Indicates that a device has the ability to comply with the message.

Toggle. Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field, which may contain an arbitrary value.

AUTO-NEGOTIATION LINK PARTNER (LP) NEXT PAGE TRANSMIT REGISTER

Table 14 shows the auto-negotiation link partner register bit descriptions.

Table 14: Next Page Transmit Register (Address 08d, 08h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Next Page	RO	1 = Additional Next Page(s) will follow 0 = Last page	0
14	Reserved	RO	Ignore when read	0
13	Message Page	RO	1= Message page 0 = Unformatted page	0
12	Acknowledge 2	RO	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	0
10:0	Message/Unformatted Code Field	RO		0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Next Page. Indicates whether this is the last Next Page.

Message Page. Differentiates a Message Page from an Unformatted Page.

Acknowledge 2. Indicates that Link Partner has the ability to comply with the message.

Toggle. Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An 11-bit-wide field, encoding 2048 possible messages.

Unformatted Code Field. An 11-bit-wide field, which may contain an arbitrary value.

100BASE-X Auxiliary Control Register

The 100BASE-X auxiliary control register bit descriptions are shown in Table 15.

Table 15: 100BASE-X Auxiliary Control Register (Address 16d, 10h)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Write as 0, ignore when read	0
13	Transmit Disable	R/W	1 = transmitter disabled in PHY 0 = normal operation	0
12:11	Reserved	R/W	Write as 0, ignore when read	0
10	Bypass 4B5B Encoder/Decoder	R/W	1 = Transmit and receive 5B codes over MII pins 0 = Normal MII interface	0
9	Bypass Scrambler/Descrambler	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass NRZI Encoder/Decoder	R/W	1 = NRZI encoder and decoder is disabled 0 = NRZI encoder and decoder is enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = Baseline wander correction disabled 0 = Baseline wander correction enabled	0
5:0	Reserved	R/W	Write as 000000; ignore when read	000000

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Transmit Disable. The transmitter can be disabled by writing a 1 to bit 13 of MII Register 10h. When the transmitter is disabled, in the TX mode, the transmitter output (TD±) is forced into MLT3 zero value. The transmitter is enabled at reset, as well as when a 0 is written to this bit.

Bypass 4B5B Encoder/Decoder. The 4B5B encoder and decoder may be bypassed by writing a “1” to bit 10 of MII Register 10h. The transmitter sends 5B codes from the TXER and TXD[3:0] pins directly to the scrambler. TXEN is ignored and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places de-scrambled and aligned 5B codes onto the RXER and RXD[3:0] pins. CRS is still asserted when a valid frame is received.

Bypass Scrambler/Descrambler. The stream cipher function can be disabled by writing a 1 to bit 9 of MII register 10h. The stream cipher function can be re-enabled by writing a 0 to this bit.

Bypass NRZI Encoder/Decoder. The NRZI encoder and decoder can be bypassed by writing a 1 to bit 8 of the MII Register 10h, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) can be re-enabled by writing a 0 to this bit.

Bypass Receive Symbol Alignment. Receive symbol alignment can be bypassed by writing a 1 to bit 7 of MII Register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes are placed directly on the RXER and RXD[3:0] pins.

Baseline Wander Correction Disable. The baseline wander correction circuit can be disabled by writing a 1 to bit 6 of MII register 10h. The BCM5208R corrects for baseline wander on the receive data signal when this bit is cleared.

Reserved Bits. The Reserved bits of the 100BASE-X Auxiliary Control Register must be written as 0 at all times. Ignore the BCM5208R outputs when these bits are read.

100BASE-X AUXILIARY STATUS REGISTER

See Table 16 for an explanation of the bit descriptions for the 100BASE-X auxiliary status register.

Table 16: 100BASE-X Auxiliary Status Register (Address 17d, 11h)

Bit	*Name*	*R/W*	*Description*	*Default*
15:10	Reserved	RO	Ignore when read	000000
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7:6	Reserved	RO	Ignore on Read	00
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 =No false carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = No ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 =No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High, (LL and LH clear after read operation)*

Locked. The PHY returns a 1 in bit 9 when the de-scrambler is locked to the incoming data stream. Otherwise it returns a 0.

Current 100BASE-X Link Status. The PHY returns a 1 in bit 8 when the 100BASE-X link status is good. Otherwise it returns a 0.

False Carrier Detected. The PHY returns a 1 in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise it returns a 0.

Bad ESD Detected. The PHY returns a 1 in bit 4 if an end of stream delimiter error has been detected since the last time this register was read. Otherwise it returns a 0.

Receive Error Detected. The PHY returns a 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise it returns a 0.

Transmit Error Detected. The PHY returns a 1 in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise it returns a 0.

Lock Error Detected. The PHY returns a 1 in bit 1 if the de-scrambler has lost lock since the last time this register was read. Otherwise it returns a 0.

MLT3 Code Error Detected. The PHY returns a 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise it returns a 0.

100BASE-X Receive Error Counter

The 100BASE-X receive error counter increments each time the BCM5208R receives a non-collision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting Receive Errors until cleared. See Table 17 for the bit descriptions.

Table 17: 100BASE-X Receive Error Counter (Address 18d, 012h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as “00h”; ignore when read	00h
7:0	Receive Error Counter	R/W	Number of Non-Collision packets with Receive Errors since last read	00h

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

100BASE-X False Carrier Sense Counter

The 100BASE-X false carrier sense counter increments each time the BCM5208R detects a false carrier on the receive input. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting False Carrier Sense Errors until cleared. See Table 18 for the bit descriptions.

Table 18: 100BASE-X False Carrier Sense Counter (Address 19d, 13h)

Bit	Name	R/W	Description	Default
15:8	Reserved	RO	Write as “00h”, ignore when read	00h
7:0	False Carrier Sense Counter	R/W	Number of False Carrier Sense events since last read	00h

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

AUXILIARY CONTROL/STATUS REGISTER

Table 19 shows the auxiliary control/status register bit descriptions.

Table 19: Auxiliary Control/Status Register (Address 24d, 18h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Jabber Disable	R/W	1= Jabber function disabled in PHY 0 = Jabber function enabled in PHY	0
14	Link Disable	R/W	1= Link Integrity test disabled in PHY 0 = Link Integrity test is enabled in PHY	0
13:8	Reserved	RO	Ignore when read	000000
7:6	HSQ : LSQ	R/W	These two bits define the Squelch Mode of the 10BASE-T Carrier Sense mechanism: 00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Not allowed	00
5:4	Edge Rate [1:0]	R/W	00 = 1 ns 01 = 2 ns 10 = 3 ns 11 = 4 ns	11
3	Auto-Negotiation Indicator	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Jabber Disable. 10BASE-T operation only. Bit 15 of the Auxiliary Control Register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a 1 to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

Link Disable. Writing a 1 to bit 14 of the Auxiliary Control Register allows the user to disable the Link Integrity state machines and place the BCM5208R into forced Link Pass status. Writing a 0 to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

Test Mode. Active-high test mode control bit. Must be written with 0 for normal operation.

HSQ and LSQ. Extend or decrease the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high- and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5208R to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high

level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Edge Rate. Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode. These bits are logically ANDed with the ER[1:0] input pins to produce the internal edge-rate controls (Edge_Rate[1] AND ER[1], Edge_Rate[0] AND ER[0]).

Auto-Negotiation Indicator. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5208R. A combination of a 1 in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 3 of the Auxiliary Control Register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 0 when one of following cases is true:

- The ANEN pin is low AND the F100 pin is low.
- Bit 12 of the Control Register has been written 0 AND bit 13 of the Control Register has been written 0. When bit 8 of the Auxiliary Control Register is 0, the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. Bit 1 of the Auxiliary Control Register is a read-only bit that shows the true current operation speed of the BCM5208R. A 1 bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208R is always operating at 10BASE-T speed.

Full-Duplex Indication. Bit 0 of the Auxiliary Control Register is a read-only bit that returns a 1 when the BCM5208R is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY STATUS SUMMARY REGISTER

The auxiliary status summary register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bitsare included with their primary register descriptions in this document. Bits 10:8, the Auto-Negotiation HCD, are only set for full Auto-Negotiation process, and not for either Parallel Detection or forced-speed modes. Table 20 shows the bit descriptions.

Table 20: Auxiliary Status Summary Register (Address 25d, 19h)

Bit	*Name*	*R/W*	*Description*	*Default*
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed	0
14	Auto-Negotiation Flp-Link Good-Check	RO LH	1 = Auto-Negotiation FLP-Link Good Check	0
13	Auto-Negotiation Acknowl-edge Detected	RO LH	1 = Auto-Negotiation acknowledge detected	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-Negotiation for link partner ability	0
11	Auto-Negotiation Pause	RO	BCM5208R and link partner Pause Operation bit set	0
10:8	Auto-Negotiation HCD	RO	000 = No Highest Common Denominator 001 = 10BASE-T 010 = 10BASE-T full-duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX full-duplex 11x = Undefined	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel Detection fault	0
6	Link Partner Remote Fault	RO		
5	Link Partner Page Received	RO LH	1 = New Page has been received	0
4	Link Partner Auto-Negotiation Able	RO	1 = Link Partner is Auto-Negotiation capable	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	0
2	Link Status	RO LL	1 = Link is up (link pass state)	0
1	Auto-Negotiation Enabled	RO	1 = Auto-Negotiation enabled	1
0	Jabber Detect	RO LL	1 = Jabber condition detected	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

INTERRUPT REGISTER

Table 21 shows the bit descriptions for the interrupt register.

Table 21: Interrupt Register (Address 26d, 1Ah)

Bit	*Name*	*R/W*	*DESCRIPTION*	*Default*
15	FDX LED Enable	R/W	Full-Duplex LED Enable	0, see Note A
14	INTR Enable	R/W	Interrupt Enable	0
13:12	Reserved	RO		0
11	FDX Mask	R/W	Full-Duplex Interrupt Mask	1
10	SPD Mask	R/W	SPEED Interrupt Mask	1
9	LINK Mask	R/W	LINK Interrupt Mask	1
8	INTR Mask	R/W	Master Interrupt Mask	1
7:4	Reserved	RO		0
3	FDX Change	RO LH	Duplex Change Interrupt	0
2	SPD Change	RO LH	Speed Change Interrupt	0
1	LINK Change	RO LH	Link Change Interrupt	0
0	INTR Status	RO LH	Interrupt Status	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Note A: *This bit defaults to a '1' only when LNKLED#{1} is pulled down and LNKLED#{4} is pulled up during power-on reset.*

FDX LED Enable. Setting this bit enables the FDX LED mode. Bits 14 and 15 of this register are mutually exclusive. Only one can be set at a time. When FDXLED mode is enabled, XMTLED# becomes FDXLED# and RCVLED# becomes ACTLED#.

Interrupt Enable. Setting this bit enables Interrupt Mode. Bits 14 and 15 of this register are mutually exclusive. Only one can be set at a time. When Interrupt Mode is enabled, XMTLED# becomes INTR# and RCVLED# becomes ACTLED#. If both bits 14 and 15 are set at the same time, the FDXLED# overrides the INTR# output, even though the interrupt's FDX, SPD, and LINK change status bits will behave as in normal interrupt operation.

FDX Mask. When this bit is set, changes in duplex mode do not generate an interrupt.

SPD Mask. When this bit is set, changes in operating speed do not generate an interrupt.

Link Mask. When this bit is set, changes in link status do not generate an interrupt.

Interrupt Mask. Master Interrupt Mask. When this bit is set, no interrupts are generated, regardless of the state of the other MASK bits.

FDX Change. A 1 indicates a change of duplex status since the last register read. A register read clears the bit.

SPD Change. A 1 indicates a change of speed status since the last register read. A register read clears the bit.

Link Change. A 1 indicates a change of link status since the last register read. A register read clears the bit.

Interrupt Status. Represents status of the INTR# pin. A 1 indicates that the interrupt mask is off and that one or more of the change bits are set. A register read clears the bit.

AUXILIARY MODE 2 REGISTER

The bit descriptions for auxiliary mode 2 register are shown in Table 22.

Table 22: Auxiliary Mode 2 (Address 27d, 1Bh)

Bit	*Name*	*R/W*	*DESCRIPTION*	*Default*
15:8	Reserved	RO	Ignore when read	FFh
7	Block 10BASE-T Echo Mode	R/W	1=10BASE-T half-duplex TXEN does not echo onto RXDV 0=10BASE-T half-duplex TXEN echoes onto RXDV	0, see Note B
6	Traffic Meter LED Mode	R/W	1=Traffic Meter LED Mode ON 0=Traffic Meter LED Mode OFF	0
5	Activity LED Force ON	R/W	1=Activity LEDs forced ON 0=Activity LEDs not forced	0
4	Serial LED Mode	R/W	1=Serial LED Mode enabled 0=Serial LED Mode disabled	0, see Note C
3	SQE Disable Mode	R/W	1=SQE not transmitted in 10BASE-T half-duplex 0=SQE transmitted in 10BASE-T half-duplex	0, see Note B
2	Reserved	RO	Ignore when read	0
1	Qual Parallel Detect Mode	R/W	1=Parallel Detect Qualification Mode ON 0=Parallel Detect Qualification Mode OFF	0, see Note B
0	Reserved	RO	Ignore when read	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Note B: *This bit defaults to a "1" if LNKLED#{1} is pulled low during power-on reset.*

Note C: *This bit defaults to a "1" if both LNKLED#{1} and LNKLED#{4} are pulled low during power-on reset.*

Block 10BASE-T Echo Mode. Default 0. When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal will not echo onto the RXDV pin. The TXEN will echo onto the CRS pin, and the CRS deassertion directly follow the TXEN deassertion.

Traffic Meter LED Mode. Default is 0. When asserted, the Receive and Transmit (Activity) LEDs (XMTLED# and RCV-LED# pins) do not blink based on the internal LED-CLK (approximately 80ms ON time). Instead, they blink based on the rate of Receive and Transmit activity. Each time a Receive or a Transmit operation occurs, the respective LED turns on for a minimum of 5ms. With light traffic, the LEDs blink at a low rate. During medium to heavy traffic (packets within 5ms of each other), the LEDs remain on.

Activity LED Force On. Default is 0. When asserted, the Receive and Transmit (Activity) LEDs (XMTLED# and RCV-LED# pins) are turned on. When 0, they have no effect on the Activity LEDs. The Activity Force ON bit has higher priority than Activity LED Force Inactive, bit 4, Register 1Dh.

Serial LED Mode. Default is 0. When asserted, the 4 slices' LED outputs will be serially shifted out on the 2nd slices' LED outputs.

The sequence of outputs for the different Serial modes are: FDX, Global Interrupt, Speed, Link, Slice Interrupt, Activity when the Interrupt mode is set; FDX, '1', Speed, Link, FDX, Activity when the FDXLED mode is set and, FDX, '1', Speed, Link, Transmit, Receive when neither Interrupt nor FDXLED modes are selected. When this bit is 0, the four LED outputs per slice are operated in parallel. See Table 3 on page 6 for more details.

SQE Disable Mode. Default is 0. When asserted, disables SQE pulses when operating in 10BASE-T half-duplex mode.

Qualified Parallel Detect Mode. This bit allows the Auto-Negotiation/Parallel Detection process to be qualified with information in the Advertisement Register. Default value is 0.

If this bit is not set, and the local BCM5208R device is enabled to Auto-Negotiate and the far-end device is a 10BASE-T or 100BASE-TX non-Auto-Negotiating legacy type, the local device Auto-Negotiate/Parallel detects the far-end device, regardless of the contents of its Advertisement Register, 04h.

If this bit is set, the local device compares the link speed detected to the contents of its Advertisement Register. If the particular link speed is enabled in the Advertisement register, the local device asserts link. If the link speed is disabled in this register, then the local device does not assert link and continues monitoring for a matching capability link speed.

10BASE-T Auxiliary Error and General Status Register

The bit descriptions for the 10BASE-T auxiliary error and general status register are shown in Table 23.

All error bits in the auxiliary error status register are read-only and are latched high. When certain types of errors occur in the BCM5208R, one or more corresponding error bits become "1". They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RXER output pin at the time the error occurs.

Table 23: 10BASE-T Auxiliary Error and General Status Register (Address 28d, 1Ch)

Bit	*Name*	*R/W*	*Description*	*Default*
15:11	Reserved	RO	Ignore when read	x
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T)	0
9	EOF Error	RO	1 = EOF detection error (10BASE-T)	0
8	Polarity Inversion	RO	1 = Channel Polarity Inverted 0 = Channel Polarity Correct	0
7:5	Revision	RO	Revision Number	001
4	Reserved	RO	Ignore when read	0
3	Auto-Negotiation Indication	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

Manchester Code Error. Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

EOF Error. Indicates that the EOF (end of frame) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

Polarity. Reflects the Polarity status of the receive channel pair. The BCM5208R can automatically invert the polarity of the receive channel. No data errors are reported to indicate that the automatic polarity inversion is occurring. Instead, this bit returns a 1 whenever the polarity of the receive channel is inverted.

Revision. Read-only bits that return the revision number of the BCM5208R. The current revision is labelled 001.

Auto-Negotiation Indication. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5208R. A combination of a 1 in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 15 of the Auxiliary Mode Register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 0 when one of following cases is true:

- The ANEN pin is low AND the F100 pin is low.
- Bit 12 of the Control Register has been written 0 AND bit 13 of the Control Register has been written 0.

When bit 8 of the Auxiliary Control Register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. A read-only bit that shows the true current operation speed of the BCM5208R. A 1 bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5208R is always operating at 10BASE-T speed.

Full-Duplex Indication. A read-only bit that returns a 1 when the BCM5208R is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY MODE REGISTER

The bit descriptions for the auxiliary mode register are shown in Table 24.

Table 24: Auxiliary Mode Register (Address 29d, 1Dh)

Bit	*Name*	*R/W*	*Description*	*Default*
15:5	Reserved	R/W	Write as “000h”, ignore when read	000h
4	Activity LEDs Force Inactive		1 = Disable XMT/RCV Activity LED outputs 0 = Allow XMT/RCV Activity LED outputs	0
3	Link LED Force Inactive		1 = Disable Link LED output 0 = Allow Link LED output	0
2	Reserved	RO		0
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0
0	Reserved	RO		0
Note: *Default is 00 for all PHYs if RPTR pin is high during reset*				

Activity LEDs Force Inactive. When set to 1, the XMTLED# and RCVLED# output pins are forced into their inactive state regardless of the mode (normal, FDX, Interrupt, or Serial) these outputs are configured to. When 0, XMTLED# and RCVLED# output pins are enabled.

Link LED Force Inactive. When set to 1, the Link LED output pin is forced into its inactive state. When 0, Link LED output is enabled.

Block TXEN Mode. When this mode is enabled, short IPGs of 1, 2, 3 or 4 TXC cycles all result in the insertion of two IDLEs before the beginning of the next packet's JK symbols.

AUXILIARY MULTIPLE PHY REGISTER

The bit descriptions for the auxiliary multiple PHY register are shown in Table 25.

Table 25: Auxiliary Multiple PHY Register (Address 30d, 1Eh)

Bit	*Name*	*R/W*	*Description*	*Default*
15	HCD_TX_FDX	RO	1 = Auto-Negotiation result is 100BASE-TX full-duplex	0
14	HCD_T4	RO	0 = BCM5208R does not support 100BASE-T4 ability	0
13	HCD_TX	RO	1 = Auto-Negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto-Negotiation result is 10BASE-T full-duplex	0
11	HCD_10BASE-T	RO	1 = Auto-Negotiation result is 10BASE-T	0
10:9	Reserved	RO	Ignore when read	0
8	Restart Auto-Negotiation	R/W (SC)	1 = Restart Auto-Negotiation process 0 = (No effect)	0
7	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process Completed 0 = Auto-Negotiation process not Completed	0
6	FLP-Link Good-Check	RO	1 = Auto-Negotiation FLP-Link Good-Check	0
5	Acknowledge Detected	RO	1 = Auto-Negotiation Acknowledge Detected	0
4	Ability Detect	RO	1 = Auto-Negotiation waiting for LP Ability	0
3	Super Isolate	R/W	1 = Super Isolate mode 0 = Normal Operation	0
2:1	Reserved	R/W	Write as "00", ignore when read	00
0	RXER Code Mode	R/W	1 = Enable RXER Code Mode 0 = Disable RXER Code Mode	0

Note: *R/W = Read/Write, RO = Read only, SC = Self Clear, LL = Latched Low, LH = Latched High (LL and LH clear after read operation)*

HCD Bits. Bits 15:11 of the Auxiliary Multiple PHY Register are five read-only bits that report the Highest Common Denominator (HCD) result of the Auto-Negotiation process. Immediately upon entering the Link Pass state after each reset or Restart Auto-Negotiation, only one of these five bits is 1. The Link Pass state is identified by a 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time Auto-Negotiation is restarted or the BCM5208R is reset. Note that for their intended application, these bits uniquely identify the HCD only after the first Link Pass after reset or restart of Auto-Negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the Link Partner is different, more than one of the above bits may be active. These bits are only set for full Auto-Negotiation hand-shake, and not for Parallel Detection of Forced speed modes. Note that bit 14, HCD_T4, is never set in the BCM5208R.

Restart Auto-Negotiation. A self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, Auto-Negotiation must be enabled. Writing a 1 to this bit restarts Auto-Negotiation. Since the bit is self-clearing, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Control Register.

Auto-Negotiation Complete. This read-only bit returns a 1 after the Auto-Negotiation process has been completed. It remains 1 until the Auto-Negotiation process is restarted, a Link Fault occurs, or the chip is reset. If Auto-Negotiation is disabled or the process is still in progress, the bit returns a 0.

FLP-Link Good-Check. This read-only bit returns a 1 when the Auto-Negotiation arbitrator state machine has entered the FLP-link Good-Check state. It remains this value until the Auto-Negotiation process is restarted, a Link Fault occurs, Auto-Negotiation is disabled, or the BCM5208R is reset.

Acknowledge Detected. This read-only bit is set to 1 when the Arbitrator state machine exits the Acknowledged Detect state. It remains high until the Auto-Negotiation process is restarted, or the BCM5208R is reset.

Ability Detect. This read-only bit returns a 1 when the Auto-Negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the Auto-Negotiation process begins, and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns a 0 any time the Auto-Negotiation state machine is not in the Ability Detect state.

Super Isolate. Writing a 1 to this bit places the BCM5208R into the Super Isolate mode. Similar to the Isolate mode, all MII inputs are ignored, and all MII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5208R to coexist with another PHY on the same adapter card, with only one being activated at any time.

RXER Code Mode. Writing a 1 to bit 0 of the Auxiliary Mode Register enables the RXER Code mode during 10BASE-T operation. In this mode, when a receive data error occurs, indicated by pins RXDV=1 and RXER=1, the RXD[3:0] bus contains a non-zero 4-bit encoded value indicating the type of error. This feature provides the user with more detailed information regarding the status of the system. Writing a 0 to this bit or resetting the chip restores normal operation.

Note that this mode does not disrupt normal communication with the MAC layer, and can safely be used at all times. Also, please note that the RXER Code mode is not available in 10BASE-T Serial mode. In 100BASE-X operation, the RXER code mode is always active. See Table 2 on page 4 for more information.

BROADCOM TEST REGISTER

The Broadcom test register bits are reserved and should never be written.

Table 26: Broadcom Test (Address 31d, 1Fh)

Bit	*Name*	*R/W*	*DESCRIPTION*	*Default*
Reserved—Do Not Write				

Section 6: Timing and AC Characteristics

All MII Interface pins comply with IEEE 802.3u timing specifications (See Reconciliation Sub-layer and Media Independent Interface in IEEE 802.3u timing specifications). All digital output timing is specified at C_L = 30 pF.

Output rise/fall times are measured between 10% and 90% of the output signal swing. Input rise/fall times are measured between V_{IL} max. and V_{IH} min. Output signal transitions are referenced to the midpoint of the output signal swing. Input signal transitions are referenced to the midpoint between V_{IL} max. and V_{IH} min. See Table 27 and Table 28 for timing parameters. See Figure 4 on page 41 for an illustration of clock and reset timing.

Table 27: Clock Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
CK25 Cycle Time	CK_CYCLE	39.998	40	40.002	ns
CK25 High/Low Time	CK_HI CK_LO	18	20	22	ns
CK25 Rise/Fall Time	CK_EDGE	–	–	4	ns

Table 28: Reset Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Reset Pulse Length with stable CK25 Input	RESET_LEN	400	–	–	ns
Activity after end of Reset	RESET_WAIT	100	–	–	µs
RESET Rise/Fall Time	RESET_EDGE	–	–	10	ns

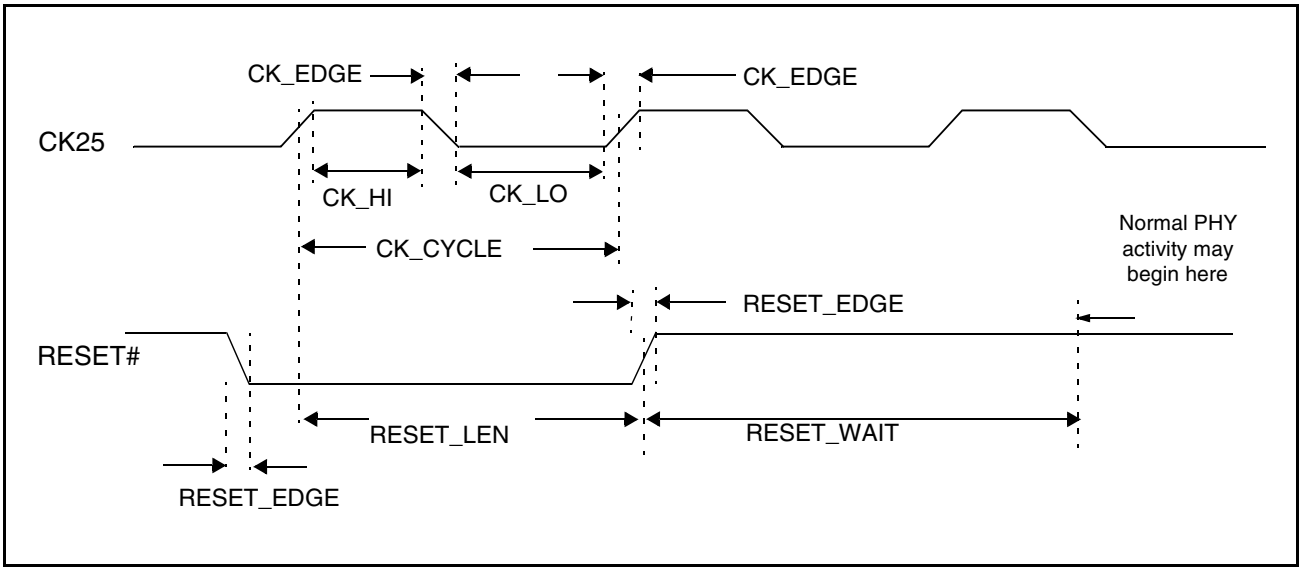


Figure 4: Clock and Reset Timing

Table 29 provides the parameters for 100BASE-X transmit timing. Figure 5 on page 42 illustrates 100BASE-TX transmit start of packet timing and Figure 6 on page 43 shows the 100BASE-TX transmit end of packet timing.

Table 29: 100BASE-X Transmit Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
TXC Cycle Time			40		ns
TXC High/Low Time		16	20	24	ns
TXC Rise/Fall Time		2	–	5	ns
TXEN, TXER, TXD[3:0] Setup Time to TXC rising	TXEN_SETUP	12	–		ns
TXEN, TXER, TXD[3:0] Hold Time from TXC rising	TXEN_HOLD	0	–	–	ns
TD± after TXEN Assert	TXEN_TDATA	60	–	80	ns
TXD to TD± Steady State Delay	TXD_TDATA	60	–	80	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	–	30	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	–	30	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL	–	–	30	ns
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP	–	–	30	ns
TXEN, TXER, TXD[3:0] Setup Time to CK25 rising		2	–	--	ns
TXEN, TXER, TXD[3:0] Hold Time from CK25 rising		10	–	–	ns

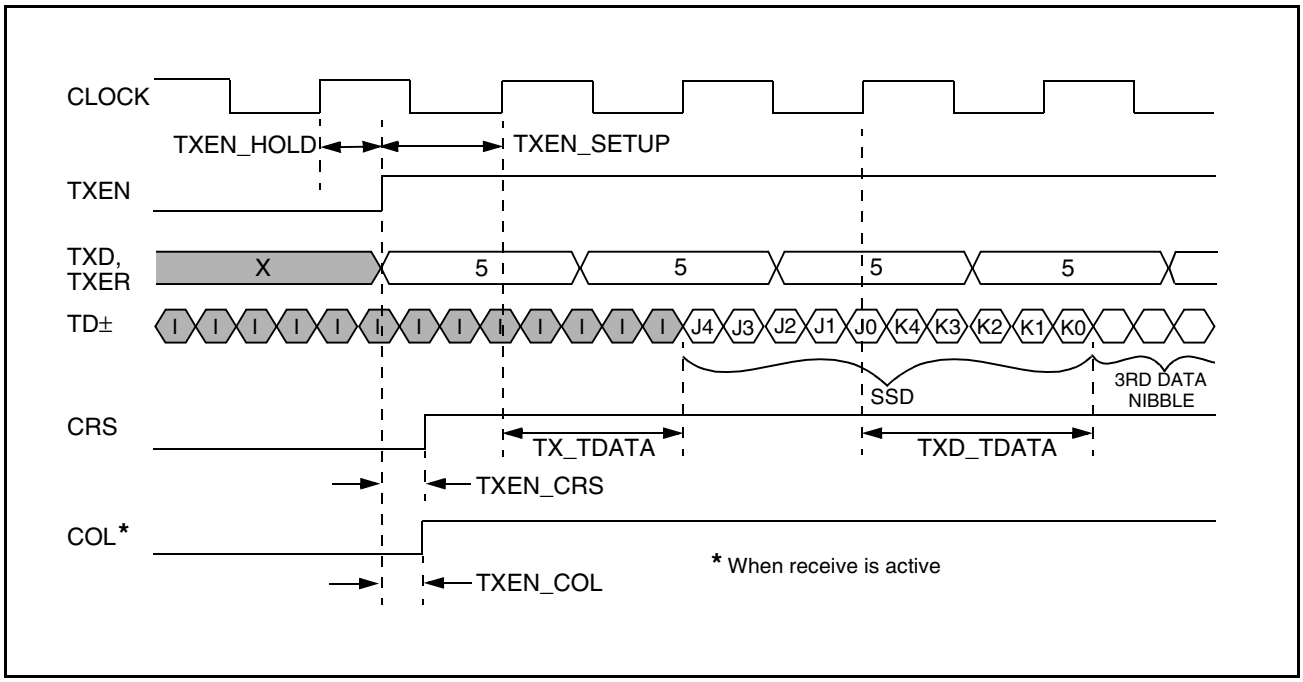


Figure 5: Transmit Start of Packet Timing (100BASE-TX)

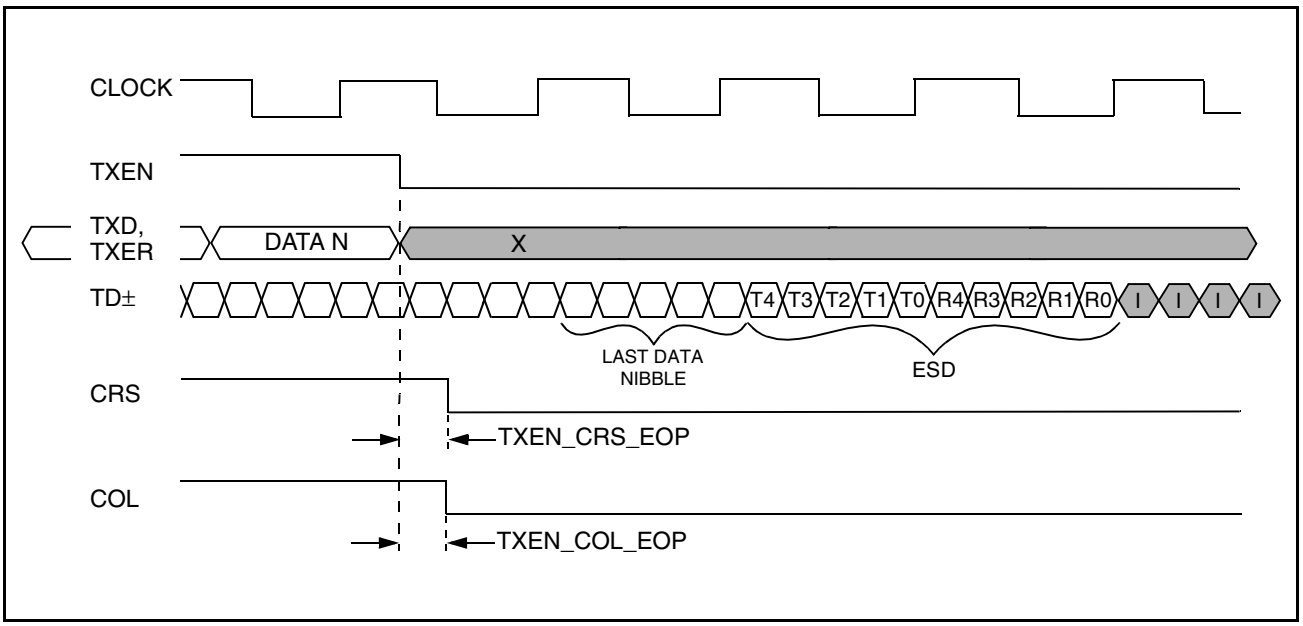


Figure 6: Transmit End of Packet Timing (100 Base-TX)

Table 30 provides the parameters for 10BASE-T transmit timing.

Table 30: 10BASE-T Transmit Timing—Parallel Mode

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
TXC Cycle Time (10BASE-T)	TXC_CYCLE	395	400	405	ns
TXC High/Low Time (10BASE-T)		197.5	200	202.5	ns
TXC Rise/Fall Time		2		5	ns
TXEN, TXD[3:0] valid after TXC Rising	TXEN_VALID			25	ns
TXEN, TXD[3:0] Hold after to TXC Rising	TXEN_HOLD_DTE	75			ns
TD+/- after TXEN Assert	TXEN_TDATA	–	400	450	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	50	100	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	770	1200	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL				
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP				
Idle on Twisted Pair after TXEN De-Assert	TX_QUIET	––	460	500	ns

On the foloowing pages, Table 31 provides the parameters for 100BASE-X receive timing. Figure 7 illustrates 100BASE-TX receive start of packet timing and Figure 8 shows 100BASE-TX receive end of packet timing. Figure 9 shows 100BASE-TX receive packet premature end. Figure 10 illustrates link failure or stream cipher error during receive packet. False carrier sense timing is shown in Figure 11.

Table 31: 100BASE-X Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
RXC Cycle Time		39.5	40	40.5	ns
RXC High/Low Time (RXDV Asserted)		18	20	22	ns
RXC High Time (RXDV Deasserted)		18	20	54	ns
RXC Low Time (RXDV Deasserted)		18	20	38	ns
RXC Rise/Fall Time		2	–	5	ns
RXDV, RXER, RXD[3:0] Delay from RXC Falling		-3	–	3	ns
CRS Deassert from RXC Falling (Valid EOP Only)		-3	–	3	ns
CRS Assert after RD±	RX_CRS	90	–	120	ns
CRS Deassert after RD± (Valid EOP)	RX_CRS_EOP	130	–	160	ns
CRS Deassert after RD± (premature end)	RX_CRS_IDLE	170	–	200	ns
RXDV Assert after RD±	RX_RXDV	130	–	160	ns
RXDV Deassert after RD±	RX_RXDV_EOP	130	–	160	ns
RXDV Assert after CRS		35	–	45	ns
RD± to RXD Steady State Delay	RX_RXD	150	–	180	ns
COL Assert after RD± (while TX)	RX_COL	90	–	120	ns
COL Deassert after RD± (Valid EOP)	RX_COL_EOP	130	–	160	ns
COL Deassert after RD± (Premature End)	RX_COL_IDLE	170	–	200	ns
RXEN high to RXC, RXDV, RXER, RXD[3:0] Delay		0		50	ns
RXC, RXDV, RXER, RXD[3:0] High-Z from RXEN Low		20		70	ns

Note: *RXC minimum high and low times are guaranteed when RXEN is asserted or deasserted. The MII port will always tristate while RXC is low.*

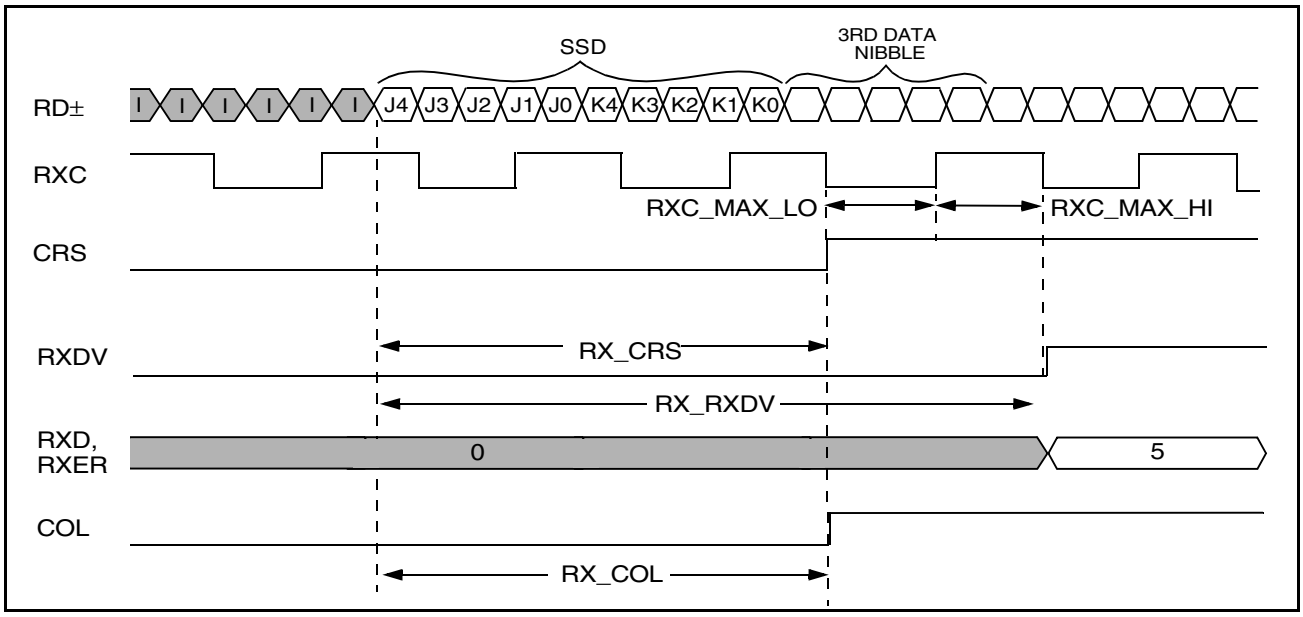


Figure 7: Receive Start of Packet Timing (100BASE-TX)

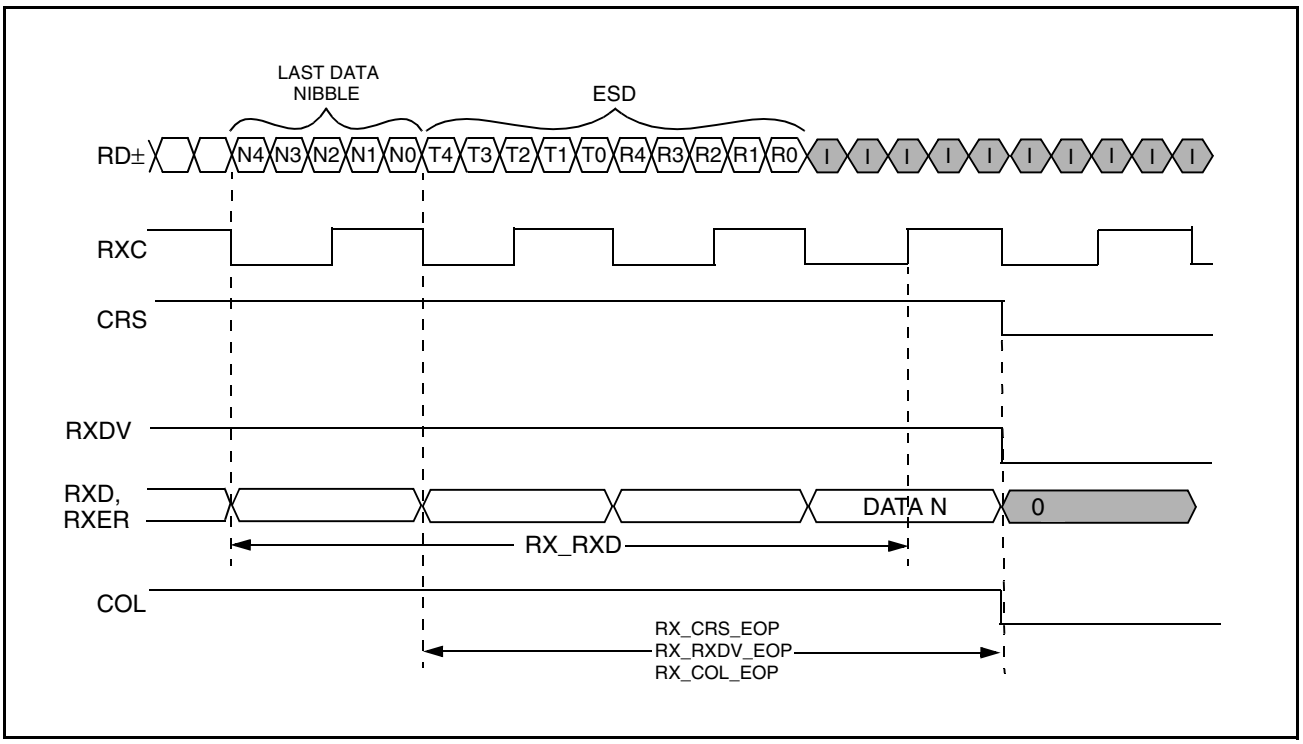


Figure 8: Receive End of Packet Timing (100BASE-TX)

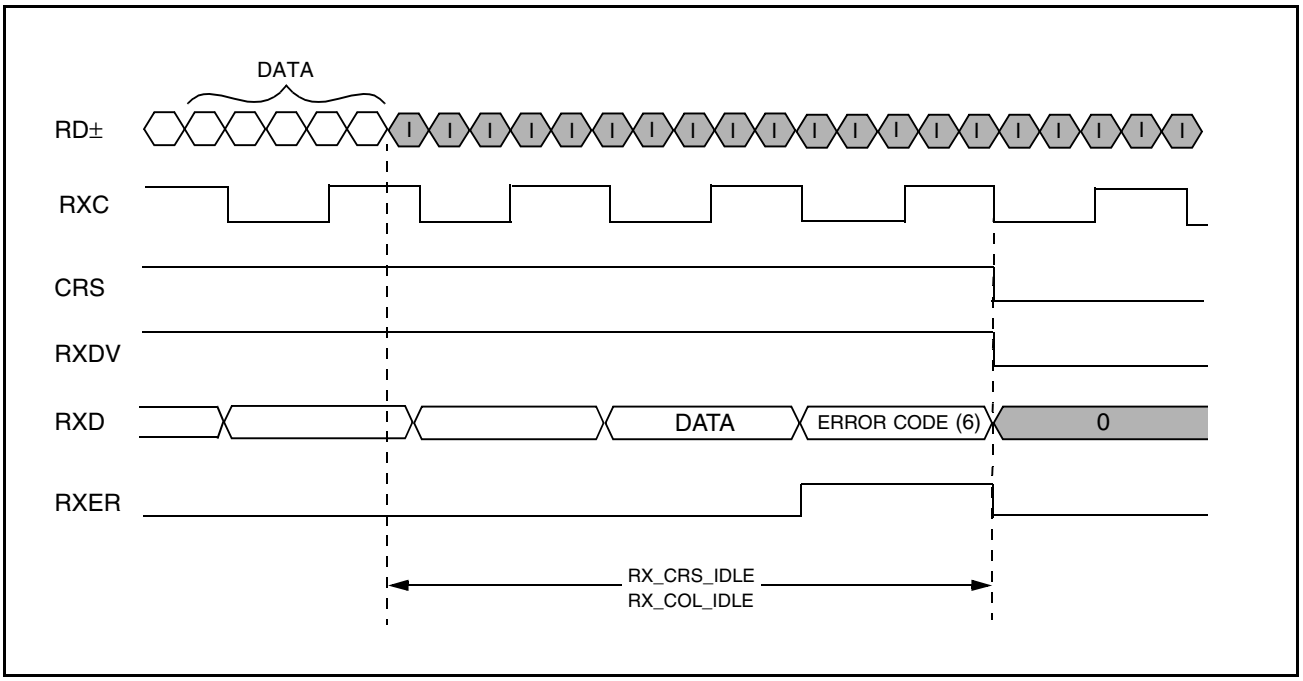


Figure 9: Receive Packet Premature End (100BASE-TX)

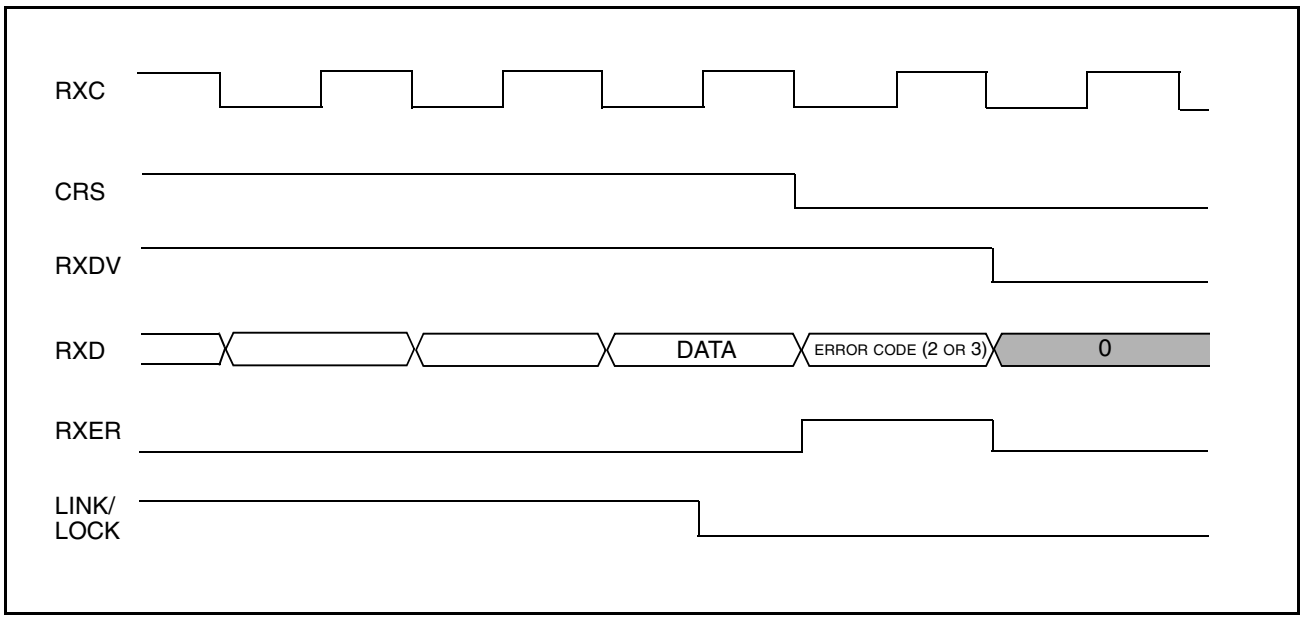


Figure 10: Link Failure or Stream Cipher Error During Receive Packet

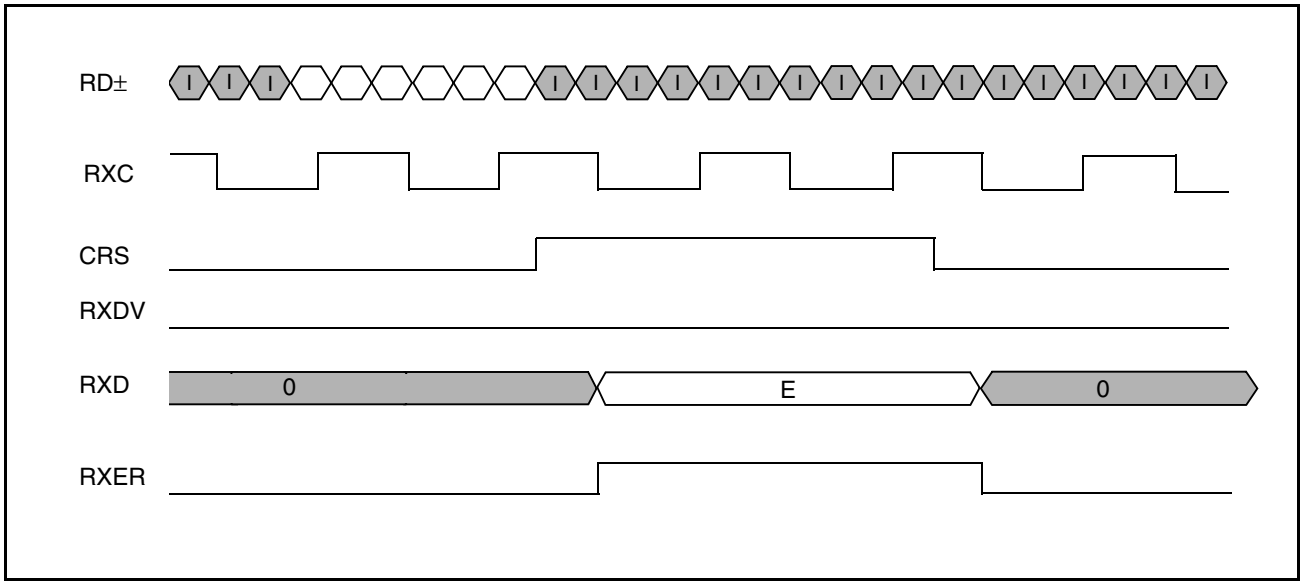


Figure 11: False Carrier Sense Timing (100BASE-TX)

Table 32 provides the parameters for 10BASE-T receive timing. 10BASE-T collision timing parameters are shown in Table 33.

Table 32: 10BASE-T Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
RXC Cycle Time	RXC_CYCLE	370.0	400	430.0	ns
RXC High/Low Time		150.5	200	240.5	ns
CRS Assert after First Rising Edge of Preamble with Positive Start-of-Idle	RX_CRS_BT	100	150	250	ns
CRS Assert after First Falling Edge of Preamble with Negative Start-of-Idle	RX_CRS_BT	100	150	250	ns
RXC Valid after CRS Assert	RXC_VALID	–	–	2000	ns
RXDV Assert after Receive Analog Data	RX_RXDV	–	1900	2300	ns
RXDV Deassert after Receive Analog EOP Ends	RX_NOT_RXDV	–	510	560	ns
CRS Deassert after Receive Analog EOP Ends	RX_NOT_RXDV	–	510	560	ns
Note: *Positive Start of Idle contains four "1" data samples, which implies correct polarity, and Negative Start-of-Idle contains four "0" data samples, which implies reversed polarity. Refer to IEEE 802.3, Clause 14, Figure 14-10.*					

Table 33: 10BASE-T Collision Timing

Parameter	Symbol	Min	Typ	Max	Unit
COL Assert after First Rising Edge of Preamble with Positive Start-of-Idle	RX_COL	–	250	300	ns
COL Assert after First Falling Edge of Preamble with Negative Start-of-Idle	RX_COL	–	250	300	ns
COL Deassert after TXEN Deassert (While Receiving)	TXEN_NOT_COL	–	440	490	ns
COL Assert after TXEN Assert (While Receiving)	TXEN_COL	–	50	100	ns
COL Deassert after Receive Analog Ends (While Transmitting)	RX_NOT_COL	–	400	450	ns

Table 34, Table 35, Table 36 and Table 37 provide the parameters for loopback timing, auto-negotiation, and LED timing. Figure 12 illustrates serial mode LED timing.

Table 34: Loopback Timing

Parameter	Symbol	Min	Typ	Max	Unit
TXD to RXD Steady State Propagation Delay		–	160	–	ns
LPBK Setup Time to TXEN		500	–	–	ns
LPBK Hold Time from TXEN		200	–	–	ns

Table 35: Auto-Negotiation Timing

Parameter	Symbol	Min	Typ	Max	Unit
Link Test Pulse Width		–	100	–	ns
FLP Burst Interval		5.7	16	22.3	ms
Clock Pulse to Clock Pulse		111	123	139	us
Clock Pulse to Data Pulse (Data = 1)		55.5	62.5	69.5	us

Table 36: LED Timing (Parallel Mode)

Parameter	Symbol	Min	Typ	Max	Unit
LED On Time (XMTLED, RCVLED)		–	80	–	ms
LED Off Time (XMTLED, RCVLED)		–	80	–	ms

Table 37: LED Timing (Serial Mode)

Parameter	Symbol	Min	Typ	Max	Unit
Shift Clock	SCLK		1		MHz
LED Serial Mode Data Set-Up	SDO_SETUP		200		ns
LED Serial Mode Data Hold	SDO_HOLD		200		ns
LED Frame Pulse Set-Up	SFRM_SETUP		200		ns
LED Frame Pulse Hold	SFRM_HOLD		200		ns

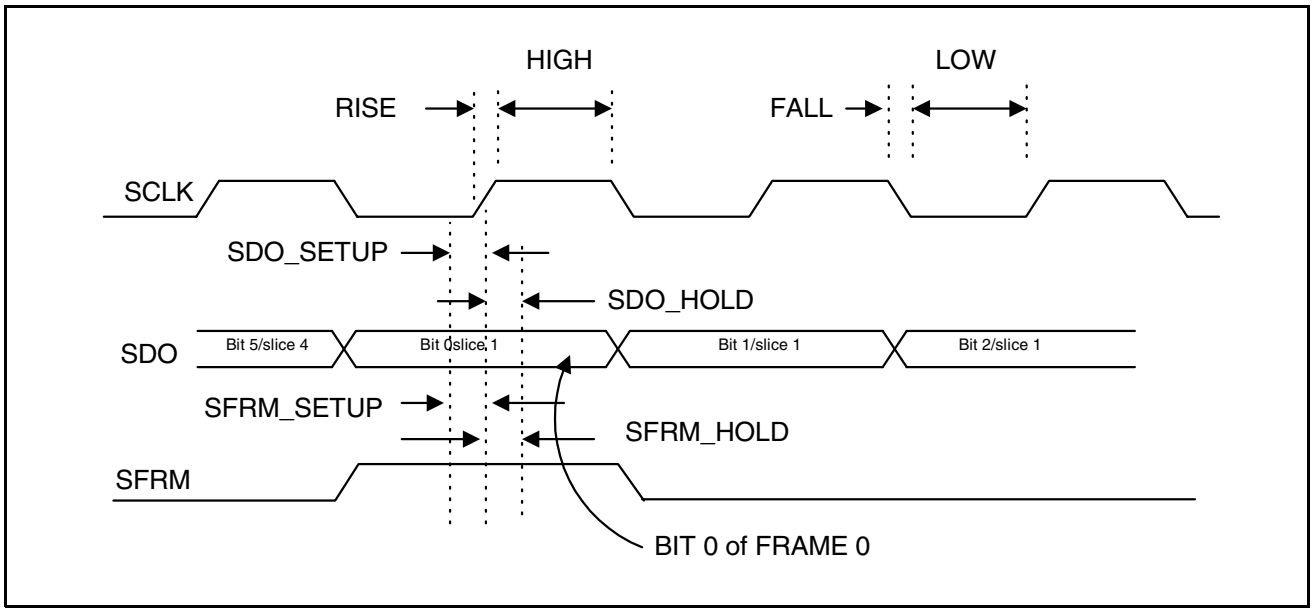


Figure 12: LED Timing (Serial Mode)

Table 38: LED Timing (Low Cost Serial Mode)

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Shift Clock (LC Ser SCLK)	T_{cy}		80		ns
Data Set-up (LC ser SDO#)	T_S	20			ns
Data Hold	T_H	20			ns
Refresh	T_{REF}		5.2		ms

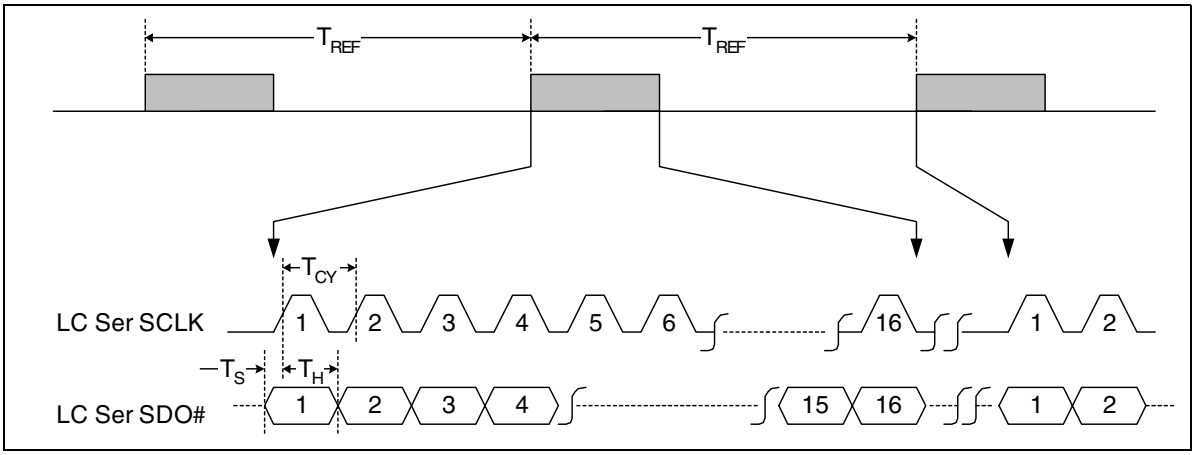


Figure 13: LED Timing (Low Cost Serial Mode)

Management data interface timing parameters are described in Table 39. Figure 14 and Figure 15 illustrate two types of management interface timing.

Table 39: Management Data Interface Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
MDC Cycle Time		80	-	-	ns
MDC High/Low		30	-	-	ns
MDC Rise/Fall Time		-	-	10	ns
MDIO Input Setup Time from MDC rising		10	-	-	ns
MDIO Input Hold Time from MDC rising		10	-	-	ns
MDIO Output Delay from MDC rising		0	-	50	ns

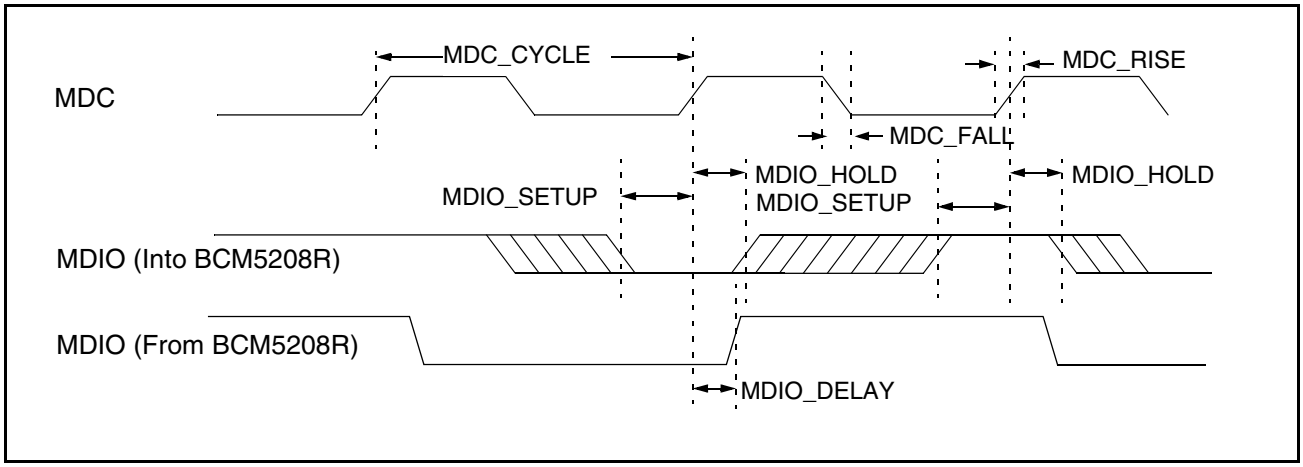
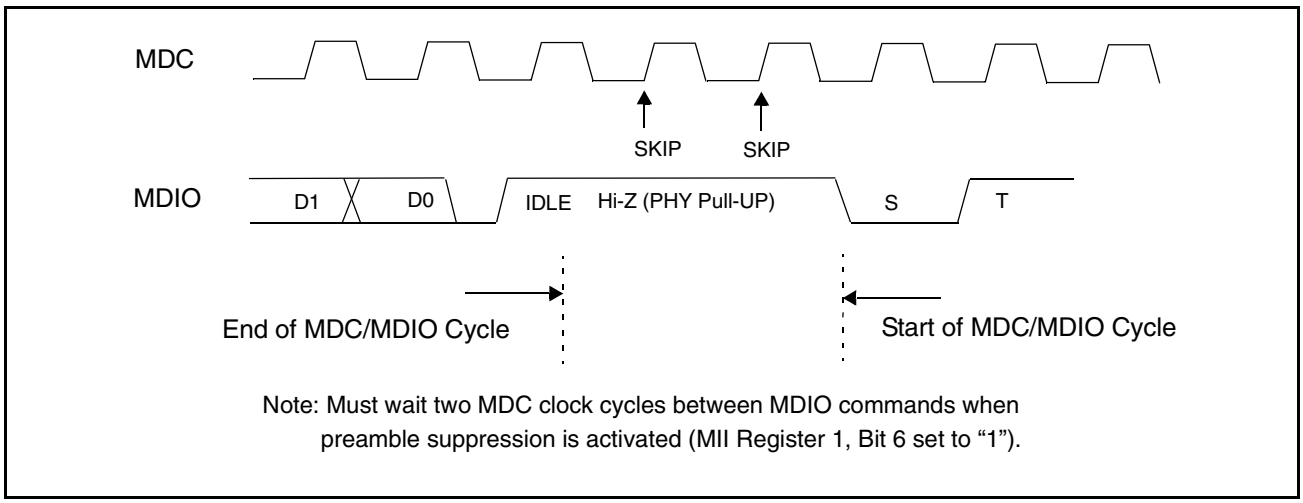


Figure 14: Management Interface Timing



Note: Must wait two MDC clock cycles between MDIO commands when preamble suppression is activated (MII Register 1, Bit 6 set to “1”).

Figure 15: Management Interface Timing (with Preamble Suppression On)

Section 7: Electrical Characteristics

This section covers the electrical characteristics of the BCM5208R.

Table 40 covers the absolute maximum ratings for the BCM5208R. The recommended operating conditions are shown in Table 41. Table 42 gives the electrical characteristics of the BCM5208R.

Table 40: Absolute Maximum Ratings

Symbol	*Parameter*	*Min*	*Max*	*Units*
V_{DD}	Supply Voltage	3.00	3.60	V
V_I	Input Voltage	GND – 0.3	IVDD + 0.3	V
I_I	Input Current			mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge		1000	V

Note: *These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.*

Table 41: Recommended Operating Conditions

Symbol	*Parameter*	*Pins*	*Operating Mode*	*Min*	*Max*	*Units*
V_{DD}	Supply Voltage	AVDD, DVDD, OVDD		3.135	3.465	V
		IVDD		3.135	5.25	V
V_{IH}	High-Level Input Voltage	All Digital Inputs		2.0		V
V_{IL}	Low-Level Input Voltage	All Digital Inputs			0.8	V
V_{IDIFF}	Differential Input Voltage	RD± {1:4}	100BASE-TX	700		mV
V_{ICM}	Common Mode Input Voltage	RD± {1:4}	100BASE-TX	1.55	1.95	V
T_A	Ambient Operating Temperature			0	70	°C

Table 42: Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Min	Typ	Max	Units
I_{DD}	Total Supply Current	AVDD, DVDD, OVDD, IVDD	100BASE-TX		612	650	mA
V_{OH}	High-Level Output Voltage	All LED Outputs	I_{OH} = –15 mA	2.4			V
		All Digital Outputs, Except LED Outputs	I_{OH} = –10 mA	2.4			V
		TD± {1:4}	Driving Loaded Magnetics Module			VDD + 1.5	V
V_{OL}	Low-Level Output Voltage	All Digital Outputs	I_{OL} = 8 mA			0.4	V
		TD± {1:4}	driving loaded magnetics module	VDD – 1.5			V
I_I	Input Current	Digital Inputs with Pull-Up Resistors	V_I = IVDD			+100	µA
			V_I = DGND			-200	µA
		Digital Inputs with Pull-Down Resistors	V_I = IVDD			+200	µA
			V_I = DGND			-100	µA
		All Other Digital Inputs	DGND ≤ V_I ≤ IVDD			±100	µA
I_{OZ}	High-Impedance Output Current	All Three-state Outputs	DGND ≤ V_O ≤ OVDD				µA
		All Open-Drain Outputs	V_O = OVDD				µA
V_{BIAS}	Bias Voltage	VREF, RDAC		1.18		1.30	V

Section 8: Application Examples

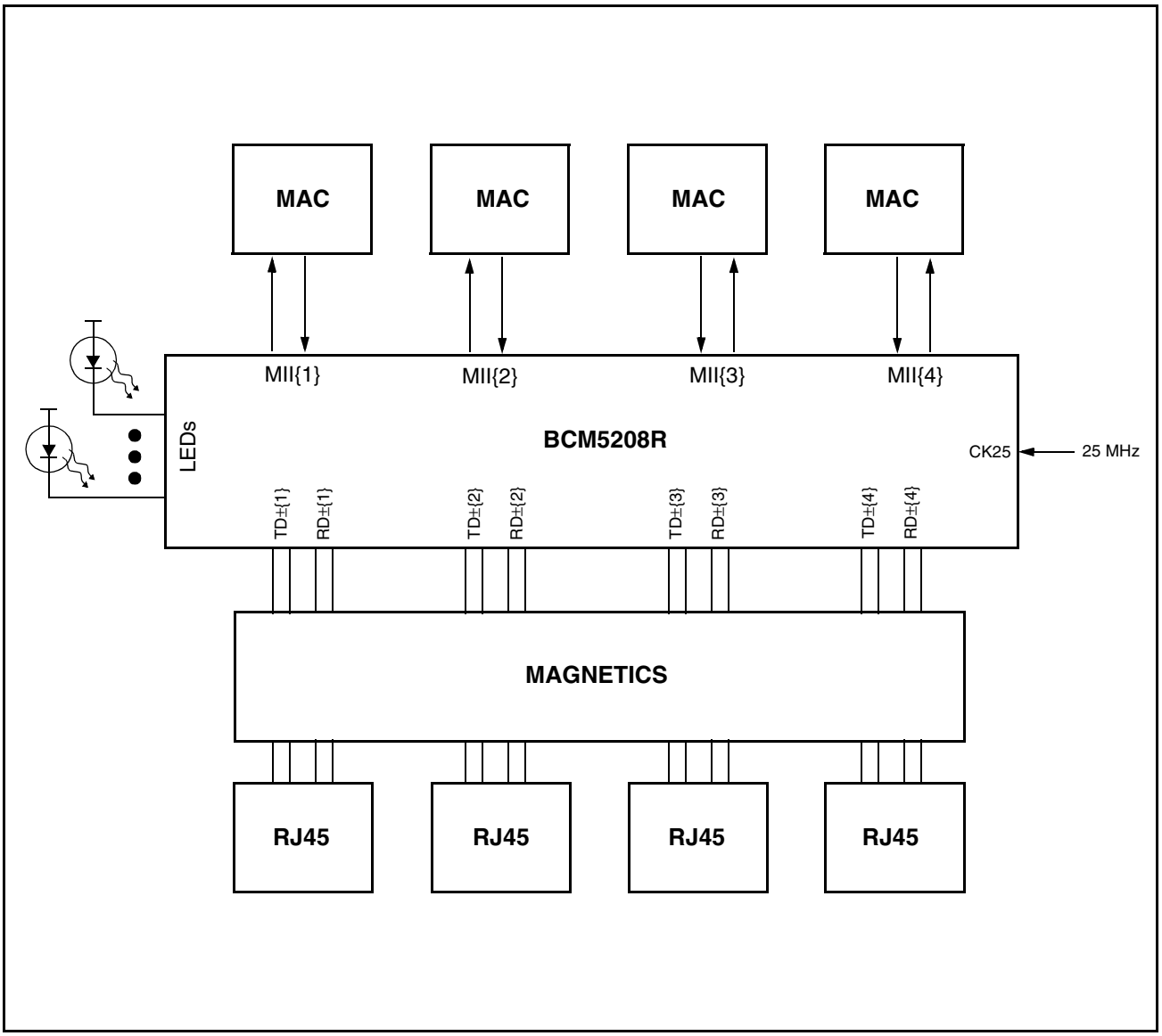
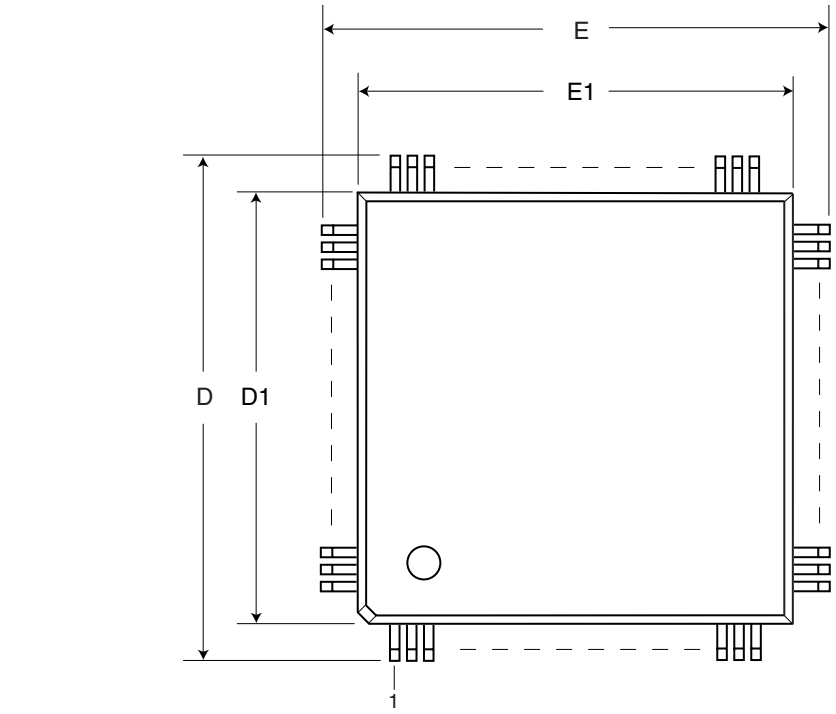
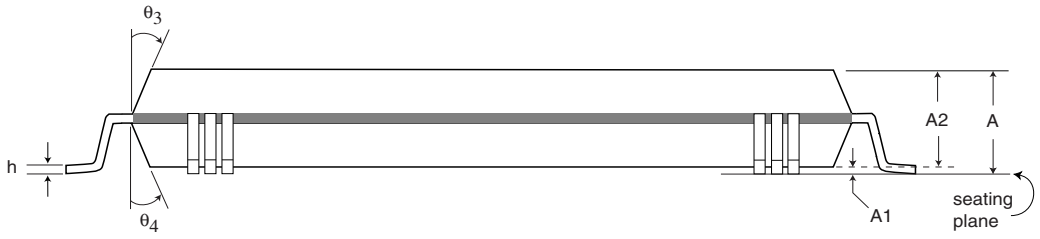


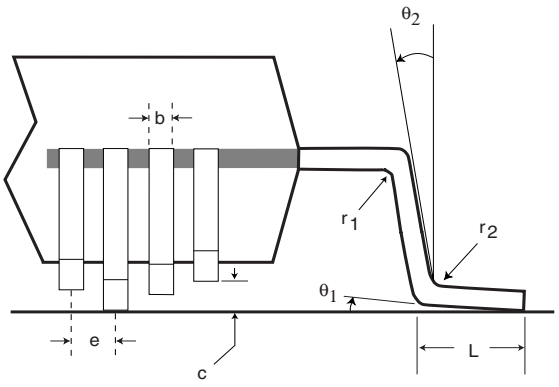
Figure 16: Switch Application





Symbol	Millimeter		
	Min	Nom	Max
A	—	—	4.10
A1	0.25	0.37	0.50
A2	3.39	3.49	3.59
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
L	0.30	0.60	0.75
b	0.15	0.22	0.30
h	0.13		0.23
e	0.50 BSC		
c	—	0.08	0.102
r_1	—	0.20	—
r_2	—	0.30	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	10°	—
θ_4	—	10°	—

208-pin detail



Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

Figure 17: 208-Pin PQFP

Section 9: Ordering Information

Table 43: Ordering Information

Part Number	Package	Ambient Temperature
BCM5208R KPF	208-PQFP	0° to 70° C (32° to 158° F)

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