

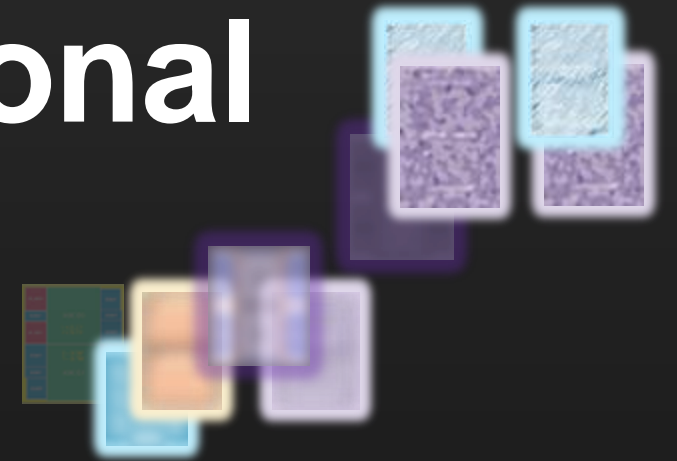
ENABLING AI Infrastructure

3.5D XDSiP™ Platform Technology

ASIC Products Division

December 5th, 2024

Delivering Multi-Generational Custom AI Accelerators over the Past Decade



2014

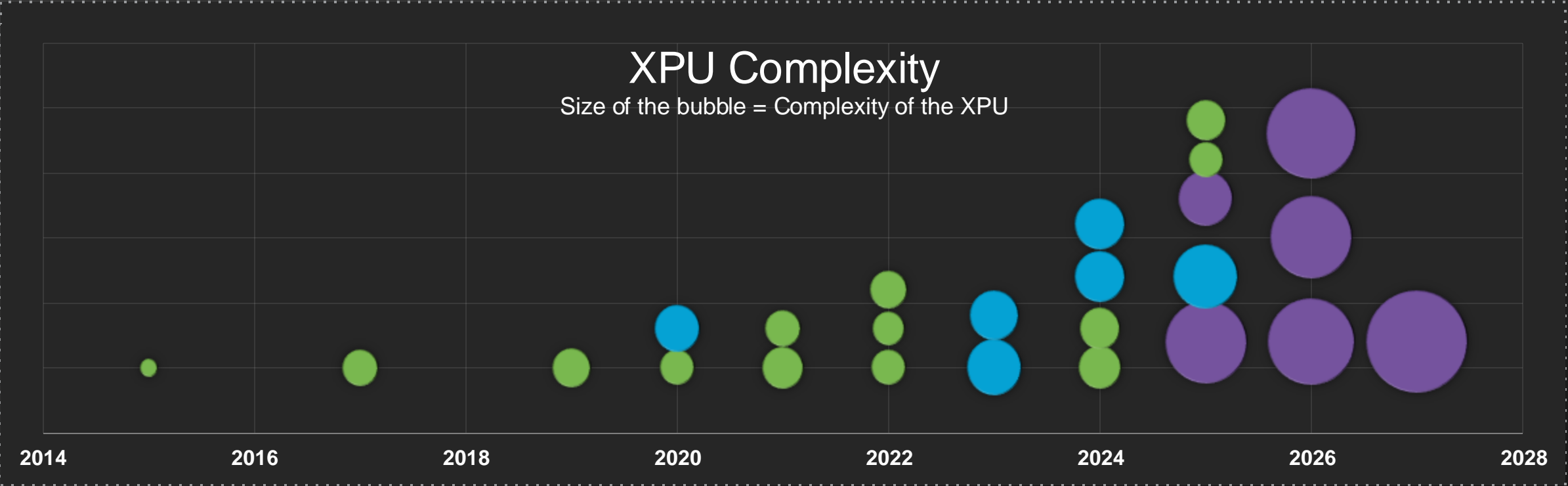
2021

2022-2023

2024-2025

2026 &
Beyond

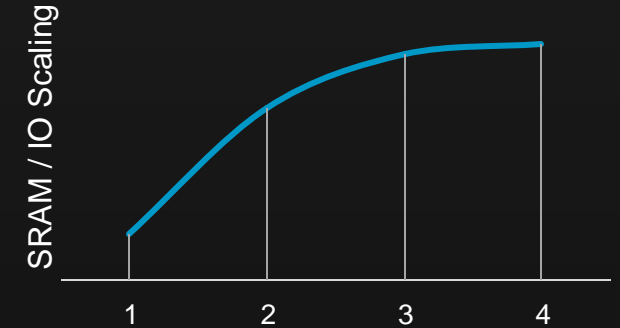
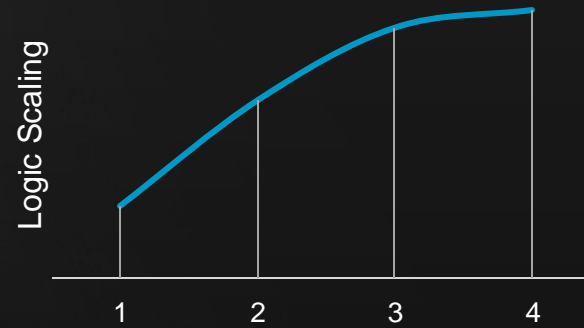
Consumer-AI XPU Complexity and Performance Continuously Increasing



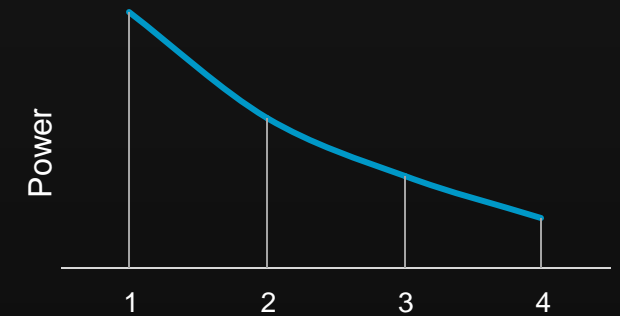
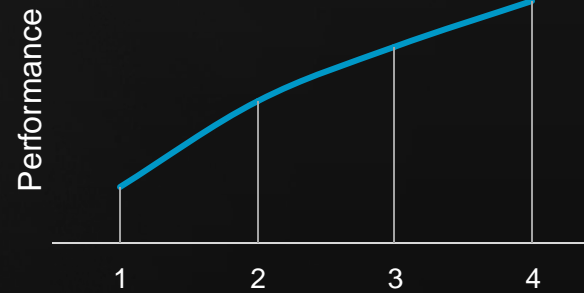
F (Complexity) = {Compute Performance, Network Bandwidth, Memory Bandwidth, Power Delivery, Thermal Integrity, Mechanical Reliability}

Process Technology Trends Create Challenge for XPU Designers

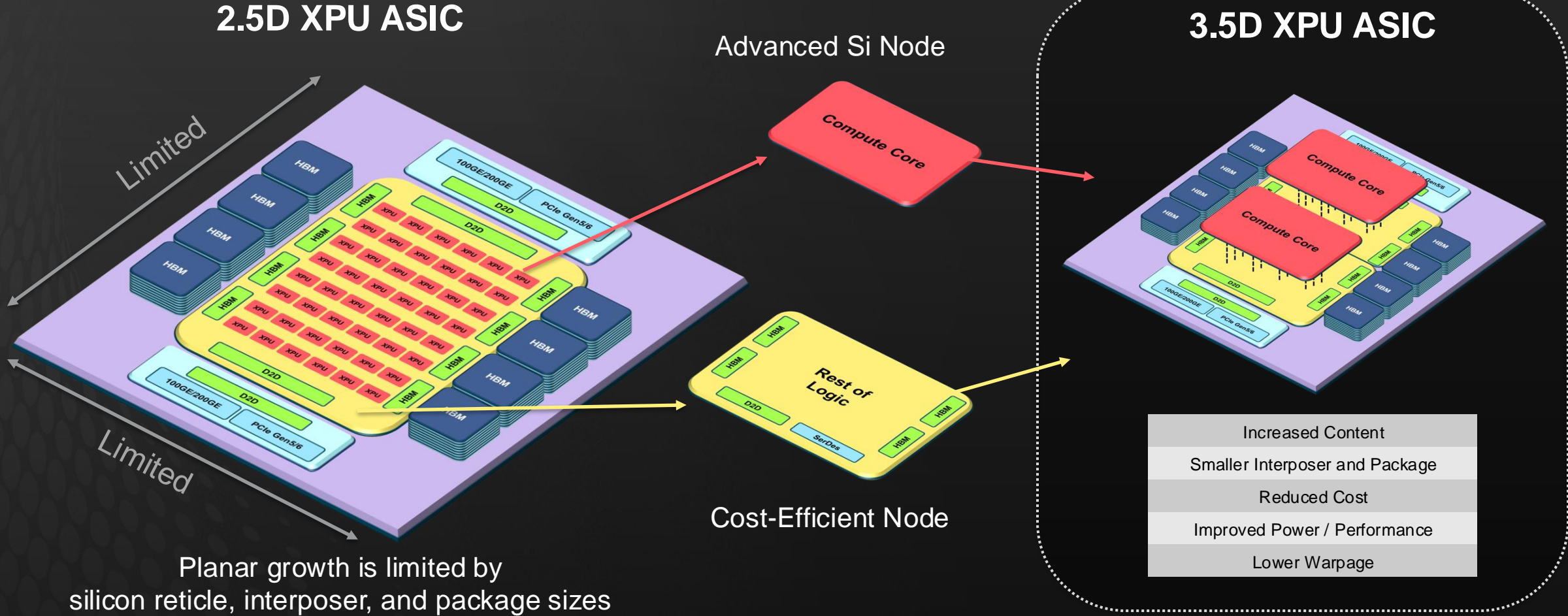
Logic & SRAM
Scaling Slowing Down



Performance & Power
Scaling Continues

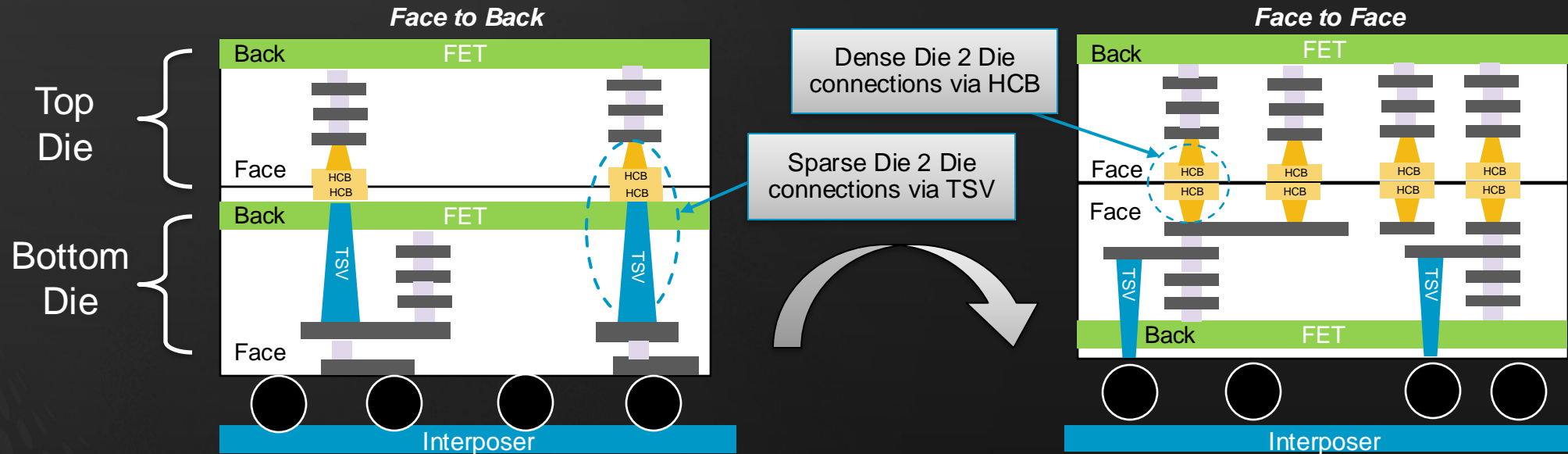


3.5D XDSiP Enables Computing Performance Growth



Face-to-Face 3.5D Allows Greater Density and Higher Performance

Increases Architecture and Design Flexibility



Metrics	Face to Back
D2D Signal Density	Limited by TSV density
D2D Signal Performance	Higher parasitic loading
Design Flexibility	Reduced options for Die-to-Die connection data paths

Face to Face
7x available signal connections through HCB
Shorter signal routing, higher performance
High flexibility to split ASIC architecture between top & bottom dies

3.5D XDSiP™ Custom XPU Developments

3.5D XDSiP #1



- 2x 3D stacks, 2x I/O Chiplets
- 12x HBM3, 100x100 package

3.5D XDSiP #2



- 3x Top on 1x Bottom, 1x I/O Chiplet
- 6x HBM3, 100G, D2D PHY

3.5D XDSiP #3



- 2x 3D stacks, 2x I/O Chiplets
- 8x HBM4, LPDDR5, 200G, D2D

3.5D XDSiP #4



- 4x 3D stacks, 1x I/O Chiplet
- PCIe, DDR, D2D

3.5D XDSiP #5



3.5D XDSiP #6



Broadcom 3.5D XDSiP

Key Points



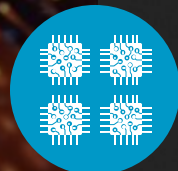
Industry's First Face-to-Face 3.5D for Next Gen XPU's



Breaking Through Scaling Barriers with $>6000\text{mm}^2$ of Si and 12 HBM's



Increased Performance and Efficiency at Lower Cost



Multiple 3.5D XPU's in Development with Production in 2026

ENABLING AI Infrastructure

OPEN // SCALABLE // POWER EFFICIENT