BCM16K and BCM5235
Board Design Guidelines

Design Guide

16000-DG105
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Chapter 1: Introduction

This document provides board design-specific tips and guidelines for the Broadcom BCM16K and BCM5235. It focuses on the external interfaces, power handling, and hardware environments required by this device.

1.1 System Overview

The BCM16K and BCM5235 performs high-speed operations on large-rule databases for a wide range of telecommunications applications, including Data Center and Enterprise switches and routers. It provides network awareness and enables real-time modifications and updates to the routing configuration, making it ideal for packet classification, policy enforcement, and forwarding.

It supports the PAM-4 (4-level Pulse Amplitude Modulation) mode for 56.25 Gb/s, 51.5625 Gb/s, 30.0 Gb/s, and legacy NRZ (Non-Return to Zero Modulation) 28.125 Gb/s and 27.34375 Gb/s line rates for search ports. It supports PAM-4 mode for 53.125 Gb/s and NRZ mode for 25.78125 Gb/s for statistics ports.

Using the processor requires careful PCB design, a power delivery network (PDN) including decoupling capacitor selection, low jitter and high timing performance of the CLK source, and careful routing of both the CLK and the high-speed serial links.

The processor supports the interfaces listed below.

- Clock Inputs:
  - SREFCLK[0–1]_P, SREFCLK[0–1]_N – Differential input, reference clock for the 56 Gb/s PAM-4 SerDes interface
  - CREFCLKP, CREFCLKN – Differential input, reference clock for the device core
  - PCREFCLKP, PCREFCLKN – Differential input, reference clock for the 5 Gb/s PCIe Generation 2 interface
- High-Speed Interlaken/Record Over Packet (ROP) Interface:
  - Up to 48 serial links with line rates from 12.5 Gb/s to 56.25 Gb/s data rate
  - Up to 56.25 Gb/s data rate with PAM-4 modulation
  - 1.8V Current Mode Logic (CML) signaling
- PCIe 2.0 Interface (a PCIe interface is required in all design projects):
  - One-lane receiver (Rx) and one-lane transmitter (Tx)
  - 5 Gb/s data rate
  - Meets PCIe 2.0 specifications
- Management Data Port (MDIO interface):
  - Single-ended clock input (management data clock), open drain. Pull-up through a 1 kΩ resistor to 1.8V supply.
  - Single-ended bidirectional I/O, open drain. Pull-up through a 1 kΩ resistor to 1.8V supply.
  - 1.8V signaling. Not 3.3V tolerant.
  - Per IEEE 802.3ae, Clause 45
  - Used for serial interface and port configuration
- Inter-Integrated Circuit (I^2C interface):
  - Single-ended clock input (SCL), open drain. Pullup through a 1 kΩ resistor to 1.8V supply when the interface is used.
  - Single-ended bidirectional I/O, open drain. Pullup through a 1 kΩ resistor to 1.8V supply when the interface is used.
  - 1.8V signaling. Not 3.3V tolerant.
- JTAG:
  - JTAG interface with AC capability (IEEE 1149.1 and IEEE 1149.6)
  - 1.8V signaling. Not 3.3V tolerant.

- Miscellaneous:
  - Static configuration pins, and so on.
  - Test pins (for factory use only)
  - 1.8V signaling. Not 3.3V tolerant.

Chapter 2: Power Supplies

2.1 Overview

The power supply inputs are shown in Table 1.

Table 1: Power Supply Inputs

Power Rail	Voltage [V_{out}] (mV)	Absolute Voltage Tolerance [$\Delta V_{out, max}$] (mV)	Max AC Ripple [R_C] (%)	Power Consumption (W)	Load Current Step [$\Delta I_{load,max}$] (A)	Comments
VDD	850 (AVS)	25	1.5	133[a]	50	Powers core logic circuits. (Core) Power consumption is application dependent.
VDDM	850	25	1.5	12.86[a]	1.0	Powers SRAM circuits. (SRAM)
VDD18	1800	90	1.5	0.51	0.14	Supply for low-speed I/Os and misc. circuits. (HVA)
VDDCPLL	1800	55	1.5	0.06	0.01	PLL supply for core logic circuits. (HVA)
VDDPC	800	25	1.5	0.07	0.01	Analog supply for PCIe circuits. (LVA)
VDDPCPLL	800	25	1.5	0.06	0.01	PLL supply for PCIe circuits. (LVA)
VDDS1	800	25	1.25	2.0[b]	0.18	SerDes [0–7] Analog supply circuits. (LVA)
VDDS2	800	25	1.25	2.0[b]	0.18	SerDes [08–15] Analog supply circuits. (LVA)
VDDS3	800	25	1.25	2.0[b]	0.18	SerDes [16–23] Analog supply circuits. (LVA)
VDDS4	800	25	1.25	2.0[b]	0.18	SerDes [24–31] Analog supply circuits. (LVA)
VDDS5	800	25	1.25	2.0[c]	0.18	SerDes [32–39] Analog supply circuits. (LVA)
VDDS6	800	25	1.25	2.0[c]	0.18	SerDes [40–47] Analog supply circuits. (LVA)
VDDSL	900	25	1.25	9.22[d]	0.18	SerDes [0–47] Digital supply circuits. (LVD)
VDDS08PLL1	800	25	0.375	0.08	0.02	SerDes [0–7] PLL supply circuits. (LVA)
VDDS08PLL2	800	25	0.375	0.08	0.02	SerDes [8–15] PLL supply circuits. (LVA)
VDDS08PLL3	800	25	0.375	0.08	0.02	SerDes [16–23] PLL supply circuits. (LVA)
VDDS08PLL4	800	25	0.375	0.08	0.02	SerDes [24–31] PLL supply circuits. (LVA)

Table 1: Power Supply Inputs (Continued)

Power Rail	Voltage [V_{out}] (mV)	Absolute Voltage Tolerance [$\Delta V_{out, max}$] (mV)	Max AC Ripple [R_c] (%)	Power Consumption (W)	Load Current Step [$\Delta I_{load,max}$] (A)	Comments
VDDS08PLL5	800	25	0.375	0.08	0.02	SerDes [32–39] PLL supply circuits. (LVA)
VDDS08PLL6	800	25	0.375	0.08	0.02	SerDes [40–47] PLL supply circuits. (LVA)
VDDS18PLL	1800	55	1.5	0.03	0.01	SerDes [0–47] PLL supply circuits. (HVA)
VDD12	1200	35	1.25	1.32	0.25	SerDes termination voltage supply. (HVA)

a. Power consumption is application dependent. The number in this table reflects power consumption for an aggressive application.

b. The power for VDDS1 to 4 is active upon power up, including after reset deassertion. Unused octets are powered down during interface initialization by KBPSDK. When powered down, each octet consumes approximately 250 mW. See VDDS Power Consumption During Initialization for more details.

c. VDDS5 and 6 consume approximately 250 mW upon power up including after reset deassertion.Used octets are powered up to the values indicated in the table during statistics port initialization by KBPSDK. See VDDS Power Consumption During Initialization for more details.

d. Indicates power consumption when all 32 search lanes (31 to 0) and all 16 statistics lanes (47 to 32) are activated at 56 or 53G. For power consumption under different lane configurations, please contact Broadcom and see examples in VDDSL Power Consumption Examples for more details.

NOTE: Power consumption depends on the specific device, usage, and configuration. Values shown are for power supply planning only. Contact your Broadcom representative for estimation of power consumption under specific usage conditions.

The supply type is given in parenthesis in the Comments section. This is used in the power-on and power-off sequence.

Absolute voltage tolerance refers to the amount of deviation from the nominal (going both positive and negative) that the voltage can vary at the ball of the device including DC variation and transient loads. For example, if the nominal voltage is 0.8V and the tolerance is 25 mV, then the voltage at the device ball must be (under all conditions) between 0.775V and 0.825V.

The max. AC ripple % is calculated as:

$$Rc = \frac{(\Delta Vout, pp)}{2Vout} \times 100\%$$

2.1.1 VDDS Power Consumption During Initialization

After power-on/reset deassertion and before KBPSDK interface initialization, SerDes octets 1 through 4 are in a semi-powered-up state while octets 5 and 6 are in a powered-down state. Therefore, there are scenarios under which the start-up power can be greater than the power consumption after SerDes initialization is completed by the KBPSDK.

Total VDDS power consumption upon power-up is 7.12W. Once the ports are initialized, the power for each VDDS octet is as shown in Table 1 when powered up or as indicated in footnotes b and c when powered down.

Example 1: 2 ports x 8 lanes search lanes at 56G + 2 ports x 4 lanes statistics lanes at 53G

In this configuration, a total of four octets are activated during interface and port-macro initialization, and lanes 0 to 7, 16 to 23, 32to 35, and 40 to 43 are used. Therefore, total VDDS power after initialization = 4 x 2.0W + 2 x 0.25W = 8.5W.

Since 8.5W > 7.12W (power-on power), the system designer should design for 8.5W VDDS.

Example 2: 2 ports x 4 lanes statistics lanes at 53G, no search lanes

In this configuration, a total of two octets are activated during interface initialization. Therefore, total VDDS power after initialization = 2 x 2.0W + 4 x 0.25W = 5.0W.

Since 5.0W < 7.12W (power-on power), the system designer should design the regulator for 7.12W VDDS to account for power-on power, but use 5.0W during thermal simulations.

2.1.2 VDDSL Power Consumption Examples

Example 1: 2 ports x 8 lanes search lanes at 56G + 2 ports x 4 lanes statistics lanes at 53G

VDDSL power = 6.41W

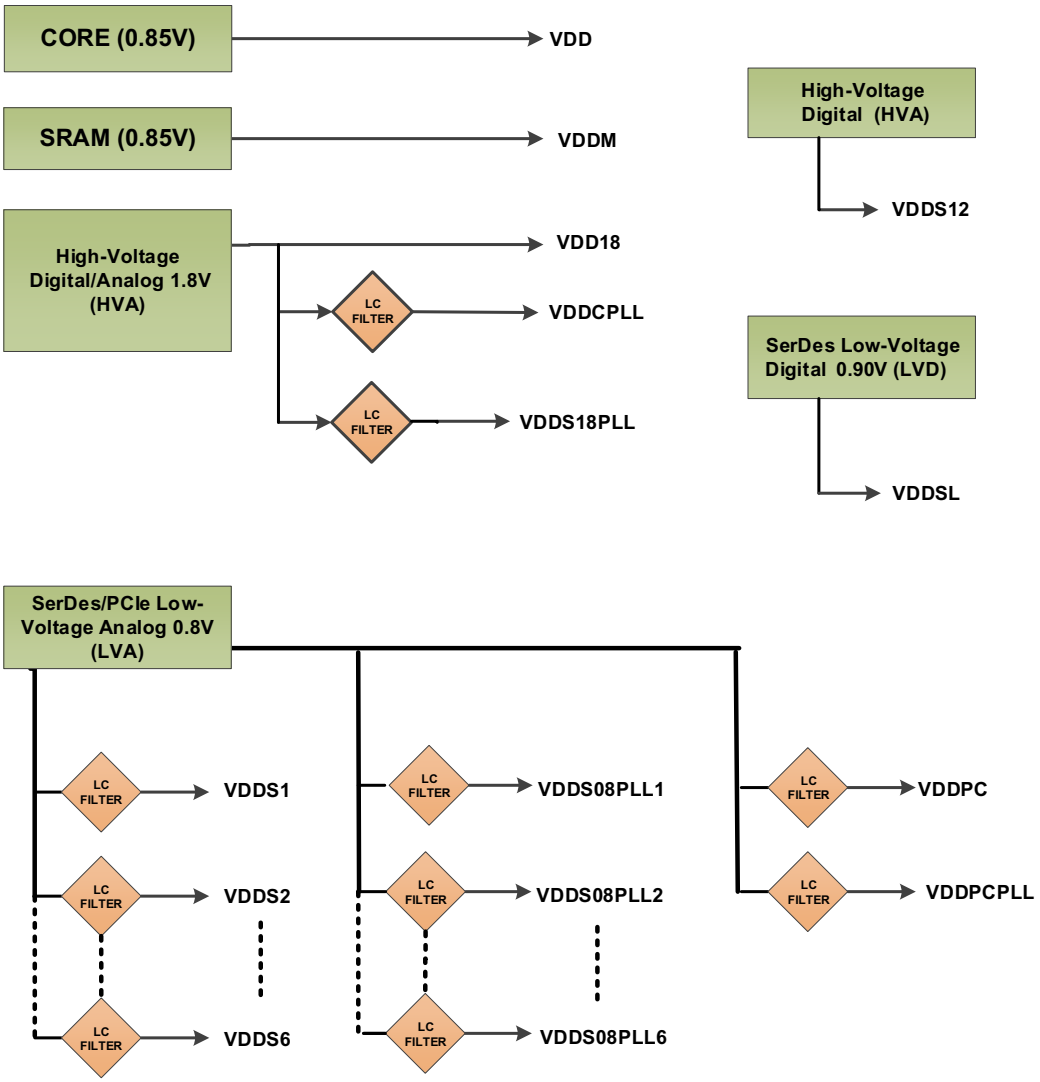
Example 2: 2 ports x 8 lanes search lanes at 28G + 2 ports x 4 lanes statistics lanes at 25G

VDDSL power = 5.09W

2.2 Power Supply Regulator Recommendations

A dedicated power supply is not required for all of the rails listed in Table 1. In fact, the rails can be condensed into six power supplies.

Figure 1: Block Diagram of Recommended Power Supply Assignment



2.3 Core, SRAM, I/O, and Core-PLL Supplies

2.3.1 VDD Supply – (Core)

A VDD at 0.85V typical value powers the core logic. A high-performance regulator designed for high power and fast-changing CPU-type loads is recommended for the core power supply. Except for very low device activity cases, a multiphase supply topology with 4 to 6 phases is required, depending on device utilization and activity factor. Desirable features for the core voltage regulator are fast transient response modes (non-linear control), dynamic phase shedding (improved light load efficiency), remote voltage sensing, and load-line regulation. Without non-linear control, it is difficult for systems in the higher end of the power range to meet the absolute voltage tolerance specification under idle to full load step.

2.3.1.1 Adjustable DC Voltage and Dynamic Sense

2.3.1.1.1 System Design

NOTE: AVS connection and operation are required for proper device operation.

The processor uses an automatic voltage scaling (AVS) technique to reduce the ill effects of a wide process variation. AVS involves adjusting the regulator voltage on the main VDD power supply level, as appropriate, for each silicon die. Slow silicon die use a higher voltage to ensure they run at the proper frequency. Fast silicon die use a lower voltage to reduce the power consumption. This ensures a part that runs at the desired frequency with minimal power consumption. It is required to have AVS enabled and running in order to guarantee proper device operation. To implement AVS, the voltage regulator on the PCB must be programmed on a per-device basis. This happens once upon power-up and determines which voltage it requires through the process provided below. Temperature is not adjusted, since the processor only asks for a static voltage from the regulator at all times.

AVS uses two chip pins called AVSA and AVSD as shown in the AVS connectivity diagram in Figure 2 on page 13. Initially, both switches in the processor are open and the regulator starts with a nominal V_{FB}, which is set by the R_{top} and R_{bot} voltage divider. After the initial start-up, the switches close and the AVSA pin will output the desired voltage to set the external regulator. This value will determine the steady-state DC value of the regulator and is governed by the silicon corner of the device, the temperature, and internal software settings. The regulator adjusts its output voltage in response to its V_{FB}. In steady state, $V_{REF} = V_{FB}$. The various components in Figure 2 on page 13 have constraints as depicted. R_{test} is to be used to test the AVS system as described in "Regulator Testing Procedure" on page 18. It is recommended to add a test point at V_{ADC} where an external voltage supply can be connected. C_{ADC} ensures a slow varying output voltage and guarantees stability. It can be greater than the recommended value of 220 nF. C_{adc} acts to filter noise and maintain the feedback pin near its DC level. It can be less than the recommended value of 1 nF. The following equation governs the voltage relationship between V_{AVS}, V_{ADC}, and V_{FB}:

$$V_{AVS} = (1 + R_{top}/R_{bot}) \times V_{REF} + (R_{top}/R_{ADC}) \times (V_{REF} - V_{ADC}) \quad \text{(Equation 1)}$$

If there were no AVS (so that $V_{REF} = V_{ADC}$), the second term of the equation drops out. R_{top} and R_{bot} are chosen using a nominal voltage for both V_{REF} and V_{AVS}. V_{REF} is determined by the given regulator and it is required to be in the range of 0.40V to 0.80V. The nominal start-up V_{AVS} is 0.85V, which implies that the first term of the equation is equal to 0.85V. This can be rewritten to determine the R_{top} to R_{bot} ratio.

$$R_{top}/R_{bot} = (0.85/V_{REF}) - 1 \quad \text{(Equation 2)}$$

The regulator must be able to provide voltage in the range of 0.72V to 0.95V. The V_{ADC} voltage can range from 0 to 1.8V, but must be limited from 0.24V to 1.42V to maintain linearity in the DAC. To determine the R_{ADC} to R_{top} ratio, Equation 1 can be rewritten.

$$R_{ADC}/R_{top} = (V_{REF} - V_{ADC}) / (V_{AVS} - 0.85) \quad \text{(Equation 3)}$$

When V_{AVS} is at a maximum, V_{ADC} is at a minimum, and vice versa. An R_{ADC}/R_{top} ratio of 2.0 meets (equivalently $R_{top} = 0.5 \times R_{ADC}$) the requirements for AVS and for V_{ADC} for all possible values of V_{REF}. It is required to use this specific ratio to control update times. The DAC can drive a maximum current of 100 µA. This limits R_{ADC} as per Equation 4.

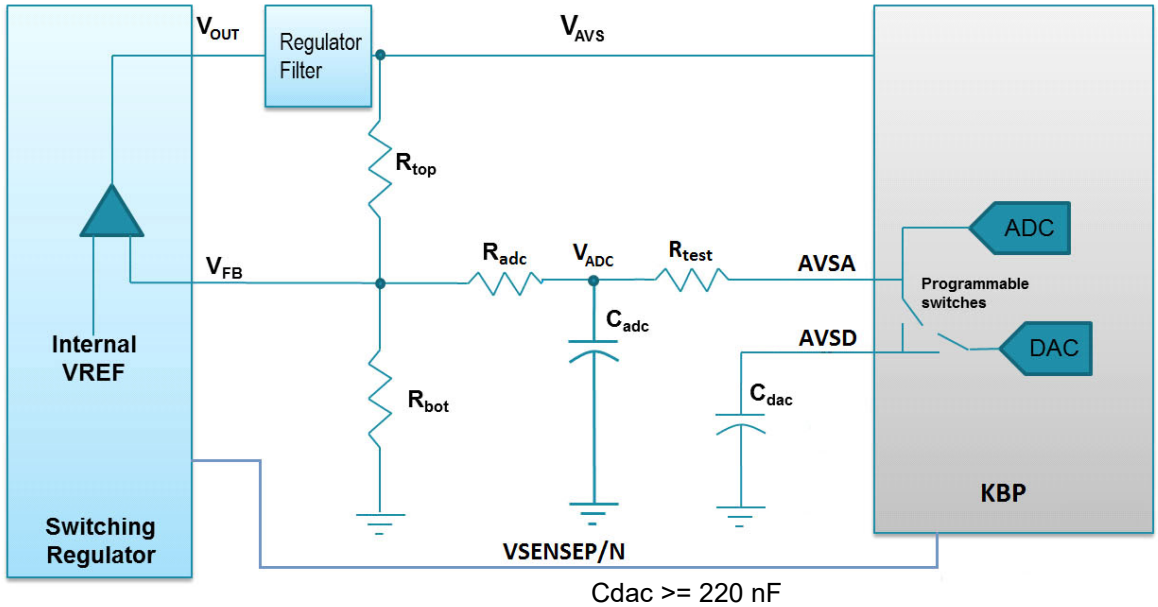
$$R_{ADC} \geq (V_{ADC} - V_{REF}) / 100e{-}^{6} \quad \text{(Equation 4)}$$

Plugging in 1.42V as a maximum for V_{ADC} and 0.40V as a minimum for V_{REF} gives a value of greater than 10.2 kΩ. It is required that all resistor values be tightly controlled with a tolerance of 1% or less. Note that the regulator input impedance on V_{FB} may not be infinite and this should be taken into account when determining resistor values. Table 2 on page 13 shows the ideal voltage of V_{AVS} for a given V_{REF} and V_{ADC} voltage given an R_{top} of 6 kΩ, R_{ADC} value of 12 kΩ, and R_{bot} chosen for the appropriate V_{REF} (7.5 kΩ for V_{REF} = 0.5V). The yellow highlighted portion shows the full AVS range that the regulator could output to the device. The table is derived from Equation 1, above. It is required that the regulator V_{REF} allow for the full AVS range. The BCM16K and BCM5235 will change V_{ADC} until it receives the desired V_{AVS} that it has determined. The processor sets the V_{ADC} and expects the required V_{AVS} that it has determined.The accuracy of the DAC is around 2 mV.

The device has two sense pins for the regulator called VSENSEP and VSENSEN. These pins are appropriate for dynamic feedback of the chip voltage in order to compensate for low frequency noise. Some regulator remote voltage sense inputs are sensitive to high frequency noise. It is recommended to filter VSENSEP/VSENSEN connections using an RC filter. The VSENSE pins take a sample of the voltage of the top metal layer in the die and route separately in the package to dedicated balls. They should be routed as a trace on the board to the regulator sense pins. The VSENSE pins should be able to work in conjunction with AVS.

CAUTION! Each of these VSENSE pins can source or sync a maximum of 35 mA. If this current is exceeded, the device will be damaged.

Figure 2: AVS System Configuration



V_{OUT}: Output of Switching Regulator
V_{AVS}: V_{DD} Supply of the SOC

Cdac >= 220 nF
Cadc <= 1 nF
Radc >= 10.2 Kohm
Rtop = 0.5 * Radc
Rtest = 0 ohm

Table 2: Expected V_{AVS} with Different V_{ADC} and V_{REF} Combinations

V_{REF}	0.50	0.55	0.60	0.65	0.70	0.75	0.80	0.85
V_{ADC}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}
1.33	0.435	0.460	0.485	0.510	0.535	0.560	0.585	0.610
1.32	0.440	0.465	0.490	0.515	0.540	0.565	0.590	0.615
1.31	0.445	0.470	0.495	0.520	0.545	0.570	0.595	0.620
1.3	0.450	0.475	0.500	0.525	0.550	0.575	0.600	0.625
1.29	0.455	0.480	0.505	0.530	0.555	0.580	0.605	0.630
1.28	0.460	0.485	0.510	0.535	0.560	0.585	0.610	0.635
1.27	0.465	0.490	0.515	0.540	0.565	0.590	0.615	0.640
1.26	0.470	0.495	0.520	0.545	0.570	0.595	0.620	0.645
1.25	0.475	0.500	0.525	0.550	0.575	0.600	0.625	0.650
1.24	0.480	0.505	0.530	0.555	0.580	0.605	0.630	0.655
1.23	0.485	0.510	0.535	0.560	0.585	0.610	0.635	0.660
1.22	0.490	0.515	0.540	0.565	0.590	0.615	0.640	0.665
1.21	0.495	0.520	0.545	0.570	0.595	0.620	0.645	0.670
1.2	0.500	0.525	0.550	0.575	0.600	0.625	0.650	0.675
1.19	0.505	0.530	0.555	0.580	0.605	0.630	0.655	0.680
1.18	0.510	0.535	0.560	0.585	0.610	0.635	0.660	0.685
1.17	0.515	0.540	0.565	0.590	0.615	0.640	0.665	0.690

Table 2: Expected V_{AVS} with Different V_{ADC} and V_{REF} Combinations (Continued)

V_{REF}	0.50	0.55	0.60	0.65	0.70	0.75	0.80	0.85
V_{ADC}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}
1.16	0.520	0.545	0.570	0.595	0.620	0.645	0.670	0.695
1.15	0.525	0.550	0.575	0.600	0.625	0.650	0.675	0.700
1.14	0.530	0.555	0.580	0.605	0.630	0.655	0.680	0.705
1.13	0.535	0.560	0.585	0.610	0.635	0.660	0.685	0.710
1.12	0.540	0.565	0.590	0.615	0.640	0.665	0.690	0.715
1.11	0.545	0.570	0.595	0.620	0.645	0.670	0.695	0.720
1.1	0.550	0.575	0.600	0.625	0.650	0.675	0.700	0.725
1.09	0.555	0.580	0.605	0.630	0.655	0.680	0.705	0.730
1.08	0.560	0.585	0.610	0.635	0.660	0.685	0.710	0.735
1.07	0.565	0.590	0.615	0.640	0.665	0.690	0.715	0.740
1.06	0.570	0.595	0.620	0.645	0.670	0.695	0.720	0.745
1.05	0.575	0.600	0.625	0.650	0.675	0.700	0.725	0.750
1.04	0.580	0.605	0.630	0.655	0.680	0.705	0.730	0.755
1.03	0.585	0.610	0.635	0.660	0.685	0.710	0.735	0.760
1.02	0.590	0.615	0.640	0.665	0.690	0.715	0.740	0.765
1.01	0.595	0.620	0.645	0.670	0.695	0.720	0.745	0.770
1	0.600	0.625	0.650	0.675	0.700	0.725	0.750	0.775
0.99	0.605	0.630	0.655	0.680	0.705	0.730	0.755	0.780
0.98	0.610	0.635	0.660	0.685	0.710	0.735	0.760	0.785
0.97	0.615	0.640	0.665	0.690	0.715	0.740	0.765	0.790
0.96	0.620	0.645	0.670	0.695	0.720	0.745	0.770	0.795
0.95	0.625	0.650	0.675	0.700	0.725	0.750	0.775	0.800
0.94	0.630	0.655	0.680	0.705	0.730	0.755	0.780	0.805
0.93	0.635	0.660	0.685	0.710	0.735	0.760	0.785	0.810
0.92	0.640	0.665	0.690	0.715	0.740	0.765	0.790	0.815
0.91	0.645	0.670	0.695	0.720	0.745	0.770	0.795	0.820
0.9	0.650	0.675	0.700	0.725	0.750	0.775	0.800	0.825
0.89	0.655	0.680	0.705	0.730	0.755	0.780	0.805	0.830
0.88	0.660	0.685	0.710	0.735	0.760	0.785	0.810	0.835
0.87	0.665	0.690	0.715	0.740	0.765	0.790	0.815	0.840
0.86	0.670	0.695	0.720	0.745	0.770	0.795	0.820	0.845
0.85	0.675	0.700	0.725	0.750	0.775	0.800	0.825	0.850
0.84	0.680	0.705	0.730	0.755	0.780	0.805	0.830	0.855
0.83	0.685	0.710	0.735	0.760	0.785	0.810	0.835	0.860
0.82	0.690	0.715	0.740	0.765	0.790	0.815	0.840	0.865
0.81	0.695	0.720	0.745	0.770	0.795	0.820	0.845	0.870
0.8	0.700	0.725	0.750	0.775	0.800	0.825	0.850	0.875
0.79	0.705	0.730	0.755	0.780	0.805	0.830	0.855	0.880
0.78	0.710	0.735	0.760	0.785	0.810	0.835	0.860	0.885
0.77	0.715	0.740	0.765	0.790	0.815	0.840	0.865	0.890

Table 2: Expected V_{AVS} with Different V_{ADC} and V_{REF} Combinations (Continued)

V_{REF}	0.50	0.55	0.60	0.65	0.70	0.75	0.80	0.85
V_{ADC}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}
0.76	0.720	0.745	0.770	0.795	0.820	0.845	0.870	0.895
0.75	0.725	0.750	0.775	0.800	0.825	0.850	0.875	0.900
0.74	0.730	0.755	0.780	0.805	0.830	0.855	0.880	0.905
0.73	0.735	0.760	0.785	0.810	0.835	0.860	0.885	0.910
0.72	0.740	0.765	0.790	0.815	0.840	0.865	0.890	0.915
0.71	0.745	0.770	0.795	0.820	0.845	0.870	0.895	0.920
0.7	0.750	0.775	0.800	0.825	0.850	0.875	0.900	0.925
0.69	0.755	0.780	0.805	0.830	0.855	0.880	0.905	0.930
0.68	0.760	0.785	0.810	0.835	0.860	0.885	0.910	0.935
0.67	0.765	0.790	0.815	0.840	0.865	0.890	0.915	0.940
0.66	0.770	0.795	0.820	0.845	0.870	0.895	0.920	0.945
0.65	0.775	0.800	0.825	0.850	0.875	0.900	0.925	0.950
0.64	0.780	0.805	0.830	0.855	0.880	0.905	0.930	0.955
0.63	0.785	0.810	0.835	0.860	0.885	0.910	0.935	0.960
0.62	0.790	0.815	0.840	0.865	0.890	0.915	0.940	0.965
0.61	0.795	0.820	0.845	0.870	0.895	0.920	0.945	0.970
0.6	0.800	0.825	0.850	0.875	0.900	0.925	0.950	0.975
0.59	0.805	0.830	0.855	0.880	0.905	0.930	0.955	0.980
0.58	0.810	0.835	0.860	0.885	0.910	0.935	0.960	0.985
0.57	0.815	0.840	0.865	0.890	0.915	0.940	0.965	0.990
0.56	0.820	0.845	0.870	0.895	0.920	0.945	0.970	0.995
0.55	0.825	0.850	0.875	0.900	0.925	0.950	0.975	1.000
0.54	0.830	0.855	0.880	0.905	0.930	0.955	0.980	1.005
0.53	0.835	0.860	0.885	0.910	0.935	0.960	0.985	1.010
0.52	0.840	0.865	0.890	0.915	0.940	0.965	0.990	1.015
0.51	0.845	0.870	0.895	0.920	0.945	0.970	0.995	1.020
0.5	0.850	0.875	0.900	0.925	0.950	0.975	1.000	1.025
0.49	0.855	0.880	0.905	0.930	0.955	0.980	1.005	1.030
0.48	0.860	0.885	0.910	0.935	0.960	0.985	1.010	1.035
0.47	0.865	0.890	0.915	0.940	0.965	0.990	1.015	1.040
0.46	0.870	0.895	0.920	0.945	0.970	0.995	1.020	1.045
0.45	0.875	0.900	0.925	0.950	0.975	1.000	1.025	1.050
0.44	0.880	0.905	0.930	0.955	0.980	1.005	1.030	1.055
0.43	0.885	0.910	0.935	0.960	0.985	1.010	1.035	1.060
0.42	0.890	0.915	0.940	0.965	0.990	1.015	1.040	1.065
0.41	0.895	0.920	0.945	0.970	0.995	1.020	1.045	1.070
0.4	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075
0.39	0.905	0.930	0.955	0.980	1.005	1.030	1.055	1.080
0.38	0.910	0.935	0.960	0.985	1.010	1.035	1.060	1.085
0.37	0.915	0.940	0.965	0.990	1.015	1.040	1.065	1.090

Table 2: Expected V_{AVS} with Different V_{ADC} and V_{REF} Combinations (Continued)

V_{REF}	0.50	0.55	0.60	0.65	0.70	0.75	0.80	0.85
V_{ADC}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}	V_{AVS}
0.36	0.920	0.945	0.970	0.995	1.020	1.045	1.070	1.095
0.35	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
0.34	0.930	0.955	0.980	1.005	1.030	1.055	1.080	1.105
0.33	0.935	0.960	0.985	1.010	1.035	1.060	1.085	1.110
0.32	0.940	0.965	0.990	1.015	1.040	1.065	1.090	1.115
0.31	0.945	0.970	0.995	1.020	1.045	1.070	1.095	1.120
0.3	0.950	0.975	1.000	1.025	1.050	1.075	1.100	1.125
0.29	0.955	0.980	1.005	1.030	1.055	1.080	1.105	1.130
0.28	0.960	0.985	1.010	1.035	1.060	1.085	1.110	1.135
0.27	0.965	0.990	1.015	1.040	1.065	1.090	1.115	1.140
0.26	0.970	0.995	1.020	1.045	1.070	1.095	1.120	1.145
0.25	0.975	1.000	1.025	1.050	1.075	1.100	1.125	1.150
0.24	0.980	1.005	1.030	1.055	1.080	1.105	1.130	1.155
0.23	0.985	1.010	1.035	1.060	1.085	1.110	1.135	1.160

2.3.1.1.2 Alternate Regulator Configuration

Some regulators do not contain a V_{FB} pin and only have VSENSE pins. The VSENSE of the regulator responds to dynamic voltage changes and adjusts V_{AVS} quickly. The AVS system works with this regulator configuration. In this case, an alternate connection topology is used as illustrated in Figure 3. In this topology, the output of VSENSE on the SoC is very close to V_{AVS}, and all of the above equations to find the component values are still valid. The C_{adc} will be half the value of the previous topology as there are two capacitors to rails instead of just one.

The above analysis assumes large input impedance for the V_{FB} node of the regulator so that the effective resistance of Rtop and Rbot is not changed. However, if the regulator has low input impedance the voltages created by the above equations do not hold as there is another parallel resistance path. To reduce this issue, lower values of Radc, Rtop and Rbot can be used but this can cause the DAC to source too much current. The solution is to use an operational amplifier as depicted in Figure 4. The op amp will have high impedance which limits the DAC current but allows for lower values of the resistor network. It is important that the values of the resistor network are not too low as the VSENSE pins can only source 35 mA of current. The added high value resistors depicted in Figure 4 ensure a starting voltage on the op-amp. This configuration can be used for both implementations of AVS depicted in Figure 2 and Figure 3.

To choose the resistor values for R_{op1} and R_{op2} in Figure 4, the ratio can be found by taking a voltage divider with V_{AVS} and thus V_{SENSEP} set to 0.85V, V_{FB} set to the appropriate value based on the regulator and V_{ADC} set to the appropriate look-up value in Table 2. The absolute value of R_{op} should be in the 100 kΩ range. For example, for a regulator with V_{FB} set to 0.55V, V_{ADC} should be set to 0.55V. With R_{op1} set to 100 kΩ, R_{op2} should be set to 185 kΩ.

Figure 3: Alternate AVS Configuration

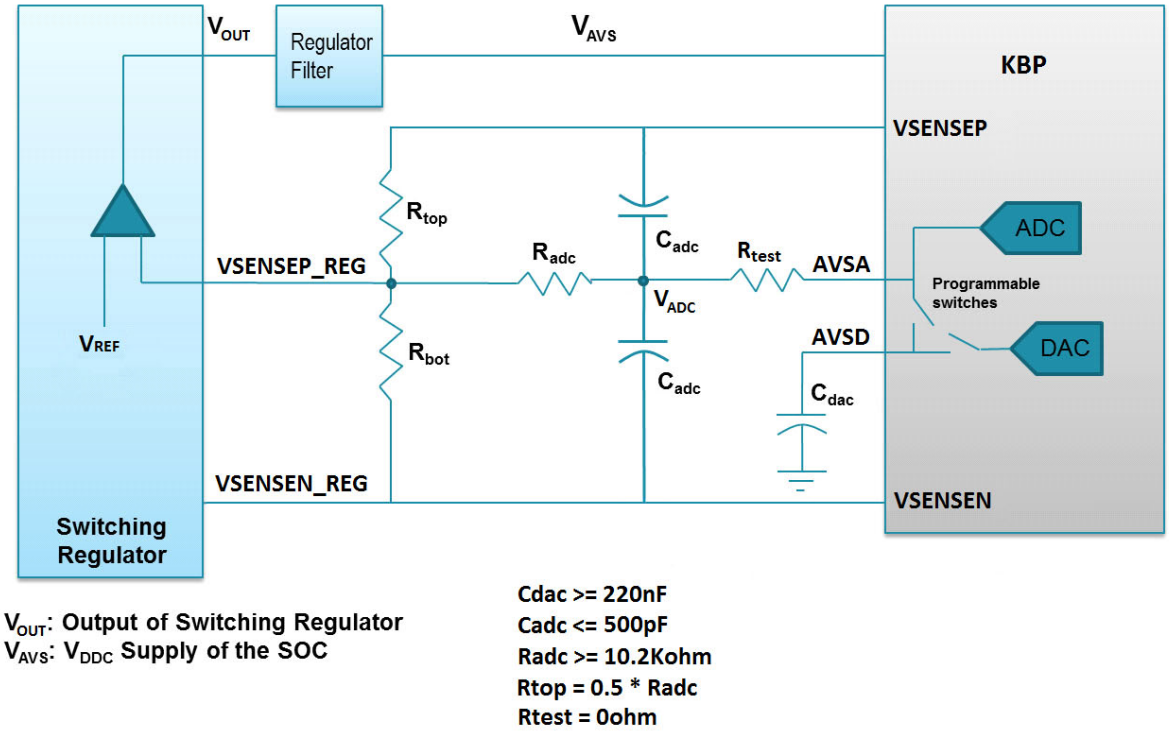
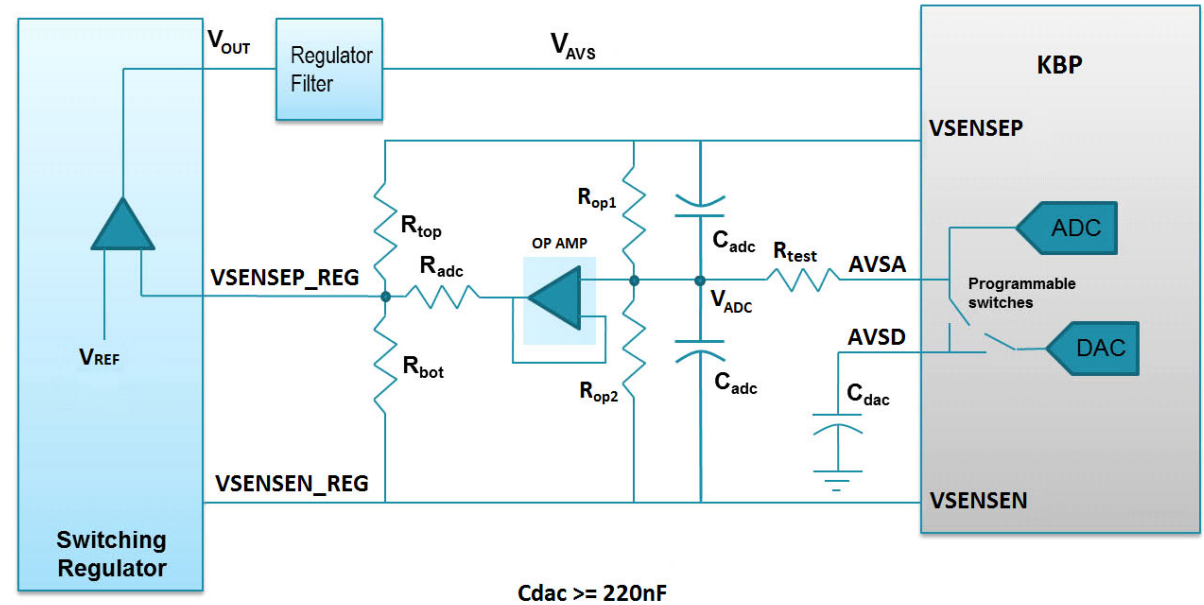


Figure 4: Alternate AVS Configuration with Op Amp

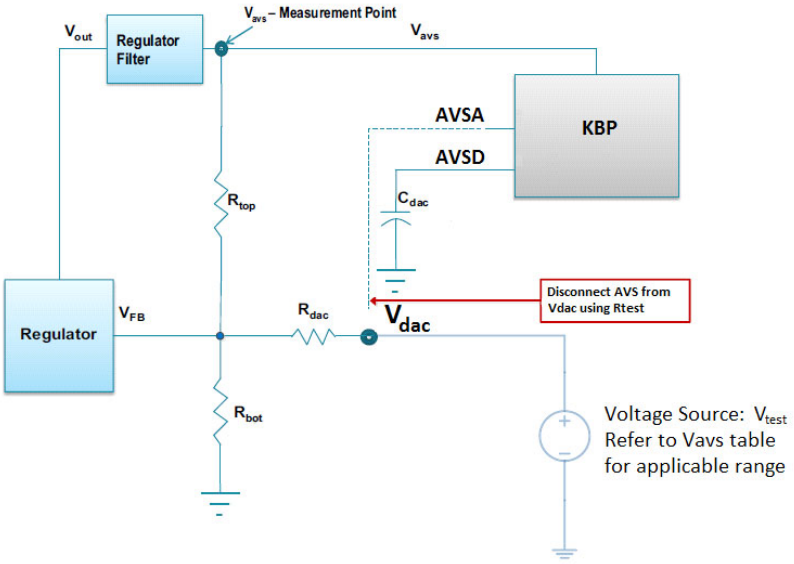


V_{OUT}: Output of Switching Regulator
V_{AVS}: V_{DDC} Supply of the SOC

Cdac >= 220nF
Cadc <= 500pF
Radc >= 10.2Kohm
Rtop = 0.5 * Radc
Rtest = 0ohm

2.3.1.1.3 Regulator Testing Procedure

Figure 5: Configuration to Test Switching Regulator



The applied voltage is not allowed by the chip hardware to drop below, or go above, a certain voltage. These levels depend on the silicon speed and temperature of an individual part. Use the following to test the switching regulator that supplies the AVS voltage. See to Figure 5.

CAUTION! There is a risk of damaging the device if the initial voltage level from the voltage source used in this test is not set in the safe 0.75V–0.80V voltage range.

1. Start with a system board with all the components installed, including the AVS components specified in these guidelines.
2. Disconnect the R_{test} resistor from the device by lifting its terminal on the R_{ADC} side from its connection pad. R_{test} is optional and can be shorted. In this case, the R_{ADC} terminal on the BCM16K and BCM5235 side is to be lifted from its connection pad. See Figure 5.
3. To protect the BCM16K and BCM5235 against accidental damage, set the external voltage source V_{test} (connected to the test point at V_{ADC}) to an initial safe value in the range of 0.75V–0.80V.
4. Power up the board.
5. Attach the external voltage source to the added test point at V_{ADC}, which is now disconnected from the device. If the R_{test} resistor was not used, connect the external supply to the lifted R_{ADC} resistor terminal.
6. Slowly vary the voltage from the external voltage source (V_{test} connected at V_{ADC}) in the highlighted range indicated in Table 2 for the specific regulator's V_{REF}. Since the safe starting voltage is somewhere in the middle of the range, it is necessary to vary the voltage in the upward and downward directions to cover the full range.
   – It is very important to stay within the allowed range in Table 2. Going outside the allowed range in Table 2 might damage the device.
   – In Table 2, the yellow cells reflects the expected AVS voltage for each V_{REF} level.
   – For example, if the regulator being used has a nominal V_{REF} value of 0.6, the allowed V_{test} range is from 0.86V to 0.40V to cover the AVS operating range of 0.72V to 0.95V.
7. Measure the V_{AVS} voltage at the top terminal of R_{top} at each V_{test} input level using a voltmeter.

NOTE: Measuring the V_{AVS} voltage at any other location may show discrepancies relative to the expected voltage in the table due to board IR-voltage drop.

8. After the V_{test} sweep is completed and the data is collected from steps 6 and 7 above, return the voltage-source voltage to the initial safe zone (0.75V–0.80V) and disconnect from the board.
   – Only after the voltage source is disconnected from the board can the V_{test} supply be turned off.
9. The board can be safely powered off after V_{test} is disconnected.
10. Plot the measured V_{AVS} and the corresponding expected voltages from Table 2 (for the specific V_{REF} of the chosen regulator) against V_{ADC} and compare the results.
    – The BCM16K and BCM5235 VDD voltage V_{AVS} as a function of the external voltage source should follow Equation 1 with V_{ADC} set to V_{test} values.
    – It is expected that the curves be within 2% of each other and the relationship to V_{ADC} is linear. If this condition is not met, the AVS system will not function as needed. Choosing a different regulator is recommended.

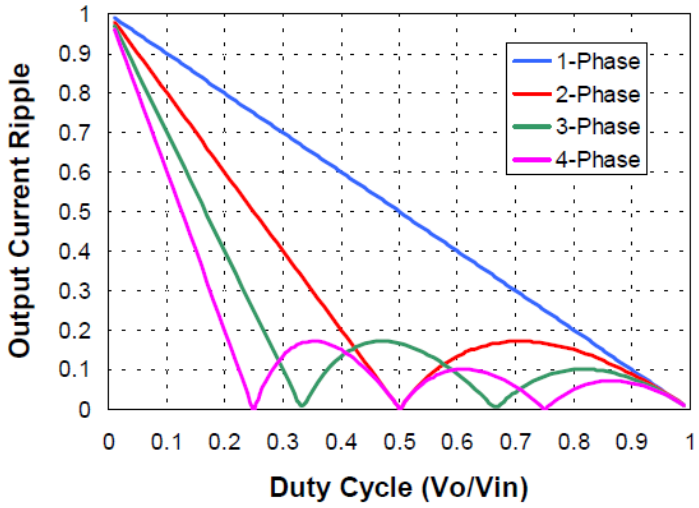
2.3.1.2 Multi-Phase Topologies for VDD Core

Use of a multi-phase topology has the following advantages:

- Reduced output voltage ripple as a result of inductor current ripple cancellation.
- Faster transient response as a result of smaller inductors.
- Possible to reduce overall solution size.
- Efficiency improvements.

It is recommended to use a multi-phase regulator for the VDD core voltage.

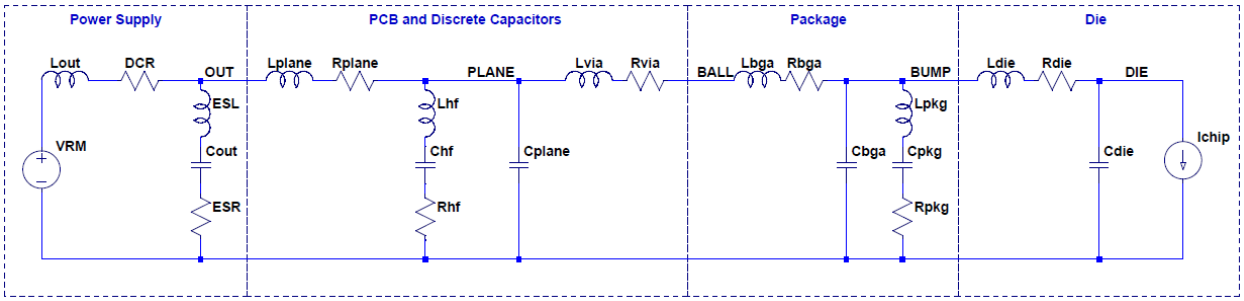
Figure 6: Normalized Output Current Ripple vs. Duty Cycle



2.4 VDD Core Power Delivery Network and Decoupling Scheme

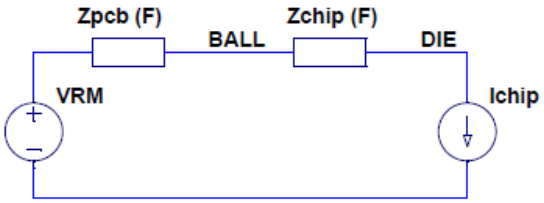
The output impedance of a perfect voltage source is zero, meaning the source can supply any current with no change in voltage. In a real system supplying power to an integrated circuit, the output impedance is composed of several components and many parasitic elements. A lumped element model of a typical system is shown in Figure 7.

Figure 7: Components and Parasitic Elements of a Typical Power Delivery Network



The power delivery network can be thought of as a voltage source with a frequency-dependent source impedance. Using Thevenin's Theorem, the source impedance can be found easily as a combination of the components in Figure 7. In Figure 8, it is split amongst PCB (controlled by the system designer) and chip components (controlled by the vendor).

Figure 8: Equivalent Circuit Split Into PCB and Chip Impedances



The voltage range for the core VDD supply is specified as ±3%. It is assumed that this will be split evenly amongst the regulator variation (AC + DC) and the AC ripple at the BGA caused by the chip noise. Thus the device's specification for maximum AC ripple is 1.5% or 12 mV for an 800 mV supply.

The change in load current varies greatly depending on the application. The factors that affect this load current are the search rate, number of active blocks, and the operating frequency. The device can experience extremely high current spikes in the worst case. The maximum current change is 50 A/ns, although this is unlikely to occur under practical applications. Active blocks should be limited as much as possible.

The impedance of the PDN is given by:

$$Zpdn,\ max(f) = \frac{Vn,\ chip}{Ichip\ (f)}$$

Thus, Zpdn, max (f) should be around 0.24 mΩ over the frequency range of the loop bandwidth of the regulator to the effective frequency the board can decouple. The loop bandwidth of a typical buck converter switch regulator is in the 100 kHz range. The effective frequency the board can decouple is on the order of 10 MHz. These parameters are summarized in Table 3.

Table 3: Design Parameters for Core Supply PDN Analysis

Parameter	Symbol	Specification/Target
Chip noise budget	$V_{n, chip}$	12 mV
Maximum PCB impedance	$Z_{pcb, max}$	0.24 mΩ
PCB impedance bandwidth	$f_{H, pcb}$	100 kHz to 10 MHz

The inductance (ESL) of the decoupling capacitors is dominated by the component dimensions, and also highly depends on the loop area created by connection to power planes. It is extremely important to reduce the ESL of the decoupling as much as possible. This is achieved through thoughtful placement and layout techniques:

1. Place vias in pads of 0603 or 0402 capacitors.
2. Use low-inductance capacitors. (for example, reverse geometry or land grid array capacitors).
3. Place as many via as possible for each pad of large capacitors – 0805 and larger.
4. Place the via very near the pad (with very short or no trace) of a capacitor, where via-in-pad violates DFM rules.
5. Minimize via length when possible.

   If power planes are close to top-side, placing capacitors on top-side surrounding the chip will result in significantly lower mounting inductance versus placing the capacitors on the bottom-side.

The resistance (ESR) of the capacitor is due to metal resistance and depends on the material properties of the component. Since it is a function of material properties, the ESR value differs dramatically across different vendor offerings of equivalent components. The ESR must be supplied by the capacitor vendor (or measured) and should be kept as low as possible.

It is highly recommended to place 0402 decoupling capacitors in the power and ground via array under the chip. This area is essentially free real estate since it cannot be used by any other components. It is recommended to start decoupling by adding one 0402 capacitor per VDD/GND pair.

The decoupling scheme starts with high-frequency decoupling capacitors placed in the power and ground via array under the chip. Figure 8 illustrates such a placement. Progressively higher valued capacitors ring the device which lowers the impedance at lower frequencies. The bottom side of the board may also be used to ring the device with capacitors. X2Y capacitors should also be considered as they can achieve a lower ESL. The complete decoupling scheme should be simulated to achieve the recommended impedance over the wide frequency range.

Figure 9: Recommended Decoupling Capacitor Placement Under the Device

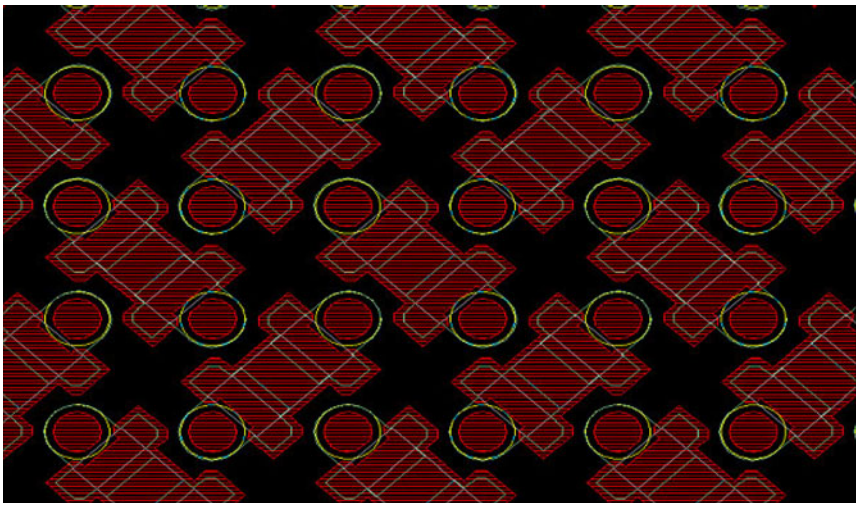


Table 4 provides list of VDD-Core-Supply decoupling capacitors from a real board example. The board has two, 2-oz cupper planes for the VDD and two, 2-oz cupper planes as Reference (GROUND) adjacent to the VDD planes.

Table 4: Core Supply PDN Example Decoupling Component Summary

Item	Qty	Capacitor	Value	ESL (H)	ESR (Ohm)	PKG	Vendor	Placement Location
a	40	ECASD60D477M4R5K00	470 µF	1.63E-09	0.00276	7343	Murata	Output of the 10-Phase Regulator
b	40	GRM31CR60J107ME39	100 µF	5.78E-10	0.00292	1206	Murata	Output of the 10-Phase Regulator
1	30	T528Z337M2R5ATE008	330 µF	3.66E-10	0.0065	7343	KEMET	4th Postion
2	20	CL21X226MQQNNNE	22 µF	5.68E-10	0.00315	0805	Samsung	4th Postion
3	25	GRM21BR61C106KE15K	10 µF	4.17E-10	0.00499	0805	Murata	3rd Position
4	30	LLL317R71A105MA01L	1 µF	1.87E-10	0.0042	0612	Murata	3rd Position
5	25	LLL31MR60J106ME01L	10 µF	3.07E-10	0.00437	0612	Murata	2nd Position
6	50	LLL153C80G105ME21D	1 µF	1.07E-10	0.0054	0204	Murata	2nd Position
7	88	LG224Z474MAT2S1	0.47 µF	5.93E-11	0.0037	0306	AVX	1st Position
8	34	W2L14Z225MAT1S	2.2 µF	6.50E-11	0.00166	0508	AVX	1st Position
9	60	GRM155R71A474KE01D	0.47 µF	1.95E-10	0.018	0402	Murata	Place under the BGA
10	60	CL05A474KQ5NNNC	0.47 µF	2.55E-10	0.0168	0402	Samsung	Place under the BGA
11	70	CL05B224KO5NNNC	0.22 µF	3.06E-10	0.014	0402	Samsung	Place under the BGA

Figure 10 illustrates the recommended bypass capacitors placement for the VDD core supply based on the capacitors listed in Table 4.

Figure 10: VDD Core Supply Bypass Capacitor Placement

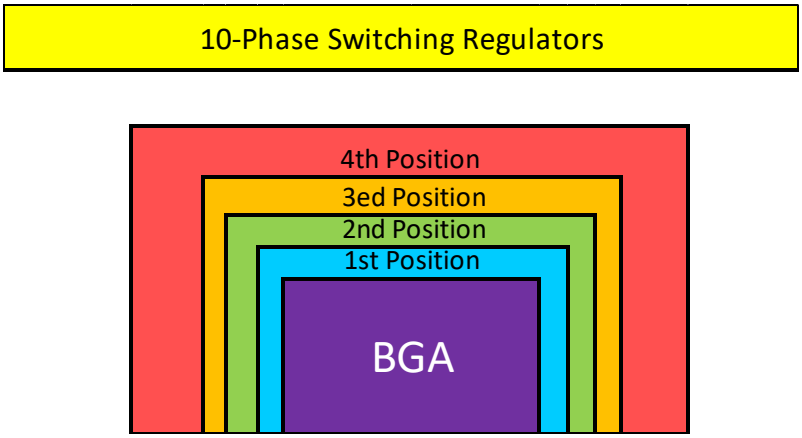
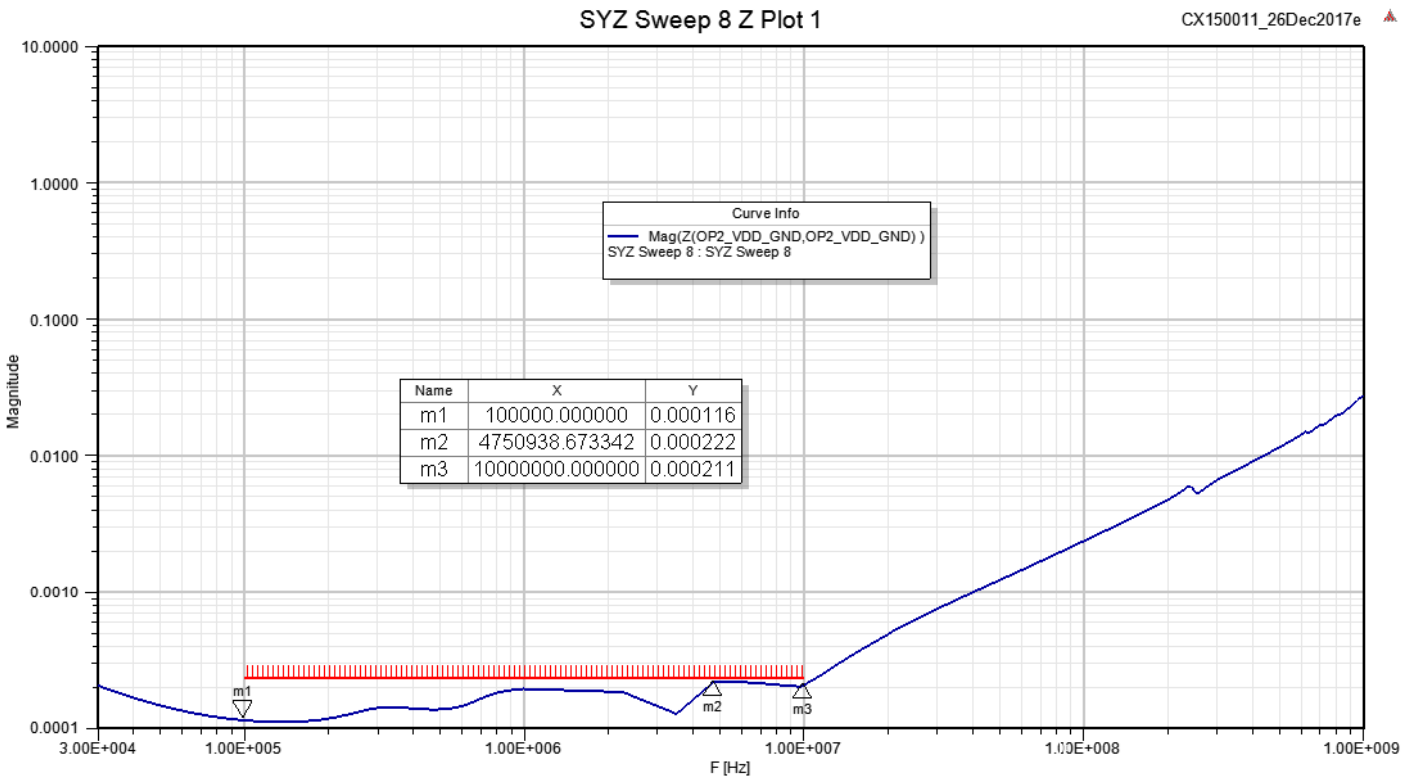


Figure 11 is the VDD PDN's Z11 impedance versus frequency plot obtained by running 3D EM Simulation of the board and the bypass capacitors' S-parameters.

Figure 11: Z11 Impedance vs. Frequency Plot of VDD Core Looking at the BGA



2.4.1 VDDM Digital Supply and PDN Specification – SRAM Memory

VDDM powers the SRAM on the chip. Its value is specified at 0.85V. A separate power supply is required for VDDM as it is a different voltage from VDD or the analog supplies. Due to the high current requirement, a switching regulator is recommended to power VDDM.

Following the same narrative mentioned for the VDD Core Voltage, the VDDM PDN parameters are summarized in Table 5.

Table 5: VDDM PDN Design parameters

Parameter	Symbol	Specification/Target
Chip noise budget	Vn, chip	12 mV
Maximum transient current	Ichip (f)	1A
Maximum PCB Impedance	Zpcb, max	0.012Ω
PCB Impedance Bandwidth	fH, pcb	100 kHz to 10 MHz

Table 6 provides list of VDDM supply decoupling capacitors from a real board example. The board uses one 1-oz cupper for the VDDM planes.

Table 6: Recommended VDD Core Supply Decoupling Capacitors

Item	Qty	Capacitor	Value	ESL (H)	ESR (Ohm)	PKG	Vendor	Placement Location
1	2	ECASD60D477M4R5K00	470 µF	1.63E-09	0.00276	7343	Murata	2nd Position
2	3	CL31B106KLHNNN	10 µF	3.72E-10	0.01	1206	Samsung	1st Position
3	3	LLL31MR70J475MA01	4.7 µF	2.94E-10	0.0026	`0612	Murata	1st Position
4	20	GRM155R61A105KE15	1 µF	3.72E-10	0.01	`0402	Murata	Place under the BGA

Table 12 illustrates recommended bypass capacitors placement for the VDDM supply rail based on the capacitors listed on Table 6.

Figure 12: VDDM Supply Bypass Capacitor Placement

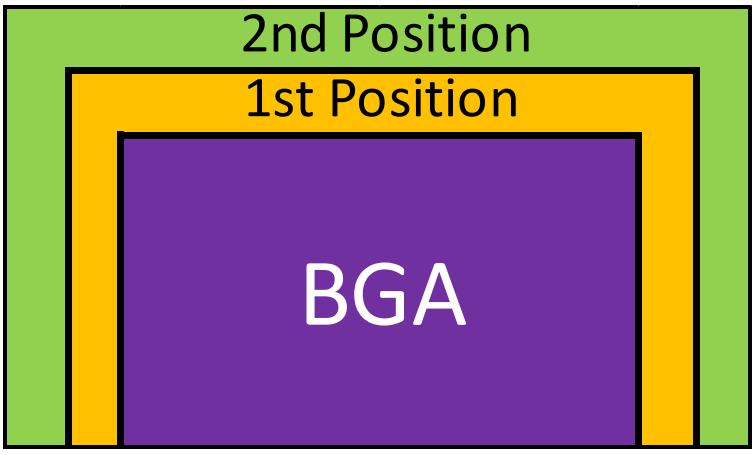
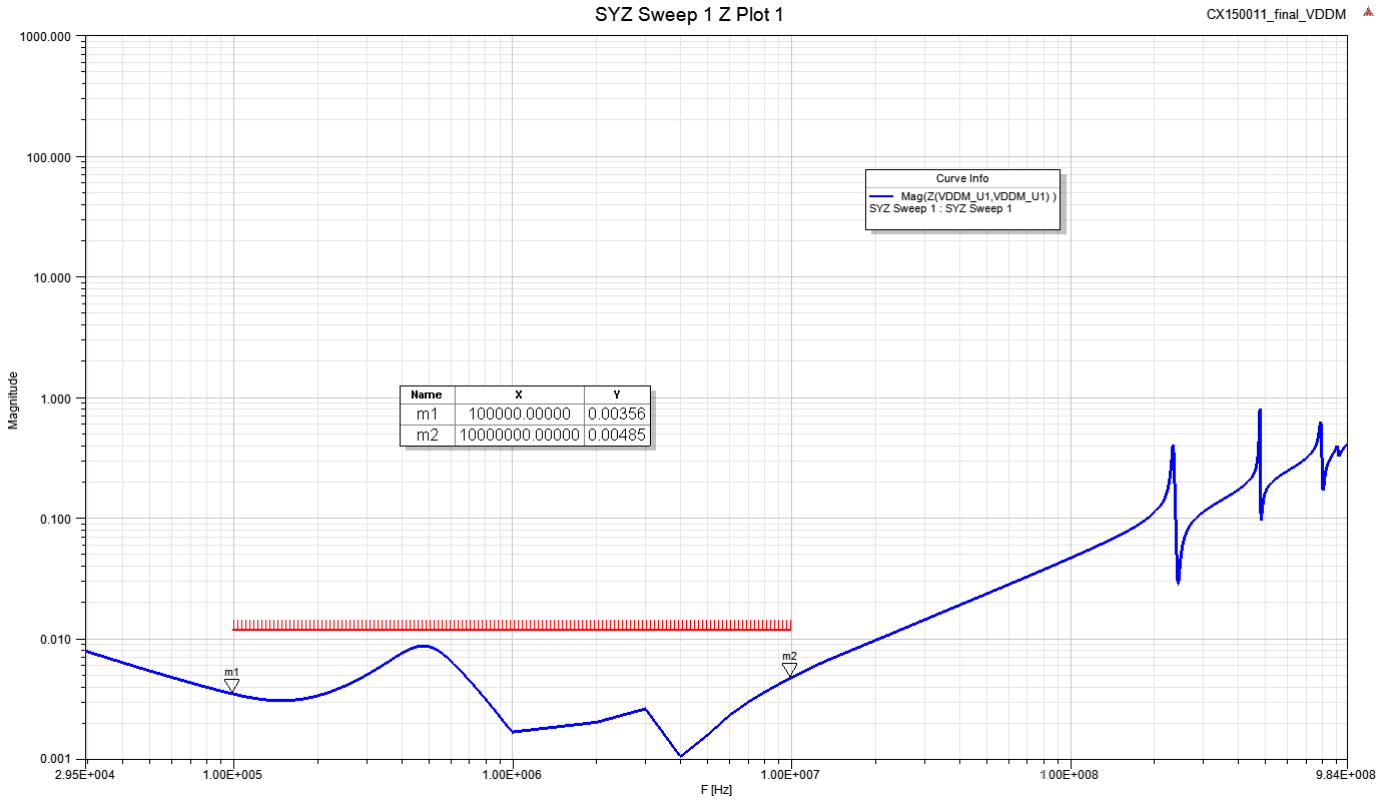


Figure 13: Z11 Impedance vs. Frequency Plot of VDD Core Looking at the BGA



2.4.2 VDD18 Digital Supply and PDN Recommendation (HVA)

A VDD18 at, 1.8V typical value, powers the low-speed I/Os, for example, MDIO and I^2C plus miscellaneous circuits inside the chip. It is recommended to place one 1 µF 0402 capacitor per power pin under the BGA.

2.4.3 VDDCPLL Analog Supply and Filtering Specification (HVA)

A VDDCPLL, at 1.8V typical value, powers the core logic PLL circuitry. It is an analog rail and sensitive to noise. Filtering is required to prevent unwanted noise from getting coupled into this rail. See Table 7 for filter recommendations.

Table 7: Filter Recommendations

Filter Requirement	Component Type
Ferrite bead filter, second order – Bandwidth < 100 kHz, DCR ≤ 0.1Ω and capacitors with DCR < 15 mΩ	120Ω at 100 MHz, ferrite bead[a], Low ESR 10 µF cap, and one 0.1 µF (0402 PKG) cap per pin.

a. A ferrite bead should have a low DC resistance (DCR) of 360 mΩ or less. This limits the DC drop across the ferrite/inductor to 1% of the supply.

2.5 56 Gb/s PAM-4 SerDes Supplies Specifications

There are 48 x 56 Gb/s PAM-4 SerDes. They come in blocks of eight. For example, one block consists of eight [Tx and Rx] differential serial links which is referred to as an octet. There are total of six octets and each octet has the following power rails:

- VDDS[1–6] = 0.8V
- VDDS08PLL[1–6] = 0.8V
- VDDS18PLL = 1.8V
- VDDSL = 0.90V
- VDD12 = 1.2V

The supplies are summarized in Table 1.

2.5.1 VDDS[1–6] Analog Supply and Filtering Specification

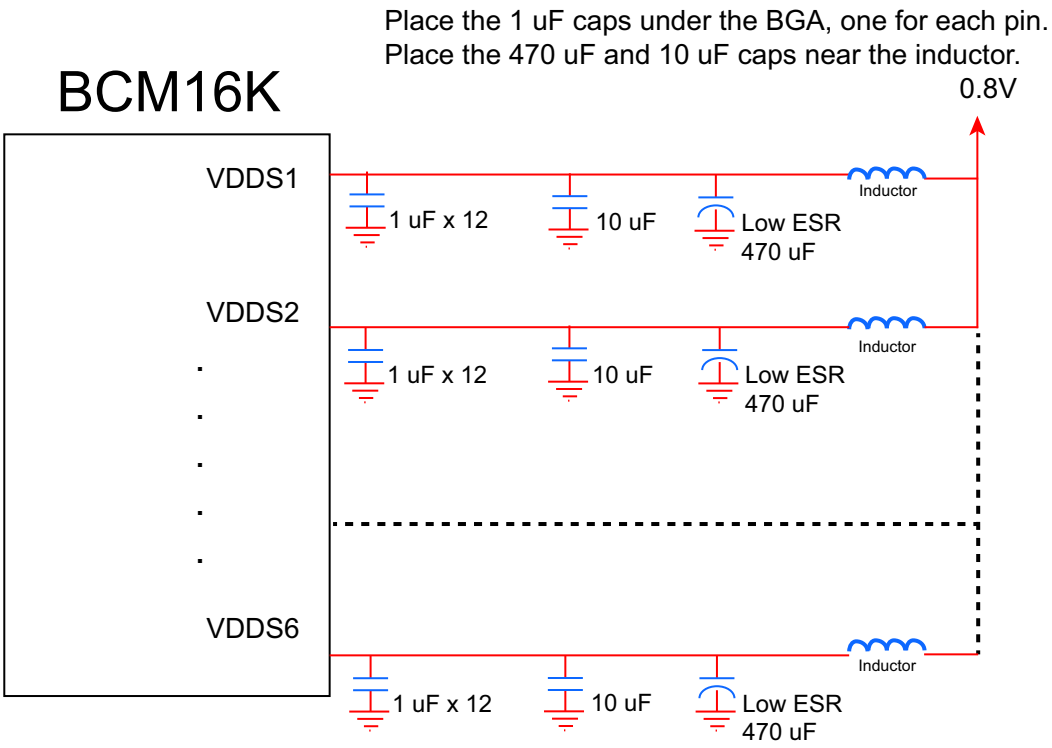
A VDDS[1–6], at 0.8V typical value, supply power to the SerDes's Tx and Rx circuits. Use one filter network per VDDS[1–6]. Use one 0.1 µF (0402) capacitor per pin. Table 8 and Figure 14 identify both the circuit and the components for recommended power supply filtering. See Table 8 for supply specification.

Table 8: VDDS[1–6] Analog Supply and Filtering Specification

Filter Requirement	Component Type
LC filter or ferrite bead filter, second order - Bandwidth < 50 kHz	For Each Octet (TX and RX Combine): ■ One 1 µH L[a], 5.5A, 600Ω at 100 MHz inductor. ■ One low ESR 470 µF cap or two low ESR 220 µF caps. ■ One 10 µF cap. ■ One 1 µF cap (0402) for each pin placed under the BGA.

a. The inductor or ferrite bead should have a low DC resistance (DCR) of 9 mΩ or less at least 3A. This limits the DC drop across the ferrite/inductor to 1% of the supply. The voltage specification listed above must be met regardless of the IR drop.

Figure 14: Circuit Components



2.5.2 VDDS08PLL[1–6] Analog Supply and Filtering Specification

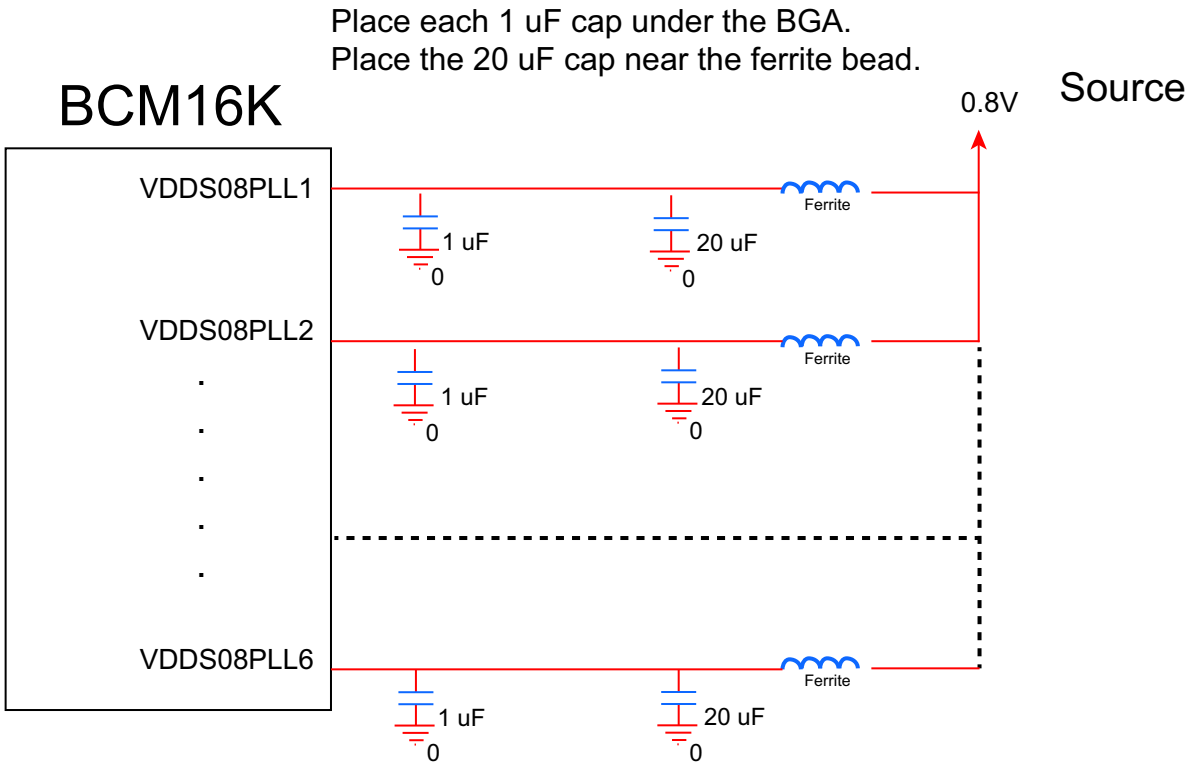
A VDDS08PLL[1–6], at 0.8V typical value, supplies power to SerDes's PLL circuits. Use one filter network per VDDS08PLL[1–6] rail and use one 1 µF (0402) capacitor per pin under the BGA. Table 9 and Figure 15 identify both the circuit and the components for recommended power supply filtering. See Table 9 for supply specification.

Table 9: VDDS08PLL[1–6] Analog Supply and Filtering Specification

Filter Requirement	Component Type
LC filter or ferrite bead filter, second order - Bandwidth < 50 kHz	For each octet: ■ 1.5A, 600Ω at 100 MHz, ferrite bead[a]. ■ One 20 µF cap. ■ One 1 µF cap (0402) for each pin placed under the BGA.

a. The inductor or ferrite bead should have a low DC resistance (DCR) of 65 mΩ or less. This limits the DC drop across the ferrite/inductor to 1% of the supply. The voltage specification listed above must be met regardless of the IR drop.

Figure 15: Circuit Components



2.5.3 VDDS18PLL Analog Supply and Filtering Specification

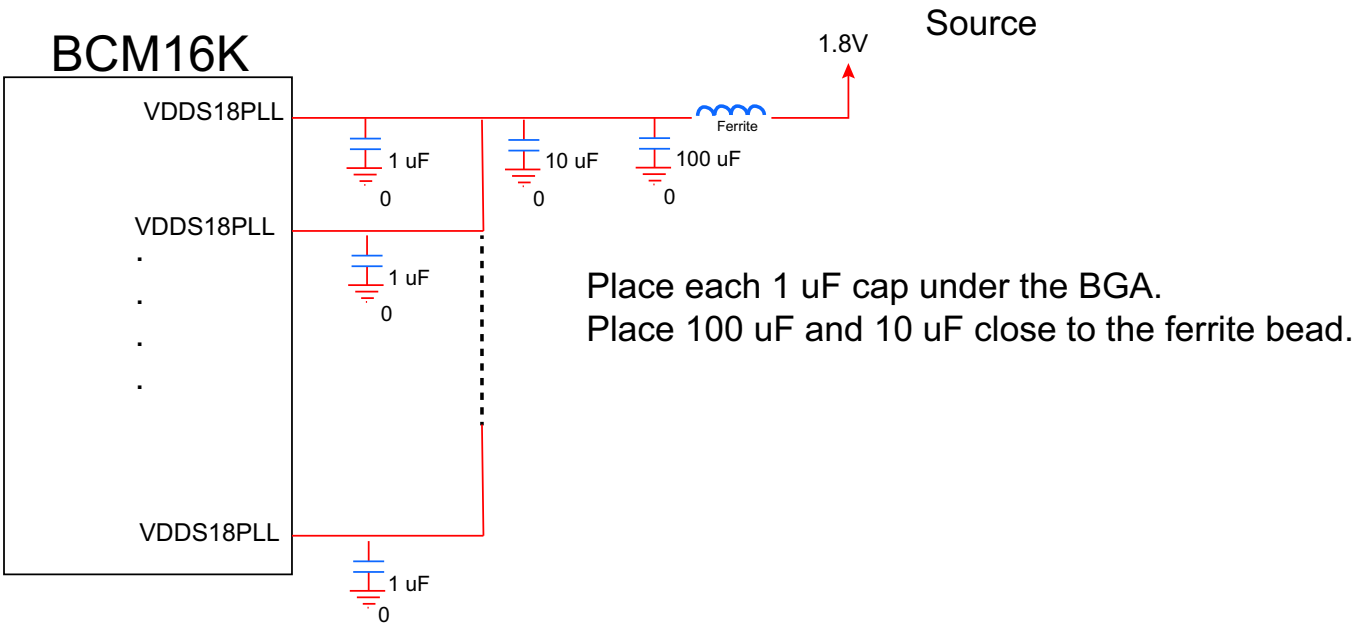
A VDDS18PLL, at 1.8V typical value, supplies power to SerDes's PLL circuits. Use one filter network for all VDDS18PLL rails and use one 1 uF (0402) capacitor per pin under the BGA. Table 10 and Figure 16 identify both the circuit and the components for recommended power supply filtering (see Table 10 for supply specification).

Table 10: VDDS18PLL Analog Supply and Filtering Specification

Filter Requirement	Component Type
LC filter or ferrite bead filter, second order – Bandwidth < 50 kHz	■ 2A, 120Ω at 100 MHz, ferrite bead[a]. ■ One 100 µF cap ■ One 10 µF cap ■ One 1 µF cap (0402) for each pin placed under the BGA.

a. Inductor or ferrite bead should have a low DC resistance (DCR) of 560 mΩ or less. This limits the DC drop across the ferrite/inductor to 1% of the supply. The voltage specification listed above must be met regardless of the IR drop.

Figure 16: Circuit Components



2.5.4 VDDSL Digital Supply and PDN Specification

A VDDSL, at 0.90V typical value, powers the digital circuits inside the SerDes blocks. Use a separate regulator for VDDSL. No filtering is required. This is a digital rail and requires one 1 µF (0402) capacitor per pin for bypassing purposes. Place the capacitor right under the BGA. See Table 11 for supply specification.

2.5.5 VDD12 Supply and PDN Specification

A VDD12, at 1.2V typical value, powers the SerDes termination circuits. No filtering is required. It requires one 1 uF (0402) capacitor per pin for bypassing purposes. Place the capacitor right under the BGA. See Table 11 for supply specification.

SerDes supplies are summarized in Table 11.

Table 11: SerDes Supply Specifications

	Supply/Conditions	Min.	Typical	Max.
Absolute Voltage	VDDS[1–6], VDDS08PLL[1–6]	0.775V	0.80V	0.825V
	VDDS18PLL	1.745V	1.8V	1.855V
	VDD12	1.165V	1.2V	1.235V
	VDDSL	0.87V	0.90V	0.93V
Source current	VDDS[1–6]	–	770 mA	900 mA
	VDDS08PLL[1–6]	–	100 mA	120 mA
	VDDS18PLL	–	25 mA	32 mA
	VDD12	–	550 mA	800 mA
	VDDSL	–	600 mA	720 mA
uAC ripple ratio	10 kHz to 100 MHz	–	–	--
	VDDSL			1.5%
	VDDS18PLL[1–6], VDD12, VDDS[1–6]	–	–	1.25%
	VDDS08PLL[1–6]	–	–	0.375%

NOTE: Power supply pins are required to be fanned out to individual vias to connect to power supply planes. Sharing vias with multiple supply pins significantly increases the BGA loop inductance and is prohibited.

2.6 PCIe 2 SerDes Supplies and Filtering

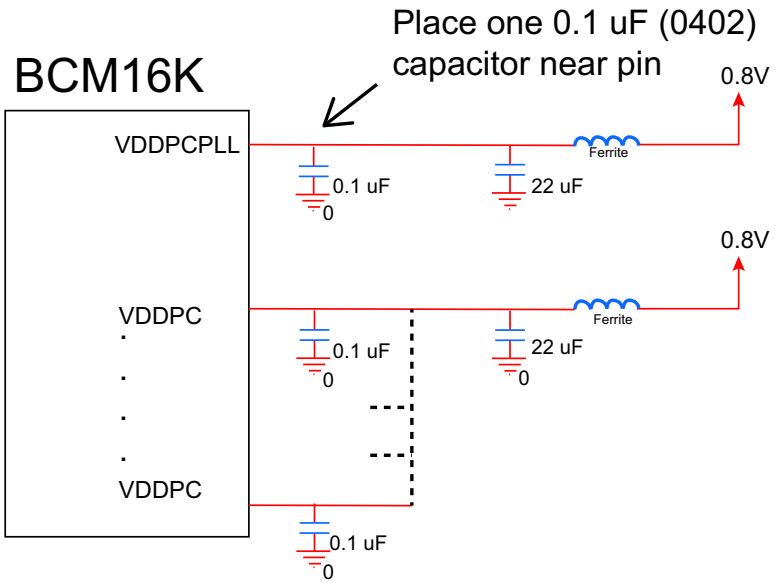
The PCIe SerDes has two different supplies:

- VDDPC – The Tx and Rx supply sourced from a 0.8V regulator.
- VDDPCPLL – The PCIe-PLL supply sourced from a 0.8V regulator.

Each rail should have its own filter. Place a 0.1 µF, 0402 capacitor on the bottom side of the board right under the corresponding BGA pin.

Figure 17 illustrates proper power supply filtering for both VDDPC and VDDPCPLL.

Figure 17: SerDes Supplies and Filtering



The PCIe SerDes supplies are summarized in Table 12.

Table 12: PCIe SerDes Core and PLL Supply Specifications

Specification	Supply/Conditions	Min.	Typical	Max.
Absolute Voltage	VDDPC	0.775V	0.80V	0.825V
	VDDPCPLL	0.775V	0.80V	0.825V
Source Current	VDDPC	–	50 mA	60 mA
	VDDPCPLL	–	50 mA	60 mA
AC Ripple Ratio	10 kHz to 100 MHz	–	–	–
	VDDPC, VDDPCPLL	–	–	1.5%

Table 13 describes the recommended filter for both PCIe supplies.

Table 13: Filter Recommendations for PCIe SerDes Core and PLL Supplies

Supply	Filter Requirement	Component Type
VDDPC, VDDPCPLL	Ferrite bead filter, second order – Bandwidth < 100 kHz	300Ω at 100 MHz ferrite bead, Low ESR 22 µF cap, and one 0.1 µF cap (0402) per pin.

The chosen inductor or ferrite bead should have a low DC resistance (DCR) of 133 mΩ or less. This limits the DC drop across the ferrite/inductor to 1% of the supply. The voltage specification listed in Table 13 must be met regardless of the IR drop.

2.7 Power Planes and Stack-up Placement

Due to the high level of digital switching current on the core supply, it is very important to minimize the via inductance between the power plane and BGA pins, as any increased inductance in the power path has a direct impact on the level of on-chip supply noise. Minimizing via inductance is accomplished by assigning the core power supply to a plane layer close to the component mounting side, effectively minimizing via length and inductive loop area. It is required to place the core supply plane within five layers of the component mounting side.

The board plane capacitance provides excellent decoupling and it is recommended to use multiple power and ground planes dedicated to the VDD and VSS rails. A power and ground plane pair separated by 4 mils of Megtron 6 has an approximate capacitance of 2 nF per 10 square inches. At a minimum, it is recommended to devote 10 square inches of the board power plane to VDD. VSS should be paired with VDD to ensure good decoupling.

The LVA and HVA supplies must be isolated from the noisy VDD supply to prevent noise coupling into the sensitive analog supplies. This can be achieved by physical separation and ground planes.

The LVA supply also exhibits switching current, though to a much lesser extent compared to the core supply. The LVA power plane can be placed as deep as 12 layers from the component mounting side.

Adjacent power/ground planes in the stack-up are very important in high-performance PCB designs. The added plane capacitance significantly lowers PDN impedance at high frequency. Wherever possible, it is recommended to utilize unused copper area to build additional plane capacitors with power/ground planes.

2.8 Sharing Supplies with Other Devices

Ideally, each device in the system is powered by its own, dedicated power supply. However, it is understood that when PCB real estate becomes constrained, component count may need to be reduced to fit the design within the allocated area, and the easiest method of doing so is to consolidate power supplies for multiple devices. This section provides some guidance on this topic. Below is a general procedure to follow to identify devices that may be consolidated. In this section, the device's power supply input will be referred to as a load.

1. Group loads by nominal voltage.
2. Split groups into sub-groups by load type (analog/digital, high power/low power, SerDes/non-SerDes), noise sensitivity, voltage tolerance, and so on.
3. Split sub-groups again by spatial location on the PCB.

After step 3, some judgment is required to determine which sub-groups could be powered by a single supply, which require further division, and which could be merged to share a single supply. Things to consider are IR voltage drop, transient load conditions, supply efficiency versus output current, and available real estate.

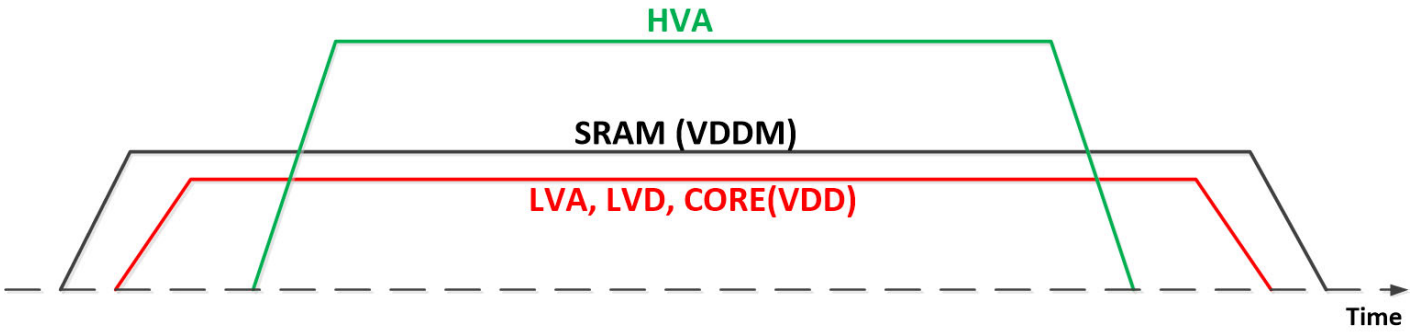
As mentioned previously, the LVA supplies are candidates for sharing. In this case, it is required to filter each supply even if the ripple specification is met.

2.9 Power-On and Power-Off Requirements

The main requirement to power on/off the device is not to allow the voltage difference between HVA, SRAM, and other supplies to exceed 1.0V. This should be accomplished using a sequenced supply power-up and power-down approach. The power supply ramp rates must be in the range of 5 mV/µs to 0.2 mV/µs (1 mV/µs recommended). The SRAM supply turns on first followed by the LVA/Core, and HVA supplies. The SRAM supply is allowed to turn on at the same time as the LVA/Core supplies. Each supply should be at full rail voltage before the next supply starts to ramp. The power-down sequence is the reverse order starting with HVA supplies followed by LVA/Core and finally SRAM supplies. The edge rates apply over the entire range of voltage. It is important that the device power-on from rails all at 0V to start with and power-off to a final voltage of 0V.

Before power-up, it is required that all signal inputs are low so as to avoid turning on the ESD diodes and damaging the device. Figure 18 illustrates the recommended power-on and power-off requirement.

Figure 18: Consecutive Approach Power Sequence and Reset Timing



2.10 Initialization Requirements

There are two initialization sequence requirements shown below. Figure 19 shows the recommended initialization sequence during normal operation and Figure 20 shows an example of the initialization required during debug.

Figure 19: Required Initialization Sequence During Normal Operation

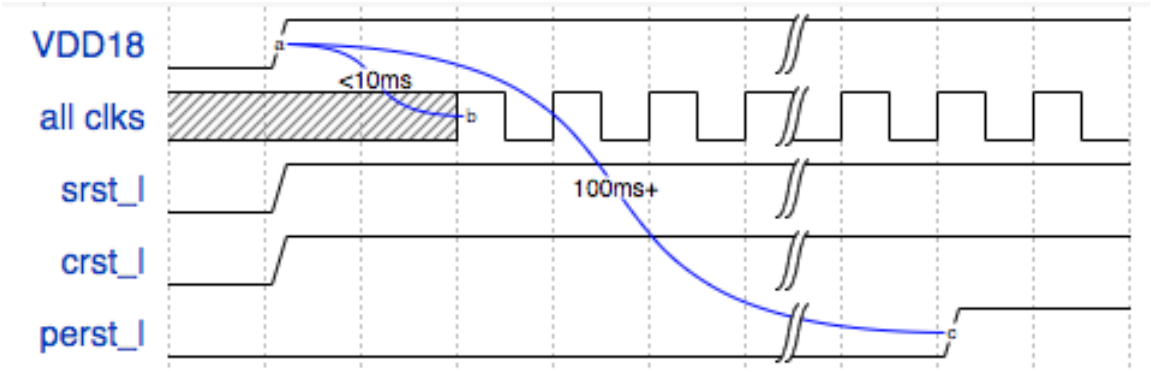
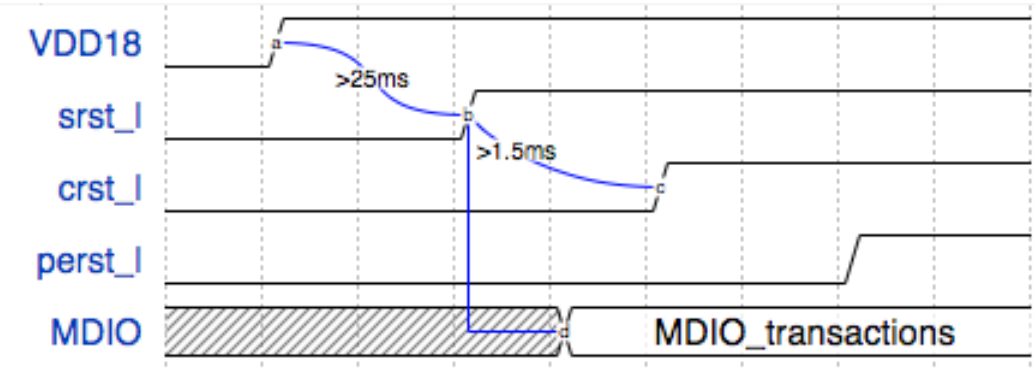


Figure 20: Example of Debug Initialization Sequence

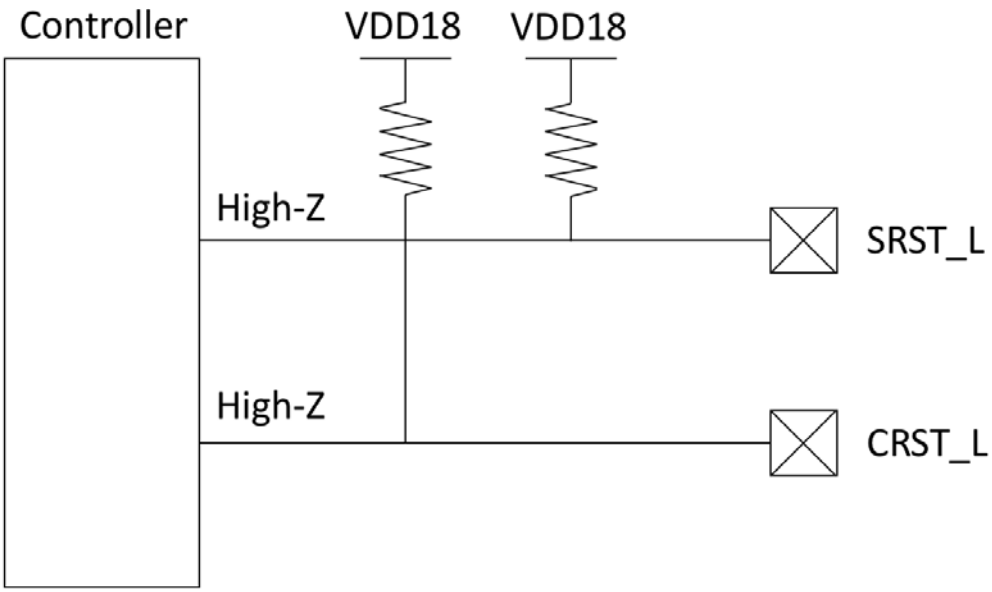


Under normal operation, SRST_L and CRST_L must be pulled high to VDD18 at power up, and all of the clocks must be stable within 10 ms of VDD18 stability. Once PCIe interface is up and running, the software continues to initialize the device over the PCIe interface.

Under debug, the system must be able to drive SRST_L and CRST_L with timing requirements as shown in Figure 20. Moreover, designers should ensure that the MDIO interface to the KBP is available anytime after SRST_L deassertion, before CRST_L and PERST_L deassertion.

To support both sequences, the recommended SRST_L and CRST_L connections are shown in Figure 21. The reset pins should be pulled up to VDD18 using 4.7 kΩ resistors, and also be connected to a controller. Under normal operation, the controller must keep these pins high-Z so that these pins are pulled high to VDD18 as VDD18 ramps up to 1.8V (as shown in Figure 19).

Figure 21: SRST and CRST Recommendation

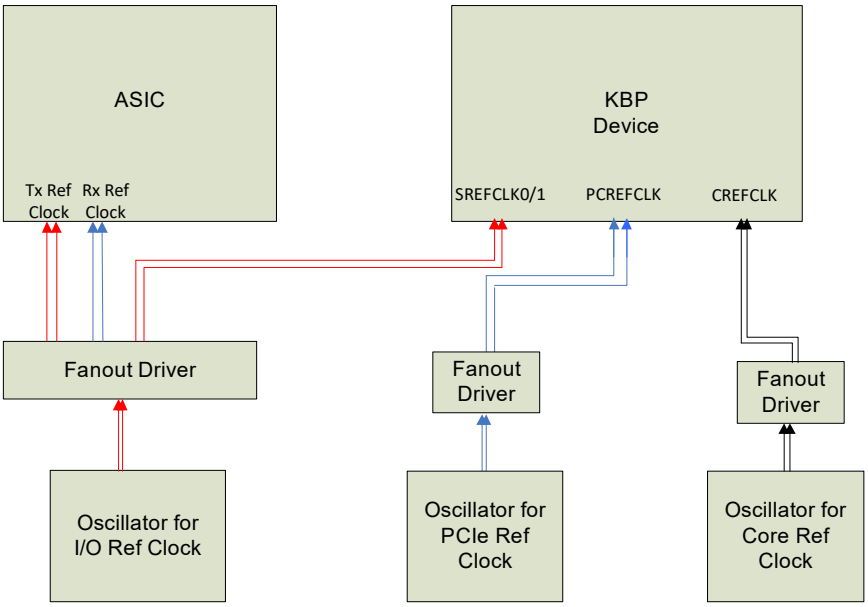


Chapter 3: Clocks

3.1 Overview

Figure 22 gives a general picture of the ideal clock topology.

Figure 22: Clock Topology Showing SREFCLK, PCREFCLK, and CREFCLK



This topology may not be possible to implement if the ASIC or host device's SerDes circuits require a reference clock frequency that does not match the specification of 156.25 MHz. In this case, the total PPM difference between the ASIC or host device's reference clock source and the device's reference clock source must not exceed 50 ppm.

All reference clocks are 100Ω differential clocks and each pair should be routed together with minimal skew between the positive and negative traces. They should also be shielded on all sides by their respective ground planes (VSS for the SerDes clocks and core clock). This means having VSS planes on top and bottom of the traces and lateral shielding traces or planes for the same layer of the traces. All lateral shielding needs to be stitched well to the above and below planes.

All reference clocks are terminated internally with a nominal differential termination of 100Ω. External termination is not required. To prevent ESD diodes from turning on and possibly damaging the device, it is required that the reference clocks (core clock, PCIe, and ILA SerDes reference) only turn on after the power-on sequence when all supplies are stable. This also applies to clocks which have on-board AC-coupling capacitors.

3.2 SerDes Reference Clocks

SREFCLK is the clock reference for the high-speed SerDes circuits, while PCREFCLK is the clock reference for the PCIe 2.0 circuits. Since the SerDes data rate is derived using the reference clock frequency, a precise reference is required to hit the desired data rate. Ideally, transmit and receive circuits on either side of the SerDes link operate at precisely the same data rate, which is the case when both reference clocks are derived from the same source. However, if this is not possible or is difficult to implement, the receiver circuits are able to handle small deviations in data rate. Table 14 shows the reference clock requirements for the high-speed SerDes clock SREFCLK.

Table 14: SREFCLK Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency	–	–	156.25	–	MHz
Frequency Offset	Between different REFCLKs	–50	–	+50	ppm
Signaling	CML	–	–	–	–
Amplitude	Differential Peak-Peak at Ball	0.8	1.0	1.4	V
Edge Rate	20%–80%		300	400	ps
Duty Cycle		40	50	60	%
Input Impedance	Differential	80	100	120	Ω
Common Mode Voltage	Internally biased	–	0.4	–	V
Integrated Phase Noise	12 kHz – 20 MHz	–	–	0.3	ps RMS
Phase Noise	at 10 kHz	–	–	–110	dbc/Hz
	at 100 kHz	–	–	–130	dbc/Hz
	at 1 MHz	–	–	–130	dbc/Hz
	at 10 MHz	–	–	–150	dbc/Hz
	at 100 MHz	–	–	–150	dbc/Hz

The two SREFCLK signals must be externally AC coupled into the device with 10 nF or greater capacitors. Table 15 shows the reference clock requirements for the PCIe reference clock PCREFCLK.

3.3 PCIe Reference Clock

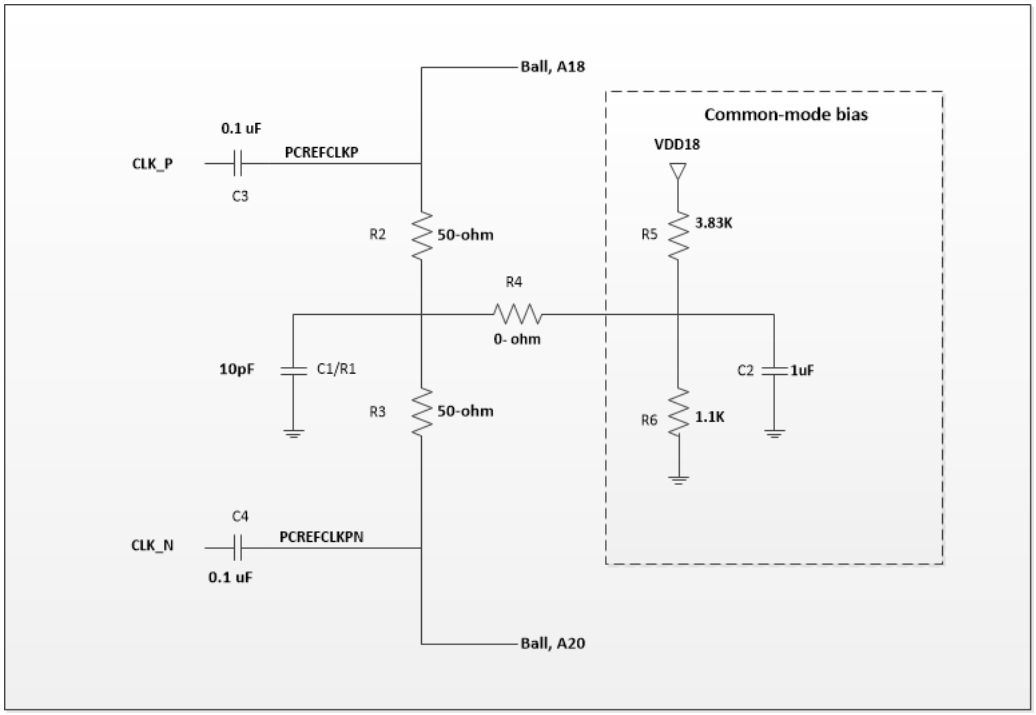
Table 15: PCREFCLK Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency	–	–	100	–	MHz
Frequency Offset	Between different REFCLKs	–100	–	+100	ppm
Signaling	CML	–	–	–	–
Amplitude	Differential Peak-Peak at Ball	0.6	–	1.6	V
Amplitude	Single-Ended Absolute Voltage[a]	–0.4		VDDPCPLL + 0.4	V
Common Mode Voltage	At the BGA Ball	0.1	–	0.7	V
Edge Rate	30%–70%	–	–	470	ps
Duty Cycle	–	40	50	60	%
Input Impedance	Differential	–	120	–	Ω
Integrated Phase Noise	12 kHz–20 MHz	–	–	1	ps RMS

a. Violating the Single-Ended Absolute Voltage could damage the device.

For PCREFCLK, AC-coupling, external termination, and external bias circuit is required (see Figure 23).

Figure 23: PCREFCLK Termination



3.4 Core Clock

The CREFCLK input supplies the clock to the core logic circuits. The clock input feeds a PLL and multiplier block generates a clock in the range of 250 MHz–1 GHz, depending on CPSEL configuration settings. See the data sheet for details on the CPSEL configuration. Table 16 gives the reference clock requirements for the core clock CREFCLK.

Table 16: CREFCLK Requirements

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency	–	–	156.25	–	MHz
Frequency Offset	Error in desired frequency	–100	–	+100	ppm
Signaling	CML	–	–	–	–
Amplitude	Differential Peak-Peak at Ball	0.5		1.8	V
Edge Rate	20%–80% with 500 mV swing			375	ps
Duty Cycle	–	30	50	70	%
Input Impedance	Differential	80	100	120	Ω
Common Mode Voltage	Internally biased	–	0.9	–	V
Integrated Phase Noise	12 kHz – 20 MHz	–	–	1	ps RMS

AC-coupling capacitors are not built into the device for CREFCLK. External 10 nF AC-coupling capacitors are required to be placed on the board.

Chapter 4: Thermal and Mechanical Considerations

4.1 Measuring Die Temperature

The 16 nm device includes an on-die temperature sensor. The scheme and error is TBD.

4.1.1 Cooling Considerations

System designers must consider heat management in their designs. The processor is a high-thermal density device manufactured with state-of-the-art process technology. The amount of heat generated on these high-speed circuits creates a significant thermal management challenge. Special attention must be paid to power budgets and heat removal requirements.

Thermal dissipation performance must be understood prior to integrating on a printed circuit board to ensure the device operates within its defined temperature limits. A proper heat sink and appropriate air flow must be provided to ensure device functionality and reliability.

The system designers must take into account the thermal effect on the downstream devices in the airflow from the heat generated by the upstream device as the downstream device will end up with higher T_A.

The appropriate heat requirement and air flow can be calculated using the equations below. The junction temperature is equal to the ambient temperature plus an offset proportional to the internal power dissipation P.

$T_J = T_A + \theta_{JA} \times P$

Where:

- T_J = Junction Temperature
- T_A = Ambient Temperature
- θ_{JA} = Thermal Resistance
- P = Power of the Device

θ_{JA} includes the temperature rise from junction to case and case to the outside ambient environment.

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

The system designer must provide heat sink and air flow to provide an adequate value for θ_{CA}. Adequate cooling must be provided to operate properly. The system designer must examine the environment, the enclosure, and the placement of the device.

4.2 Maximum Pressure Specifications

Table 17: Maximum Pressure Specifications

Parameter	Specification
Maximum Continuous Compressive Force	13.1 kg

Chapter 5: 56 Gb/s PAM-4 SerDes

5.1 Overview

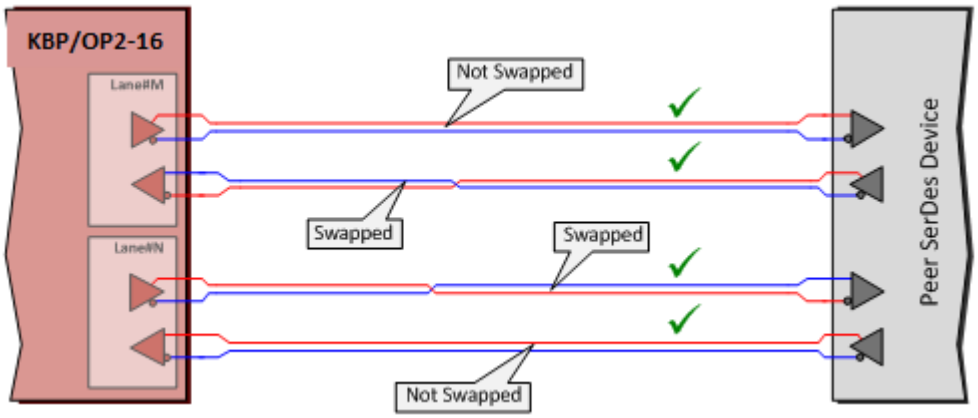
PAM-4 (4-level Pulse Amplitude Modulation) is the path forward to achieve 56 Gb/s and higher data rates. The reason that the industry is moving to PAM-4 is to help minimize channel loss. With two bits per UI, the Nyquest frequency is the same as if the device was running at 28 Gb/s NRZ (Non-Return to Zero Modulation). This means twice as much data over the same channels that are being used today for 28 Gb/s.

The tradeoffs are in the height of each eye losing about 9 dB by splitting one eye in NRZ into three eyes in PAM-4 and the complexity of the transmitter and especially the receiver. Since there are four distinct levels that must be recovered to accurately receive data, it will be much more challenging to repair the degradation of the incoming signal caused by channel impairments.

The 56 Gb/s PAM-4 SerDes has a few important features to reduce routing difficulty:

- The polarity of the 'P' and 'N' taps of each pair can be individually inverted. The configuration is software controlled via dedicated registers/bit on an individual pair basis. This feature is useful in addressing PCB layout issues related to P/N deskewing.

Figure 24: P/N Polarity Inversion Examples



- Per-link lane reversal.

  This feature *flips* the interface lane ordering. For example, in a single port configuration, lanes [15:0] can be remapped to lanes [0:15]. In dual port configuration, lanes [31:16] can be remapped to lanes [16:31] in addition to lanes [15:0] as in single port configuration. For detailed information, please refer to the Data Sheet – Section 16.4, Lane Swapping.
- Unused Tx and Rx SerDes pairs of octets can be left open (unconnected).

  Unused octets should be connected to an active supply and be powered down via software. There is no need to filter unused octets supply pins.
- When all SerDes cores in a group of certain LCPLL reference clock are not in use, this LCPLL reference clock is not required. The SREFCLK0 is used for lanes [39:32,15:0]. The SREFCLK1 is used for lanes [47:40,31:16].
- If a reference clock is not to be used, it may be left floating or tied to ground.
- All Rx links are internally AC coupled.

These AC couplings are on-die and cannot be bypassed. This internal AC coupling eliminates the need for external AC capacitors for most applications. External capacitors on the Rx are still required if the requirement for the maximum input Common Mode (VIN-CM Max) is not met. For more information, refer to the device data sheet. If external capacitors are required, use a 0201 package size capacitor to minimize the reflections caused by the structure impedance mismatch.

- Any peer device that interfaces to this SerDes must have AC coupling on its receiver.

  This peer AC coupling can be either embedded inside the peer device, or it can be implemented externally on the board level. In that case use a 0201 package size capacitor.

Refer to the appropriate data sheet for additional information.

5.2 High-Speed Routing and Board Layout Guidelines

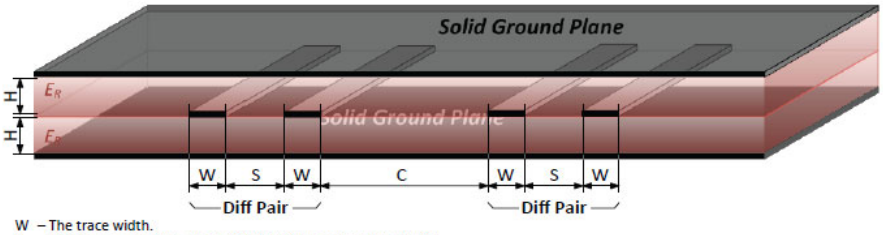
This section provides guidance on successfully implementing PCB channels with sufficient bandwidth to support 56.25 Gb/s PAM-4 differential signaling.

5.2.1 General Routing

Though the SerDes is terminated at 100Ω differential, the overall SerDes performance is improved if the user's PCB interconnect is set to a slightly lower impedance. Use 95Ω differential impedance for the Rx and Tx signals. For the breakout region under the BGA, use 25Ω for common mode signaling (or 50Ω single-ended routing). The recommended tolerance of the trace impedance is ±5%.

It is recommended to route the high-speed signals as a strip-line and not a micro-strip. Keep micro-strip routing short at less than 1 inch. Figure 25 shows a general differential pair geometry and stack-up.

Figure 25: General Differential Pair Geometry and Stack-up



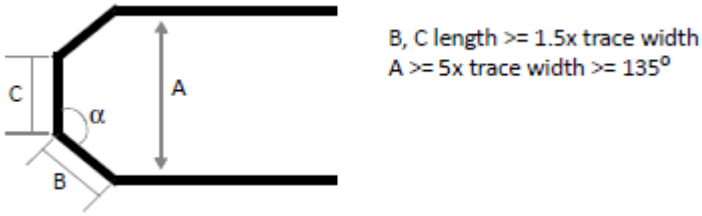
W – The trace width.
S – P/N trace separation. About 1½-2×H for loosely coupled pair.
H – The PCB dielectric height.
C – Clearance to other traces/pair. Must be ≥ 4×H.

The trace width and intra-pair spacing is determined by the impedance target, board stack-up, and other board properties. Wider traces are preferred to reduce copper loss, but should be kept to <10 mils.

Ideally, the trace routing should run in a straight line from source to destination. Avoid sharp bends in the trace routing. Use radius bend segments as illustrated in Figure 26. Curved routes are also acceptable.

NOTE: This type of routing adds skew to the P/N differential pair that must be compensated. See "Skew " on page 44 for additional information.

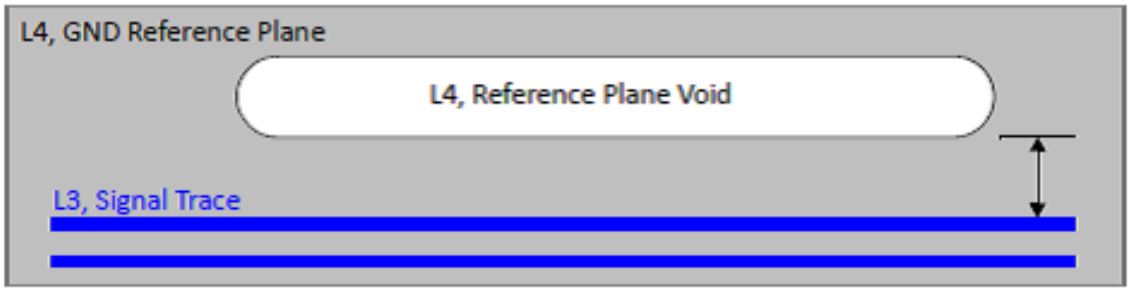
Figure 26: Using Radius Bend Segments



While a guard trace/ground patch is not required between signal pairs, if used, it must be stitched to VSS. The distance between stitching vias should be <40 mils.

All differential signals must be referenced to the VSS plane both above and below signal layer. All VSS islands along the differential pairs must be stitched with a maximum spacing of 40 mils. Splits or voids in the VSS plane area under/above the signal traces are not allowed. The edge of a split/void in the reference plane must be at least 3x signal trace width from the signal trace. Figure 27 illustrates this requirement. Avoid overlapping power and ground islands/planes of different domains.

Figure 27: Routing Near Reference Plane Voids



Finally, if connectors are being used, they must be certified for the line rate (for example, 56.25 Gb/s PAM-4).

5.2.2 Crosstalk

To minimize crosstalk, it is recommended to route the Tx and Rx lanes on separate layers.

The sum of all crosstalk sources from BGA to BGA on a victim receiver line should be kept less than –52 dB at 14 GHz (56 Gb/s PAM-4). Rx NEXT has the most impact on the BER so careful attention should be paid to this parameter.

To reduce crosstalk, large inter-pair spacing is preferred. A minimum of 4x trace width spacing is recommended. To match routing length in serpentine legs, the spacing must be 5x the trace width to minimize coupling.

5.2.3 Skew

5.2.3.1 Differential Pair Skew

Skew between differential pairs lead to mode conversion (differential signal converted to common signal, and vice versa) and can shrink the eye opening. Skew between differential pairs is a result of any asymmetry in the channels as the signals pass through the channel, such as:

- Rounding a bend during routing (outside trace ends up slightly longer than inside trace)
- Remaining back-drill stub length differences (remaining stub is typically between 6–12 mil in length)
- Local dielectric constant variation due to fiberglass weave
- Driver, package, receiver induced asymmetries

Keep differential pair lengths as closely matched as possible to within 50 µm or 2 mils. When there is a mismatch, compensate for it near the location of the mismatch.

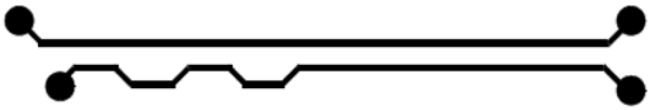
Skew compensation in bends can be done by bending in the opposite direction. However, this requires an even number of bends on the board which may not be possible. For small skews in the BGA breakout area, the trace can be lengthened right at the via as shown in Figure 30.

NOTE: The impedance becomes single-ended in serpentine routing. Use 50Ω single-ended impedance in the serpentine areas and keep them as short as possible (< 1 inch).

Figure 28: Removing Skew at the BGA Breakout Area

Figure 29 uses serpentine routing to remove large amounts of skew.

Figure 29: Using Serpentines to Remove Skew on Differential Pairs

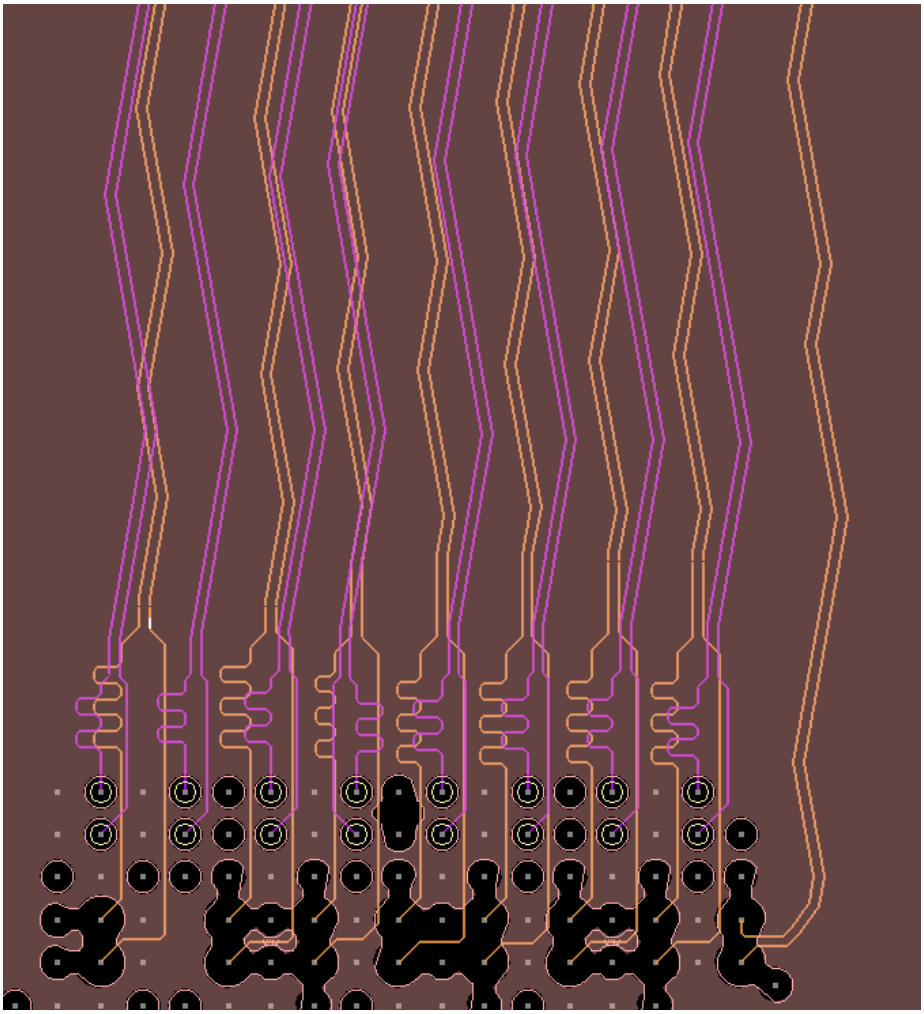


Fiber-weave-induced skew is caused by asymmetry in local dielectric constant seen by one trace versus the other. The quoted dielectric constant of a laminate is the weighted average of the glass fiber content and resin content in the laminate. By nature of the fiberglass cloth, some areas will be resin-rich (lower dielectric constant) and others will be glass-rich (higher dielectric constant). Since dielectric constant affects propagation velocity, if one leg of a P/N pair ends up running primarily over resin-rich areas and the other over glass-rich areas, the result is skew in the received differential signal.

Fortunately, there are a few methods to combat fiber weave induced skew:

- Use spread-weave-glass type dielectric material for both core and prepreg.
- Use a relatively flat-cloth-weave-type dielectric material for both core and prepreg.
  - Use a relatively flat cloth that matches the diff-pair pitch to the glass weave pitch, forcing P/N pairs to see equal variation.
  - Rotate all layers by 10°–15° on a panel. Check with the FAB vendor because this depends on design size versus panel size.
  - Route signals in a zig-zag fashion instead of straight along the X/Y axis. While this consumes more board space, it may be an appropriate trade-off to use a less expensive material. This is illustrated in Figure 30.

Figure 30: BGA Component Breakout Example with Zig-Zag Routing Employed to Mitigate Fiber Weave Skew



NOTE: If a customer uses Spread Weave Glass Dielectric Material, there is no need for zig-zag routing.

5.2.3.2 Lane-to-Lane Skew

Interlaken-LA lane-to-lane skew is highly robust. Per Interlaken–LA specification, a receiver must be capable of handling lane-to-lane skew of 214 UI. The receiver and transmitter are budgeted 174 UI, which leaves PCB routing with 40 UI. Table 18 provides the mismatch of board traces in inches for each data rate supported given a PCB dielectric constant of 3.7 (similar to Megtron 6).

Table 18: Board Mismatch Budget vs. SerDes Data Rate

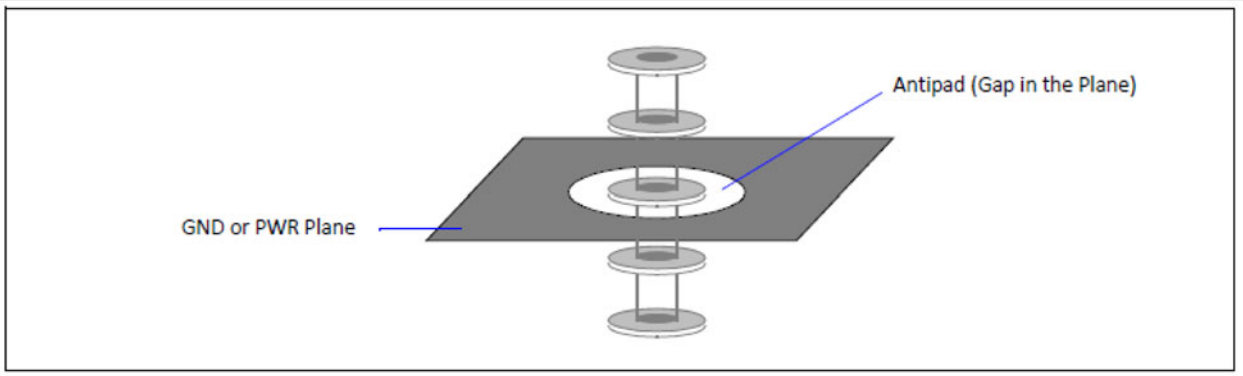
SerDes Data Rate (Gb/s)	Signaling Type	Board Trace Mismatch Budget (inches)
27.34375	NRZ	8.95
28.125	NRZ	8.70
30	PAM-4	16.31
51.5625	PAM-4	9.49
56.25	PAM-4	8.70

5.2.4 Vias and PTH

Via design is extremely critical to the performance of the high-speed SerDes links. All signal via (pad and antipad) dimensions must be optimized for the appropriate Rx and Tx impedance through simulation. A 3D electromagnetic tool such as HFSS should be used for the simulation. The VSS stitching vias must be included in this simulation. Vias for different layer transitions require separate optimization (meaning vias for L1–L4 transition may be different than vias for L1–L18 transition).

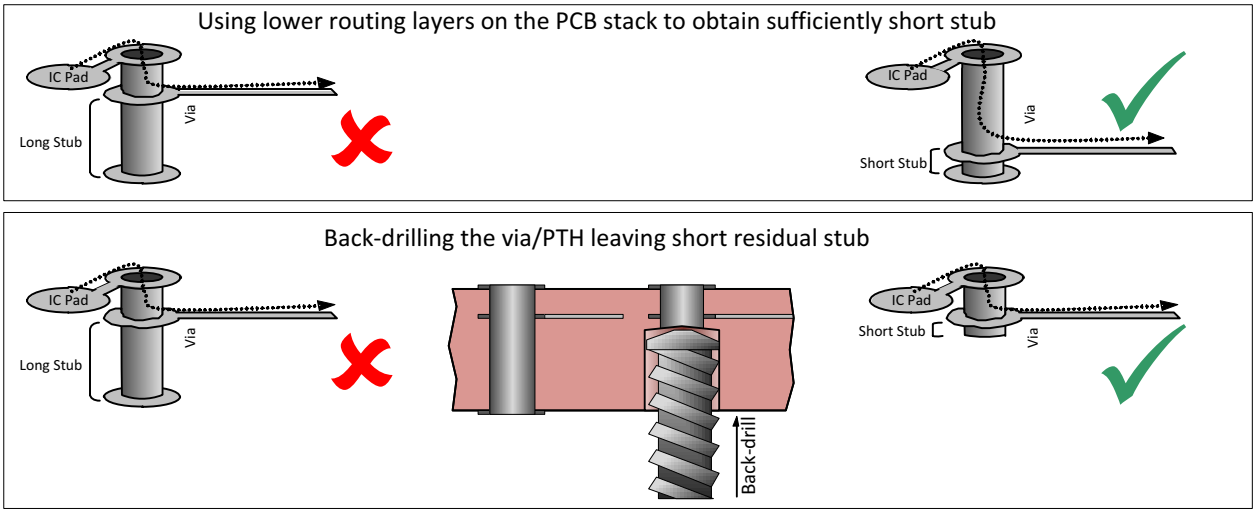
The package BGA pads, connector SMT pads, and AC-coupling capacitors (if applicable) must have a cutout in the VSS reference plane immediately under the component. Cutouts will also exist when transitioning PCB layers. The depth and dimension of the cutout should be determined by simulation to achieve optimal performance. Oblong oval or circular per via antipads are recommended. Table 31 illustrates an antipad during layer transitioning.

Figure 31: Antipad During Layer Transitioning



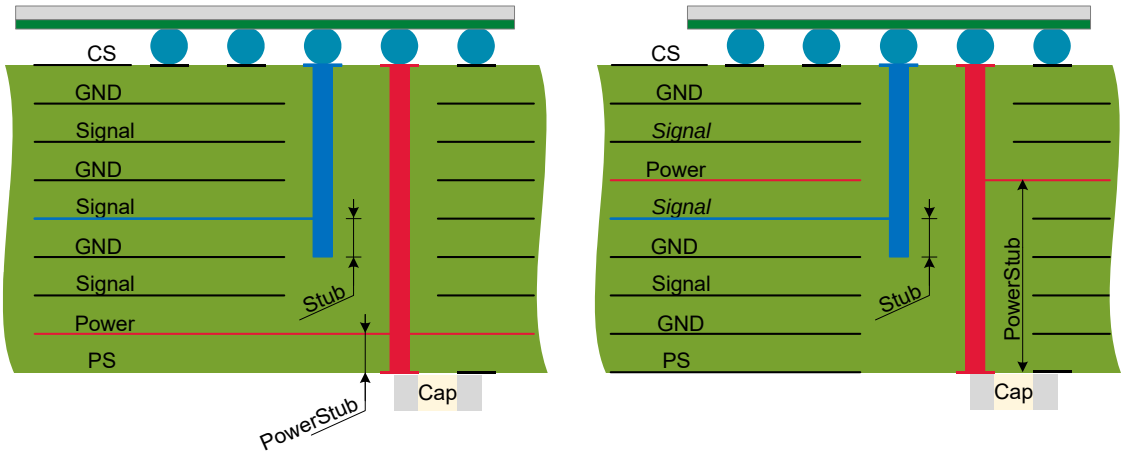
It is recommended to use via-in-pad. Blind or buried vias that have no via stubs are recommended. If via stubs do exist, they must be sufficiently short and must be removed by back-drilling. The remaining via stub must be <6 mils in size. At such data rates, via stubs add extra impedance discontinuities and capacitance. Although sufficiently short via stubs may be obtained by routing on the lower board layers, this is not recommended for the high-speed SerDes signals that should be routed in the upper PCB layers and the resulting stub back-drilled. The bottom layers are to be avoided since the BGA via is hard to optimize because of the tight 1 mm pitch and many surrounding vias which could degrade the signal. Figure 32 illustrates general techniques to reduce via stubs.

Figure 32: Via/PTH Stub Reduction Techniques



Ideally, when back drilling is used to remove stubs for signals, it would also be used on neighboring power and ground vias to eliminate reflections on the return path. This is not possible for vias that connect to a decoupling capacitor on the back side of the PCB. In this case, it is recommended that the SerDes power plane be located on a lower layer closer to the capacitor. In this case, the stub is minimized as shown in Figure 33.

Figure 33: Minimizing Power or Ground Stubs Connecting a Decoupling Capacitor



It is critical to minimize the number of vias (or layer transitions) in the signal path. The differential signal should be routed on one PCB layer. The number of vias within each leg of a differential pair must be the same. In addition, via placement across the differential pair must be symmetric. Stitching vias at layer transitions are recommended as shown in Figure 34. Pads should be removed on unused signal layers as illustrated in Figure 35.

Figure 34: Example of Ground – Shadow Via or Ground Stitching Via

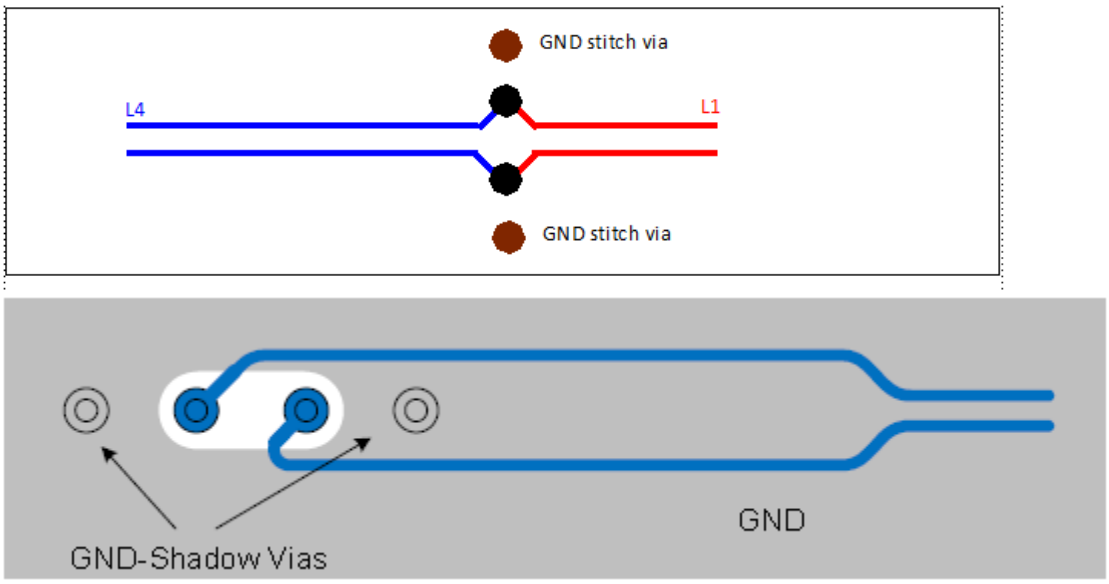


Figure 35: Removing Unused Pads to Improve Via/PTH Characteristics

5.2.5 BGA Breakout Pattern and Component Escape Routing

The Tx differential pairs are located on the perimeter of the BGA, while the Rx differential pairs are located inside the perimeter. Most designs require four signal layers to route the Interlaken-LA differential pairs in order to break out from the BGA via field. To reduce plane gap discontinuities due to back-drill clearance requirements, and having to route traces over them, it is recommended to route signals further from the BGA via field edge on higher layers with the perimeter signals being routed on the lower PCB layers. This assumes that the back-drill via opening is larger than the routing via opening and presents a larger obstacle to routing. Thus, Rx signals are routed on higher PCB layers than the Tx signals. With this methodology, via back-drill clearances do not affect the routing of any of the other signals.

With standard PCB manufacturing tolerances, maintaining differential routing through the BGA via field is not possible. Using single-ended trace segments for component escape is acceptable and this section details the recommended escape strategy and routing techniques in the case where single-ended routing is used within the BGA via field.

There are four important things to check in component escape routing:

- Widen single-ended trace segments to meet 25Ω common-mode or 50Ω single-ended impedance.
- Length match single-ended segments between positive and negative legs of the differential pair as closely as reasonably possible to reduce mode conversion.
- Avoid routing over plane gaps whenever possible.
- Keep single-ended trace segments as short as possible to reduce impedance discontinuities.

The example in Figure 36 illustrates a poorly planned component escape routing strategy, which has inadvertently crossed gaps in the reference plane.

Figure 36: Inadvertent Routing of Traces over a Plane Gap in the BGA Via Field

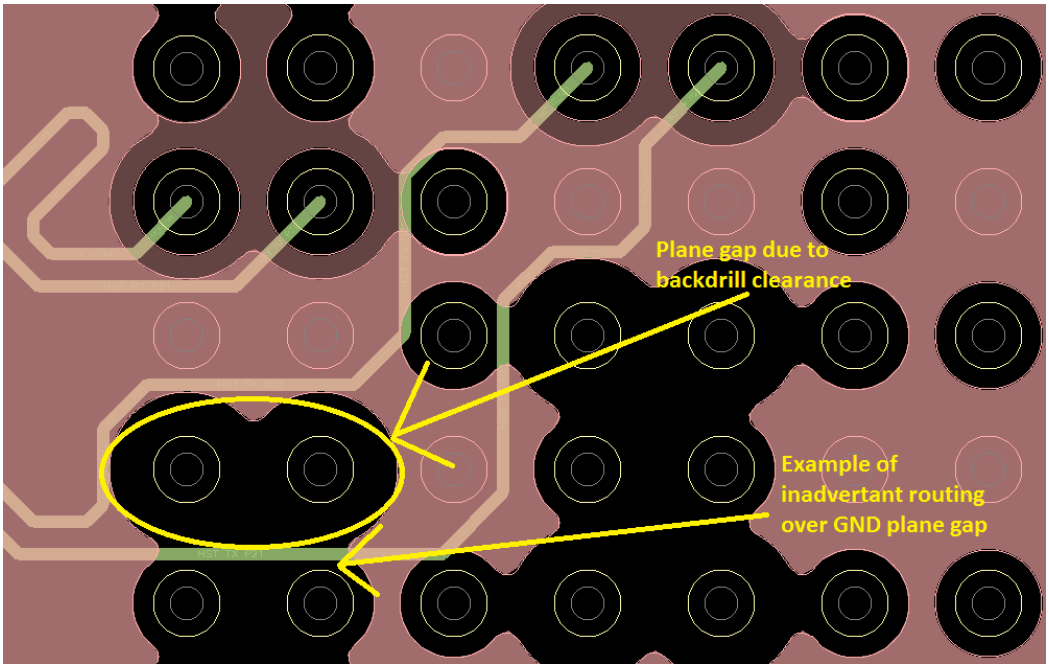


Figure 37 and Figure 38 show examples of recommended single-ended component escape routing. Rx signals are routed on higher layers than Tx signals to avoid back-drilled via gaps. Signal traces do not cross gaps in the reference planes, and single-ended segments are length matched before moving into differential routing.

Figure 37: Example Rx Differential Pair BGA Breakout

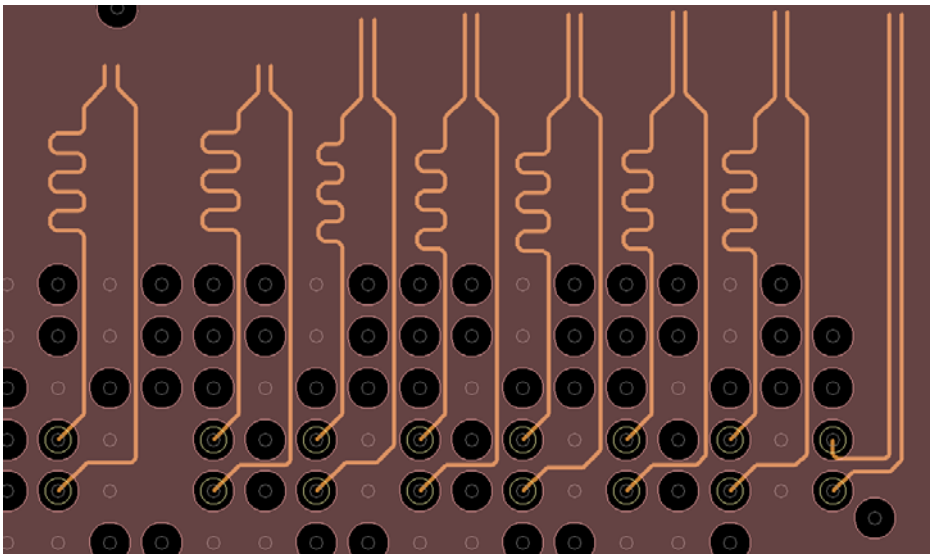
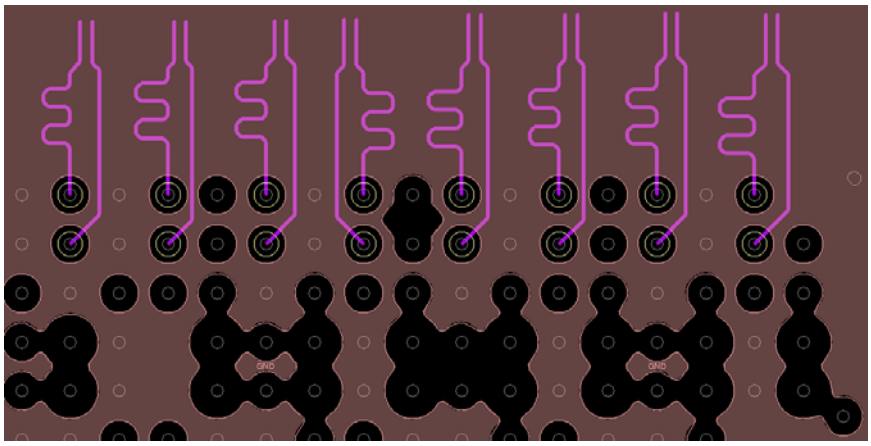


Figure 38: Example Tx Differential Pair BGA Breakout



5.2.6 Channel Length and PCB Material Selection for High-Speed Signal Layers

The maximum possible channel length depends on the PCB material properties. In terms of electrical properties, the important factor is channel return loss. The high-speed links require a channel loss target of > –15 dB. The SerDes can handle higher return losses but requires different settings, which increases the power of the link.

This section gives an example of board material selection based on a conductor width, roughness, and dielectric material to determine a general rule of thumb estimate of maximum channel length. The length is idealized and does not account for other sources of loss in the channel. It is expected that the customer will do due diligence for PCB material selection.

Given the channel lengths dictated by component placement, narrow down the list of potential PCB materials. The channel loss must be broken down into two components: dielectric and conductor attenuation. Dielectric loss is tabulated for several recommended PCB materials in Table 19.

Table 19: Dielectric Properties for Recommended High-Speed PCB Materials

Dielectric Material	Dielectric Constant	Dissipation Factor	Atten [dB/in/GHz]	Atten [dB/in] at 15 Gb/s	Atten [dB/in] at 25.78 Gb/s	Atten [dB/in] at 28.125 Gb/s
Nelco 4000 13SI	3.30	0.0080	0.03343	0.25069	0.43085	0.46996
Rogers 4003B	3.55	0.0027	0.01170	0.08775	0.15082	0.16451
Megtron 6 (R5775K Resin Based)	3.65	0.0020	0.00879	0.06591	0.11328	0.12356
Rogers 3003 (PTFE Based)	3.00	0.0013	0.00518	0.03884	0.06676	0.07281
Rogers 4350B	3.66	0.0037	0.01628	0.12210	0.20986	0.22891
Nelco 400013	3.70	0.0095	0.04203	0.31522	0.54176	0.59093
Taconic TSM-DS FastRise-27	2.70	0.0014	0.00529	0.03968	0.06820	0.07439

While often neglected, at high data rates, a significant component of total attenuation is copper loss. Due to skin effect, the surface roughness of the copper foil has a significant impact on overall signal attenuation. Surface roughness is averaged as an RMS value. Some common laminate surface roughness values are given in Table 20.

Table 20: Surface Roughness of Common Available Laminates

Profile	Surface Roughness
Standard	8 µm
Very Low Profile (VLP)	4 µm
Super/Hyper Very Low Profile (S/H-VLP)	2 µm

The factors affecting conductor loss are trace width, length, material conductivity, frequency (due to skin effect), and surface roughness. To reduce the skin effect, it is recommended to use a wider trace such as 7 to 8 mils. Other trace lengths are possible but for the purpose of the example below, an 8-mil trace is assumed.

NOTE: The standard roughness imposes a large loss on the conductor. It is recommended to use a very low or super/hyper very low profile laminate.

Copper loss and dielectric loss can be combined into an estimate of total attenuation per inch at the Nyquist frequency. Table 21 shows the attenuation per inch for various data rates, surface roughness and recommended dielectric materials. Using better dielectrics, wider traces and smooth copper can all reduce the attenuation of the signaling. It is advisable to compare each component's contribution to the attenuation and use resources appropriately to get the smallest attenuation for the cost. It is often much cheaper to use wider traces with smooth copper to reduce the total loss, than it is to use very low loss dielectrics.

Table 21: Total Attenuation per Inch on an 8 mil Trace for Various Materials, Roughness and Data Rates

	Attenuation/inch at 7.5 GHz		Attenuation/inch at 12.89 GHz		Attenuation/inch at 14.0625 GHz	
Copper Roughness						
Dielectric	**2 µm**	**4 µm**	**2 µm**	**4 µm**	**2 µm**	**4 µm**
Nelco 4000 13SI	0.59302	0.81302	0.87964	1.20464	0.93867	1.28067
Rogers 4003B	0.43008	0.65008	0.59960	0.92460	0.63322	0.97522
Megtron 6 (R5775K Resin Based)	0.40824	0.62824	0.56206	0.88706	0.59227	.93427
Rogers 3003 (PTFE Based)	0.38117	0.60117	0.51554	0.84054	0.54152	0.88352
Rogers 4350B	0.46443	0.68443	0.65864	0.98364	0.69761	1.03961
Nelco 400013	0.65755	0.87755	0.99054	1.31554	1.05964	1.40164
Taconic TSM-DS FastRise-27	0.38201	0.60201	0.51698	0.84198	0.54310	0.88510

Given total attenuation per inch, a maximum channel length can be found for each dielectric/copper combination to achieve a limit of –15 dB of total loss. Table 22 illustrates this for various data rates, surface roughness and dielectric materials. Again this is a general rule of thumb. The customer is expected to do a detailed analysis to determine precise channel loss.

Table 22: Maximum Ideal Channel Length Limits for 8 mil Traces for Various Materials, Roughness and Data Rates

	Max Channel Length with 15 dB Limit at 7.5 GHz		Max Channel Length with 15 dB Limit at 12.89 GHz		Max Channel Length with 15 dB Limit at 14.0625 GHz	
Copper Roughness						
Dielectric	**2 µm**	**4 µm**	**2 µm**	**4 µm**	**2 µm**	**4 µm**
Nelco 4000 13SI	25.3	18.4	17.1	12.5	16.0	11.7
Rogers 4003B	34.9	23.1	25.0	16.2	23.7	15.4
Megtron 6 (R5775K Resin Based)	36.7	23.9	26.7	16.9	25.3	16.1
Rogers 3003 (PTFE Based)	39.4	25.0	29.1	17.8	27.7	17.0
Rogers 4350B	32.3	21.9	22.8	15.2	21.5	14.4
Nelco 400013	22.8	17.1	15.1	11.4	14.2	10.7
Taconic TSM-DS FastRise-27	39.3	24.9	29.0	17.8	27.6	16.9

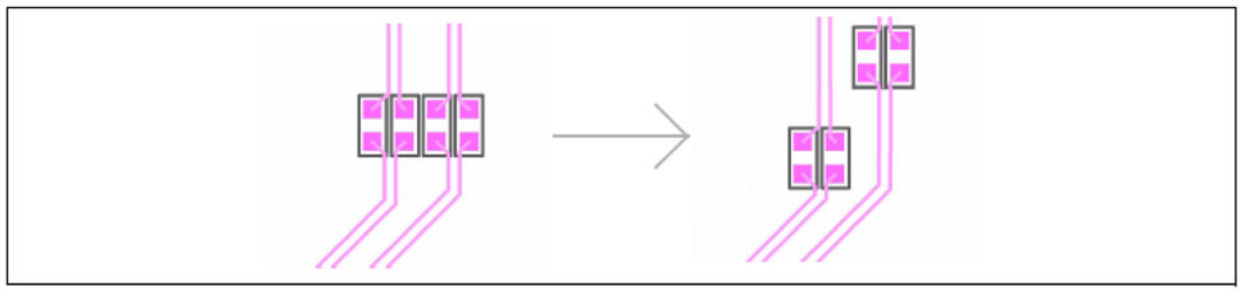
Even though micro-strip routing will be minimal to non-existent, care should be taken to the preferred PCB trace finish and plating process. Avoid using any finish or plating process that involves ferromagnetic materials such as nickel which is standard for a gold plating process. Skin-effect related losses are proportional to the square root of relative permeability of the material. For nickel, the relative permeability is 100 versus 1 for copper so a nickel-gold plating process could exhibit ten times the loss as a plain copper trace.

5.3 AC-Coupling Capacitors

The device has AC-coupling capacitors built into the device receivers to reduce external component count and improve PCB routing. However, external AC-coupling capacitors may be required on the transmit to host device receive channels. This is dependent on the host device receiver architecture.

When placing series AC-coupling capacitors on the PCB, sufficient lane-to-lane spacing should be maintained. Their placement in relation to those for an adjacent lane should not be so close as to enable coupling between lanes. The exact spacing can be determined through simulation. It is recommended to stagger the AC-coupling capacitor placement as shown in Figure 39.

Figure 39: Series AC-Coupling Capacitor Staggered Placement



Due to the increased conductor width to connect to the AC-coupling capacitor, the impedance of this part of the trace is significantly lower.

There are two methods to increase the impedance:

- Minimize the pad size of the component.
- Remove ground layers below pads until channel impedance is matched.
  - Ensure the reference plane remains the same (ground-referenced).

5.4 Unused Lanes

Unused SerDes lanes should be left open and unconnected. Unused octets should be connected to an active supply and be powered down via software. The filtering and decoupling requirements for the unused quad supplies are relaxed so as to not require extra board components.

5.5 Simulation

IBIS/AMI models are provided for simulation and validation of the system performance. The full channel should be simulated especially for data rates above 10 Gb/s or for long channels with a great deal of loss. The simulation will validate the eye at the receiver and whether the BER is acceptable.

In addition to the IBIS/AMI model, an S4P model of the package receiver and transmitter are provided as well as an S4P model of an example channel.

The recommended simulation tools are Agilent ADS and SiSoft QCD. CSP LinkEye is not available for this SerDes core.

More detail can be found in the IBIS/AMI model package.

5.6 Receiver Eye Mask

TBD

Chapter 6: PCIe 2 Interface

6.1 Overview

The device has one PCIe 2.0 lane consisting of one transmit and receive lane that runs at 5 Gb/s data rate. Since the data rate is much lower than the Interlaken-LA interface, many stringent guidelines for the PCB may be relaxed. Also, the board material and processing is optimized for higher speeds, giving the relatively slow PCIe lane additional margin.

6.2 High-Speed Routing Guidelines

This section provides guidance on successfully implementing a PCB channel with sufficient bandwidth to support a 5 Gb/s PCIe 2 lane.

6.2.1 General Routing

- Use a 100Ω differential trace impedance for the Rx and Tx signals. The tolerance on this impedance is ±5%. For the breakout region under the BGA, use 25Ω for common mode signaling.
- The PCIe lane can be routed either as a strip-line or as a micro-strip.
- Wider traces are preferred to reduce copper loss, but should be kept to <10 mils. Use a loosely coupled differential pair and avoid sharp bends in the trace routing.
- While a guard trace/ground patch is not required between the signal pair, if used it must be stitched to VSS. The distance between stitching vias should be <40 mils.
- All differential signals must be referenced to the VSS plane. All VSS islands along the differential pairs must be stitched with a maximum spacing of 40 mils. Splits or voids in the VSS plane area under/above the signal traces are not allowed. The edge of a split/void in the reference plane must be at least 3x signal trace width from the signal trace. Avoid overlapping power and ground islands/planes of different domains.

6.2.2 Crosstalk

- To minimize crosstalk, it is recommended to route the Tx and Rx lanes on separate layers.
- To reduce crosstalk, large inter-pair spacing is preferred. A minimum of 4x trace width spacing is recommended. In serpentine legs to match routing length the spacing must be 5x the trace width to minimize coupling.

6.2.3 Differential Pair Skew

Keep differential pair lengths as closely matched as possible to within 500 µm or 20 mils. When there is a mismatch, compensate for it near the location of the mismatch.

6.2.4 Vias and PTH

- All signal via (pad and antipad) dimensions must be optimized for the appropriate Rx and Tx impedance through simulation. Vias for different layer transitions require separate optimization (for example, vias for the L1 to L4 transition may be different than vias for the L1 to L18 transition).
- The package BGA pads, connector SMT pads, and AC-coupling capacitors must have a cutout in the VSS reference plane immediately under the component. Cutouts will also exist when transitioning PCB layers. The depth and dimension of the cutout should be determined by simulation to achieve optimal performance.
- Use via-in-pad. Blind or buried vias, which have no via stubs, are recommended. If via stubs do exist, they must be sufficiently short by using lower routing layers on the PCB stack or they must be removed by back-drilling. The remaining via stub must be <10 mils in size.
- It is critical to minimize the number of vias (or layer transitions) in the signal path. The differential signal should be routed on one PCB layer. The number of vias within each leg of a differential pair must be the same. In addition, via placement across the differential pair must be symmetric. Stitching vias at layer transitions are recommended. Pads should be removed on unused layers.

6.2.5 BGA Breakout Pattern and Component Escape Routing

Using single-ended trace segments for component escape is acceptable. There are four important things to check for component escape routing:

- Single-ended trace segments should be widened to meet 50Ω impedance.
- Length-match single-ended segments between positive and negative legs of the differential pair as closely as reasonably possible.
- Avoid routing over plane gaps whenever possible.
- Keep single-ended trace segments as short as possible to reduce impedance discontinuities.

6.3 AC-Coupling Capacitors

For the PCIe Rx pins, external AC-coupling capacitors are required. The recommended value is 100 nF. For the chip receiving device PCIe Tx signals, it is required to have AC coupling (either built-in or on the board).

See PCIe Reference Clock for AC-coupling requirements for the reference clock.

Chapter 7: Misc. Layout Guidance

7.1 RESCAL Resistor Placement

The RESCAL[1:0] pins each need a 4.53 kΩ resistor with ≤1% accuracy connected to VSS. Analog circuits connected to the RESCAL[1:0] pins are sensitive to trace routing parasitics. Parasitic resistance is required to be small relative to the 1% variation of the resistors. It is recommended to use 0402 resistors and place them in the via array on the bottom side of the device. Adjacent to each RESCAL BGA is a corresponding VSS BGA making for easy placement of each resistor.

7.2 Open Drain Signals

The following signals are open drain and require an external pull-up resistor to drive to a logic 1 value:

- MDIO
- MDC
- SCL
- SDA
- GIO_L

Each of these signals requires a 1 kΩ resistor connected to the VDD18 supply. The maximum voltage allowed on any low speed I/O is 1.98V. Voltages above this such as 2.5V or 3.3V will damage the device.

The drive strength of the I/O driving these signals is nominally 50Ω and varies from 45Ω to 55Ω.

7.3 DNC Signals

Some pins in the BGA pin list are designated DNC, which means “Do Not Connect” and these pins should remain floating.

7.4 Weak Drive Signals

Several pins have a weak internal drive on the pin. As an input, it is meant to provide a default logic level when not driven.

The following pins are weakly driven to a logic 1 (1.8V) value:

- TDI
- TMS
- TRST_L.

The following pins are weakly driven to a logic 0 value: MSEL[1:0]. The drive strength is rather weak at > 20 kΩ (over all conditions) so it is recommended that these pins always be driven.

7.5 Static Configuration Signals

Several pins may only be used as a static configuration. In this case, do not drive the signal directly with the power supply, but connect through a 1 kΩ resistor to VDD18 or VSS. These signals include MPID[4:0] and MSEL[1:0].

7.6 I^2C Interface

TBD

7.7 TDO

TDO is an output-only driver pin. It is not recommended to attach any pull-up or pull-down resistors on this signal.

Revision History

16000-DG105; January 18, 2019

Updated:

- System Design
- Table 2, Expected VAVS with Different VADC and VREF Combinations
- Regulator Testing Procedure

16000-DG104; August 14, 2018

Updated:

- Table 8, VDDS[1–6] Analog Supply and Filtering Specification
- Figure 14, Circuit Components
- Table 9, VDDS08PLL[1–6] Analog Supply and Filtering Specification
- Figure 16, Circuit Components
- Overview
- Table 14, SREFCLK Requirements
- Table 16, CREFCLK Requirements
- AC-Coupling Capacitors

16000-DG103; May 31, 2018

Updated:

- Power-On and Power-Off Requirements

Added:

- Initialization Requirements
- PCIe Reference Clock

16000-DG102; March 12, 2018

Updated:

- Table 1, Power Supply Inputs
- System Design
- VDD Core Power Delivery Network and Decoupling Scheme
- Figure 18, Consecutive Approach Power Sequence and Reset Timing

16000-DG101; August 31, 2017

Updated:

- System Design
- Alternate Regulator Configuration
- Regulator Testing Procedure

16000-DG100; July 24, 2017

Initial release.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