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BCM8752 PRODUCT Brief

DUAL-CHANNEL 10 GbE SFI-TO-XFI PHY WITH EDC

FEATURES

- Dual-channel SFI-to-XFI Physical Layer (PHY) developed in low-power 65 nm CMOS process technology
- Supports SFP+ SR, LR, and LRM optical interfaces
- Supports SFP+ copper twin-ax cable
- Programmable amplitude control on 10G serial transmitter interface
- MDIO interface-compliant with IEEE 802.3ae Clause 45 with extended indirect address register access
- Support for XFP/XFI interfaces
- SFI and XFI interface: Serial 10.3125 Gbps CML
- PCS 64B/66B scrambler/descrambler
- SFI receive equalization
- Integrated microcontroller and AGC with a wide dynamic range
- Loopback modes supporting IEEE standard modes
- Built-In Self-Test (BIST) on SFI and XFI serial interfaces
- Low-power dissipation: 1W/10 GbE port
- Core supply—1.0V, I/O—3.3V
- 12 mm x 12 mm BGA package, 1-mm ball pitch

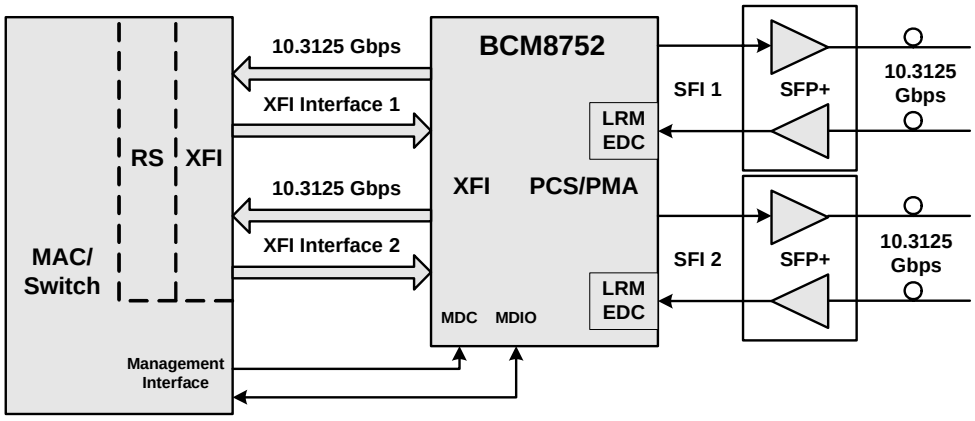
SUMMARY OF BENEFITS

- Single-reference clock input, enables use of a low-cost 156.25 MHz oscillator
- 1 GbE mode, with support for IEEE 802.3™ Clause 37 AN
- Transmit preemphasis for flexible placement of PHY
- Link Alarm Status Interrupt (LASI) output for both channels
- Advanced diagnostics on SFP+ interface, including eye-mapping, SNR, and BER
- Standard two-wire serial interface (BSC) support for external E2, XFP, SFP, SFP+

APPLICATIONS

- High-density 10 GbE SFP+ line cards
- SFP+ optical SR, LR, and LRM modules
- SFP+ copper twin-ax

BCM8752 Functional Block Diagram



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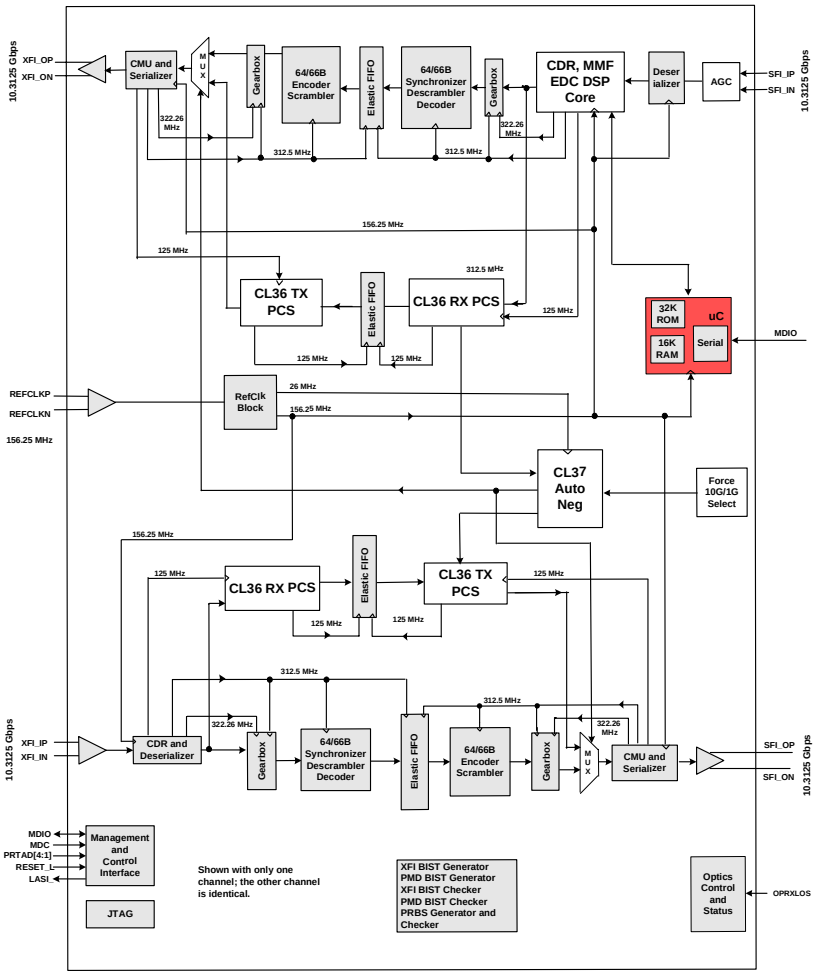
OVERVIEW



BCM8752 Block Diagram

The BCM8752 is a dual-channel 10 GbE SFI-to-XFI (10-Gigabit serial electrical interface) PHY that incorporates an Electronic Dispersion Compensation (EDC) equalizer supporting SFP+ line-card applications.

The BCM8752 is a multirate PHY targeted for optical fiber and copper twin-ax applications. It interfaces with both limiting- and linear-based SFP+ and SFP modules, and SFP+ copper twin-ax cable. The BCM8752 is fully compliant with the 10 GbE SFP+ standard and also supports 1000BASE-X for 1 GbE operation.

The BCM8752 is developed using an all-DSP high-speed front end, providing the highest performance and most flexibility for line-card designers. An on-chip microcontroller implements the control algorithm for the DSP core.

On-chip clock synthesis is performed by the high-frequency, low-jitter, Phase-Locked Loops (PLLs). Individual clock recovery is performed on the device by synchronizing directly to the respective incoming data streams. A single 156.25 MHz reference clock input is required for the device.

The BCM8752 Ethernet PHY is a fully integrated 10-Gigabit serial Ethernet retimer interface. The SFI, XFI, PCS, and PMA functions include 64B/66B coding, Clock Multiplication Unit (CMU), and Clock and Data Recovery (CDR).

The BCM8752 is available in a 12 mm x 12 mm, 1 mm pitch, 121-pin BGA, RoHS-compliant package.

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