



## MULTIRATE 10-GBPS SONET/SDH/10GbE/FC/FEC MUX

### FEATURES

- 10-Gigabit MSA (Multi-Source Agreement) compliant
- NRZ, RZ, and encoder selection
- Serial data output crosspoint adjustment
- Fully integrated Clock Multiplication Unit (CMU) supports multiple data rates: OC-192, 10GbE, 10GFC, and their FEC data rates.
- 16:1 multiplexer with LVDS data input
- Configurable divide by 16 or 32 clock modes
- Configurable LVDS input clock-to-data bus timing skew control
- On-chip 16 x 10 FIFO eliminates system timing issues.
- Serial data polarity inversion selection
- Bit order reversal selection
- Low-jitter 10-gigabit output clock for retiming clocked laser drivers
- Lock detect
- Core power supply: 1.2V
- I/O power supply: CML at 1.2V, LVDS and CMOS at 1.2V or 3.3V
- Power consumption: 450 mW
- Standard CMOS fabrication process
- 127-pin BGA package available in standard and Pb-free version

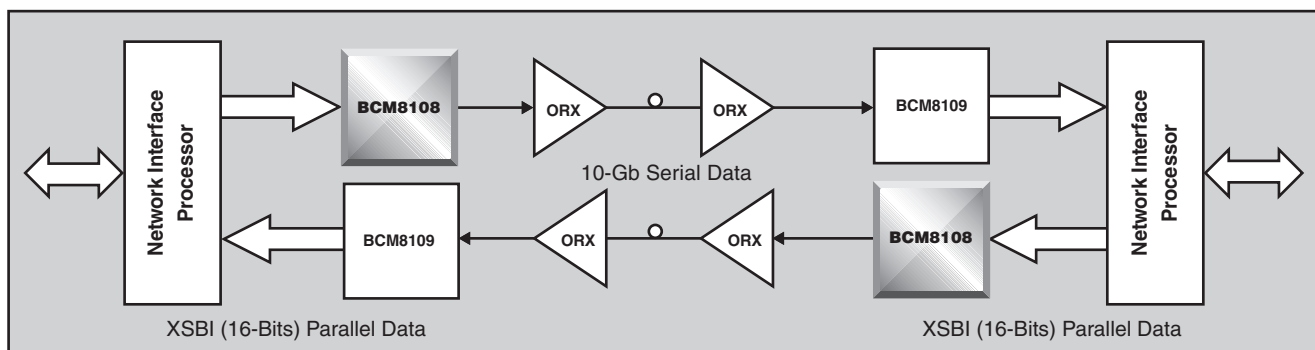
### SUMMARY OF BENEFITS

- Compliant with Optical Internetworking Forum (OIF), Telcordia®, ITU-T, ANSI, and IEEE 802.3ae industry standards.
- Reduces design cycle and time-to-market.
- High level of integration allows for higher port density solutions.
- Uses the most effective silicon economy of scale for CMOS-based devices.
- Low-power consumption eliminates the need for external cooling sources.

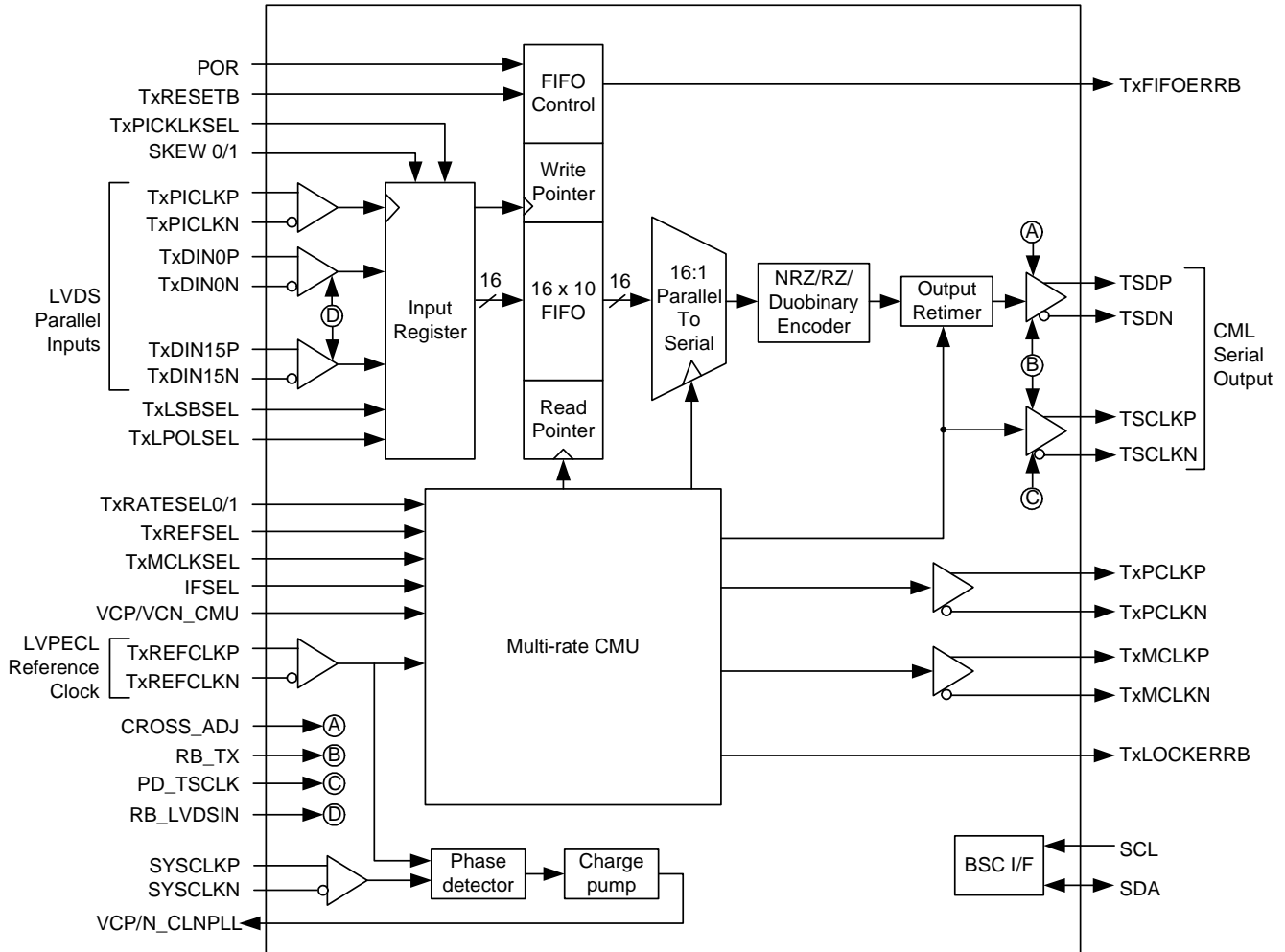
### APPLICATIONS

- OC-192/STM-64/10GE transmission equipment
- SONET/SDH optical modules
- NRZ, RZ, or duobinary
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbones
- SONET test equipment
- Terabit routers
- Edge routers

### BCM8108 Functional Block Diagram



# OVERVIEW



The BCM8108 is a fully integrated MSA-compliant multirate SONET/SDH/10GE/FC/FEC transmitter operating at OC-192 (9.953 Gbps), 10GE (10.3125 Gbps), 10GFC (10.513 Gbps), and Forward Error Correction (FEC) data rates (10.664/10.709, 11.096, or 11.31 Gbps). The BCM8108 provides selectable NRZ, RZ, or duobinary encoders, a serializer, and a Clock Multiplication Unit (CMU). The low-jitter LVDS interface and onboard low-jitter PLL exceed Optical Internetworking Forum (OIF), IEEE 802.3ae, Telcordia, ANSI, and ITU-T jitter standards.

The BCM8108 reference clock input frequency is user-selectable to the line rate divided by either 16 or 64. The two reference clock outputs can be squelched under user control.

The BCM8108 provides skew control between the LVDS transmit parallel input clock and data to accommodate difficult timing variances. A 10-word FIFO decouples the parallel input timing domain from the serial output timing domain.

The BCM8108 provides a CML serial output clock to retime the data at the optical interface. The CML serial output data crosspoint may be adjusted to precompensate for eye asymmetry.

The BCM8108 can be powered with a single 1.2V supply or dual 1.2/3.3V supply without any special power supply sequencing requirements.

The BCM8108 is a register-based device; settings can be controlled via the Broadcom Serial Control (BSC) interface.

The BCM8108 comes in a 11 mm x 11 mm, 127-pin BGA package.

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