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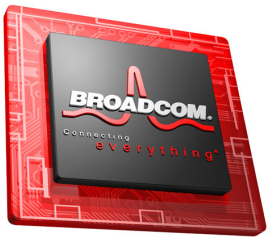
BCM8071
PRODUCT Brief



SERIAL 10G BASE-KR TO XAUI™ BACKPLANE TRANSCEIVER

FEATURES

- **Targeted to meet the draft IEEE 802.3ap standard**
- **High performance DFE/FFE receive equalizer with full adaptation on-chip**
- **High performance equalization supports new and legacy backplane channels.**
- **Auto-negotiates to 1.25/10G**
- **Multiple interface support**
  - PMD
    - Serial 10.3125-Gbps CML
  - Programmable amplitude control on 10G serial transmitter
  - 4-lane XAUI™ (3.125 Gbps)
- **Transmit pre-emphasis and receive equalization on the XAUI interface**
- **Power dissipation: < 2W**
- **Core supply: 1.0V; I/O: 3.3V**
- **Loss-of-signal detection**
- **Link activity indicator outputs**
- **Integrated packet generator and checker**
- **13 mm x 13 mm, FBGA, RoHS compliant package**

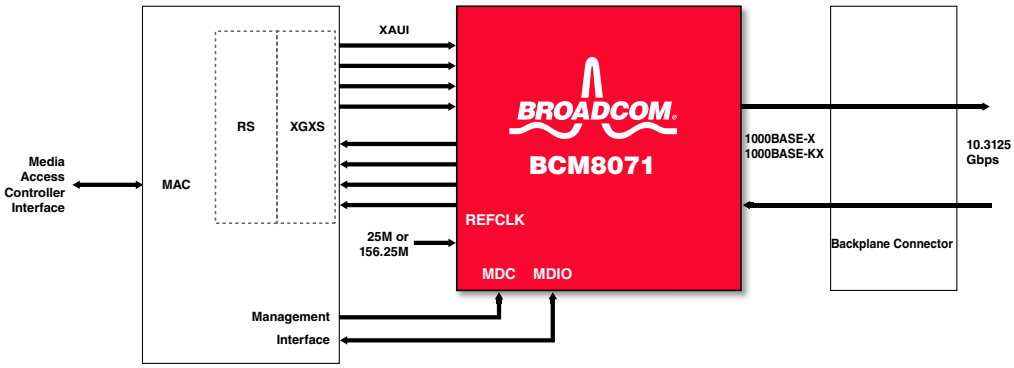
SUMMARY OF BENEFITS

- **New 10 GbE serial transceiver supporting high-bandwidth backplane requirements**
- **MDIO interface compliant to IEEE 802.3ae clause 45 with extended indirect address register access**
- **Single reference clock input enables use of a 156.25-MHz oscillator or low-cost 25-MHz crystal.**
- **Integrated microcontroller with no external memory required**
- **Simplifies manufacturability with integrated built-in self test (BIST) and loopback modes on the 10G serial and XAUI interfaces.**
- **XAUI link synchronization/deskew**
- **XGXS 8B/10B error detection ENDEC**
- **PCS 64B/66B scrambler/descrambler**

APPLICATIONS

- **Backplane links**
- **Copper-cable stackable links**
- **On-board and board-board links**

BCM8071 Functional Block Diagram



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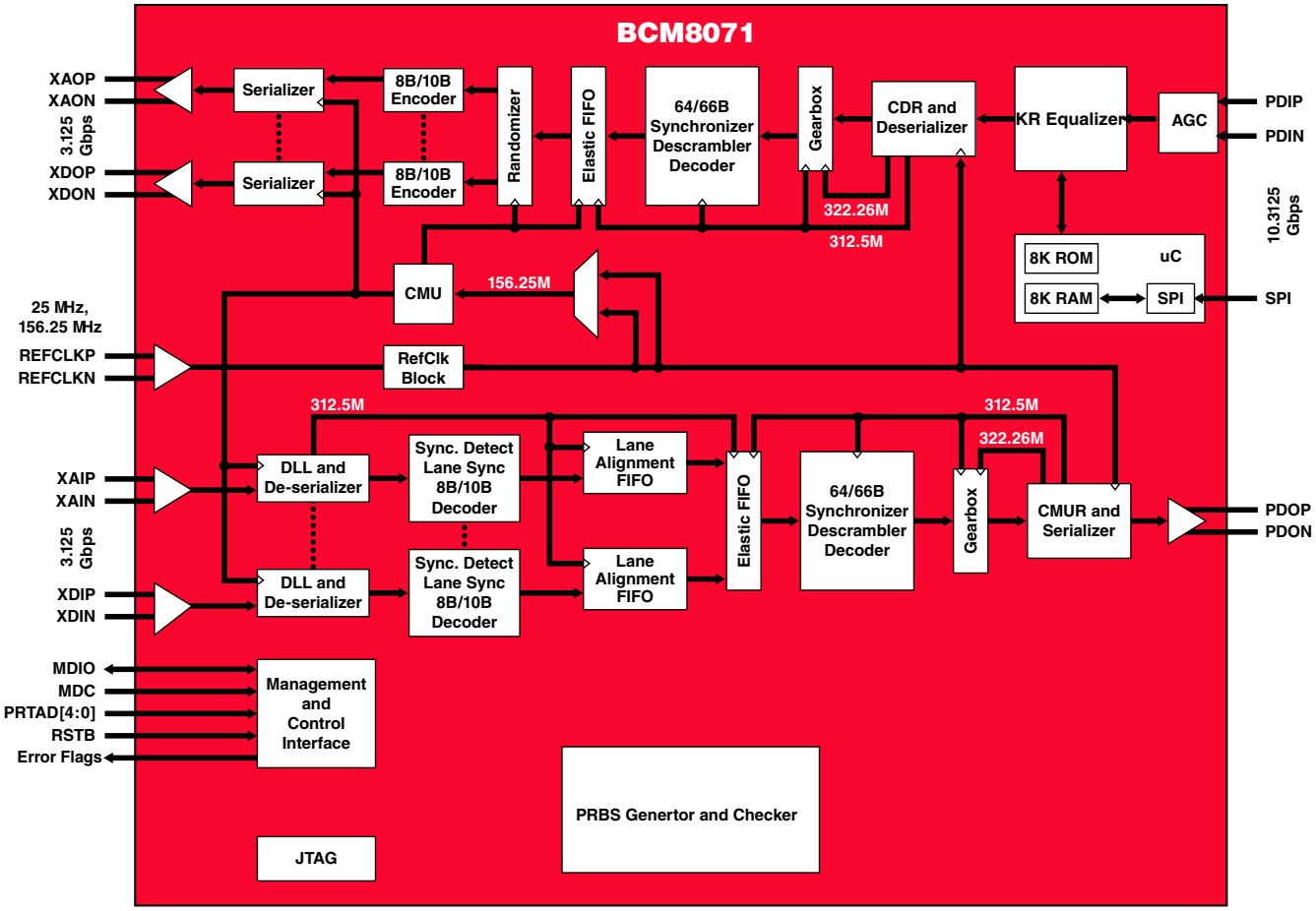
OVERVIEW



BCM8071 Block Diagram

The BCM8071 is a 10-GbE Serial Transceiver targeting the new IEEE 10G BASE-KR standard for running 10G serial data over backplane systems. The device incorporates a sophisticated receive equalizer that extends the life of legacy systems today running 1G or XAUI data rates by providing a 4x or 10x bandwidth improvement on each channel.

An on-chip microcontroller provides users with flexibility and ease of use by automatically adjusting the equalizer parameters based on the performance of each backplane channel.

On-chip clock synthesis is performed by the high-frequency low-jitter phase-locked loops for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing directly to the respective incoming data streams. An external 25-MHz or 156.25-MHz oscillator is required for the reference clock input.

The BCM8071 Ethernet 10G BASE-KR PHY is a fully integrated SerDes (10.3125 Gbps) interface device performing the extension functions for a 10-GbE Reconciliation Sublayer (RS) interface. The XGXS, PCS, and PMA functions include 8B/10B coding, 64B/66B coding, SerDes, Clock Multiplication Unit (CMU), and Clock and Data Recovery (CDR).

The BCM8071 is available in a 13 mm × 13 mm, FBGA, RoHS compliant package.

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