PLX PCIe Switch Power Consumption

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In a typical electronic design it is hard to predict the power consumption of each individual component in a system under various conditions. Hence, designers tend to be conservative and develop their power rails/supplies for worst-case scenarios. This includes designing systems to worst-case power consumption and dissipation of the heat caused by that power consumption.

The power consumption of silicon with high-speed SerDes depends on the following factors:

- Number of gates and geometries
- Operating temperature
- Process Variation
- Core and line (SerDes) frequency/clock
- Core and SerDes voltages
- Traffic type

PLX Technology has been designing PCI Express (PCIe) components for over five years and has already released its third-generation PCIe switch architecture. The designers at PLX have considered the factors listed above to minimize the power consumption of its switches. The RTL has been optimized to reduce the gate count in 0.13 micron silicon technology. PLX devices run on standard PCI Express specified clock rates. The core and SerDes run at 1V with five percent variation for limiting power consumption. The SerDes can be programmed for drive power to suit the application, hence, reducing the power consumption even further. In addition, unused SerDes can be turned off for additional power savings. PLX designs and tests its switches for industrial temperature, but users can achieve additional power savings at commercial temperature. PLX switches are designed to consume less power in host-centric traffic when compared to peer-to-peer designs, thereby offering additional benefits for most applications as they are based on a host-centric usage model.

The following tables show power consumption in host centric usage at commercial temperature:

ExpressLane™ Gen 2 & Gen 1 PCI Express SWITCHES

PCI-SIG Base Spec.	Part Number	Lanes	Ports	Latency (ns)	Dual Cast	Read Pacing	DBA*	NT*	HPC*	Power Typ. (W)	Package Size (mm^2)
Gen 2	PEX 8648	48	12	140	Yes	Yes	Yes	Yes	3	4.0	27 x 27
Gen 2	PEX 8632	32	12	145	Yes	Yes	Yes	Yes	3	2.8	27 x 27
Gen 2	PEX 8624	24	6	145	Yes	Yes	Yes	Yes	3	3.0	19 x 19
Gen 2	PEX 8616	16	4	150	Yes	Yes	Yes	Yes	2	2.2	19 x 19
Gen 2	PEX 8612	12	3	150	Yes	Yes	Yes	Yes	2	2.0	19 x 19
Gen 1	PEX 8548	48	9	110	—	—	Yes	—	3	4.9	37.5 x 37.5
Gen 1	PEX 8547	48	3	110	—	—	Yes	—	0	4.9	37.5 x 37.5
Gen 1	PEX 8533	32	6	115	—	—	Yes	—	3	3.3	35 x 35
Gen 1	PEX 8532	32	8	275	—	—	—	Yes	8	5.7	35 x 35
Gen 1	PEX 8525	24	5	115	—	—	Yes	—	3	2.6	31 x 31
Gen 1	PEX 8524	24	6	275	—	—	—	Yes	6	3.9	31 x 31
Gen 1	PEX 8518	16	5	150	—	—	—	Yes	5	2.6	23 x 23
Gen 1	PEX 8517	16	5	150	—	—	—	Yes	4	2.6	27 x 27
Gen 1	PEX 8516	16	4	275	—	—	—	Yes	4	2.6	27 x 27
Gen 1	PEX 8512	12	5	150	—	—	—	Yes	5	2.2	23 x 23
Gen 1	PEX 8509	8	8	118	—	—	Yes	—	3	1.2	15 x 15
Gen 1	PEX 8508	8	5	150	—	—	—	Yes	5	1.6	19 x 19
Gen 1	PEX 8505	5	5	138	—	—	Yes	—	3	0.8	15 x 15

The PLX PCIe Switch family includes the widest selection, highest performance, lowest latency, lowest power, most feature rich, and highly flexible/configurable devices in the industry. *DBA = Dynamic Buffer Allocation; NT = Non-Transparency; HPC = Hot-Plug Controllers