System Engineering Note
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SCSI Bus Mode Detection and Change as a Function of DIFFSENS
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This system engineering note discusses considerations of SCSI bus mode change mechanics as associated with the DIFFSENS signal in different environments: single ended, high-voltage differential (HVD) SCSI, and low-voltage differential (LVD) SCSI. This relates to the specifications outlined in version 20B of the SPI-2 (SCSI Parallel Interconnect 2) document.

This document dictates that devices shall not allow signal drivers to leave a high impedance state during initial power up until both of the following conditions are satisfied:

1. The device is capable of logical operation for at least 100 ms. This 100 ms delay allows time for the DIFFSENS pin to connect after the initial power connection in the case of insertion of a device into an active system, and

2. The DIFFSENS mode detected has remained stable for an additional 100 ms after the first 100 ms period.

Also, a device shall not change its present signal driver or receiver mode based on the DIFFSENS voltage level unless a new mode is sensed continuously for at least 100 ms.

The termination on the bus determines the bus mode, which in turn determines the voltage level of the DIFFSENS signal. Additionally, placement of drives on the bus influences the level of DIFFSENS.

These levels are:

SE	-0.35 to + 0.5V
HVD	2.4 to 5.5V
LVD	0.7 to 1.9V

The DIFFSENS signal is an input to the SCSI controller. In a multi-mode bus environment, the level of DIFFSENS and the bus mode will change. Following are examples of bus mode changes and sequence on a SCSI bus.

LVD Bus Switching to Single-Ended

At power up, the bus will come up at the default for the termination, unless a drive is on the bus. For example, a SCSI bus with a SYM53C896 device and an LVD multi-mode terminator will come up in LVD mode. DIFFSENS will be set to approximately 1.3V, and the data and control signals will be at 1.4V and 1.0V when driven. These levels are at approximately 1.15 and 1.25 volts when not driven.

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Register STEST4 (52h), bits 6 and 7, will be set to 11 to indicate LVD mode. If a single-ended device is placed on the bus, these results occur:

1. The drive pulls the DIFFSENS signal to less than 0.5 Volts. This input signal to the SCSI processor is interpreted as a change to a single-ended bus.

2. A delay (filter) of approximately 180 ms takes place, which in turn changes the STEST4 bits to 10 indicating single-ended mode. Also, the bus mode change interrupt (SIST1 register bit 4) is asserted to indicate a bus mode change.

3. The control and data signals change to driving single-ended levels.

Should an ISR be used to service a bus mode change, this interrupt bit may be used.

Bus Mode Change from Single Ended to LVD

This configuration involves a single-ended device on an LVD SCSI bus, LVD termination, and other LVD drives. When the single-ended drive is removed from the bus, these sequences occur:

1. Initially, signal levels are at 2.7 and 0.0 Volts. DIFFSENS is at approximately 0.0 volts.

2. When the single-ended device is removed, the termination switches immediately, (within 1 ms), and the DIFFSENS voltage switches to 1.3 volts.

3. The DIFFSENS signal is input to the SCSI processor, where the voltage level is interpreted for the correct bus mode.

   Note: According to the SCSI Parallel Interconnect specification, devices should wait at least 100 ms following change of DIFFSENS to change to the new bus mode in order to allow for possible noise on the line.

4. The SYM53C896 observes a filter of approximately 180 ms following detection of a change in DIFFSENS.

5. The STEST4 register bits, 6 and 7, change from 10 to 11. The SCSI bus mode change interrupt in SIST1 should also be asserted indicating a bus mode change at the same time the STEST4 bits change.

6. Data and control signal voltage levels on the SCSI bus should now reflect LVD levels, which would be 1.4 and 1.0 Volts.

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These observations have been made during the transition from SE to LVD regarding SCSI RST/, in which the interrupt for bus mode change is not asserted correctly.

1. Initially, signal levels are at 2.7 and 0.0 Volts. DIFFSENS is at approximately 0.0 volts.

2. The single-ended device is removed, the termination switches immediately, on the order of 1 ms, and the DIFFSENS voltage switches to 1.3 volts.

3. The DIFFSENS signal is input to the SCSI processor, where the voltage level is interpreted for the correct bus mode.

4. The SYM53C896 device observes a delay of approximately 180 ms following the detection of a change in DIFFSENS.

    A. STEST4 bits 6 and 7 change to 11, to reflect LVD.

    B. A SCSI RST/ received interrupt is asserted in SIST0. The bus mode change interrupt may be stacked behind the SCSI RST/ received interrupt, but not in all cases.

This seems to occur due to the termination switches being set around 1.0 ms. These signal lines, including the RST/, switch from 2.7 and 0.0 volts to 1.4 and 1.0 volts. Because the SCSI processor is waiting for more than 100 ms in accordance with the SPI-2 specification, and is still monitoring RST/ for a single-ended voltage, it also detects a SCSI RST/ prior to the bus mode change.

If an ISR service is required for this bus mode change and the interrupts are stacked, the asserted interrupt can be detected after the SCSI RST/ received interrupt clears. In the case of no asserted bus mode change interrupt, detection of the STEST4 bits can provide a means to indicate a required Interrupt service routine.

HVD SCSI bus

While the LVD and single-ended SCSI buses can switch from one mode to the other due to sharing of multi-mode termination such as the Unitrode 5630 or Dallas 2118, the HVD bus requires a separate interface. This interface is described below.

The HVD bus interface to the SCSI processor requires pull up resistors on all control and data signals (-) with the exception of BSY/, RST/, and SEL/, which are wired -or signals and require a pull down resistor. The associated DIR (=) signals do not require pull up or pull down resistors. These signals are then directed to differential transceivers, such as the TI 976A2 and then terminated prior to the connector.

Voltage levels for HVD and DIFFSENS are pulled to +5.0 Volts. The DIFFSENS signal is an input to both the SCSI processor and differential transceivers. Should a single-ended or LVD SCSI device be placed on the HVD bus, the DIFFSENS signal will be pulled to 1.3 or 0.0 Volts. Accordingly, the differential transceivers and the HVD drivers of the SCSI processor are disabled to avoid possible damage to these devices.

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Previous versions of the SYM53C895 and SYM53C896

Refer to SEN 892 Version 2.0 for more discussion about DIFFSENS and bus mode changes in the SYM53C895 that did not observe a wait of at least 100 ms. That article discusses a means to implement the SPI-2 specification of waiting 100 ms following issue of a DIFFSENS change. The latest revision of the SYM53C895 (Rev C0 P/N 609-0393426) and SYM53C896 (Rev B0 P/N 609-0393055, and C0 P/N 609-0393415) implement a filter of more than 100 ms, and that article does not apply to these devices.

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