Power-Up Guidelines for the LSI53C1030/LSI53C1020

System Engineering Note

S11051, Version 1.0

1 Revision Record

Revision	Date	Remarks
Version 1.0	4/2003	Initial release of document

2 Introduction

This engineering note provides signaling guidelines for powering up the LSI53C1030/LSI53C1020 controller. Designs must meet these guidelines to guarantee successful power-up of the LSI53C1030/LSI53C1020.

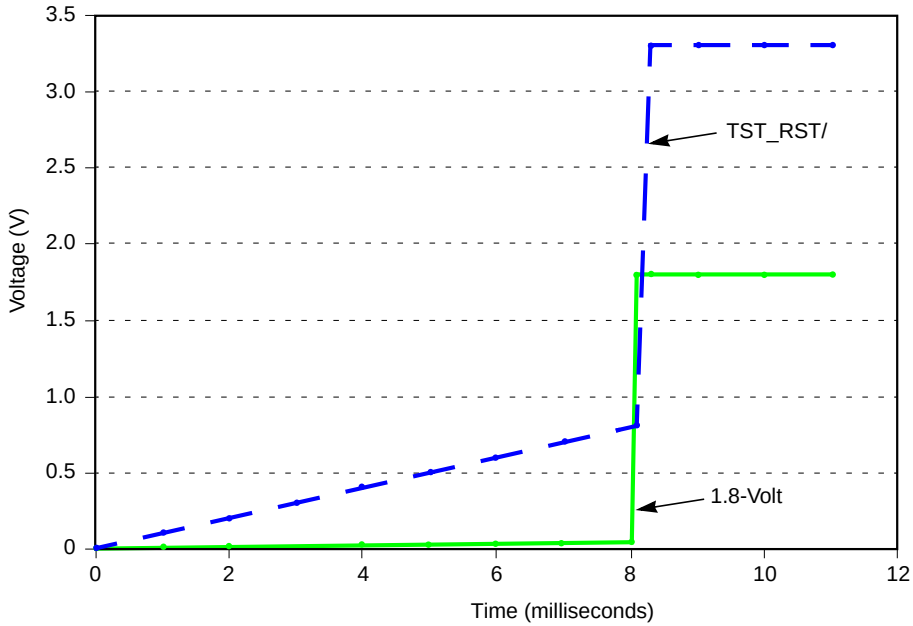
3 Signaling Guidelines

Designs must meet one of the following conditions to properly reset the controller. It is not necessary that designs meet both conditions.

- The 1.8 volt (V) power rail cannot be more than 50 millivolts (mV) above ground before the 1.8 V core voltage switches on. The optimal conditions are to hold the 1.8 V core voltage at ground until switching it on and driving it to 1.8 V. The 1.8 V core voltage can drift as high as 50 mV above ground without affecting the internal POR cell. If the 1.8 V power rail drifts above 50 mV, LSI Logic cannot guarantee the operation of the internal POR cell and, as such, cannot guarantee a proper reset of the phase lock loop (PLL) circuits.
- Hold the TST_RST/ signal lower than 800 mV when powering the 1.8 V supply. If the TST_RST/ pin is higher than 800 mV, LSI Logic cannot guarantee a proper reset of the PLL circuits.

Figure 1 illustrates the LSI53C1030/LSI53C1020 power-up sequence.

Figure 1 LSI53C1030/LSI53C1020 Power-Up Sequence



If neither of the above guidelines can be met, then LSI Logic recommends connecting an external POR circuit to TST_RST/ to hold the pin low until all the power supplies are in a known, good state.

These voltage values assume worst-case scenarios. LSI Logic cannot guarantee proper operation of the LSI53C1030/LSI53C1020 under conditions that violate these guidelines.

4 Other Guidelines

The above guidelines are in conjunction with the power-up sequencing guidelines stated in SEN S11019, and do not supersede the SEN S11019 guidelines. Figure 2 illustrates the SEN S11019 power-up sequencing guidelines.

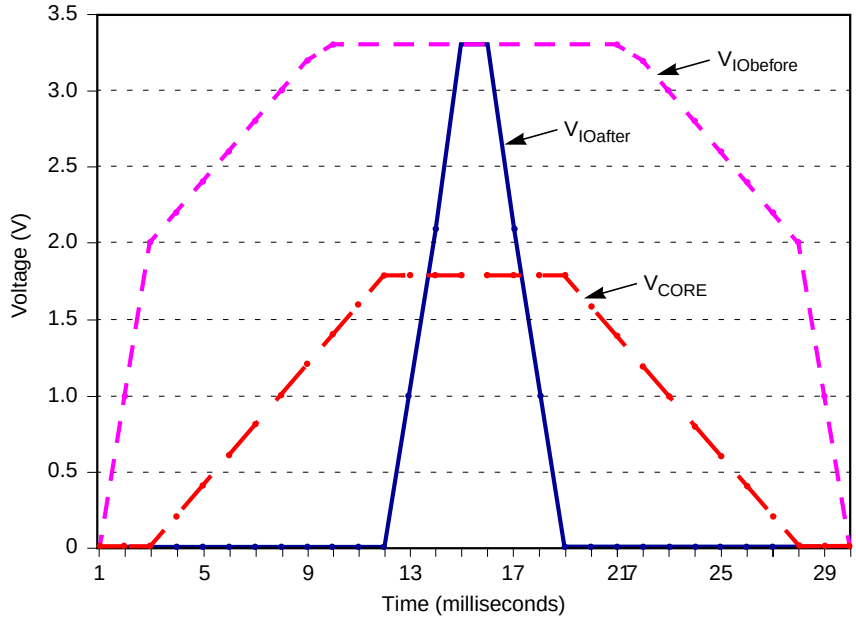
The power-up sequencing guidelines in SEN S11019 are:

- Power-up V_{CORE} (1.8 V) before V_{IO} (3.3 V). Figure 2 shows that V_{CORE} is stable at 1.8 V before $V_{IOafter}$ begins to rise.
- If powering-up V_{CORE} first is not possible, ensure that:

  $$V_{IO} < (V_{CORE} + 2\ V)$$

  applies at all times. In Figure 2, $V_{IObefore}$ rises before V_{CORE}, but at no time is $V_{IObefore}$ greater than V_{CORE} + 2 V.

Figure 2 LSI53C1030/LSI53C1020 Power Cycling



5 Symptoms of Incorrect Power-Up Sequence

The most common symptoms of improper power-up sequencing are:

- The host bus adapter (HBA) is unresponsive, which causes an “Adapter Malfunctioning” report from the LSI Logic SCSI BIOS.
- The HBA responds to limited PCI commands, but cannot interact with devices on the SCSI bus.

This behavior is a result of the PLLs not resetting.

Notes

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