NVSRAM Power Sequencing
System Engineering Note

S11044 Version 1.0

Revision Record

Revision	Date	Remarks
1.0	09/02	Initial release of this System Engineering Note.

1 Introduction

Integrated Mirroring™ (IM) firmware requires a 32 Kbytes NVSRAM to perform write journaling, which verifies that both drives in the IM volume are synchronized and have identical data. Write journaling uses an NVSRAM to retain data in case of a power failure.

This SEN provides information on the power down sequence involving the NVSRAM and the SCSI I/O controller. A system integrator can use this SEN to understand the necessary event ordering to ensure that the intended data is saved. This information applies to designs using the LSI53C1030, LSI53C1020, and LSI53C1035 PCI-X to Ultra320 SCSI controllers.

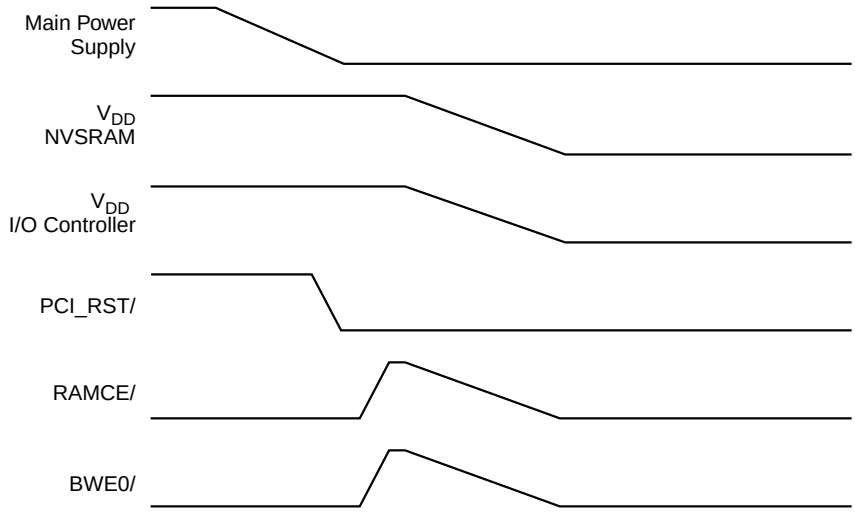
2 NVSRAM Considerations

There is a possibility of corruption of NVSRAM contents on power-down if the NVSRAM store operation begins before the I/O controller stops writing to NVSRAM. Figure 1 shows the signal and voltage sequencing that is required to avoid storing incorrect data.

There are three power down sequence considerations during writes to NVSRAM. Meeting these considerations ensures that the IM feature functions correctly.

1. PCI_RST/ must assert as power starts to go out of specification so that the I/O controller stops sending data. The I/O controller typically receives PCI_RST/ before the power supply to the I/O controller drops below specification. PCI_RST/ asserts when the main system power supply dropping, which typically occurs before the derived power supplies (5 V, 3.3 V, 2.5 V, 1.8 V) start to drop.
2. As the power supplied to the NVSRAM circuit decreases and the store to EEPROM begins, the NVSRAM part must stop accepting data. As a result of power failure to the I/O controller, the RAMCE/ and BWE0/ signals are invalid. The NVSRAM must ignore these control signals when it detects the power supply failure and begins storing data from SRAM to EEPROM.
3. If the supply to the NVSRAM differs from the supply to the I/O controller, the slopes of the power supply during a power failure might differ enough to affect the timing of the data storage. This can change the data storage timing and affect the data store process.

Figure 1 Power Sequencing



Notes

Headquarters

LSI Logic Corporation
North American Headquarters
Milpitas CA
Tel: 408.433.8000

LSI Logic Europe Ltd
European Headquarters
Bracknell England
Tel: 44.1344.426544
Fax: 44.1344.481039

LSI Logic K.K.
Headquarters
Tokyo Japan
Tel: 81.3.5463.7821
Fax: 81.3.5463.7820

To receive product literature, visit us at http://www.lsilogic.com.
For a current list of our distributors, sales offices, and design resource centers, view our web page located at http://www.lsilogic.com/contacts/na_salesoffices.html.

ISO 9000 Certified

Doc. No. DB05-000095-00