GPIO Pin Definitions for the LSI53C1030 and LSI53C1020

System Engineering Note

S11041 Version 1.0

Revision Record

Revision	Date	Remarks
Version 1.0	4/4/2002	Initial Release.

1 Introduction

This engineering note describes the general purpose I/O (GPIO) pins and their associated memory pages on the LSI53C1030 and LSI53C1020 Ultra320 SCSI chips.

2 Overview

The GPIO pins allow for flexible interaction of the chip with external components. The firmware, the SCSI BIOS, and the Fusion-MPT™ device driver software layers can interact with the GPIO pins. The function code defines each software layer's interaction with the GPIO pin.

Use the NVDATA.EXE application to program the GPIO pin settings and implementation. The NVDATA.DAT file provides configuration information to the NVDATA.EXE application. Any GPIO implementation that differs from the LSI Logic's default GPIO implementation requires a different NVDATA.DAT file.

3 GPIO Memory Pages

There are two configuration pages that control the behavior of the GPIO pins, Manufacturing Page 3 and IO Unit Page 3. Manufacturing Page 3 contains the GPIO pin definition and setup information. This page is read only to the BIOS and host driver. The firmware populates the IO Unit Page 3 function code, which is read-only, from Manufacturing Page 3. IO Unit Page 3 stores the output value for GPIO outputs. The BIOS and host driver interact with GPIO pins through IO Unit Page 3. The serial EEPROM stores both pages.

3.1 Manufacturing Page 3

The OEM programs Manufacturing Page 3 when building the board. Manufacturing Page 3 is read only to the host driver. During initialization, firmware reads Manufacturing page 3 when determining the current GPIO pin configuration. Additionally, firmware reads IO Unit Page 3 to determine the output state for all GPIO outputs.

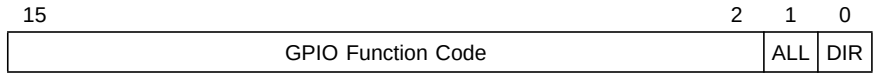
The OEM can clear bit 0 of the Manufacturing Page 3 GPIOVal field to configure the GPIO pin as an input or can set this bit to configure the GPIO pin as an output. Table 1 describes Manufacturing Page 3.

Table 1 Manufacturing Page 3

31 24	23 16	15 8	7 0	Offset
Page Type	Page Number	Page Length	Page Version	0x00
Chip ID				0x04
GPIOVal 1		GPIOVal 0		0x08
GPIOVal 3		GPIOVal 2		0x0C
GPIOVal 5		GPIOVal 4		0x10
GPIOVal 7		GPIOVal 6		0x14

Figure 1 provides a bit level description of the Manufacturing Page 3 GPIOVal field.

Figure 1 Manufacturing Page 3 GPIOVal Field Definition



GPIO Function Code **[15:2]**
Section 4 provides the GPIO function codes.

ALL **Active Level Logic** **1**
Clearing this bit configures the GPIO pin as active LOW.
Setting this bit configures the GPIO as active HIGH.

DIR **Direction** **0**
Clearing this bit configures the GPIO pin as an input.
Setting this bit configures the GPIO pin as an output.

3.2 IO Unit Page 3

The BIOS and host drivers use IO Unit Page 3 to determine the GPIO pin configuration, to read the current state of GPIO pins that are configured as inputs, and to set the output state of GPIO pins that are configured as outputs. The firmware maintains IO Unit Page 3 using information from Manufacturing Page 3. The GPIO function code bits are read only and can not be changed via IO Unit Page 3.

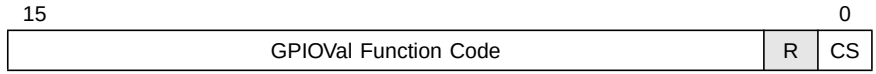
If the Manufacturing Page 3 setting configures the GPIO pin as an input, bit 0 of the IO Unit Page 3 GPIOVal field is read only to the host and provides the current GPIO pin setting. If the Manufacturing Page 3 setting configures the GPIO pin as an output, the host can write bit 0 of the IO Unit Page 3 GPIOVal field to control the GPIO pin. Firmware sets the initial values of the output pins from the previous values saved in the IO Unit Page 3 GPIOVal field. Therefore, the output pin values are persistent across reboots. Table 2 provides the format of IO Unit Page 3.

Table 2 IO Unit Page 3

31 24	23 16	15 8	7 0	Offset
Page Type	Page Number	Page Length	Page Version	0x00
Reserved			GPIO Count	0x04
GPIOVal 1		GPIOVal 0		0x08
GPIOVal 3		GPIOVal 2		0x0C
GPIOVal 5		GPIOVal 4		0x10
GPIOVal 7		GPIOVal 6		0x14

Figure 2 provides a bit level description of the IO Unit Page 3 GPIOVal field.

Figure 2 IO Unit Page 3 GPIOVal Field Definition



GPIO Function Code **[15:2]**

Section 4 provides the GPIO function codes.

Reserved **1**

This bit is reserved. Do not access reserved bits or fields.

Current Setting **0**

Clearing this bit disables the GPIO pin. Setting this bit enables the GPIO pin.

4 GPIO Function Codes

The GPIO function codes are predefined 14-bit codes that are associated with a function. The OEM can assign a single function to each GPIO pin. To assign a function to the GPIO pin, the OEM writes a function code to the Manufacturing Page 3 GPIOVal field. Because the host cannot write the GPIO function code field, the host cannot change the function code for a GPIO pin.

The lowest bit of the GPIO function code field assigns the GPIO pin to a SCSI channel. Clearing the lowest bit of the GPIO function code assigns the GPIO function code to SCSI Channel 0 (Channel A). Setting the lowest bit assigns the GPIO function code to SCSI Channel 1

(Channel B). For example, function code 0x0002 corresponds to SCSI Channel 0 termination control, while function code 0x0003 corresponds to SCSI Channel 1 termination control. Use SCSI Channel 0 settings for LSI53C1020-based designs.

Table 3 contains a list of the predefined GPIO function codes.

Table 3 GPIO Function Code Definitions

Function Code	Associated Function
0x0000	Unused GPIO Pin
0x0001	Reserved
0x0002	SCSI Channel A Termination Control
0x0003	SCSI Channel B Termination Control
0x0004	Disable SCSI Channel A
0x0005	Disable SCSI Channel B
0x0006	SCSI Channel A Cable Detect 0
0x0007	SCSI Channel B Cable Detect 0
0x0008	SCSI Channel A Cable Detect 1
0x0009	SCSI Channel B Cable Detect 1
0x000A – 0x3FFF	Reserved

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