LSI53C1030 External Memory Interface

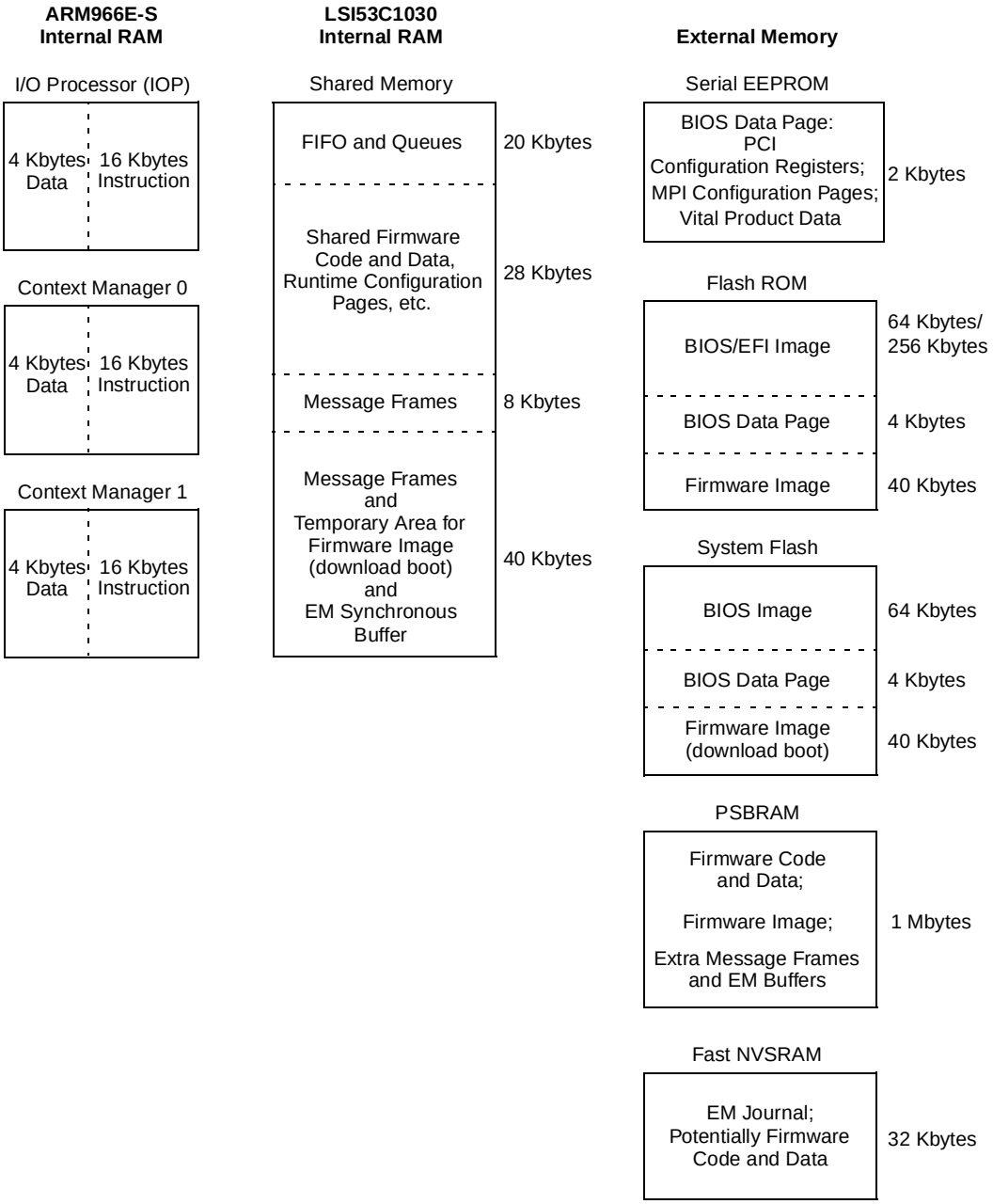
Systems Engineering Note

S11023

Version 1.0

This SEN provides information to help design a memory interface to the LSI53C1030. Figure 1 shows what internal and external memory sections are available and describes their use. A list of frequently asked questions (FAQs) explains design considerations for the external memory interface.

Figure 1 Internal and External Memory Sections and Sizes



1 Frequently Asked Questions (FAQs)

The following ten questions are FAQs relating to the LSI53C1030 external memory.

1. What configuration does LSI Logic recommend for a motherboard design with Embedded Mirroring (EM)?

   LSI Logic recommends that:

   a. The system Flash ROM contains the BIOS and firmware images.

   b. The NVSRAM contains the EM write logging and overflow code.

   c. The serial EEPROM contains the PCI configuration register values and Fusion-MPT™ architecture configuration pages.

2. What configuration does LSI Logic recommend for a motherboard design without EM?

   LSI Logic recommends that:

   a. The system Flash ROM contains the BIOS and firmware images.

   b. The serial EEPROM contains the PCI configuration register values and the Fusion-MPT architecture configuration pages.

3. What configuration does LSI Logic recommend for a host adapter design with EM?

   LSI Logic recommends that:

   a. The dedicated LSI53C1030 Flash ROM contains the BIOS and firmware images.

   b. The NVSRAM contains the EM write logging and overflow code.

   c. The serial EEPROM contains the PCI configuration register values and the Fusion-MPT architecture configuration pages.

4. What configuration does LSI Logic recommend for a host adapter design without EM?

   LSI Logic recommends that:

   a. The dedicated LSI53C1030 Flash ROM contains the BIOS and firmware images.

   b. The serial EEPROM contains the PCI configuration register values and the Fusion-MPT architecture configuration pages.

5. Is it possible to use the LSI53C1030 with no external memory?

   No. The LSI53C1030 always requires a serial EEPROM to store the Fusion-MPT configuration pages.

6. Is the Fusion-MPT driver ever responsible for downloading firmware? Can a board designer configure a system without a local or system Flash ROM?

   A Flash ROM or system Flash ROM must be available to store the firmware for the LSI53C1030. The SCSI BIOS initiates the download of the firmware to the LSI53C1030's on-chip RAM.

7. How much Flash ROM does the LSI53C1030 require?

   The amount of Flash ROM that the LSI53C1030 requires depends on the system configuration. Table 1 provides the Flash ROM requirements for various system configurations.

Table 1 LSI53C1030 Flash ROM Requirements

System Configuration	Total Flash ROM Size	Flash ROM Section Size
Motherboard with or without Embedded Mirroring	128 Kbytes	40 Kbytes for the compressed firmware image (64 Kbytes of code and initialized data) 64 Kbytes for the SCSI BIOS image
Host Adapter Board	128 Kbytes	64 Kbytes for the firmware 64 Kbytes for the SCSI BIOS
Host Adapter Board or Motherboard with the SCSI EFI[1] BIOS	512 Kbytes	64 Kbytes for firmware At least 256 Kbytes for the SCSI EFI BIOS

1. The Extensible Firmware Interface (EFI) BIOS supports 64-bit microprocessors (IA64: Intel Architecture 64).

8. When does the LSI53C1030 require Pipelined Synchronous Burst RAM (PSBRAM)?

   Firmware has no immediate requirement for a PSBRAM. To meet future design requirements, the LSI53C1030 provides a PSBRAM interface that enables board designers to store extra message frames, EM buffers, or firmware code and data in a PSBRAM. A motherboard or host adapter board design **cannot** use a PSBRAM in conjunction with an NVSRAM.

9. What is NVSRAM? When does the LSI53C1030 require an NVSRAM?

   An NVSRAM is a non-volatile SRAM package that retains the SRAM data upon power down. The NVSRAM uses one of two methods. The first is to store the SRAM data to an EEPROM upon power down. A 68 µF capacitor that is tied to Vcap guarantees the store operation regardless of power down slew rate. The NVSRAM transfers data from EEPROM to SRAM at restoration of power. The second method uses a battery backed SRAM to sustain the SRAM data on power down.

   EM write logging requires an NVSRAM. Firmware code/data overflow may also require an NVSRAM. For EM, the primary use of the NVSRAM is to increase the reliability of re-synching the mirrored drives.

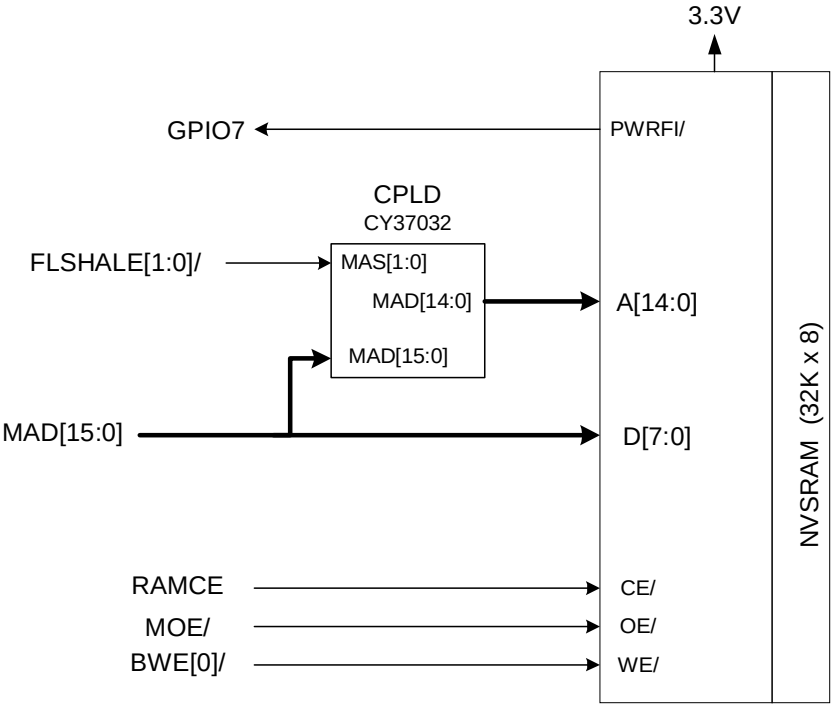
   Table 2 lists several potential vendor part numbers and provides comparisons of size, voltage, back-up style, and access time.

Table 2 NVSRAM Part Information

NVSRAM Manufacturer	Part Number	Size	Back-up	Vdd	Access Time
ST Micro	M48Z32	32 Kbytes	Lithium cell	3.3 V	100 nsec
Simtek	STK14C88	32 Kbytes	EEPROM	3.3 V	20 - 45 nsec
Dallas	DS1230W	32 Kbytes	Lithium cell	3.3 V	150 nsec

Figure 2 provides a block diagram of the NVSRAM interface.

Figure 2 NVSRAM Block Diagram



10. Can LSI Logic provide example part numbers for the external memory interfaces?

    Table 3 provides example part numbers for use with the LSI53C1030 memory interface.

Table 3 Example External Memory Interface Part Numbers

External Memory	Example Part Number	Memory Size
Serial EEPROM	24C16	16 Kbits (2 Kbyte)
Flash ROM	29LV040	4 Mbit (512 Kbyte)
NVSRAM	Simtek STK14C88[1]	32 Kbytes – EEPROM backed
NVSRAM	ST Micro M48Z32	32 Kbytes – Battery backed
PSBRAM	MT58L1MY18P	1 Mbyte (1M x 18)

1. The Simtek STK14C88 5V, 350 mil, 32k x 8, SOIC part requires a 68 µF or larger super cap.

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