Design Considerations for the LSI53C1010R and LSI53C1030

Systems Engineering Note

S11019

Version 1.2

1 Introduction

This SEN describes the necessary considerations to permit drop-in migration from the LSI53C1010R to the LSI53C1030. The LSI53C1010R is a 66 MHz PCI Dual Channel Ultra160 SCSI Multifunction controller in a 456 BGA package. The LSI53C1030 is a 133 MHz PCI-X Dual Channel Ultra320 SCSI Multifunction controller in a 456 BGA package.

The LSI53C1010R is the same electrical design as the proven LSI53C1010, but is repackaged to have the same package footprint as the LSI53C1030. Due to the package and pinout differences between the LSI53C1010 and LSI53C1030, a drop-in migration from the LSI53C1010 to the LSI53C1030 is not possible. The pinout of the LSI53C1010R enables drop-in migration from a design using the LSI53C1010R to a design using the LSI53C1030. This SEN details the necessary considerations to create a board that accommodates either the LSI53C1010R or the LSI53C1030.

Unless otherwise stated, the design considerations that apply to the LSI53C1010R and the LSI53C1030 also apply to the LSI53C1000R and LSI53C1020 devices.

2 Differences between the LSI53C1010R and LSI53C1030

Table 1 lists the signal differences between the LSI53C1010R and the LSI53C1030.

Table 1 Signal Differences between the LSI53C1010R and the LSI53C1030

Ball #	LSI53C1010R Signal Name	LSI53C1010R Signal Description	LSI53C1030 Signal Name	LSI53C1030 Signal Description
D4	NC	–	TRACEPKT0	Trace Port for Embedded Trace Macrocell (ETM)
B2	NC	–	TRACEPKT1	ETM Trace Port
F5	NC	–	TRACEPKT2	ETM Trace Port
E4	NC	–	TRACEPKT3	ETM Trace Port
C2	NC	–	TRACEPKT4	ETM Trace Port
E3	NC	–	TRACEPKT5	ETM Trace Port
G5	NC	–	TRACEPKT6	ETM Trace Port
F4	NC	–	TRACEPKT7	ETM Trace Port
B3	NC	–	TRACECLK	ETM Trace Clock
D5	NC	–	PIPESTAT0	ARM966E-S Pipeline Status
E6	NC	–	PIPESTAT1	ARM966E-S Pipeline Status
C3	NC	–	PIPESTAT2	ARM966E-S Pipeline Status
E5	NC	–	TRACESYNC	ETM Trace Synchronization
AA4	NC	–	TCK_ICE	JTAG Test Clock
Y5	NC	–	TMS_ICE	Test Mode Select for the ETM and In-Circuit Emulator (ICE) debug logic
AB3	NC	–	TDI_ICE	JTAG Test Data In for the ETM/ICE Debug Logic

Table 1 Signal Differences between the LSI53C1010R and the LSI53C1030 (Cont.)

Ball #	LSI53C1010R Signal Name	LSI53C1010R Signal Description	LSI53C1030 Signal Name	LSI53C1030 Signal Description
AD2	NC	–	TDO_ICE	JTAG Test Data Out for the ETM/ICE Debug Logic
AB4	NC	–	TRST_ICE	JTAG Test Reset for the ETM/ICE Debug Logic
AA5	NC	–	RTCK_ICE	JTAG Test Clock Acknowledge for the ETM/ICE Debug Logic
AA22	NC	–	CLKMODE_0	Test Pin for LSI Logic Only
R1	NC	–	A_RBIAS	Bias Current for LVD Pads
N2	NC	–	VDDC	Core Power Pin
P2	NC	–	VSSC	Core Ground Pin
AD3	NC	–	VDDC	Core Power Pin
AB5	NC	–	VSSC	Core Ground Pin
D15	NC	–	VDDC	Core Power Pin
C14	NC	–	VSSC	Core Ground Pin
AF15	NC	–	VDDC	Core Power Pin
AD14	NC	–	VSSC	Core Ground Pin
AD9	NC	–	PCI5VBIAS	PCI 5 V tolerant pins: These signals connect to 5 V in a 5 V signaling system or to 3.3 V in a 3.3 V signaling system.
AE6	NC	–	PCI5VBIAS	
AC10	NC	–	PCI5VBIAS	
AF12	NC	–	PCI5VBIAS	
AD18	NC	–	PCI5VBIAS	
AB22	NC	–	PCI5VBIAS	
Y22	NC	–	PCI5VBIAS	
W25	NC	–	PCI5VBIAS	
M23	NC	–	PCI5VBIAS	

Table 1 Signal Differences between the LSI53C1010R and the LSI53C1030 (Cont.)

Ball #	LSI53C1010R Signal Name	LSI53C1010R Signal Description	LSI53C1030 Signal Name	LSI53C1030 Signal Description
E23	NC	–	MAD8	High Byte of the External Memory Interface.[1]
F22	NC	–	MAD9	
C24	NC	–	MAD10	
E22	NC	–	MAD11	
D23	NC	–	MAD12	
B25	NC	–	MAD13	
E21	NC	–	MAD14	
D22	NC	–	MAD15	
B24	NC	–	MADP0	Parity for MAD[7:0]
C22	NC	–	MADP1	Parity for MAD[15:8]
E20	NC	–	MCLK	Memory Clock for the Synchronous RAM
D21	NC	–	ADSC/	Address Strobe Controller
B23	NC	–	ADV/	Advance for SRAM Burst Address Counter
D20	NC	–	RAMCE/	SRAM Synchronous Chip Select
E24	NC	–	BWE1/	Memory Byte Write Enable for High Byte
C25	NC	–	HB_LED/	Heartbeat LED or GPIO
N23	NC	–	SPAREPAD1	Reserved
A24	NC	–	DIS_PCI_FSN/	PCI Frequency Synthesizer (FSN) Enable
C5	NC	–	TN	Test Pin for LSI Logic Only
AE5	NC	–	PVT1	Biasing for PCI Signals. Connect a 50 Ω resistor between PVT1 and PVT2.
AF4	NC	–	PVT2	
AB21	NC	–	VDDA	Analog Circuit Power (PLL)

Table 1 Signal Differences between the LSI53C1010R and the LSI53C1030 (Cont.)

Ball #	LSI53C1010R Signal Name	LSI53C1010R Signal Description	LSI53C1030 Signal Name	LSI53C1030 Signal Description
AD24	NC	–	VSSA	Analog circuit ground (PLL, DIFFSENS)
AE2	VDDA1	Analog Circuit Power (PLL)	TESTHCLK	Test Pin for LSI Logic Only
AB6	VSSA1	Analog Circuit Ground (PLL, DIFFSENS)	TESTACLK	Test Pin for LSI Logic Only
AC9	CLK	PCI Clock	NC	–
AC22	NC	–	CLK	PCI Clock
AC2	ENABLE66	Enables 66 MHz PCI	CLKMODE_1	Test Pin for LSI Logic Only
AC23	NC	–	GPIO0	General Purpose I/O
AE25	NC	–	GPIO1	General Purpose I/O
K24	AGPIO2	General Purpose I/O	GPIO2	General Purpose I/O
H25	AGPIO3	General Purpose I/O	GPIO3	General Purpose I/O
M25	BGPIO0	Serial EEPROM Data to SCSI Channel B	GPIO4	General Purpose I/O
L25	BGPIO1	Serial EEPROM Clock to SCSI Channel B	GPIO5	General Purpose I/O
L23	BGPIO2	General Purpose I/O	GPIO6	General Purpose I/O
K25	BGPIO3	General Purpose I/O	GPIO7	General Purpose I/O
K23	BGPIO4	General Purpose I/O	B_LED/	SCSI Channel [0] Activity LED Driver or a GPIO
J23	AGPIO4	General Purpose I/O	A_LED/	SCSI Channel [1] Activity LED Driver or a GPIO
H26	AGPIO0	Serial EEPROM Data to SCSI Channel A or an Activity LED	SerialDATA	Serial EEPROM Interface
J25	AGPIO1	Serial EEPROM Clock to SCSI Channel A	SerialCLK	Serial EEPROM Interface
J24	MAS1	High Order Address Byte Memory Address Strobe	FLSHALE1/	High Order Address Byte Memory Address Strobe

Table 1 Signal Differences between the LSI53C1010R and the LSI53C1030 (Cont.)

Ball #	LSI53C1010R Signal Name	LSI53C1010R Signal Description	LSI53C1030 Signal Name	LSI53C1030 Signal Description
K22	MAS0	Low Order Address Byte Memory Address Strobe	FLSHALE0/	Low Order Address Byte Memory Address Strobe
G26	MOE/	Memory Output Enable	MOE/	Memory Output Enable
G25	MCE/	Memory Chip Enable	FLSHCE/	Memory Chip Enable
H23	MWE/	Memory Write Enable	BWE0/	Memory Byte Write Enable for the Low Byte
D7	TEST_HSC	Test Halt SCSI Clock	TESTCLKEN	Test Pins for LSI Logic Only
E7	SCAN_MODE	Scan Mode	SCANMODE	

1. Refer to the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Controller Technical Manual for a complete description of the MAD pin functionality.

The LSI53C1010 INT_DIR pin controls the routing of the interrupt pins INTA, INTB, ALT_INTA, and ALT_INTB. The INT_DIR pin is not present on the LSI53C1010R. Software controls the interrupt direction on the LSI53C1010R by programming bits [1:0] of the SCSI Test One (STEST1) register.

3 Power Supply Consideration

This section details the power supply considerations necessary to design a board that is capable of supporting either the LSI53C1030 or the LSI53C1010R.

3.1 Core and I/O Voltages

LSI Logic fabricates the LSI53C1030 with the G12™ process and the LSI53C1010R with the SYM9 process. For G12 chips, the core power requires 1.8 V and the I/O power requires 3.3 V. For SYM9 chips, both core and I/O power require 3.3 V. Tolerance for 5 V PCI signals requires a 5 V bias supply. But if a system uses only 3.3 V PCI signaling, the 5 V bias pins can connect to 3.3 V.

Legacy LSI53C1010 board designs supply V_{DD}_CORE and V_{DD}_IO by a single regulator with either a single power plane or multiple connected

power planes. Board designs that accommodate both the LSI53C1010R and LSI53C1030 require separate V_{DD}_CORE and V_{DD}_IO power planes. For an LSI53C1010R board design, short the power planes together and connect them to 3.3 V using either 0 Ω resistors or inductors. Remove these resistors or inductors to migrate the board design to support the LSI53C1030. This separates the core and I/O power planes. Then, supply 1.8 V to V_{DD}_CORE and 3.3 V to V_{DD}_IO. The LSI53C1030 board requires a voltage regulator to supply 1.8 V, 2 A.

3.2 Power Sequences

Power V_{DD}_CORE up before V_{DD}_IO. If this is not possible, be certain that V_{DD}_IO is less than V_{DD}_CORE plus 2.0 V. The power down sequence is in the reverse order as the power up sequence.

3.3 Voltage Margins

The LSI53C1010R requires a 3.3 V ±5% supply for 3.3 V. For the LSI53C1030, the PCI interface can provide V_{DD}_IO. The PCI interface is a 3.3 V ±10% supply. The high speed capability of the G12 process provides timing margins that allow for the additional voltage margin. Furthermore, the majority of the logic runs at 1.8 V, which originates from a voltage regulator.

3.4 Voltage Regulators

To improve efficiency use switching voltage regulators instead of linear voltage regulators. Because of their small size and low impedance, LSI Logic recommends decoupling the switching voltage regulator circuit using solid tantalum bypass capacitors.

3.5 Noise Filters

To maximize the benefits of the internal split ground system, place a bypass capacitor between ground and each V_{DD} ball, except for VDDA balls. Capacitor values of 0.01 µF, 0.001 µF, or some combination of 0.01 µF and 0.001 µF provide adequate isolation. LSI Logic recommends using package types with X7R or COG dielectrics due to their frequency response characteristics.

VDDA and VSSA pins supply power and ground for the analog cells. Table 2 lists these pins. Protect the LSI53C1010R against power supply

noise coupling by placing ferrite beads between each VDDA ball and 3.3 V. Also, place a ferrite bead between each VSSA ball and ground. LSI Logic recommends using ferrite beads with a rating of 150 Ω at 100 MHz. Protect the LSI53C1030 against power supply noise by placing a 1 Ω resistor between 1.8 V and VDDA. Place a 0.2 µF capacitor to ground on the chip side of the resistor. There are no ferrite beads in the LSI53C1030 analog noise filter circuit.

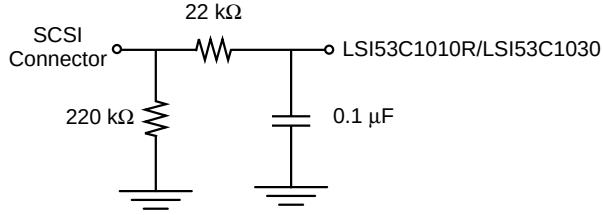
Table 2 VDDA and VSSA Pins

Ball #	LSI53C1030 signal	Ball #	LSI53C1010R signal
C1	VDDA	C1	VDDA0
AB21	VDDA	AE2	VDDA1
H5	VSSA	H5	VSSA0
AD24	VSSA	AB6	VSSA1

4 DIFFSENS

The DIFFSENS input to the LSI53C1010R and the LSI53C1030 requires filtering. LSI Logic recommends the filter shown in Figure 1.

Figure 1 DIFFSENS Filtering



5 RBIAS

To generate the proper LVD pad bias current connect a 10 kΩ, 1% RBIAS resistor between the A_VDDBIAS/B_VDDBIAS pins and the A_RBIAS/B_RBIAS pins. These pins do not need to connect to the supply voltage. Both the G12 and the SYM9 process technologies

require the 10 kΩ resistor value. Table 3 summarizes the connections for the A_RBIAS/B_RBIAS and A_VDDBIAS/B_VDDBIAS circuits.

Table 3 A_RBIAS/B_RBIAS and A_VDDBIAS/B_VDDBIAS Connections

Ball #	LSI53C1010R	LSI53C1030	LSI53C1000R	LSI53C1020
R1	NC	A_RBIAS	NC	A_RBIAS
A11	B_RBIAS	B_RBIAS	B_RBIAS	NC
T1	A_VDDBIAS	A_VDDBIAS	A_VDDBIAS	A_VDDBIAS
B13	B_VDDBIAS	B_VDDBIAS	B_VDDBIAS	NC

6 LSI53C1030 Layout Considerations

The preceding considerations enable a board design to accommodate either the LSI53C1030 or the LSI53C1010R. To operate the LSI53C1030 in a 133 MHz PCI-X Ultra320 SCSI environment, a board designer must also consider board skew, capacitance, and impedance matching. To ensure proper operation in this environment:

- Use 5 mil traces with 5 mil spacing to achieve the proper SCSI trace impedance.
- Route the PCI/PCI-X signals on the inside layer to achieve a 50 Ω to 60 Ω impedance.
- Split the V_{DD}_CORE and V_{DD}_IO voltage planes. Be certain to match the signal traces with the plane that the signal references.

7 Heat Sink Requirements

There are no special air flow or heat sink requirements for the LSI53C1010R. Refer to SEN S11027, “Heat Sink for the LSI53C1030,” for information concerning heat sinks and air flow requirements for the LSI53C1030.

8 SCSI Clock Requirements

Provide a 40 MHz oscillator to the LSI53C1010R SCLK input. Provide an 80 MHz oscillator to the LSI53C1030 SCLK input.

9 GPIO Considerations

The LSI53C1010R requires two serial EEPROMs, one for each channel. The LSI53C1010R provides a separate bus for each channel interface to the serial EEPROM.

The LSI53C1030 requires a single serial EEPROM and the GPIO pins do not associate with a specific channel. The SerialDATA and SerialCLK signals connect the EEPROM with the LSI53C1030. A serial EEPROM downloads subsystem vendor ID information to the LSI53C1030, which then routes the information to the appropriate registers. Use a 24C16, 2 Kbyte serial EEPROM for this application.

Table 4 summarizes the GPIO pin differences between the LSI53C1010R and the LSI53C1030.

Table 4 GPIO Signal Differences Between the LSI53C1010R and the LSI53C1030

Ball #	LSI53C1010R	LSI53C1010R Function	LSI53C1030	LSI53C1030 Function
AC23	NC	Not Connected	GPIO0	General Purpose I/O
AE25	NC	Not Connected	GPIO1	General Purpose I/O
K24	AGPIO2	General Purpose I/O	GPIO2	General Purpose I/O
H25	AGPIO3	General Purpose I/O	GPIO3	General Purpose I/O
M25	BGPIO0	Serial EEPROM Data / Activity LED	GPIO4	General Purpose I/O
L25	BGPIO1	Serial EEPROM Clock	GPIO5	General Purpose I/O
L23	BGPIO2	General Purpose I/O	GPIO6	General Purpose I/O
K25	BGPIO3	General Purpose I/O	GPIO7	General Purpose I/O

Table 4 GPIO Signal Differences Between the LSI53C1010R and the LSI53C1030 (Cont.)

Ball #	LSI53C1010R	LSI53C1010R Function	LSI53C1030	LSI53C1030 Function
K23	BGPIO4	Programs the Flash	B_LED/	SCSI Channel [0] Activity LED or a GPIO
J23	AGPIO4	Programs the Flash	A_LED/	SCSI Channel [0] Activity LED or a GPIO
H26	AGPIO0	Data to Serial EEPROM/Activity LED	SerialDATA	Serial EEPROM Interface
J25	AGPIO1	Clock to Serial EEPROM	SerialCLK	Serial EEPROM Interface

10 LSI53C1030 Flash and SRAM Memory Interface

The LSI53C1030 provides Flash ROM, NVSRAM, pipelined synchronous burst static RAM (PSBRAM), and serial EEPROM interfaces. The LSI53C1030 does not require a PSBRAM for operation, but the user may store additional code in the PSBRAM. The Flash ROM interface stores SCSI BIOS and firmware images for the LSI53C1030. The Flash ROM is optional if the LSI53C1030 is not the boot device and a suitable driver exists to initialize the LSI53C1030. The NVSRAM supports integrated mirroring. The nonvolatile external serial EEPROM stores configuration parameters for the LSI53C1030.

Refer to SEN S11023, “LSI53C1030 External Memory Interface” and the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller Technical Manual for more information concerning the LSI53C1030 Flash ROM and SRAM interface.

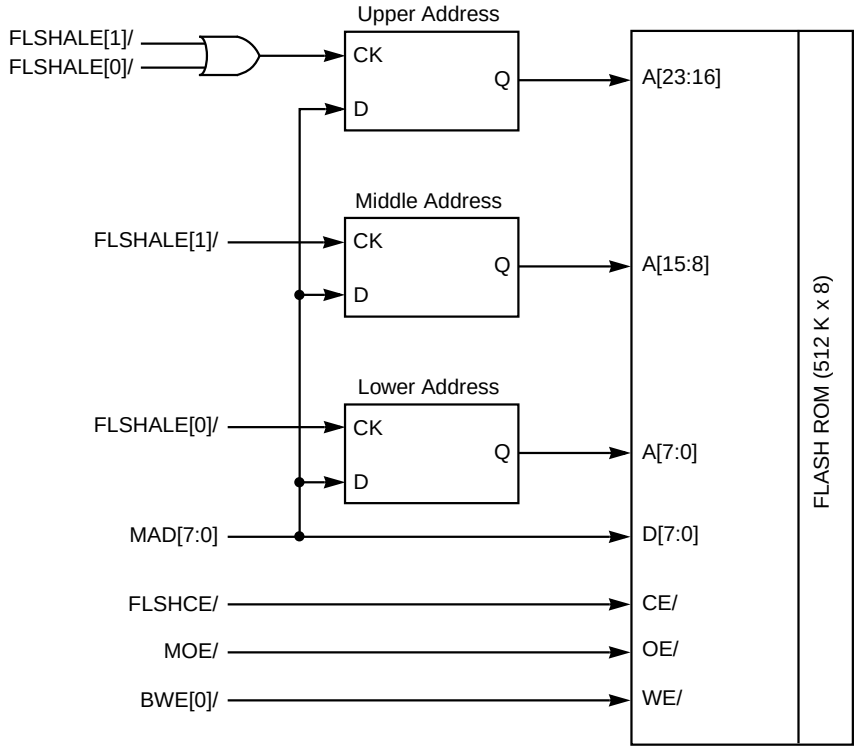
10.1 Flash ROM Interface

The Flash ROM interface stores SCSI BIOS and firmware images for the LSI53C1030. The Flash ROM is optional if the LSI53C1030 is not the boot device and a suitable driver exists to initialize the LSI53C1030. The Flash ROM interface multiplexes the 8-bit address and data buses on the MAD[7:0] pins. The interface latches the address into three 8-bit latches to support up to 16 Mbytes of address space through 24 address bits. The interface supports the byte read, byte write, word read, and word write instructions. The LSI53C1030 Dword aligns Dword reads, word

aligns word reads, and byte aligns byte reads. The remaining bits from word and byte reads are meaningless.

The Power-On sense pin configurations define the size of the Flash address space. The LSI53C1030 defines only the middle (MA[15:8]) and lower (MA[7:0]) address ranges if the Flash addressable space is 64 Kbytes and below. The LSI53C1030 defines the upper (MA[23:16]), middle (MA[15:8]), and lower (MA[7:0]) address ranges if the Flash addressable space is 128 Kbytes and above. Figure 2 provides an example of a Flash ROM configuration.

Figure 2 FLASH ROM Block Diagram



The LSI53C1030 implements a Flash signature recognition mechanism to determine if the Flash contains a valid image. The Flash may be present and not contain a valid image before its initial programming or during board testing. The first access to the Flash is a 16-byte burst read beginning at Flash address 0x000000. The LSI53C1030 compares the values read to the Flash signature values that Table 5 provides. If the

signature value match, the LSI53C1030 performs the instruction located at Flash address 0x000000. If the signature values do not match, the LSI53C1030 records an error and ignores the Flash instruction. The Flash signature does not include the first three bytes of Flash memory as these bytes contain a branch offset instruction.

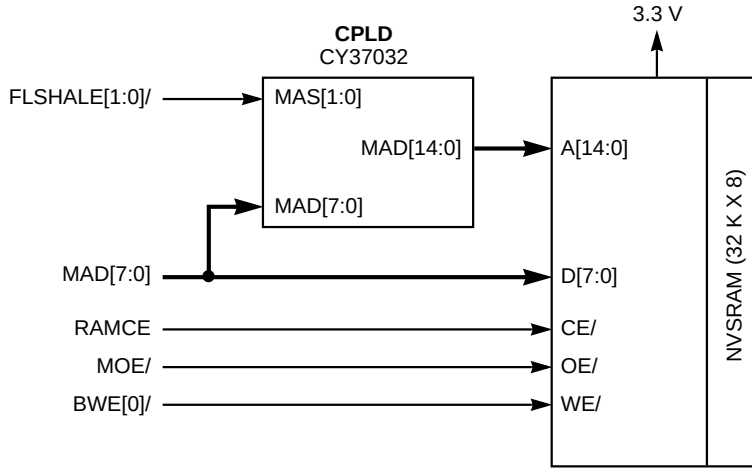
Table 5 Flash Signature Value

Flash Address	Flash Signature Values			
Bytes [3:0]	0xEA	XX	XX	XX
Bytes [7:4]	0x5A	0xEA	0xA5	0x5A
Bytes [11:8]	0xA5	0x5A	0xEA	0xA5
Bytes [15:12]	0x5A	0xA5	0x5A	0xEA

10.2 NVSRAM

The NVSRAM supports integrated mirroring on the LSI53C1030. Keeping a second disk as mirror requires that the LSI Logic Fusion-MPT™ firmware perform writes to both the boot drive and the mirror drive. The mirroring of the boot drive is transparent to the BIOS, drivers, and operating system. Figure 3 provides a block diagram illustrating how to connect the NVSRAM. The design may employ the CPLD to latch the address instead of using three separate address latches. The NVSRAM is selected through the RAMCE when the MAD3 pull-up option is pulled HIGH.

Figure 3 NVSRAM Block Diagram



10.3 PSBRAM Interface

The PSBRAM interface operates at 80 MHz to support a maximum burst rate of 128 Mbytes/s and supports word, half-word, and byte reads and writes. The LSI53C1030 dword aligns dword accesses, word aligns word accesses, and byte aligns byte accesses. The remaining bits from word and byte accesses are meaningless.

The address and data bus is 16-bits wide. The PSBRAM interface multiplexes four control signals to provide 20 address bits, which support up to 1 Mbyte of word address space. The FLSHALE[1:0] control signals always provide Address [19:18]. The MADP[1:0] control signals provide Address [17:16] on address phases and optional, programmable-sense byte parity on data read/write phases.

Figure 4 and Figure 5 provide examples of PSBRAM configurations that the LSI53C1030 supports. These examples use 1 M x 16/18 and 512 K x 16/18 PSBRAMs. The LSI53C1030 also supports other RAM depths up to an expansion depth of two. The board designer must consider RAM depth at board build-time since the use of the expansion chip selects (CS0, CS1/) address hookups depend on the RAM depth.

Figure 4 Single Bank without Depth Expansion

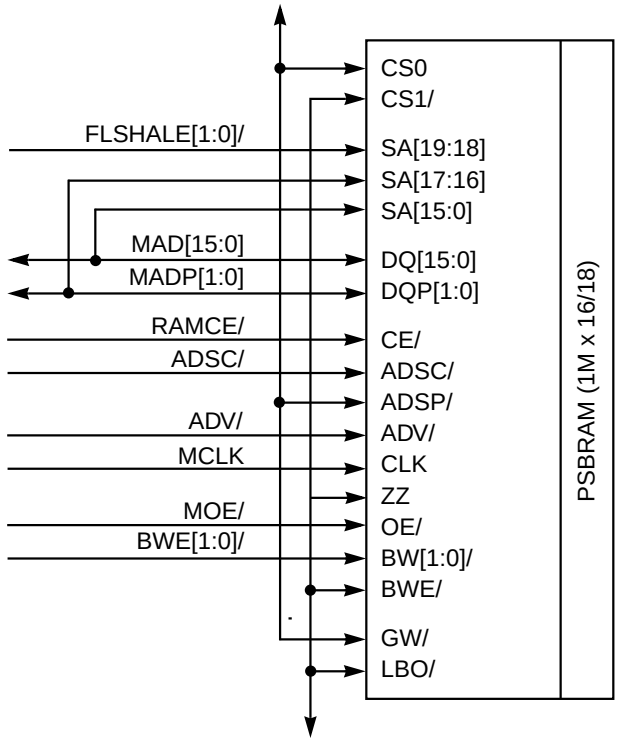
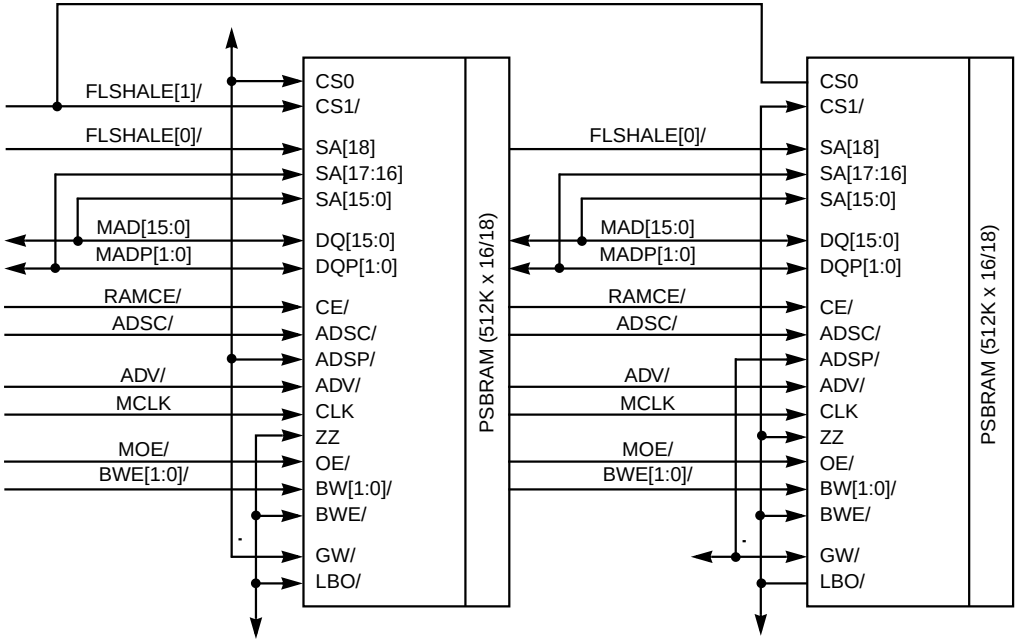


Figure 5 Single Bank with Depth Expansion



11 PCI Bus Considerations

The PCI clock pin BGA position is different on the LSI53C1010R than on the LSI53C1030. A board designer must give special consideration to routing this signal. Route the PCI clock to the LSI53C1030 CLK pin (ball AC22) first and obtain the 2.5 inch trace length required by the PCI specification. Then route a trace to the LSI53C1010R CLK (ball AC9) to create a T-trace that uses only one leg at any time.

Connect a 49.9 Ω, 1% resistor between PVT1 and PVT2 to properly bias the PCI signals.

Host Adapter Boards (HABs) must provide a pull-up/pull-down option for the PCI-X capability pin (PCIXCAP, PCI connector pin 38B) on the PCI expansion connector to indicate if the card is capable of PCI-X. See the PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a, for details. Table 6 summarizes PCIXCAP pin indications.

Table 6 PCIXCAP Pin Indications

PCIXCAP connection	Add-in card PCI capability
Directly to ground	Not PCI-X Capable
Through a 0.01 µF capacitor to ground	PCI-X, 133 MHz Capable
Through a 10 kΩ resistor in parallel with 0.01 µF capacitor to ground	PCI-X, 66 MHz Capable

12 MAD Pin Power On Options

Provide both pull-up options for all of the signals listed in Table 7. These signals all have internal pull-downs. Table 1 describes the default setting.

Table 7 LSI53C1010R and LSI53C1030 Power Up Options

Ball #	Signal	LSI53C1010R Function[1]	LSI53C1030 Function[2]
C22	MADP1	–	Reserved
B24	MADP0	–	Enables PCI-X
D22	MAD15	–	Enables 133 PCI-X
E21	MAD14	–	Enables 64-Bit PCI/PCI-X
B25	MAD13	–	Enables 66 MHz PCI/PCI-X
D23	MAD12	–	Reserved
E22	MAD11	–	ID Control [1]
C24	MAD10	–	ID Control [0]
F22	MAD9	–	Reserved
E23	MAD8	–	Reserved
D26	MAD7	Enable Serial EEPROM Autodownload	Enable Serial EEPROM Autodownload
E25	MAD6	Reserved	Enables the IOP Boot

Table 7 LSI53C1010R and LSI53C1030 Power Up Options (Cont.)

Ball #	Signal	LSI53C1010R Function[1]	LSI53C1030 Function[2]
H22	MAD5	Reserved	PCI Function and SCSI Channel Configuration
F24	MAD4	Channel B IRQ Routing	
G23	MAD3	ROM Size Configuration	Reserved
D25	MAD2		ROM Size Configuration
F23	MAD1		
G22	MAD0	Slow ROM	Reserved

1. Refer to the LSI53C1010R PCI to Dual Channel Ultra160 SCSI Multifunction Controller Technical Manual for a complete signal description.
2. Refer to the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller Technical Manual for a complete signal description.

13 Test Signals

For debug purposes, include three headers in the board design. The first header is a 20-pin header for Multi-ICE debugging through the ICE JTAG port. This header is essential for debugging both the firmware and the design functionality. The connector is a 20-pin header that mates with the IDC sockets mounted on a ribbon cable. Table 8 details the pinout.

Table 8 20-Pin Header Pinout

Pin Number	Signal	Pin Number	Signal
1	VDD (3.3V)	11	RTCK_ICE
2	VDD (3.3V)	12	VSS
3	TRST_ICE[1]	13	TDO_ICE
4	VSS	14	VSS
5	TDI_ICE[1]	15	TST_RST/[1]
6	VSS	16	VSS
7	TMS_ICE[1]	17	No connect
8	VSS	18	VSS
9	TCK_ICE[1]	19	No connect
10	VSS	20	VSS

1. The designer must connect a 4.7 kΩ resistor from this signal to 3.3 V.

The second header that LSI Logic considers essential is a 38-pin connector for use with the Embedded Trace Macrocell (ETM) included in the LSI53C1030. The ETM provides real time analysis of ARM code execution. Table 9 details the pinout.

Table 9 38-Pin Connector Pinout

Pin Number	Signal	Pin Number	Signal
1	NC	20	TRACEPKT5
2	NC	21	TRST_ICE
3	NC	22	TRACEPKT4
4	NC	23	VDD (3.3 V)
5	VSS	24	TRACEPKT3
6	TRACECLK	25	VSS
7	VSS	26	TRACEPKT2
8	VSS	27	VDD (3.3 V)
9	TST_RST	28	TRACEPKT1
10	VSS	29	VDD (3.3 V)
11	TDO_ICE	30	TRACEPKT0
12	VSS	31	VSS
13	RTCK_ICE	32	TRACESYNC
14	VSS	33	VSS
15	TCK_ICE	34	PIPESTAT2
16	TRACEPKT7	35	VSS
17	TMS_ICE	36	PIPESTAT1
18	TRACEPKT6	37	VSS
19	TDI_ICE	38	PIPESTAT0

Note that the TRACEPKT[7:0], TRACESYNC, TRACECLK, and PIPESTAT[2:0] signals may require series termination depending on trace length and impedance. Please reference http://www.tm.agilent.com and download *Trace Port Analysis for ARM ETM User's Guide*. This User's Guide contains information on series termination, part numbers for the 38-pin connector, information on the connector pinout, and setup configurations. While LSI Logic Corporation can neither recommend nor suggest vendors or parts, the

Trace Port Analysis for ARM ETM User Guide recommends the AMP Mictor connector for this application.

The third header relates to the LSI53C1030's internal test mux. The test mux is similar to the LSI53C1010's text mux, however more pins are available to bring specific internal signals out to test points. The test mux pins include the MAD[15:0], MADP[1:0], GPIO[7:0], A_LED/, B_LED/, TRACEPKT[7:0], and PIPESTAT[2:0] pins. The MAD[15:0] bus enables observation of the internal buses while the remaining pins enable observation of other internal signals. Routing the test mux pins to test points or, preferably, to a header is essential to the initial design of an LSI53C1030 evaluation board. Besides maintenance of the MAD bus pin order, the order in which the signals route to the header is insignificant. LSI Logic recommends a layout with two, 2 x 10 arrays of 25 mil square posts, with 100 mil spacing. Stack the arrays to resemble a 4 x 10 array, but maintain at least a 300-mil space between the two arrays. This allows space for simultaneous 2 x 10 logic analyzer connections on both arrays.

14 LSI53C1010R Pinout

Table 9 contains the pinout for the LSI53C1010R.

Table 9 456-Ball Alphabetical Signal List LSI53C1010R

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
ACK64/	AB20	AD45	T25	A_SD5+	R2	B_SATN+	D13	B_SREQ+	C18
AD0	AC21	AD46	T23	A_SD6-	T5	B_SBSY-	A15	B_SRST-	E15
AD1	AE23	AD47	T22	A_SD6+	R5	B_SBSY+	B15	B_SRST+	A16
AD2	AC20	AD48	U25	A_SD7-	R4	B_SCD-	E16	B_SSEL-	B17
AD3	AF24	AD49	U23	A_SD7+	P3	B_SCD+	D17	B_SSEL+	C17
AD4	AD21	AD50	W26	A_SD8-	H1	B_SD0-	B8	B_VDDBIAS	B13
AD5	AB19	AD51	V25	A_SD8+	H2	B_SD0+	A8	C_BE0/	AE21
AD6	AE22	AD52	U24	A_SD9-	J4	B_SD1-	D9	C_BE1/	AE18
AD7	AF23	AD53	V23	A_SD9+	H4	B_SD1+	B9	C_BE2/	AB14
AD8	AC19	AD54	V24	A_SD10-	G2	B_SD2-	C9	C_BE3/	AB13
AD9	AE20	AD55	U22	A_SD10+	G1	B_SD2+	E10	C_BE4/	AD26
AD10	AF20	AD56	V22	A_SD11-	F2	B_SD3-	D10	C_BE5/	Y23
AD11	AB18	AD57	Y26	A_SD11+	D1	B_SD3+	E11	C_BE6/	AC25
AD12	AB17	AD58	Y25	A_SD12-	AD1	B_SD4-	B10	C_BE7/	AA23
AD13	AC18	AD59	W23	A_SD12+	AC1	B_SD4+	C10	CLK	AC9
AD14	AE19	AD60	AA25	A_SD13-	AB2	B_SD5-	B11	DEVSEL/	AC16
AD15	AD17	AD61	AC26	A_SD13+	AA3	B_SD5+	D11	ENABLE66	AC2
AD16	AC14	AD62	AB25	A_SD14-	AA2	B_SD6-	A12	FRAME/	AB15
AD17	AC15	AD63	W22	A_SD14+	Y2	B_SD6+	B12	GNT/	AE8
AD18	AE14	A_DIFFSENS	E2	A_SD15-	Y1	B_SD7-	E13	IDDTN	Y4
AD19	AF16	A_GPIO0	H26	A_SD15+	W5	B_SD7+	E12	IDSEL	AC13
AD20	AF11	A_GPIO1	J25	A_SDP0-	P4	B_SD8-	A19	INTA/	AC8
AD21	AE13	A_GPIO2	K24	A_SDP0+	P5	B_SD8+	B19	INTB/	AE7
AD22	AD13	A_GPIO3	H25	A_SDP1-	W2	B_SD9-	E18	IRDY/	AE15
AD23	AC12	A_GPIO4	J23	A_SDP1+	W1	B_SD9+	A20	M66EN	AC5
AD24	AB12	ALT_INTA/	AF7	A_SIO-	K5	B_SD10-	D19	MAD0	G22
AD25	AE12	ALT_INTB/	AB9	A_SIO+	J5	B_SD10+	B20	MAD1	F23
AD26	AE11	A_SACK-	M5	A_SMSG-	L2	B_SD11-	B21	MAD2	D25
AD27	AC11	A_SACK+	L5	A_SMSG+	L1	B_SD11+	A23	MAD3	G23
AD28	AB11	A_SATN-	M4	A_SREQ-	J2	B_SD12-	A3	MAD4	F24
AD29	AE10	A_SATN+	N5	A_SREQ+	J3	B_SD12+	A4	MAD5	H22
AD30	AF8	A_SBSY-	N3	A_SRST-	M1	B_SD13-	C6	MAD6	E25
AD31	AE9	A_SBSY+	N4	A_SRST+	M2	B_SD13+	B5	MAD7	D26
AD32	N24	A_SCD-	K3	A_SSEL-	L4	B_SD14-	E8	MAS0/	K22
AD33	N25	A_SCD+	K4	A_SSEL+	K2	B_SD14+	B6	MAS1/	J24
AD34	L26	A_SD0-	W4	A_VDDBIAS	T1	B_SD15-	D8	MCE/	G25
AD35	M26	A_SD0+	V3	B_DIFFSENS	B22	B_SD15+	B7	MOE/	G26
AD36	R26	A_SD1-	V4	B_GPIO0	M25	B_SDP0-	D12	MWE/	H23
AD37	T26	A_SD1+	V5	B_GPIO1	L25	B_SDP0+	C13	NC[1]	A24
AD38	P25	A_SD2-	V2	B_GPIO2	L23	B_SDP1-	A7	NC	B2
AD39	P24	A_SD2+	U3	B_GPIO3	K25	B_SDP1+	E9	NC	B3
AD40	R23	A_SD3-	U5	B_GPIO4	K23	B_SIO-	E17	NC	B23
AD41	P23	A_SD3+	U4	B_RBIAS	A11	B_SIO+	D18	NC	B24
AD42	P22	A_SD4-	U2	B_SACK-	D14	B_SMSG-	B16	NC	B25
AD43	R22	A_SD4+	T4	B_SACK+	E14	B_SMSG+	D16	NC	C2
AD44	R25	A_SD5-	T2	B_SATN-	B14	B_SREQ-	B18		

1. NC pins are not connected.

Table 10 456-Ball Alphabetical Signal List LSI53C1010R (Cont.)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
NC[1]	C3	NC	AD2	VDD_IO	F1	VSS_IO	A21	VSS_IO	R12
NC	C5	NC	AD3	VDD_IO	G24	VSS_IO	A25	VSS_IO	R13
NC	C14	NC	AD9	VDD_IO	H3	VSS_IO	B1	VSS_IO	R14
NC	C22	NC	AD14	VDD_IO	J26	VSS_IO	B26	VSS_IO	R15
NC	C24	NC	AD18	VDD_IO	K1	VSS_IO	C4	VSS_IO	R16
NC	C25	NC	AD24	VDD_IO	L24	VSS_IO	C8	VSS_IO	T11
NC	D4	NC	AE5	VDD_IO	M3	VSS_IO	C12	VSS_IO	T12
NC	D5	NC	AE6	VDD_IO	N26	VSS_IO	C16	VSS_IO	T13
NC	D15	NC	AE25	VDD_IO	P1	VSS_IO	C20	VSS_IO	T14
NC	D20	NC	AF4	VDD_IO	R24	VSS_IO	D24	VSS_IO	T15
NC	D21	NC	AF12	VDD_IO	T3	VSS_IO	E1	VSS_IO	T16
NC	D22	NC	AF15	VDD_IO	U26	VSS_IO	F26	VSS_IO	T24
NC	D23	PAR	AF19	VDD_IO	V1	VSS_IO	G3	VSS_IO	U1
NC	E3	PAR64	AA24	VDD_IO	W24	VSS_IO	H24	VSS_IO	V26
NC	E4	PERR/	AE17	VDD_IO	Y3	VSS_IO	J1	VSS_IO	W3
NC	E5	REQ/	AD10	VDD_IO	AA26	VSS_IO	K26	VSS_IO	Y24
NC	E6	REQ64/	AD22	VDD_IO	AB1	VSS_IO	L3	VSS_IO	AA1
NC	E20	RST/	AB10	VDD_IO	AC24	VSS_IO	L11	VSS_IO	AB26
NC	E21	SCAN		VDD_IO	AD4	VSS_IO	L12	VSS_IO	AC3
NC	E22	_MODE	E7	VDD_IO	AD8	VSS_IO	L13	VSS_IO	AD7
NC	E23	SCANEN	N22	VDD_IO	AD12	VSS_IO	L14	VSS_IO	AD11
NC	E24	SCLK	F3	VDD_IO	AD16	VSS_IO	L15	VSS_IO	AD15
NC	F4	SERR/	AC17	VDD_IO	AD20	VSS_IO	L16	VSS_IO	AD19
NC	F5	STOP/	AB16	VDD_IO	AE26	VSS_IO	M11	VSS_IO	AD23
NC	F22	TCK_CHIP	AC6	VDD_IO	AF1	VSS_IO	M12	VSS_IO	AE1
NC	G5	TDI_CHIP	AF3	VDD_IO	AF5	VSS_IO	M13	VSS_IO	AF2
NC	M23	TDO_CHIP	AD6	VDD_IO	AF9	VSS_IO	M14	VSS_IO	AF6
NC	N2	TEST_HSC	D7	VDD_IO	AF13	VSS_IO	M15	VSS_IO	AF10
NC	N23	TMS_CHIP	AE4	VDD_IO	AF17	VSS_IO	M16	VSS_IO	AF14
NC	P2	TRDY/	AE16	VDD_IO	AF21	VSS_IO	M24	VSS_IO	AF18
NC	R1	TST_RST/	AD5	VDD_IO	AF25	VSS_IO	N1	VSS_IO	AF22
NC	W25	VDD_IO	A1	VDDA	C1	VSS_IO	N11	VSS_IO	AF26
NC	Y5	VDD_IO	A2	VDDA	AE2	VSS_IO	N12	VSSA	H5
NC	Y22	VDD_IO	A6	VDDC	D2	VSS_IO	N13	VSSA	AB6
NC	AA4	VDD_IO	A10	VDDC	D6	VSS_IO	N14	VSSC	B4
NC	AA5	VDD_IO	A14	VDDC	E19	VSS_IO	N15	VSSC	C21
NC	AA22	VDD_IO	A18	VDDC	J22	VSS_IO	N16	VSSC	C26
NC	AB3	VDD_IO	A22	VDDC	M22	VSS_IO	P11	VSSC	F25
NC	AB4	VDD_IO	A26	VDDC	AC7	VSS_IO	P12	VSSC	G4
NC	AB5	VDD_IO	C7	VDDC	AD25	VSS_IO	P13	VSSC	L22
NC	AB21	VDD_IO	C11	VDDC	AE3	VSS_IO	P14	VSSC	AB7
NC	AB22	VDD_IO	C15	VDDC	AE24	VSS_IO	P15	VSSC	AB8
NC	AC4	VDD_IO	C19	VSS_IO	A5	VSS_IO	P16	VSSC	AB23
NC	AC10	VDD_IO	C23	VSS_IO	A9	VSS_IO	P26	VSSC	AB24
NC	AC22	VDD_IO	D3	VSS_IO	A13	VSS_IO	R3		
NC	AC23	VDD_IO	E26	VSS_IO	A17	VSS_IO	R11		

1. NC pins are not connected.

15 LSI53C1030 Pinout

Table 11 contains the pinout for the LSI53C1030.

Table 11 456-Ball Alphabetical Signal List LSI53C1030

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
ACK64/	AB20	AD45	T25	A_SD6-	T5	B_SD0-	B8	B_VDDBIAS	B13
AD0	AC21	AD46	T23	A_SD6+	R5	B_SD0+	A8	BWE0/	H23
AD1	AE23	AD47	T22	A_SD7-	R4	B_SD1-	D9	BWE1/	E24
AD2	AC20	AD48	U25	A_SD7+	P3	B_SD1+	B9	C_BE0/	AE21
AD3	AF24	AD49	U23	A_SD8-	H1	B_SD2-	C9	C_BE1/	AE18
AD4	AD21	AD50	W26	A_SD8+	H2	B_SD2+	E10	C_BE2/	AB14
AD5	AB19	AD51	V25	A_SD9-	J4	B_SD3-	D10	C_BE3/	AB13
AD6	AE22	AD52	U24	A_SD9+	H4	B_SD3+	E11	C_BE4/	AD26
AD7	AF23	AD53	V23	A_SD10-	G2	B_SD4-	B10	C_BE5/	Y23
AD8	AC19	AD54	V24	A_SD10+	G1	B_SD4+	C10	C_BE6/	AC25
AD9	AE20	AD55	U22	A_SD11-	F2	B_SD5-	B11	C_BE7/	AA23
AD10	AF20	AD56	V22	A_SD11+	D1	B_SD5+	D11	CLK	AC22
AD11	AB18	AD57	Y26	A_SD12-	AD1	B_SD6-	A12	DEVSEL/	AC16
AD12	AB17	AD58	Y25	A_SD12+	AC1	B_SD6+	B12	DIS_PCI_FSN/	A24
AD13	AC18	AD59	W23	A_SD13-	AB2	B_SD7-	E13	DISSCSIFSN/	AC4
AD14	AE19	AD60	AA25	A_SD13+	AA3	B_SD7+	E12	FLSHALE0/	K22
AD15	AD17	AD61	AC26	A_SD14-	AA2	B_SD8-	A19	FLSHALE1/	J24
AD16	AC14	AD62	AB25	A_SD14+	Y2	B_SD8+	B19	FLSHCE/	G25
AD17	AC15	AD63	W22	A_SD15-	Y1	B_SD9-	E18	FRAME/	AB15
AD18	AE14	A_DIFFSENS	E2	A_SD15+	W5	B_SD9+	A20	CLKMODE_1	AC2
AD19	AF16	ADSC/	D21	A_SDP0-	P4	B_SD10-	D19	GNT/	AE8
AD20	AF11	ADV/	B23	A_SDP0+	P5	B_SD10+	B20	GPIO0	AC23
AD21	AE13	A_LED/	J23	A_SDP1-	W2	B_SD11-	B21	GPIO1	AE25
AD22	AD13	ALT_INTA/	AF7	A_SDP1+	W1	B_SD11+	A23	GPIO2	K24
AD23	AC12	ALT_INTB/	AB9	A_SIO-	K5	B_SD12-	A3	GPIO3	H25
AD24	AB12	A_RBIAS	R1	A_SIO+	J5	B_SD12+	A4	GPIO4	M25
AD25	AE12	A_SACK-	M5	A_SMSG-	L2	B_SD13-	C6	GPIO5	L25
AD26	AE11	A_SACK+	L5	A_SMSG+	L1	B_SD13+	B5	GPIO6	L23
AD27	AC11	A_SATN-	M4	A_SREQ-	J2	B_SD14-	E8	GPIO7	K25
AD28	AB11	A_SATN+	N5	A_SREQ+	J3	B_SD14+	B6	HBLED/	C25
AD29	AE10	A_SBSY-	N3	A_SRST-	M1	B_SD15-	D8	IDDTN	Y4
AD30	AF8	A_SBSY+	N4	A_SRST+	M2	B_SD15+	B7	IDSEL	AC13
AD31	AE9	A_SCD-	K3	A_SSEL-	L4	B_SDP0-	D12	INTA/	AC8
AD32	N24	A_SCD+	K4	A_SSEL+	K2	B_SDP0+	C13	INTB/	AE7
AD33	N25	A_SD0-	W4	A_VDDBIAS	T1	B_SDP1-	A7	IRDY/	AE15
AD34	L26	A_SD0+	V3	B_DIFFSENS	B22	B_SDP1+	E9	M66EN	AC5
AD35	M26	A_SD1-	V4	B_LED/	K23	B_SIO-	E17	MAD0	G22
AD36	R26	A_SD1+	V5	B_RBIAS	A11	B_SIO+	D18	MAD1	F23
AD37	T26	A_SD2-	V2	B_SACK-	D14	B_SMSG-	B16	MAD2	D25
AD38	P25	A_SD2+	U3	B_SACK+	E14	B_SMSG+	D16	MAD3	G23
AD39	P24	A_SD3-	U5	B_SATN-	B14	B_SREQ-	B18	MAD4	F24
AD40	R23	A_SD3+	U4	B_SATN+	D13	B_SREQ+	C18	MAD5	H22
AD41	P23	A_SD4-	U2	B_SBSY-	A15	B_SRST-	E15	MAD6	E25
AD42	P22	A_SD4+	T4	B_SBSY+	B15	B_SRST+	A16	MAD7	D26
AD43	R22	A_SD5-	T2	B_SCD-	E16	B_SSEL-	B17	MAD8	E23
AD44	R25	A_SD5+	R2	B_SCD+	D17	B_SSEL+	C17	MAD9	F22

1. NC pins are not connected.

Table 11 456-Ball Alphabetical Signal List LSI53C1030 (Cont.)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
MAD10	C24	TDI_CHIP	AF3	VDD_IO	T3	VSS_IO	C12	VSS_IO	T12
MAD11	E22	TDI_ICE	AB3	VDD_IO	U26	VSS_IO	C16	VSS_IO	T13
MAD12	D23	TDO_CHIP	AD6	VDD_IO	V1	VSS_IO	C20	VSS_IO	T14
MAD13	B25	TDO_ICE	AD2	VDD_IO	W24	VSS_IO	D24	VSS_IO	T15
MAD14	E21	TESTCLKEN	D7	VDD_IO	Y3	VSS_IO	E1	VSS_IO	T16
MAD15	D22	SCANMODE	E7	VDD_IO	AA26	VSS_IO	F26	VSS_IO	T24
MADP0	B24	TMS_CHIP	AE4	VDD_IO	AB1	VSS_IO	G3	VSS_IO	U1
MADP1	C22	TMS_ICE	Y5	VDD_IO	AC24	VSS_IO	H24	VSS_IO	V26
MCLK	E20	TRACECLK	B3	VDD_IO	AD4	VSS_IO	J1	VSS_IO	W3
MOE/	G26	TRACEPKT0	D4	VDD_IO	AD8	VSS_IO	K26	VSS_IO	Y24
TESTACLK	AB6	TRACEPKT1	B2	VDD_IO	AD12	VSS_IO	L3	VSS_IO	AA1
NC[1]	N23	TRACEPKT2	F5	VDD_IO	AD16	VSS_IO	L11	VSS_IO	AB26
NC	AC9	TRACEPKT3	E4	VDD_IO	AD20	VSS_IO	L12	VSS_IO	AC3
TESTHCLK	AE2	TRACEPKT4	C2	VDD_IO	AE26	VSS_IO	L13	VSS_IO	AD7
PAR	AF19	TRACEPKT5	E3	VDD_IO	AF1	VSS_IO	L14	VSS_IO	AD11
PAR64	AA24	TRACEPKT6	G5	VDD_IO	AF5	VSS_IO	L15	VSS_IO	AD15
PCI5VBIASa	AD9	TRACEPKT7	F4	VDD_IO	AF9	VSS_IO	L16	VSS_IO	AD19
PCI5VBIASb	AE6	TRACESYNC	E5	VDD_IO	AF13	VSS_IO	M11	VSS_IO	AD23
PCI5VBIASc	AC10	TRDY/	AE16	VDD_IO	AF17	VSS_IO	M12	VSS_IO	AE1
PCI5VBIASd	AF12	TRST_ICE	AB4	VDD_IO	AF21	VSS_IO	M13	VSS_IO	AF2
PCI5VBIASe	AD18	TST_RST/	AD5	VDD_IO	AF25	VSS_IO	M14	VSS_IO	AF6
PCI5VBIASf	AB22	VDD_IO	A1	VDDA	C1	VSS_IO	M15	VSS_IO	AF10
PCI5VBIASg	Y22	VDD_IO	A2	VDDA	AB21	VSS_IO	M16	VSS_IO	AF14
PCI5VBIASh	W25	VDD_IO	A6	VDDC	D2	VSS_IO	M24	VSS_IO	AF18
PCI5VBIASi	M23	VDD_IO	A10	VDDC	D6	VSS_IO	N1	VSS_IO	AF22
PERR/	AE17	VDD_IO	A14	VDDC	D15	VSS_IO	N11	VSS_IO	AF26
PIPESTAT0	D5	VDD_IO	A18	VDDC	E19	VSS_IO	N12	VSSA	H5
PIPESTAT1	E6	VDD_IO	A22	VDDC	J22	VSS_IO	N13	VSSA	AD24
PIPESTAT2	C3	VDD_IO	A26	VDDC	M22	VSS_IO	N14	VSSC	B4
PVT1	AE5	VDD_IO	C7	VDDC	N2	VSS_IO	N15	VSSC	C14
PVT2	AF4	VDD_IO	C11	VDDC	AC7	VSS_IO	N16	VSSC	C21
RAMCE/	D20	VDD_IO	C15	VDDC	AD3	VSS_IO	P11	VSSC	C26
REQ/	AD10	VDD_IO	C19	VDDC	AD25	VSS_IO	P12	VSSC	F25
REQ64/	AD22	VDD_IO	C23	VDDC	AE3	VSS_IO	P13	VSSC	G4
RST/	AB10	VDD_IO	D3	VDDC	AE24	VSS_IO	P14	VSSC	L22
RTCK_ICE	AA5	VDD_IO	E26	VDDC	AF15	VSS_IO	P15	VSSC	P2
CLKMODE_0	AA22	VDD_IO	F1	VSS_IO	A5	VSS_IO	P16	VSSC	AB5
SCANEN	N22	VDD_IO	G24	VSS_IO	A9	VSS_IO	P26	VSSC	AB7
SCLK	F3	VDD_IO	H3	VSS_IO	A13	VSS_IO	R3	VSSC	AB8
SerialCLK	J25	VDD_IO	J26	VSS_IO	A17	VSS_IO	R11	VSSC	AB23
SerialDATA	H26	VDD_IO	K1	VSS_IO	A21	VSS_IO	R12	VSSC	AB24
SERR/	AC17	VDD_IO	L24	VSS_IO	A25	VSS_IO	R13	VSSC	AD14
TN	C5	VDD_IO	M3	VSS_IO	B1	VSS_IO	R14		
STOP/	AB16	VDD_IO	N26	VSS_IO	B26	VSS_IO	R15		
TCK_CHIP	AC6	VDD_IO	P1	VSS_IO	C4	VSS_IO	R16		
TCK_ICE	AA4	VDD_IO	R24	VSS_IO	C8	VSS_IO	T11		

1. NC pins are not connected.

16 LSI53C1000R Pinout

Table 12 contains the pinout for the LSI53C1000R.

Table 12 456-Ball Alphabetical Signal List LSI53C1000R

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
ACK64/	AB20	AD45	T25	M66EN	AC5	NC	B25	NC	E18
AD0	AC21	AD46	T23	MAD0	G22	NC	C2	NC	E20
AD1	AE23	AD47	T22	MAD1	F23	NC	C3	NC	E21
AD2	AC20	AD48	U25	MAD2	D25	NC	C5	NC	E22
AD3	AF24	AD49	U23	MAD3	G23	NC	C6	NC	E23
AD4	AD21	AD50	W26	MAD4	F24	NC	C9	NC	E24
AD5	AB19	AD51	V25	MAD5	H22	NC	C10	NC	F4
AD6	AE22	AD52	U24	MAD6	E25	NC	C13	NC	F5
AD7	AF23	AD53	V23	MAD7	D26	NC	C14	NC	F22
AD8	AC19	AD54	V24	MAS0/	K22	NC	C17	NC	G5
AD9	AE20	AD55	U22	MAS1/	J24	NC	C18	NC	K23
AD10	AF20	AD56	V22	MCE/	G25	NC	C22	NC	K25
AD11	AB18	AD57	Y26	MOE/	G26	NC	C24	NC	L23
AD12	AB17	AD58	Y25	MWE/	H23	NC	C25	NC	L25
AD13	AC18	AD59	W23	NC[1]	A3	NC	D4	NC	M23
AD14	AE19	AD60	AA25	NC	A4	NC	D5	NC	M25
AD15	AD17	AD61	AC26	NC	A7	NC	D8	NC	N2
AD16	AC14	AD62	AB25	NC	A8	NC	D9	NC	N23
AD17	AC15	AD63	W22	NC	A12	NC	D10	NC	P2
AD18	AE14	ALT_INTA/	AF7	NC	A15	NC	D11	NC	R1
AD19	AF16	A_VDDBIAS	T1	NC	A16	NC	D12	NC	W25
AD20	AF11	B_RBIAS	A11	NC	A19	NC	D13	NC	Y5
AD21	AE13	B_VDDBIAS	B13	NC	A20	NC	D14	NC	Y22
AD22	AD13	C_BE0/	AE21	NC	A23	NC	D15	NC	AA4
AD23	AC12	C_BE1/	AE18	NC	A24	NC	D16	NC	AA5
AD24	AB12	C_BE2/	AB14	NC	B2	NC	D17	NC	AA22
AD25	AE12	C_BE3/	AB13	NC	B3	NC	D18	NC	AB3
AD26	AE11	C_BE4/	AD26	NC	B5	NC	D19	NC	AB4
AD27	AC11	C_BE5/	Y23	NC	B6	NC	D20	NC	AB5
AD28	AB11	C_BE6/	AC25	NC	B7	NC	D21	NC	AB9
AD29	AE10	C_BE7/	AA23	NC	B8	NC	D22	NC	AB21
AD30	AF8	CLK	AC9	NC	B9	NC	D23	NC	AB22
AD31	AE9	DEVSEL/	AC16	NC	B10	NC	E3	NC	AC4
AD32	N24	DIFFSENS	E2	NC	B11	NC	E4	NC	AC10
AD33	N25	ENABLE66	AC2	NC	B12	NC	E5	NC	AC22
AD34	L26	FRAME/	AB15	NC	B14	NC	E6	NC	AC23
AD35	M26	GNT/	AE8	NC	B15	NC	E8	NC	AD2
AD36	R26	GPIO0	H26	NC	B16	NC	E9	NC	AD3
AD37	T26	GPIO1	J25	NC	B17	NC	E10	NC	AD9
AD38	P25	GPIO2	K24	NC	B18	NC	E11	NC	AD14
AD39	P24	GPIO3	H25	NC	B19	NC	E12	NC	AD18
AD40	R23	GPIO4	J23	NC	B20	NC	E13	NC	AD24
AD41	P23	IDDTN	Y4	NC	B21	NC	E14	NC	AE5
AD42	P22	IDSEL	AC13	NC	B22	NC	E15	NC	AE6
AD43	R22	INTA/	AC8	NC	B23	NC	E16	NC	AE7
AD44	R25	IRDY/	AE15	NC	B24	NC	E17		

1. NC pins are not connected.

Table 12 456-Ball Alphabetical Signal List LSI53C1000R (Cont.)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
NC[1]	AE25	SD12-	AD1	VDD_IO	F1	VSS_IO	A21	VSS_IO	R12
NC	AF4	SD12+	AC1	VDD_IO	G24	VSS_IO	A25	VSS_IO	R13
NC	AF12	SD13-	AB2	VDD_IO	H3	VSS_IO	B1	VSS_IO	R14
NC	AF15	SD13+	AA3	VDD_IO	J26	VSS_IO	B26	VSS_IO	R15
PAR	AF19	SD14-	AA2	VDD_IO	K1	VSS_IO	C4	VSS_IO	R16
PAR64	AA24	SD14+	Y2	VDD_IO	L24	VSS_IO	C8	VSS_IO	T11
PERR/	AE17	SD15-	Y1	VDD_IO	M3	VSS_IO	C12	VSS_IO	T12
REQ/	AD10	SD15+	W5	VDD_IO	N26	VSS_IO	C16	VSS_IO	T13
REQ64/	AD22	SDP0-	P4	VDD_IO	P1	VSS_IO	C20	VSS_IO	T14
RST/	AB10	SDP0+	P5	VDD_IO	R24	VSS_IO	D24	VSS_IO	T15
SACK-	M5	SDP1-	W2	VDD_IO	T3	VSS_IO	E1	VSS_IO	T16
SACK+	L5	SDP1+	W1	VDD_IO	U26	VSS_IO	F26	VSS_IO	T24
SATN-	M4	SERR/	AC17	VDD_IO	V1	VSS_IO	G3	VSS_IO	U1
SATN+	N5	SIO-	K5	VDD_IO	W24	VSS_IO	H24	VSS_IO	V26
SBSY-	N3	SIO+	J5	VDD_IO	Y3	VSS_IO	J1	VSS_IO	W3
SBSY+	N4	SMSG-	L2	VDD_IO	AA26	VSS_IO	K26	VSS_IO	Y24
SCAN		SMSG+	L1	VDD_IO	AB1	VSS_IO	L3	VSS_IO	AA1
_MODE	E7	SREQ-	J2	VDD_IO	AC24	VSS_IO	L11	VSS_IO	AB26
SCANEN	N22	SREQ+	J3	VDD_IO	AD4	VSS_IO	L12	VSS_IO	AC3
SCD-	K3	SRST-	M1	VDD_IO	AD8	VSS_IO	L13	VSS_IO	AD7
SCD+	K4	SRST+	M2	VDD_IO	AD12	VSS_IO	L14	VSS_IO	AD11
SCLK	F3	SSEL-	L4	VDD_IO	AD16	VSS_IO	L15	VSS_IO	AD15
SD0-	W4	SSEL+	K2	VDD_IO	AD20	VSS_IO	L16	VSS_IO	AD19
SD0+	V3	STOP/	AB16	VDD_IO	AE26	VSS_IO	M11	VSS_IO	AD23
SD1-	V4	TCK_CHIP	AC6	VDD_IO	AF1	VSS_IO	M12	VSS_IO	AE1
SD1+	V5	TDI_CHIP	AF3	VDD_IO	AF5	VSS_IO	M13	VSS_IO	AF2
SD2-	V2	TDO_CHIP	AD6	VDD_IO	AF9	VSS_IO	M14	VSS_IO	AF6
SD2+	U3	TEST_HSC	D7	VDD_IO	AF13	VSS_IO	M15	VSS_IO	AF10
SD3-	U5	TMS_CHIP	AE4	VDD_IO	AF17	VSS_IO	M16	VSS_IO	AF14
SD3+	U4	TRDY/	AE16	VDD_IO	AF21	VSS_IO	M24	VSS_IO	AF18
SD4-	U2	TST_RST/	AD5	VDD_IO	AF25	VSS_IO	N1	VSS_IO	AF22
SD4+	T4	VDD_IO	A1	VDDA	C1	VSS_IO	N11	VSS_IO	AF26
SD5-	T2	VDD_IO	A2	VDDA	AE2	VSS_IO	N12	VSSA	H5
SD5+	R2	VDD_IO	A6	VDDC	D2	VSS_IO	N13	VSSA	AB6
SD6-	T5	VDD_IO	A10	VDDC	D6	VSS_IO	N14	VSSC	B4
SD6+	R5	VDD_IO	A14	VDDC	E19	VSS_IO	M15	VSSC	C21
SD7-	R4	VDD_IO	A18	VDDC	J22	VSS_IO	N16	VSSC	C26
SD7+	P3	VDD_IO	A22	VDDC	M22	VSS_IO	P11	VSSC	F25
SD8-	H1	VDD_IO	A26	VDDC	AC7	VSS_IO	P12	VSSC	G4
SD8+	H2	VDD_IO	C7	VDDC	AD25	VSS_IO	P13	VSSC	L22
SD9-	J4	VDD_IO	C11	VDDC	AE3	VSS_IO	P14	VSSC	AB7
SD9+	H4	VDD_IO	C15	VDDC	AE24	VSS_IO	P15	VSSC	AB8
SD10-	G2	VDD_IO	C19	VSS_IO	A5	VSS_IO	P16	VSSC	AB23
SD10+	G1	VDD_IO	C23	VSS_IO	A9	VSS_IO	P26	VSSC	AB24
SD11-	F2	VDD_IO	D3	VSS_IO	A13	VSS_IO	R3		
SD11+	D1	VDD_IO	E26	VSS_IO	A17	VSS_IO	R11		

1. NC pins are not connected.

17 LSI53C1020 Pinout

Table 13 contains the pinout for the LSI53C1020.

Table 13 LSI53C1020 Signal List by Signal Name

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
ACK64/	AB20	AD45	T25	FLSHALE1/	J24	NC	A19	NC	E15
AD0	AC21	AD46	T23	FLSHCE/	G25	NC	A20	NC	E16
AD1	AE23	AD47	T22	FRAME/	AB15	NC	A23	NC	E17
AD2	AC20	AD48	U25	GNT/	AE8	NC	A24	NC	E18
AD3	AF24	AD49	U23	GPIO0	AC23	NC	B5	NC	N23
AD4	AD21	AD50	W26	GPIO1	AE25	NC	B6	NC	AB9
AD5	AB19	AD51	V25	GPIO2	K24	NC	B7	NC	AC9
AD6	AE22	AD52	U24	GPIO3	H25	NC	B8	NC	AE7
AD7	AF23	AD53	V23	GPIO4	M25	NC	B9	PAR	AF19
AD8	AC19	AD54	V24	GPIO5	L25	NC	B10	PAR64	AA24
AD9	AE20	AD55	U22	GPIO6	L23	NC	B11	PCI5VBIAS	AD9
AD10	AF20	AD56	V22	GPIO7	K25	NC	B12	PCI5VBIAS	AE6
AD11	AB18	AD57	Y26	HB_LED/	C25	NC	B13	PCI5VBIAS	AC10
AD12	AB17	AD58	Y25	IDDTN	Y4	NC	B14	PCI5VBIAS	AF12
AD13	AC18	AD59	W23	IDSEL	AC13	NC	B15	PCI5VBIAS	AD18
AD14	AE19	AD60	AA25	INTA/	AC8	NC	B16	PCI5VBIAS	AB22
AD15	AD17	AD61	AC26	IRDY/	AE15	NC	B17	PCI5VBIAS	Y22
AD16	AC14	AD62	AB25	M66EN	AC5	NC	B18	PCI5VBIAS	W25
AD17	AC15	AD63	W22	MAD0	G22	NC	B19	PCI5VBIAS	M23
AD18	AE14	ADSC/	D21	MAD1	F23	NC	B20	PERR/	AE17
AD19	AF16	ADV/	B23	MAD2	D25	NC	B21	PIPESTAT0	D5
AD20	AF11	ALT_INTA/	AF7	MAD3	G23	NC	B22	PIPESTAT1	E6
AD21	AE13	A_LED/	J23	MAD4	F24	NC	C6	PIPESTAT2	C3
AD22	AD13	A_RBIAS	R1	MAD5	H22	NC	C9	PVT1	AE5
AD23	AC12	A_VDDBIAS	T1	MAD6	E25	NC	C10	PVT2	AF4
AD24	AB12	B_LED/	K23	MAD7	D26	NC	C13	RAMCE/	D20
AD25	AE12	BWE0/	H23	MAD8	E23	NC	C17	REQ/	AD10
AD26	AE11	BWE1/	E24	MAD9	F22	NC	C18	REQ64/	AD22
AD27	AC11	C_BE0/	AE21	MAD10	C24	NC	D8	RST/	AB10
AD28	AB11	C_BE1/	AE18	MAD11	E22	NC	D9	RTCK_ICE	AA5
AD29	AE10	C_BE2/	AB14	MAD12	D23	NC	D10	SACK-	M5
AD30	AF8	C_BE3/	AB13	MAD13	B25	NC	D11	SACK+	L5
AD31	AE9	C_BE4/	AD26	MAD14	E21	NC	D12	SATN-	M4
AD32	N24	C_BE5/	Y23	MAD15	D22	NC	D13	SATN+	N5
AD33	N25	C_BE6/	AC25	MADP0	B24	NC	D14	SBSY-	N3
AD34	L26	C_BE7/	AA23	MADP1	C22	NC	D16	SBSY+	N4
AD35	M26	CLK	AC22	MCLK	E20	NC	D17	SCANEN	N22
AD36	R26	CLK		MOE/	G26	NC	D18	SCANMODE	E7
AD37	T26	MODE_0	AA22	NC[1]	A3	NC	D19	SCD-	K3
AD38	P25	CLK		NC	A4	NC	E8	SCD+	K4
AD39	P24	MODE_1	AC2	NC	A7	NC	E9	SCLK	F3
AD40	R23	DEVSEL/	AC16	NC	A8	NC	E10	SD0-	W4
AD41	P23	DIFFSENS	E2	NC	A11	NC	E11	SD0+	V3
AD42	P22	DIS_		NC	A12	NC	E12	SD1-	V4
AD43	R22	SCSI_FSN/	AC4	NC	A15	NC	E13	SD1+	V5
AD44	R25	FLSHALE0/	K22	NC	A16	NC	E14	SD2-	V2

1. NC pins are not connected.

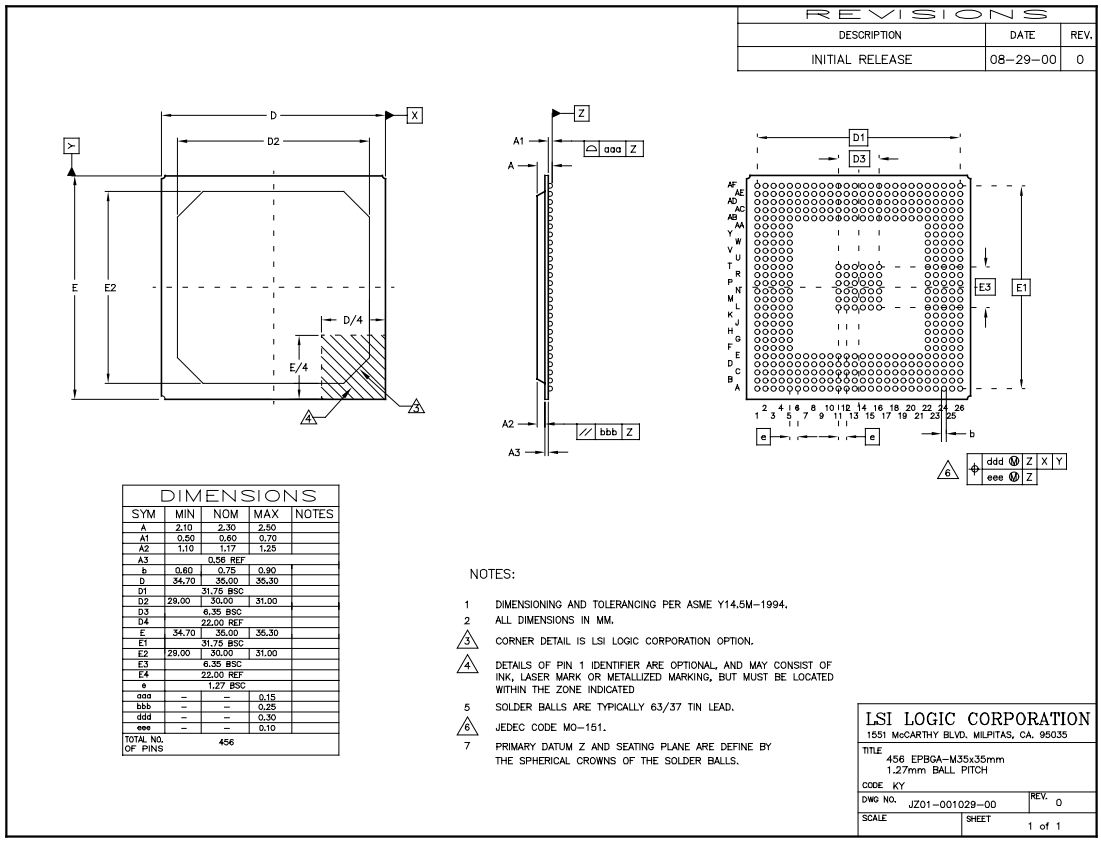
Table 13 LSI53C1020 Signal List by Signal Name (Cont.)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
SD2+	U3	TCK_ICE	AA4	VDD_IO	N26	VSS_IO	B26	VSS_IO	R15
SD3-	U5	TDI_CHIP	AF3	VDD_IO	P1	VSS_IO	C4	VSS_IO	R16
SD3+	U4	TDI_ICE	AB3	VDD_IO	R24	VSS_IO	C8	VSS_IO	T11
SD4-	U2	TDO_CHIP	AD6	VDD_IO	T3	VSS_IO	C12	VSS_IO	T12
SD4+	T4	TDO_ICE	AD2	VDD_IO	U26	VSS_IO	C16	VSS_IO	T13
SD5-	T2	TESTACLK	AB6	VDD_IO	V1	VSS_IO	C20	VSS_IO	T14
SD5+	R2	TESTCLKEN	D7	VDD_IO	W24	VSS_IO	D24	VSS_IO	T15
SD6-	T5	TESTHCLK	AE2	VDD_IO	Y3	VSS_IO	E1	VSS_IO	T16
SD6+	R5	TMS_CHIP	AE4	VDD_IO	AA26	VSS_IO	F26	VSS_IO	T24
SD7-	R4	TMS_ICE	Y5	VDD_IO	AB1	VSS_IO	G3	VSS_IO	U1
SD7+	P3	TN	C5	VDD_IO	AC24	VSS_IO	H24	VSS_IO	V26
SD8-	H1	TRACECLK	B3	VDD_IO	AD4	VSS_IO	J1	VSS_IO	W3
SD8+	H2	TRACEPKT0	D4	VDD_IO	AD8	VSS_IO	K26	VSS_IO	Y24
SD9-	J4	TRACEPKT1	B2	VDD_IO	AD12	VSS_IO	L3	VSS_IO	AA1
SD9+	H4	TRACEPKT2	F5	VDD_IO	AD16	VSS_IO	L11	VSS_IO	AB26
SD10-	G2	TRACEPKT3	E4	VDD_IO	AD20	VSS_IO	L12	VSS_IO	AC3
SD10+	G1	TRACEPKT4	C2	VDD_IO	AE26	VSS_IO	L13	VSS_IO	AD7
SD11-	F2	TRACEPKT5	E3	VDD_IO	AF1	VSS_IO	L14	VSS_IO	AD11
SD11+	D1	TRACEPKT6	G5	VDD_IO	AF5	VSS_IO	L15	VSS_IO	AD15
SD12-	AD1	TRACEPKT7	F4	VDD_IO	AF9	VSS_IO	L16	VSS_IO	AD19
SD12+	AC1	TRACESYNC	E5	VDD_IO	AF13	VSS_IO	M11	VSS_IO	AD23
SD13-	AB2	TRDY/	AE16	VDD_IO	AF17	VSS_IO	M12	VSS_IO	AE1
SD13+	AA3	TRST_ICE	AB4	VDD_IO	AF21	VSS_IO	M13	VSS_IO	AF2
SD14-	AA2	TST_RST/	AD5	VDD_IO	AF25	VSS_IO	M14	VSS_IO	AF6
SD14+	Y2	VDD_IO	A1	VDDA	C1	VSS_IO	M15	VSS_IO	AF10
SD15-	Y1	VDD_IO	A2	VDDA	AB21	VSS_IO	M16	VSS_IO	AF14
SD15+	W5	VDD_IO	A6	VDDC	D2	VSS_IO	M24	VSS_IO	AF18
SDP0-	P4	VDD_IO	A10	VDDC	D6	VSS_IO	N1	VSS_IO	AF22
SDP0+	P5	VDD_IO	A14	VDDC	D15	VSS_IO	N11	VSS_IO	AF26
SDP1-	W2	VDD_IO	A18	VDDC	E19	VSS_IO	N12	VSSA	H5
SDP1+	W1	VDD_IO	A22	VDDC	J22	VSS_IO	N13	VSSA	AD24
SerialCLK	J25	VDD_IO	A26	VDDC	M22	VSS_IO	N14	VSSC	B4
SerialDATA	H26	VDD_IO	C7	VDDC	N2	VSS_IO	N15	VSSC	C14
SERR/	AC17	VDD_IO	C11	VDDC	AC7	VSS_IO	N16	VSSC	C21
SIO-	K5	VDD_IO	C15	VDDC	AD3	VSS_IO	P11	VSSC	C26
SIO+	J5	VDD_IO	C19	VDDC	AD25	VSS_IO	P12	VSSC	F25
SMSG-	L2	VDD_IO	C23	VDDC	AE3	VSS_IO	P13	VSSC	G4
SMSG+	L1	VDD_IO	D3	VDDC	AE24	VSS_IO	P14	VSSC	L22
SREQ-	J2	VDD_IO	E26	VDDC	AF15	VSS_IO	P15	VSSC	P2
SREQ+	J3	VDD_IO	F1	VSS_IO	A5	VSS_IO	P16	VSSC	AB5
SRST-	M1	VDD_IO	G24	VSS_IO	A9	VSS_IO	P26	VSSC	AB7
SRST+	M2	VDD_IO	H3	VSS_IO	A13	VSS_IO	R3	VSSC	AB8
SSEL-	L4	VDD_IO	J26	VSS_IO	A17	VSS_IO	R11	VSSC	AB23
SSEL+	K2	VDD_IO	K1	VSS_IO	A21	VSS_IO	R12	VSSC	AB24
STOP/	AB16	VDD_IO	L24	VSS_IO	A25	VSS_IO	R13	VSSC	AD14
TCK_CHIP	AC6	VDD_IO	M3	VSS_IO	B1	VSS_IO	R14		

18 Package Drawing

Figure 6 contains the package drawing for the LSI53C1010R, LSI53C1030, LSI53C1000R, and LSI53C1020.

Figure 6 456-Pin EPBGA (KY) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code KY.**

Notes

Notes

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