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High Voltage Differential Wiring Diagram for SYM53C895, SYM53C895A, SYM53C896, SYM53C897, and SYM53C1510 SCSI I/O Processors (SIOP)

Systems Engineering Note

S11003

This document describes the correct procedure for connecting the SYM53C895, SYM53C895A, SYM53C896, and SYM53C1510 SCSI I/O Processors (SIOP).

At power up the RST+ pin is 3-stated by the SIOP. It is connected to the DE/RE/ pin for RST- on the transceiver. Each of the DE/RE/ pins on the transceiver has a pull-up resistor internal to the chip which is rated at a maximum of 100 µa. This pull-up resistor pulls the RST+ pin to approximately 4 V. RST- is pulled low by the external 1.5 kΩ resistor. The high level on RST+ allows the SIOP to drive RST- onto the SCSI bus, causing a SCSI reset. The reset remains asserted until the DIF bit (bit 5) of the STEST2 register (0x4E) is set.

To prevent the SIOP from asserting SCSI reset at power up and after a software reset, connect the RST+ signal to the transceiver with a pull-down resistor as illustrated in Figure 1. This puts the transceiver in receive mode for the RST- signal thus preventing the SIOP from driving RST- onto the SCSI bus. Similarly, connect all control lines (“ + ” signals) to the transceiver with pull-down resistors of 1.5 kΩ as illustrated in Figure 1 on the next page.

Figure 1 High Voltage Differential Wiring Diagram