TECHNICAL MANUAL

LSI53C140 Ultra2 SCSI Bus Expander

Version 2.1

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LSI LOGIC®

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Preface

This manual provides a description and electrical characteristics of the LSI53C140 Ultra2 SCSI Bus Expander chip that supports all combinations of Single-Ended, Low Voltage Differential, and High Voltage Differential SCSI bus conversions.

Audience

This document assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the processor for possible use in a system
- Engineers who are designing the processor into a system

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Using the LSI53C140**, contains general information about the LSI53C140.
- Chapter 2, **Functional Descriptions**, describes the main functional areas of the chip in more detail, including the interfaces to the SCSI bus and external memory.
- Chapter 3, **LSI53C140 Specifications**, contains the pin diagram, BGA diagram, signal descriptions, electrical characteristics, AC timing diagrams, and mechanical drawing of the LSI53C140.
- Appendix A, **Wiring Diagrams**, contain wiring diagrams that show typical LSI53C140 usage. It also contains an LSI53C140 Differential Mode wiring diagram.

- Appendix B, **Board Design Considerations**, describes LSI53C180 as a drop in replacement for the LSI53C140.
- Appendix C, **Glossary**, contains commonly used terms and their definitions.

Revision Record

Version	Date	Description
0.5	5/98	First draft of complete technical manual.
1.0	6/99	Miscellaneous. changes/corrections for product information
2.0	4/01	All product names changed from a SYM to an LSI prefix. 192-ball BGA information added in Chapter 3. Refer to Appendix B for more detailed information. Updated DC electrical specifications and test conditions.
2.1	9/01	Add differential mode wiring diagram to Appendix A per system engineer.

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end in an “n.”

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Chapter 1
Using the LSI53C140

This chapter describes the LSI53C140 Ultra2 SCSI Bus Expander and its applications. It includes these topics:

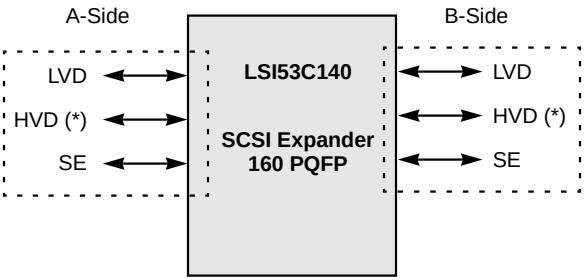
1.1 General Description

The LSI53C140 is a single chip solution allowing the extension of SCSI device connectivity and/or cable length limits. A SCSI bus expander couples bus segments together without any impact to the SCSI protocol, software, or firmware. The LSI53C140 connects Single-Ended (SE) Ultra, Low Voltage Differential (LVD) Ultra2, or High Voltage Differential (HVD) peripherals together in any combination.

The LSI53C140 is capable of supporting any combination of bus mode SE, HVD, or LVD on either the A or B Side port. This provides the system designer with maximum flexibility in designing SCSI backplanes to accommodate any SCSI bus mode.

Figure 1.1 shows the three SCSI bus modes available on the A or B Side. LVDlink™ transceivers provide the multimode LVD, SE, or HVD capability.

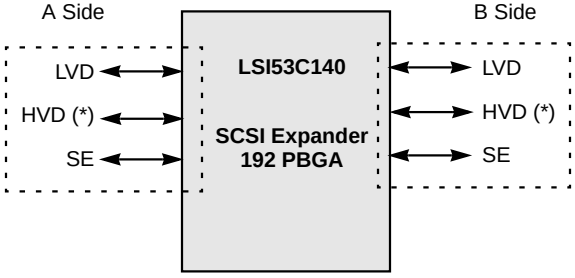
Figure 1.1 LSI53C140 SCSI Bus Modes



* All HVD requires external differential transceivers and terminations.

The LSI53C140 is also capable of supporting any combination of SE or LVD bus mode on either the A or B Side port when using a 192-ball Plastic Ball Grid Array (PBGA) package. Figure 1.1 illustrates the three SCSI bus modes available on the A or B Side.

Figure 1.2 LSI53C140 SCSI Bus Modes



* All HVD requires external differential transceivers and terminations.

Refer to the Board Design Considerations in Appendix B about the LSI53C140 to LSI53C180 as a drop in replacement along with board design information.

The LSI53C140 operates as both an expander and converter. In both SCSI bus expander and converter modes, cable segments are electrically isolated from each other. This feature maintains the signal integrity of each cable segment.

Table 1.1 shows the types of operations for the LSI53C140 160 Plastic Quad Flat Pack (PQFP).

Table 1.1 Types of Operation

Signal Type	Mode	Speed
LVD to LVD	Repeater	Ultra2
HVD to HVD[1]	Repeater	Ultra
SE to SE	Repeater	Ultra
Or any combination above for Repeater.		
LVD to HVD[1]	Converter	Ultra
LVD to SE	Converter	Ultra
HVD[1] to SE	Converter	Ultra
Or any combination above for Converter.		

1. All HVD requires external differential transceivers and terminations.

The LSI53C140 provides additional control capability through the pin level isolation mode (Warm Swap Enable). This feature permits logical disconnection of both the A Side bus and the B Side bus without disrupting SCSI transfers currently in progress. For example, devices on the logically disconnected B Side can be swapped out while the A Side bus remains active.

The LSI53C140 is based on previous bus expander technology resulting in some signal filtering and retiming to maintain signal skew budgets. The LSI53C140 is independent of software.

1.2 Applications

The LSI53C140 supports these applications:

- Server clustering environments
- Expanders creating distinct SCSI cable segments which are electrically isolated from each other

Figure 1.3 shows two LSI53C140 expanders that configure three segments. This configuration allows segments A and B to be treated as a point-to-point segment. Segment C is treated as a load segment with at least 8 inches between every node.

Figure 1.3 LSI53C140 Server Clustering

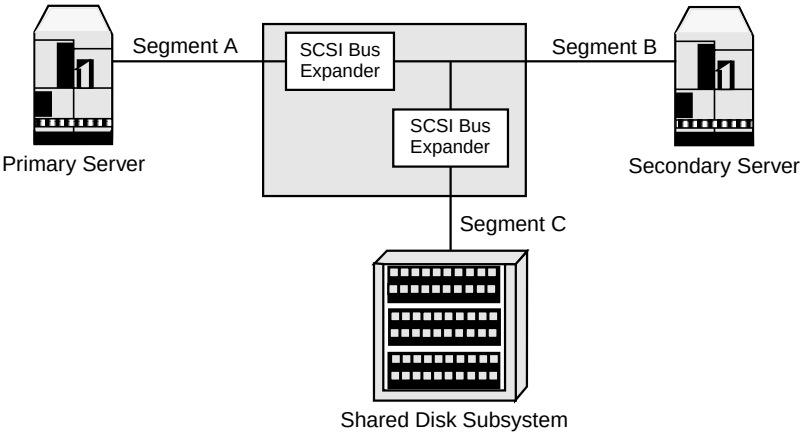


Figure 1.3 demonstrates how SCSI bus expanders are used to couple bus segments together without any impact of the SCSI protocol or software. Configurations that use the LSI53C140 in the Ultra2 mode (LVD to LVD) allow the system designer to take advantage of the inherent cable distance, device connectivity, data reliability, and increased transfer rate benefits of LVD signaling with Ultra2 SCSI peripherals.

Table 1.2 shows the various distance requirements for each SCSI bus mode.

Table 1.2 SCSI Bus Distance Requirements

Segment	Mode	Length Limit
A	LVD (Ultra2)	25 meters
	SE (Ultra)	3 meters[1]
	HVD (Ultra)	25 meters
B	LVD (Ultra2)	12 meters
	SE (Ultra)	1.5 meters
	HVD (Ultra	12 meters
C	LVD (Ultra2)	12 meters
	SE (Ultra)	1.5 meters
	HVD (Ultra)	12 meters

1. The length may be more, possibly 6 meters, as no devices are attached to it.

Figure 1.4 illustrates the cascading of the LSI53C140 to achieve four distinct SCSI segments. Segments A and D can be treated as point-to-point segments. Segments B and C are treated as load segments with at least 8-inch spacing between every node.

Figure 1.4 LSI53C140 SCSI Bus Device

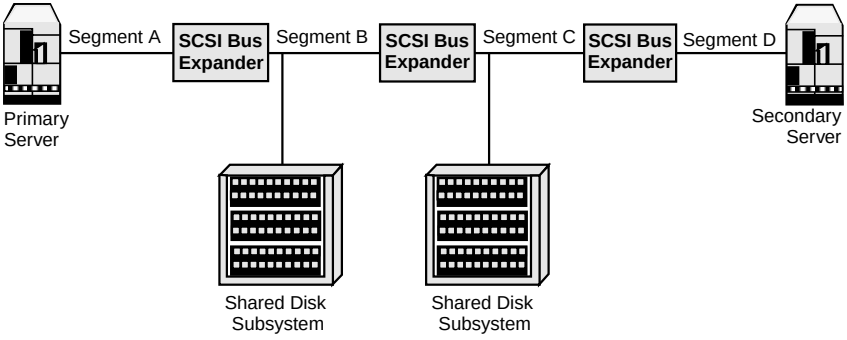


Table 1.3 shows the various distance requirements for each transmission mode.

Table 1.3 Transmission Mode Distance Requirements

Segment	Mode	Length Limit
A, D	LVD (Ultra2)	25 meters
	SE (Ultra)	1.5 meters
	HVD (Ultra)	25 meters
B, C	LVD (Ultra2)	12 meters
	SE (Ultra)	1.5 meters
	HVD (Ultra)	12 meters

1.2.1 Features

The LSI53C140 supports these features:

- Any combination of LVD, SE, or HVD transceivers
- Creates distinct SCSI bus segments that are electrically isolated from each other
- Integrated LVDlink transceivers for direct attachment to either LVD, SE, or HVD bus segments
- Operates as a SCSI Bus Expander
  - LVD to LVD (Ultra2 SCSI)
  - HVD to HVD (Ultra SCSI)
  - SE to SE (Ultra SCSI)
- Operates as a SCSI Bus Converter
  - LVD to HVD (Ultra SCSI)
  - LVD to SE (Ultra SCSI)
  - HVD to SE (Ultra SCSI)
- Targets and initiators may be located on either the A or B Side of the device

- Accepts any asynchronous or synchronous transfer speed up to Ultra2 SCSI (for LVD to LVD mode only)
- Dynamic addition/removal of SCSI bus segments by using the electrical isolation mode
- Does not consume a SCSI ID
- Propagates the RESET/ signal from one side to the other regardless of the SCSI bus state
- Notifies initiator(s) of changes in transmission mode (SE/LVD/HVD) on A or B side segments by using SCSI bus RESET/
- SCSI Busy LED driver for activity indicator
- Up to four LSI53C140s may be cascaded
- Does not require software

1.2.2 Specifications

The LSI53C140 specifications are:

- 40 MHz Input Clock
- 160-pin PQFP
- 192-ball PBGA; This package is a drop in replacement for the LSI53C180 when the design uses the LSI53C180 pinout.
- Compliant with the SCSI Parallel Interface (SPI-2)
- Compliant with SCSI Enhanced Parallel Interface (EPI) Specifications

1.3 Benefits of LVDlink

The LSI53C140 supports LVD technology for SCSI, a signaling technology that increases the reliability of SCSI data transfers over longer distances than those supported by SE SCSI technology. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. LVD provides the reliability of HVD SCSI technology without the added cost of external differential transceivers. LVD allows a longer SCSI cable and more devices on the bus. LVD provides a long-term migration path to even faster SCSI transfer rates without compromising signal integrity, cable length, or connectivity.

For backward compatibility to existing SE devices, the LSI53C140 features multimode LVDlink transceivers that can switch between LVD and SE modes.

Some features of integrated LVDlink Multimode transceivers are:

- Supports SE, LVD, or HVD technology (HVD must have external transceivers)
- Allows greater device connectivity and longer cable length
- LVDlink transceivers save the cost of external differential transceivers
- Supports a long-term performance migration path

Chapter 2
Functional Descriptions

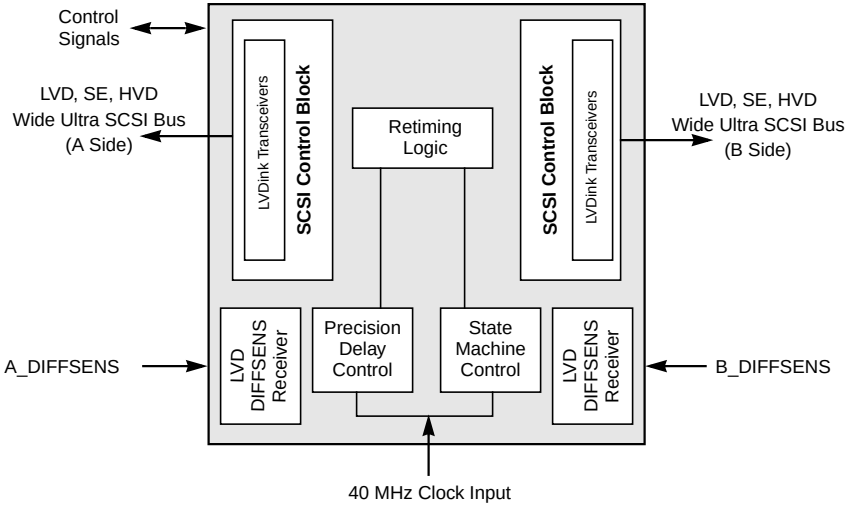
This chapter describes all signals, their groupings, and their functions. It includes these topics:

2.1 Interface Signal Descriptions

The LSI53C140 has no programmable registers, and therefore, no software requirements. SCSI control signals control all LSI53C140 functions. Figure 2.1 shows a block diagram of the LSI53C140 device divided into the following blocks:

- A Side SCSI Control Block
  - LVD, SE, and HVD drivers and receivers
- B Side SCSI Control Block
  - LVD, SE, and HVD drivers and receivers
- Retiming Logic
- Precision Delay Control
- State Machine Control

Figure 2.1 LSI53C140 Block Diagram



In its simplest form, the LSI53C140 passes data and parity from a source bus to a load bus. The side asserting, deasserting, or releasing the SCSI signals is the source side. This model of the LSI53C140 represents pieces of wire that allow corresponding SCSI signals to flow from one side to the other side. The LSI53C140 monitors arbitration and selection by devices on the bus so it can enable the proper drivers to pass the signals along. In addition, the LSI53C140 does signal retiming to maintain the signal skew budget from the source bus to the load bus.

2.1.1 SCSI A Side and B Side Control Blocks

The SCSI A Side pins are connected internally to the corresponding SCSI B Side pins, forming bidirectional connections to the SCSI bus.

In the LVD/LVD mode, the SCSI A Side and B Side control blocks connect to both targets and initiators and accept any asynchronous or synchronous data transfer rates up to the 80 Mbytes/s rate of Wide Ultra2 SCSI. TolerANT® and LVDlink technologies are part of both the A Side and B Side control blocks.

2.1.1.1 LSI53C140 Requirements for Synchronous Negotiation

The LSI53C140 builds a table of information regarding devices on the bus in on-chip RAM. The Synchronous Data Transfer Request (SDTR) and Wide Data Transfer Request (WDTR) information for each device is taken from the MSG bytes during negotiation. For all devices in the configuration to communicate accurately with each other through the LSI53C140 at Ultra2 (Fast-40) rates, it is necessary for a complete synchronous negotiation to take place between the initiator and target(s) prior to any data transfer. On a 16-bit bus, the LSI53C140 at Ultra2 approaches rates of 80 Mbytes/s. The LSI53C140 defaults to Fast-20 rates when a valid negotiation between the initiator and target has not occurred.

2.1.1.2 TolerANT Technology

In the SE mode, the LSI53C140 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven HIGH rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions without the long signal delays associated with RC-type input filters. This improved driver and receiver technology helps eliminate double clocking of data, which is the single biggest reliability issue with SCSI operations.

The benefits of TolerANT technology include increased immunity to noise on the deasserting signal edge, better performance due to balanced duty cycles, and improved SCSI transfer rates. In addition, TolerANT SCSI devices prevent glitches on the SCSI bus at power-up or power-down, so other devices on the bus are also protected from data corruption.

2.1.1.3 LVDlink Technology

To support greater device connectivity and longer SCSI cables, the LSI53C140 features LVDlink technology, the LSI Logic implementation of multimode LVD SCSI. LVDlink transceivers provide the inherent reliability of differential SCSI, and a long-term migration path of faster SCSI transfer rates.

LVDlink technology is based on current drive. Its low output current reduces the power needed to drive the SCSI bus. Therefore, the I/O drivers can be integrated directly onto the chip. This reduces the cost and complexity compared to traditional (high power) differential designs. LVDlink lowers the amplitude of noise reflections and allows higher transmission frequencies.

The LVDlink transceivers in side A and side B operate in the LVD, HVD (external differential transceivers), or SE modes. The LSI53C140 automatically detects the type of signal connected, based on the voltages detected by A_DIFFSENS and B_DIFFSENS.

2.1.2 Retiming Logic

As SCSI signals propagate from one side of the LSI53C140 to the other side, the logic circuits that retime the bus signals process the SCSI signals, as needed. This guarantees or improves the required SCSI timings. The State Machine Controls govern the retiming logic that keeps track of SCSI phases, the location of initiator and target devices, and various timing functions. In addition, the retiming logic contains numerous delay elements that are periodically calibrated by the Precision Delay Control block. This calibration occurs in order to guarantee specified timing such as output pulse widths, setup and hold times, and others.

When a synchronous negotiation takes place between devices, a nexus is formed, and the on-chip RAM stores the corresponding information for that nexus. This information remains in place until a chip reset, power down, or renegotiation occurs. This enables the chips to make more accurate retiming adjustments.

2.1.3 Precision Delay Control

The Precision Delay Control block provides calibration information to the precision delay elements in the retiming logic block in order to maintain precise timing as signals propagate through the device. As the LSI53C140 operating conditions (such as voltage and temperature) vary over time, the Precision Delay Control block periodically updates the delay settings in the retiming logic to maintain constant and precise control over bus timing.

2.1.4 State Machine Control

The State Machine Control keeps track of the SCSI bus phase protocol and other internal operating conditions. This block provides signals to the retiming logic that identify how to properly handle SCSI bus signal retiming and protocol, based on observed bus conditions.

2.1.5 DIFFSENS Receiver

The LSI53C140 contains LVD DIFFSENS receivers that detect the voltage level on the A Side or B Side DIFFSENS lines to inform the LSI53C140 of the transmission mode being used by the SCSI buses. The LVD DIFFSENS receivers are capable of detecting the voltage level of incoming SCSI signals to determine whether it is from an SE, LVD, or HVD device. A device does not change its present signal driver or receiver mode based on the DIFFSENS voltage levels unless a new mode is sensed continuously for at least 100 ms.

Transmission mode detection for SE, LVD, or HVD is accomplished through the use of the DIFFSENS lines. Table 2.1 shows the voltages on the DIFFSENS lines and modes they will cause.

Table 2.1 DIFFSENS Voltage Levels

Voltage	Mode
–0.35 to +0.5	SE
+0.7 to +1.9	LVD
+2.4 to +5.5	HVD

2.1.6 Dynamic Transmission Mode Changes

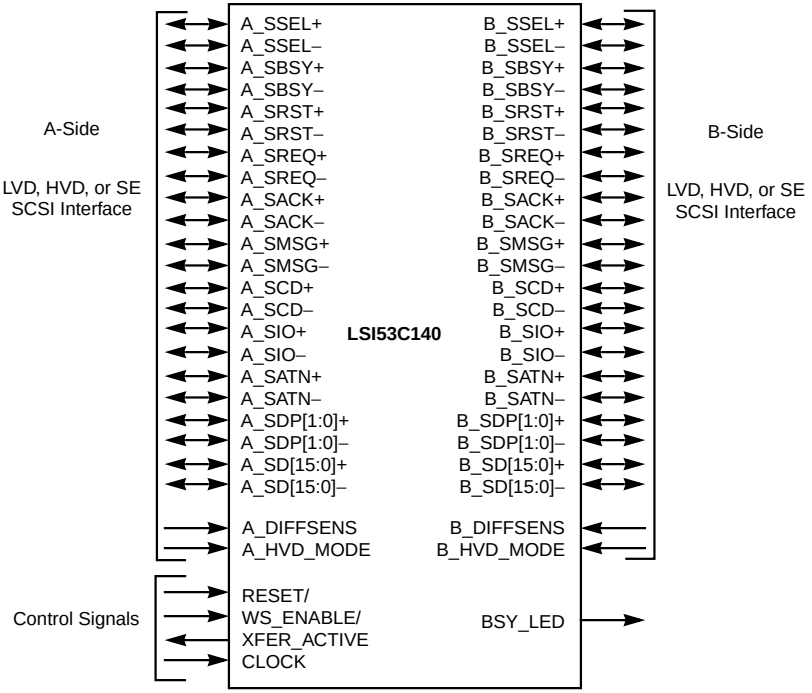
Any dynamic mode change (SE/LVD/HVD) on a bus segment is considered to be a significant event that requires the initiator to determine whether the mode change meets the requirements for that bus segment.

The LSI53C140 supports dynamic transmission mode changes by notifying the initiator(s) of changes in transmission mode (SE/LVD/HVD) on A or B side segments by using SCSI bus RESET. The DIFFSENS line detects a valid mode switch on the bus segments. After the DIFFSENS state is present for 100 ms, the LSI53C140 generates a SCSI reset on the opposite bus from the one that the transmission mode change occurred on. This reset informs any initiators residing on the opposite segment about the change in the transmission mode. Then, the initiator(s) renegotiates synchronous transfer rates with each device on that segment to ensure that there is a valid bus segment for that mode.

2.2 SCSI Signal Descriptions

Figure 2.2 shows the LSI53C140 signal grouping. A description of the signal groups follows. For a description of a specific signal, refer to Section 3.1, “General Description,” in Chapter 3. For information about signal electrical characteristics, refer to Section 3.2, “Electrical Characteristics,” in Chapter 3. For SCSI bus signal timing, see Section 3.2.4, “SCSI Interface Timing,” in Chapter 3.

Figure 2.2 LSI53C140 Signal Grouping



2.2.1 Data and Parity (SD and SDP)

The signals named A_SD[15:0]± and A_SDP[1:0]± are the data and parity signals from the A Side, and B_SD[15:0]± and B_SDP[1:0]± are the data and parity signals from the B Side of the LSI53C140. The LSI53C140 sends and receives these signals by using SCSI compatible drivers and receiver logic designed into the LSI53C140 interfaces. This logic provides the multimode LVD and SE interfaces in the chip. This logic also provides the necessary drive, sense thresholds, and input hysteresis to function correctly in a SCSI bus environment.

The LSI53C140 receives data and parity signals and passes them from the source bus to the load bus and provides any necessary edge shifting to guarantee the skew budget for the load bus. Either side of the LSI53C140 may be the source bus or the load bus. The side that is asserting, deasserting, or releasing the SCSI signals is the source side. These steps describe the LSI53C140 data processing:

1. The receiver logic accepts the asserted data as soon as it is received. Once the clock signal has been received, data is gated from the receiver latch.
2. The path is next tested to ensure the signal, if being driven by the LSI53C140, is not misinterpreted as an incoming signal.
3. The data is then leading edge filtered. The assertion edge is held for a specified time to prevent any signal bounce. The input signal controls the duration.
4. The next stage uses a latch to sample the signal. This provides a stable data window for the load bus.
5. The final step develops pull-up and pull-down controls for the SCSI I/O logic, including 3-state controls for the pull-up.
6. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

2.2.2 SCSI Bus Activity LED (BSY_LED)

Internal logic detects SCSI bus activity and generates a signal that produces an active HIGH output. This output can be used to drive a LED to indicate SCSI activity.

The internal circuitry is a digital one shot that is active HIGH with a minimum pulse width of 16 ms. The BSY_LED output current is 8 mA. This output may have an LED attached to it with the other lead of the LED grounded through a suitable resistor.

2.2.3 Select Control (SSEL)

A_SSEL and B_SSEL are control signals used during bus arbitration and selection. Whichever side asserts, SSEL propagates it to the other side. If both signals are asserted at the same time, the A Side receives SSEL and sends it to the B Side. This output has pull-down control for an open collector driver. The select control signals go through this process:

1. The input signal is blocked if it is being driven by the LSI53C140.
2. The next stage is a leading edge filter. This ensures that the output does not switch for a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
3. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

2.2.4 Busy Control (SBSY)

A_SBSY and B_SBSY signals are propagated from the source bus to the load bus. The busy control signals go through this process:

1. The bus is tested to ensure the signal, if being driven by the LSI53C140, is not misinterpreted as an incoming signal.
2. The data is then leading edge filtered. The assertion edge is held for a specified time to prevent any signal bounce. The input signal controls the duration.
3. The signal path switches the long and short filters used in the circuit depending upon the current state of the LSI53C140. The current state of the LSI53C140 State Machine that tracks SCSI phases selects the mode. The short filter mode passes data through, while the long filter mode indicates the bus free state. When the Busy (SBSY) and Select (SSEL) sources switch from side to side, the long filter mode is used. This output is then fed to the output driver, which is a pull-down open collector only.
4. A parallel function ensures that bus (transmission line) recovery is available for a specified time after the last signal deassertion on each signal line.

2.2.5 Reset Control (SRST)

The controller passes the A_SRST and B_SRST signals from the source bus to the load bus. This output has pull-down control for an open collector driver. The controller processes these reset signals in this sequence:

1. The input signal is blocked if it is already being driven by the LSI53C140.
2. The next stage is a leading edge filter. This ensures that the output does not switch during a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
3. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

When the LSI53C140 senses a true mode change on either bus, it generates a SCSI reset to the opposite bus. For example, when LVD mode changes to SE mode, a reset occurs.

2.2.6 Request and Acknowledge Control (SREQ and SACK)

The A_SREQ, A_SACK, B_SREQ, and B_SACK are clock and control signals. Their signal paths contain controls to guarantee minimum pulse widths, filter edges, and does some retiming when used as data transfer clocks. Only the leading edge is filtered in single transition clocking. SREQ and SACK have paths from the A Side to the B Side and from the B Side to the A Side. The received signal goes through these processing steps before being sent to the opposite bus:

1. The asserted input signal is sensed and forwarded to the next stage if the direction control permits it. State machines develop the direction controls that are driven by the sequence of bus control signals.
2. The signal must then pass the test of not being generated by the LSI53C140.
3. The next stage is a leading edge filter. This ensures that the output does not switch during the specified hold time after the leading edge. The duration of the input signal determines the duration of the output after the hold time. The circuit guarantees a minimum pulse rate.
4. The next stage passes the signal if it is not a data clock. If SREQ or SACK is a data clock, it delays the leading edge to improve data output setup times. The input signal again controls the duration.

5. This stage is a trailing edge signal filter. When the signal deasserts, the filter does not permit any signal bounce. The output signal deasserts at the first deasserted edge of the input signal.
6. The last stage develops pull-up and pull-down signals with drive and 3-state control.
7. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

2.2.7 Control/Data, Input/Output, Message, and Attention Controls (SCD, SIO, SMSG, and SATN)

A_SCD, A_SIO, A_SMSG, A_SATN, B_SCD, B_SIO, B_SMSG, and B_SATN are control signals that follow these processing steps:

1. The input signal is blocked if it is being driven by the LSI53C140.
2. The next stage is a leading edge filter. This ensures the output does not switch for a specified time after the leading edge. The duration of the input signal determines the duration of the output.
3. The final stage develops pull-up and pull-down controls for the SCSI I/O logic, including 3-state controls for the pull-up.
4. A parallel function ensures that bus (transmission line) recovery is for a specified time after the last signal deassertion on each signal line.

2.2.8 Differential Direction Control

A_SD[15:0], A_SDP[1:0], A_SBSY, A_SSEL, A_SCD, A_SIO, A_SMSG, A_SREQ, A_SACK, A_SATN, A_SRST, B_SD[15:0], B_SDP[1:0], B_SBSY, B_SSEL, B_SCD, B_SIO, B_SMSG, B_SREQ, B_SACK, B_SATN, and B_SRST are all multimode signals. The HVD_MODE input pins control the mode and the voltage is sensed at the DIFFSENS inputs.

When the system selects HVD signaling and the DIFFSENS line sees the proper voltage input, all the minus signal leads become SE inputs/outputs to HVD drivers/receivers. All plus signals become the HVD driver/receiver direction control signals. The A and B Sides are independently controlled. Table 2.2 describes the Direction Control signal polarity.

Table 2.2 Direction Control Signal Polarity

Signal Level	State	Effect
LOW = 0	Deasserted	Input signals into the LSI53C140.
HIGH = 1	Asserted	Drive the LSI53C140 signals onto the bus.

When the system selects SE mode due to the lack of HVD_MODE and the correct DIFFSENS voltage, the plus signal leads are internally tied to ground and the minus SCSI signals become the SE input/outputs.

When the system selects LVD mode due to the lack of HVD_MODE and the correct DIFFSENS voltage, the plus and minus signal leads are differential signal pairs.

2.2.9 A and B HVD Mode (A_HVD_MODE and B_HVD_MODE)

These inputs inform the LSI53C140 that external drivers and receivers are used in this particular application. The effect of this control is to disable the LVD and SE modes of operation from the corresponding port. Table 2.3 describes the HVD_MODE Control signal polarity.

Table 2.3 HVD_MODE Control Signal Polarities

Signal Level	State	Effect
LOW = 0	Deasserted	LSI53C140 drivers function in SE or LVD mode.
HIGH = 1	Asserted	HVD signals and controls are enabled from the port.

2.2.10 A and B Differential Sense (A_DIFFSENS and B_DIFFSENS)

These control pins determine the mode of SCSI bus signaling that is expected. Table 2.4 describes the Mode Sense Control voltage levels.

Table 2.4 Mode Sense Control Voltage Levels

Voltage	Mode
–0.35 to +0.5	SE
+0.7 to +1.9	LVD
+2.4 to +5.5	HVD

For example, if a differential source is plugged into the B Side that has been configured to run in the differential mode and if a SE source is detected, then the B Side is disabled and no B Side signals are driven. This is a protection mechanism for SE interfaces that are connected to differential drivers.

2.2.11 Control Signals

This section provides information about RESET/, WS_ENABLE, and XFER_ACTIVE pins. It also describes the function of the CLOCK input.

2.2.11.1 Chip Reset (RESET/)

This general purpose chip reset forces all of the internal elements of the LSI53C140 into a known state. It brings the State Machine to an idle state and forces all controls to a passive state. The minimum RESET/ input asserted pulse width is 100 ns.

The LSI53C140 also contains an internal Power On Reset (POR) function that is ORed with the chip reset pin. This eliminates the need for an external chip reset if the power supply meets ramp up specifications. Table 2.5 describes the RESET/ Control signal polarity.

Table 2.5 RESET/ Control Signal Polarity

Signal Level	State	Effect
LOW = 0	Asserted	The chip forces reset to all internal LSI53C140 elements.
HIGH = 1	Deasserted	LSI53C140 is not in a forced reset state.

2.2.11.2 Warm Swap Enable (WS_ENABLE/)

This input removes the chip from an active bus without disturbing the current SCSI transaction (for Warm Swap). When the WS_ENABLE/ pin is asserted, after detection of the next bus free state, the SCSI signals are 3-stated. This occurs so that the LSI53C140 no longer passes through signals until the WS_ENABLE/ pin is deasserted HIGH and both SCSI buses enter the Bus Free state. As an indication that the chip is idle, or ready to be warm swapped, the XFER_ACTIVE signal deasserts LOW. An LED or some other indicator could be connected to the XFER_ACTIVE signal. This feature of Warm Swap Enable is to isolate buses in certain situations. Table 2.6 describes the WS_ENABLE/ signal polarity.

Table 2.6 WS_ENABLE/ Signal Polarity

Signal Level	State	Effect
LOW = 0	Asserted	Requests the LSI53C140 to go off-line after detection of a SCSI Bus Free state.
HIGH = 1	Deasserted	Enables the LSI53C140 to run normally.

2.2.11.3 Transfer Active (XFER_ACTIVE)

This output is an indication that the chip has finished its internal testing, the SCSI bus has entered a Bus Free state, and SCSI traffic can now pass from one bus to the other. The signal is asserted HIGH when the chip is active. Table 2.7 describes the XFER_ACTIVE signal polarity.

Table 2.7 XFER_ACTIVE Signal Polarity

Signal Level	State	Effect
HIGH = 1	Asserted	Indicates normal operation, and enables transfers through the LSI53C140.
LOW = 0	Deasserted	Detects a Bus Free state by the LSI53C140 due to WS_ENABLE/ being low, thus disabling transfers through the device.

2.2.11.4 Clock (CLOCK)

This is the 40 MHz oscillator input to the LSI53C140. It is the clock source for the protocol control state machines and timing generation logic. This clock is not used in any bus signal transfer paths.

2.2.12 SCSI Termination

The terminator networks provide the biasing needed to pull signals to an inactive voltage level, and to match the impedance seen at the end of the cable with the characteristic impedance of the cable. Terminators must be installed at the extreme ends of each SCSI segment, and only at the ends. No SCSI segment should ever have more or less than two terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so they may be removed if not needed. Otherwise, the terminators should be disabled by means of software.

LSI Logic requires the use of multimode terminators because these terminators provide both LVD and SE termination, depending on what mode of operation is detected by the DIFFSENS pins. HVD requires a different termination configuration. The use of active termination is highly recommended.

Chapter 3
LSI53C140
Specifications

This chapter provides the electrical characteristics and descriptions associated with the 160-pin PQFP and the 192-ball PBGA packages for the LSI53C140. It includes these topics:

3.1 General Description

LSI Logic provides two packages for the LSI53C140:

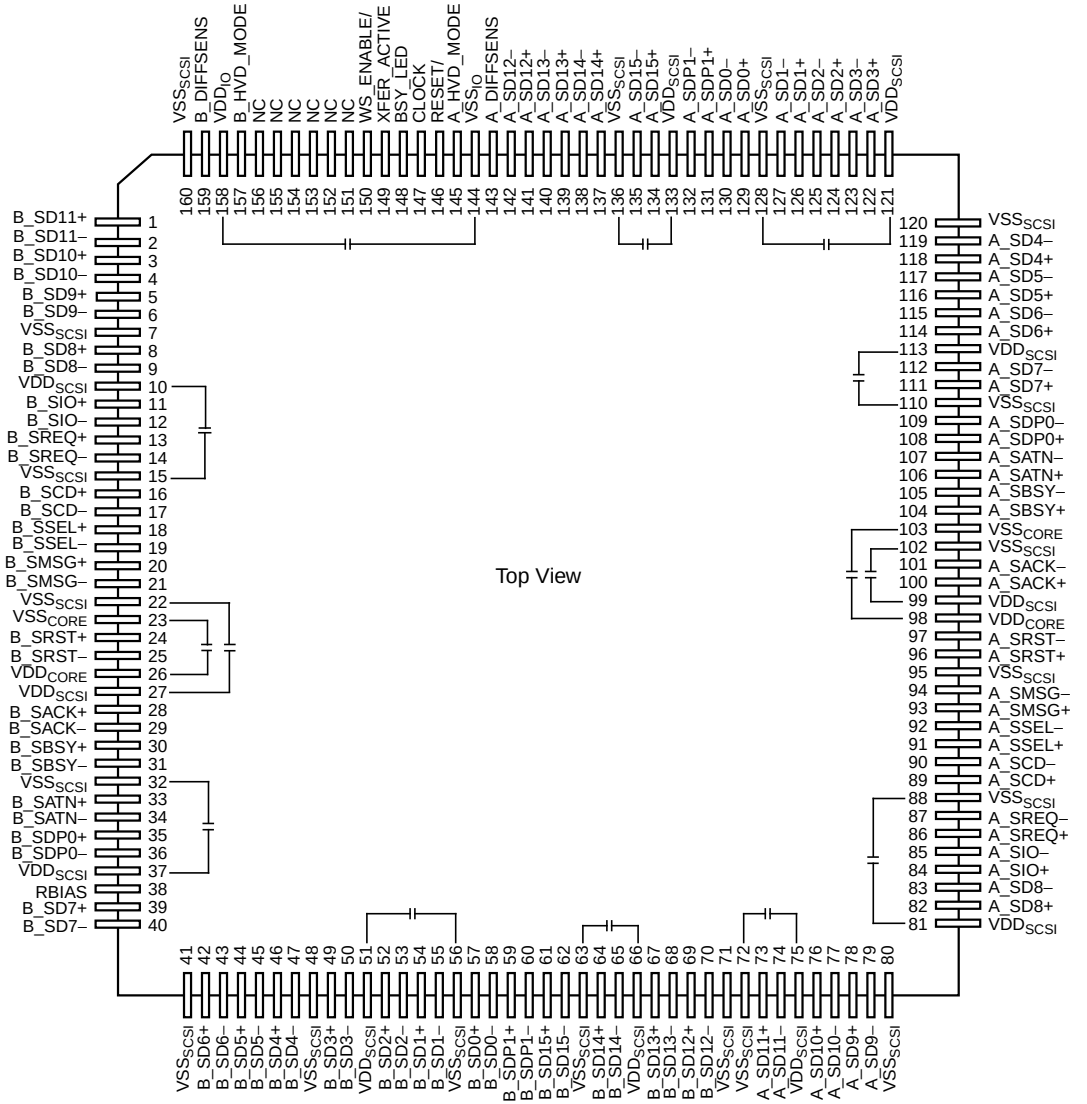
- A 160-pin PQFP package, and
- A 192-ball PBGA package.

Tables 3.1 through 3.4 list the signal descriptions grouped by function:

- SCSI A Side Interface Pins (Table 3.1)
- SCSI B Side Interface Pins (Table 3.2)
- Chip Interface Control Pins (Table 3.3)
- Power and Ground Pins (Table 3.4)

The decoupling capacitor arrangement shown in Figure 3.1 is recommended to maximize the benefits of the internal split ground system. Capacitor values should be between 0.01 µF and 0.1 µF. Figure 3.1 illustrates the 160-pin PQFP diagram.

Figure 3.1 LSI53C140 160-Pin PQFP Pin Diagram



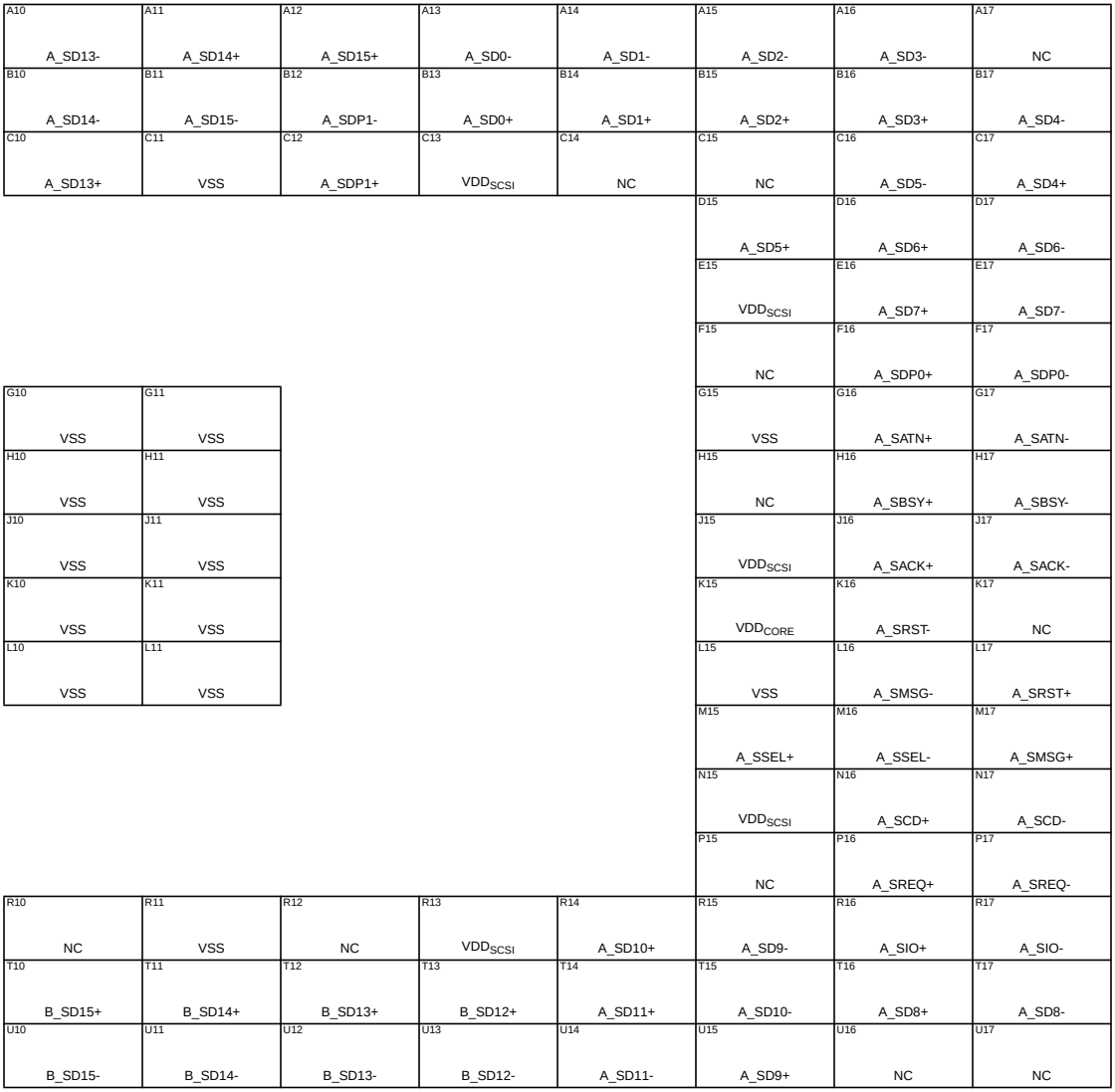
1. *NC* pins are not connected.

Figure 3.2 illustrates the 192-ball PBGA package.

Figure 3.2 LSI53C140 192-Ball PBGA Top View

A1 NC	A2 VDD_{IO}	A3 B_HVD_MODE	A4 NC	A5 NC	A6 XFER_ACTIVE	A7 RESET/	A8 A_DIFFSENS	A9 A_SD12-
B1 B_SD11+	B2 B_SD11-	B3 NC	B4 NC	B5 WS_ENABLE/	B6 BSY_LED	B7 A_HVD_MODE	B8 VDD_{CORE}	B9 A_SD12+
C1 B_SD10+	C2 B_SD10-	C3 B_DIFFSENS	C4 NC	C5 VDD_{SCSI}	C6 NC	C7 VSS	C8 CLOCK	C9 VDD_{SCSI}
D1 B_SD9+	D2 B_SD9-	D3 NC						
E1 B_SD8+	E2 B_SD8-	E3 VDD_{SCSI}						
F1 B_SIO+	F2 B_SIO-	F3 NC						
G1 B_SREQ+	G2 B_SREQ-	G3 VSS				G7 VSS	G8 VSS	G9 VSS
H1 B_SCD-	H2 B_SSEL+	H3 B_SCD+				H7 VSS	H8 VSS	H9 VSS
J1 B_SSEL-	J2 B_SMSG+	J3 VDD_{SCSI}				J7 VSS	J8 VSS	
K1 B_SMSG-	K2 B_SRST+	K3 VDD_{CORE}				K7 VSS	K8 VSS	K9 VSS
L1 B_SRST-	L2 NC	L3 VSS				L7 VSS	L8 VSS	L9 VSS
M1 B_SACK+	M2 B_SACK-	M3 B_SBSY+						
N1 B_SBSY-	N2 B_SATN+	N3 VDD_{SCSI}						
P1 B_SATN-	P2 B_SDP0-	P3 B_SDP0+						
R1 RBIAS	R2 B_SD7+	R3 B_SD7-	R4 NC	R5 VDD_{SCSI}	R6 B_SD2+	R7 VSS	R8 B_SD0-	R9 VDD_{SCSI}
T1 NC	T2 B_SD6+	T3 B_SD5+	T4 B_SD4+	T5 B_SD3+	T6 B_SD2-	T7 B_SD1+	T8 B_SD0+	T9 B_SDP1+
U1 NC	U2 B_SD6-	U3 B_SD5-	U4 B_SD4-	U5 B_SD3-	U6 NC	U7 B_SD1-	U8 VDD_{CORE}	U9 B_SDP1-

Figure 3.2 LSI53C140 192-Ball PBGA Top View (Cont.)



A10 A_SD13-	A11 A_SD14+	A12 A_SD15+	A13 A_SD0-	A14 A_SD1-	A15 A_SD2-	A16 A_SD3-	A17 NC
B10 A_SD14-	B11 A_SD15-	B12 A_SDP1-	B13 A_SD0+	B14 A_SD1+	B15 A_SD2+	B16 A_SD3+	B17 A_SD4-
C10 A_SD13+	C11 VSS	C12 A_SDP1+	C13 VDD_{SCSI}	C14 NC	C15 NC	C16 A_SD5-	C17 A_SD4+
					D15 A_SD5+	D16 A_SD6+	D17 A_SD6-
					E15 VDD_{SCSI}	E16 A_SD7+	E17 A_SD7-
					F15 NC	F16 A_SDP0+	F17 A_SDP0-
G10 VSS	G11 VSS				G15 VSS	G16 A_SATN+	G17 A_SATN-
H10 VSS	H11 VSS				H15 NC	H16 A_SBSY+	H17 A_SBSY-
J10 VSS	J11 VSS				J15 VDD_{SCSI}	J16 A_SACK+	J17 A_SACK-
K10 VSS	K11 VSS				K15 VDD_{CORE}	K16 A_SRST-	K17 NC
L10 VSS	L11 VSS				L15 VSS	L16 A_SMSG-	L17 A_SRST+
					M15 A_SSEL+	M16 A_SSEL-	M17 A_SMSG+
					N15 VDD_{SCSI}	N16 A_SCD+	N17 A_SCD-
					P15 NC	P16 A_SREQ+	P17 A_SREQ-
R10 NC	R11 VSS	R12 NC	R13 VDD_{SCSI}	R14 A_SD10+	R15 A_SD9-	R16 A_SIO+	R17 A_SIO-
T10 B_SD15+	T11 B_SD14+	T12 B_SD13+	T13 B_SD12+	T14 A_SD11+	T15 A_SD10-	T16 A_SD8+	T17 A_SD8-
U10 B_SD15-	U11 B_SD14-	U12 B_SD13-	U13 B_SD12-	U14 A_SD11-	U15 A_SD9+	U16 NC	U17 NC

3.1.1 Signal Descriptions

This section provides the descriptions for the signals associated with the LSI53C140. Figure 3.3 illustrates the functional signal grouping for the LSI53C140.

Figure 3.3 LSI53C140 Functional Signal Grouping

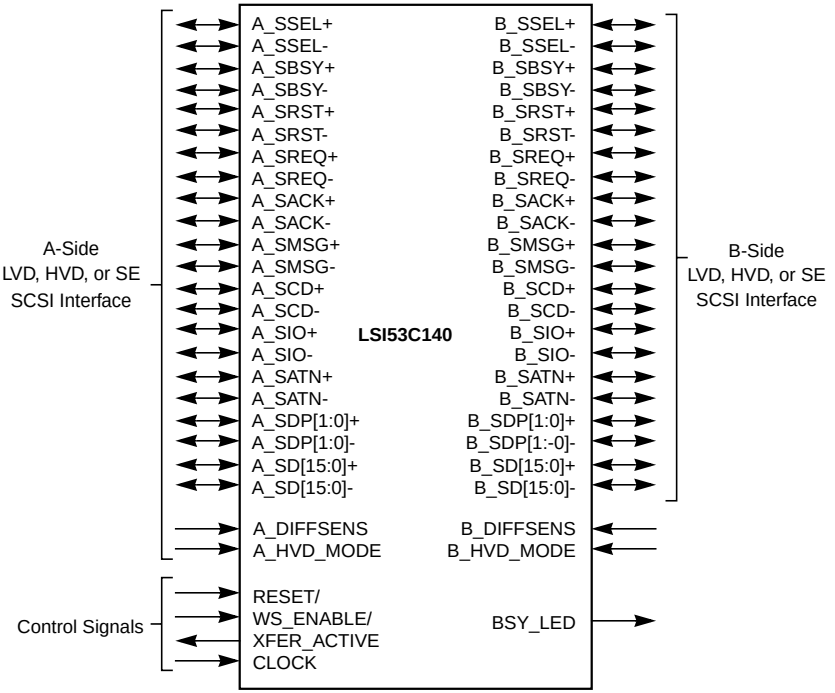


Table 3.1 lists and describes the SCSI A side interface pins for the LSI53C140.

Table 3.1 SCSI A Side Interface Pins

Name	Pin	Ball	Type	Description
A_SSEL+,–	91, 92	M15, M16	I/O	A Side SCSI bus Select control signal.
A_SBSY+,–	104, 105	H16, H17	I/O	A Side SCSI bus Busy control signal.
A_SRST+,–	96, 97	L17, K16	I/O	A Side SCSI bus Reset control signal.
A_SREQ+,–	86, 87	P16, P17	I/O	A Side SCSI bus Request control signal.
A_SACK+,–	100, 101	J16, J17	I/O	A Side SCSI bus Acknowledge control signal.
A_SMSG+,–	93, 94	M17, L16	I/O	A Side SCSI bus Message control signal.
A_SCD+,–	89, 90	N16, N17	I/O	A Side SCSI bus Control and Data control signal.
A_SIO+,–	84, 85	R16, R17	I/O	A Side SCSI bus Input and Output control signal.
A_SATN+,–	106, 107	G16, G17	I/O	A Side SCSI bus Attention control signal.
A_SDP[1:0]+,–	131, 132, 108, 109	C12, B12, F16, F17	I/O	A Side SCSI bus Data Parity signal.
A_SD[15:0]+,–	134, 135, 137, 138, 139, 140 141, 142, 73, 74, 76, 77, 78, 79, 82, 83, 111, 112, 114, 115, 116, 117, 118, 119, 122, 123, 124, 125, 126, 127, 129, 130	A12, B11, A11, B10, C10, A10, B9, A9, T14, U14, R14, T15, U15, R15, T16, T17, E16, E17, D16, D17, D15, C16, C17, B17, B16, A16, B15, A15, B14, A14, B13, A13	I/O	A Side SCSI bus Data signals.
A_DIFFSENS	143	A8	I	A Side SCSI bus Differential Sense signal.
A_HVD_MODE	145	B7	I	A Side SCSI bus HVD Mode control signal.

Table 3.2 lists and describes the SCSI B side interface pins for the LSI53C140.

Table 3.2 SCSI B Side Interface Pins

Name	Pin	Ball	Type	Description
B_SSEL+,–	18, 19	H2, J1	I/O	B Side SCSI bus Select control signal.
B_SBSY+,–	30, 31	M3, N1	I/O	B Side SCSI bus Busy control signal.
B_SRST+,–	24, 25	K2, L1	I/O	B Side SCSI bus Reset control signal.
B_SREQ+,–	13, 14	G1, G2	I/O	B Side SCSI bus Request control signal.
B_SACK+,–	28, 29	M1, M2	I/O	B Side SCSI bus Acknowledge control signal.
B_SMSG+,–	20, 21	J2, K1	I/O	B Side SCSI bus Message control signal.
B_SCD+,–	16, 17	H3, H1	I/O	B Side SCSI bus Control and Data control signal.
B_SIO+,–	11, 12	F1, F2	I/O	B Side SCSI bus Input and Output control signal.
B_SATN+,–	33, 34	N2, P1	I/O	B Side SCSI bus Attention control signal.
B_SDP[1:0]+,–	59, 60, 35, 36	T9, U9, P3, P2	I/O	B Side SCSI bus Data Parity signal.
B_SD[15:0]+,–	61, 62, 64, 65, 67, 68, 69, 70, 1, 2, 3, 4, 5, 6, 8, 9, 39, 40, 42, 43, 44, 45, 46, 47, 49, 50, 52, 53, 54, 55, 57, 58	T10, U10, T11, U11, T12, U12, T13, U13, B1, B2, C1, C2, D1, D2, E1, E2, R2, R3, T2, U2, T3, U3, T4, U4, T5, U5, R6, T6, T7, U7, T8, R8	I/O	B Side SCSI bus Data signals.
B_DIFFSENS	159	C3	I	B Side SCSI bus Differential Sense signal.
B_HVD_MODE	157	A3	I	B Side SCSI bus HVD Mode control signal.

Table 3.3 lists and describes the LSI53C140 interface control pins.

Table 3.3 Chip Interface Control Pins

Name	Pin	Ball	Type	Description
RESET/	146	A7	I	Master Reset for LSI53C140, active LOW.
WS_ENABLE/	150	B5	I	Enable/disable SCSI transfers through the LSI53C140.
XFER_ACTIVE	149	A6	O	Transfers through the LSI53C140 are enabled/disabled.
CLOCK	147	C8	I	Oscillator input for LSI53C140 (40 MHz).
BSY_LED	148	B6	O	SCSI activity LED output, 8 mA.

Table 3.4 lists and describes the LSI53C140 power and ground pins.

Table 3.4 Power and Ground Pins

Name	Pin	Ball	Type	Description
VDD_{SCSI}	10, 27, 37, 51, 66, 75, 81, 99, 113, 121, 133	C5, C9, C13, E3, E15, J3, J15, N3, N15, R5, R9, R13	I	Power supplies to the SCSI bus I/O pins.
VDD_{CORE}	26, 98	B8, K3, K15, U8	I	Power supplies to the CORE logic.
VDD_{IO}	158	A2	I	Power supplies to the I/O logic.
VSS	7, 15, 22, 32, 41, 48, 56, 63, 71, 72, 80, 88, 95, 102, 110, 120, 128, 136, 160, 23, 103, 144	C7, C11, G3, G7, G8, G9, G10, G11, G15, H7, H8, H9, H10, H11, J7, J8, J10, J11, K7, K8, K9, K10, K11, L3, L7, L8, L9, L10, L11, L15, R7, R11	I	Ground ring.
RBIAS	38	R1	I	Receiver bias control, R = 9.76 kΩ 1%.
NC	151–156	A1, A4, A5, A17, B3, B4, C4, C6, C14, C15, D3, F3, F15, H15, K17, L2, P15, R4, R10, R12, T1, U1, U6, U16, U17	N/A	No Connections.

Notes:

- All V_{DD} pins must be supplied 3.3 V. The LSI53C140 output signals drive 3.3 V.
- If the power supplies to the VDD_{IO} and VDD_{CORE} pins in a chip testing environment are separated, either power up the pins simultaneously or power up VDD_{CORE} before VDD_{IO}. The VDD_{IO} pin must always power down before the VDD_{CORE} pin.

3.2 Electrical Characteristics

This section specifies the DC and AC electrical characteristics of the LSI53C140. These electrical characteristics are in the following four categories:

- DC Characteristics
- TolerANT Technology Electrical Characteristics
- AC Characteristics
- SCSI Interface Timing

3.2.1 DC Characteristics

Tables 3.5 through 3.14 give the current and voltage specifications. Figures 3.4 through 3.6 are driver schematics for the LSI53C140.

Table 3.5 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	–55	150	°C	–
V_{DD}	Supply voltage	–0.5	4.5	V	–
V_{IN}	Input voltage	V_{SS} –0.3	7[2] 5.55[3]	V V	–
V_{IN5V}	Input voltage (5 V TolerANT pins)	V_{SS} –0.3	5.25	V	–
I_{LP}[4]	Latch-up current	±150	–	mA	–
ESD	Electrostatic discharge	–	2 K	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.
2. This voltage is for the SCSI pins.
3. This voltage is for the remaining pins.
4. – 2 V < VPIN < 8 V.

Table 3.6 Operating Conditions[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	3.13	3.47	V	–
I_{DD}	Supply current (dynamic SE)	–	130	mA	–
$I_{DD\text{-}I/O}$	Supply current (dynamic LVD)	–	600	mA	–
I_{DD}	Supply current (static)	–	1	mA	–
T_A	Operating free air	0	70	˚C	–
θ_{JA}[2]	Thermal resistance (junction to ambient air)	–	35	˚C/W	–
θ_{JA}[3]	Thermal resistance (junction to ambient air)	–	20.4	˚C/W	Zero airflow

1. Conditions that exceed the operating limits may cause the device to function incorrectly.
2. Value for QFP package.
3. Value for BGA package.

Table 3.7 LVD Driver SCSI Signals—A_SD[15:0]±, A_SDP[1:0]±, A_SCD, A_SIO±, A_SMSG±, A_SREQ±, A_SACK±, A_SBSY±, A_SATN±, A_SSEL±, A_SRST±, B_SD[15:0]±, B_SDP[1:0]±, B_SCD, B_SIO±, B_SMSG±, B_SREQ±, B_SACK±, B_SBSY±, B_SATN±, B_SSEL±, B_SRST±[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
I_O+	Source (+) current	7	12	mA	Asserted state
I_O–	Sink (–) current	–7	–12	mA	Asserted state
I_O+	Source (+) current	–3.5	–6	mA	Negated state
I_O–	Sink (–) current	3.5	6	mA	Negated state
I_{OZ}	3-state leakage	–20	20	µA	V_{PIN} = 0 V, 3.47 V

1. V_{CM} = 0.7–1.8 V, R_L = 0–110 Ω, R_{bias} = 9.76 kΩ.

Figure 3.4 LVD Driver

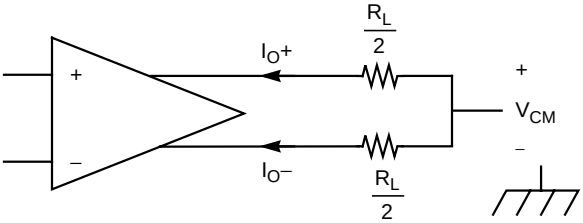


Table 3.8 LVD Receiver SCSI Signals—A_SD[15:0]±, A_SDP[1:0]±, A_SCD±, A_SIO±, A_SMSG±, A_SREQ±, A_SACK±, A_SBSY±, A_SATN±, A_SSEL±, A_SRST±, B_SD[15:0]±, B_SDP[1:0]±, B_SCD±, B_SIO±, B_SMSG±, B_SREQ±, B_SACK±, B_SBSY±, B_SATN±, B_SSEL±, B_SRST±[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_I	LVD receiver voltage asserting	60	–	mV	–
V_I	LVD receiver voltage negating	–	–60	mV	–

1. V_{CM} = 0.7–1.8 V.

Figure 3.5 LVD Receiver

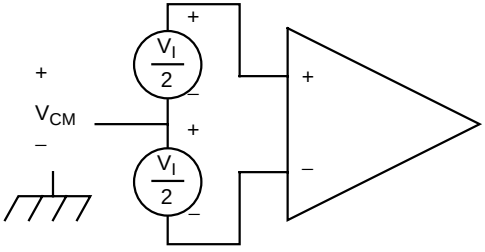


Table 3.9 DIFFSENS SCSI Signal

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	HVD sense voltage	2.4	V_{DD} +0.3	V	–
V_S	LVD sense voltage	0.7	1.9	V	–
V_{IL}	SE sense voltage	V_{SS} –0.3	0.5	V	–
I_{IN}	Input leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

Table 3.10 Input Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

Table 3.11 Bidirectional SCSI Signals—A_SD[15:0]±, A_SDP[1:0]±, A_SREQ±, A_SACK±, B_SD[15:0]±, B_SDP[1:0]±, B_SREQ±, B_SACK±

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.3	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.8	V	–
V_{OH}[1]	Output high voltage	2.0	V_{DD}	V	I_{OH} = 7.0 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	3-state leakage	–20	20	µA	V_{PIN} = 0 V, 3.47 V

1. TolerANT active negation enabled.

Table 3.12 Bidirectional SCSI Signals—A_SCD±, A_SIO±, A_SMSG±, A_SBSY±, A_SATN±, A_SSEL±, A_SRST±, B_SCD±, B_SIO±, B_SMSG ,B_SBSY±, B_SATN , B_SSEL±, B_SRST

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.3	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.8	V	–
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	3-state leakage	–20	20	µA	V_{PIN} = 0 V, 3.47 V

Table 3.13 Input Control Signals—CLOCK, RESET/, WS_ENABLE

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	5.55[1]	V	–
V_{IL}	Input low voltage	V_{SS}	0.8	V	–
I_{OZ}	Input leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

1. Operating Conditions.

Figure 3.6 External Reset Circuit

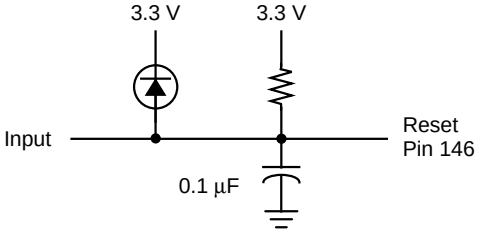


Table 3.14 Output Control Signals—BSY_LED, XFER_ACTIVE

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OZ}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

3.2.2 TolerANT Technology Electrical Characteristics

The LSI53C140 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators. Table 3.15 provides electrical characteristics for SE SCSI signals. Figures 3.7 through 3.11 provide reference information for testing SCSI signals.

Table 3.15 TolerANT Technology Electrical Characteristics[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[2]	Output high voltage	2.0	V_{DD} +0.3	V	I_{OH} = –7 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	V_{DD} +0.3	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	V_{DD} = 4.75; I_I = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.0	1.2	V	–
V_{TL}	Threshold, LOW to HIGH	1.4	1.6	V	–
V_{TH}–V_{TL}	Hysteresis	300	500	mV	–
I_{OH}[2]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply[3]
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	20	µA	V_{DD} 5%, V_{PIN} = 2.7 V

(Sheet 1 of 2)

Table 3.15 TolerANT Technology Electrical Characteristics[1] (Cont.)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{LL}	Input low leakage	–	–20	µA	V_{DD} ±5%, V_{PIN} = 0 V
I_{PD}	Power down leakage	–	20	µA	V_{DD} = 0 V, V_{PIN} = 1.2 V
R_I	Input resistance	20	–	MΩ	SCSI pins[4]
C_P	Capacitance per pin	–	15	pF	PQFP
t_R[2]	Rise time, 10% to 90%	4.0	18.5	ns	Figure 3.7
t_F	Fall time, 90% to 10%	4.0	18.5	ns	Figure 3.7
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.50	V/ns	Figure 3.7
dV_L/dt	Slew rate, HIGH to LOW	0.15	0.50	V/ns	Figure 3.7
ESD	Electrostatic discharge	2	–	kV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	Figure 3.8
	Ultra filter delay	10	15	ns	Figure 3.8
	Ultra2 filter delay	5	8	ns	Figure 3.8
	Extended filter delay	40	60	ns	Figure 3.8

(Sheet 2 of 2)

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, SACK/. (Minus Pins) SCSI mode only.
3. Single pin only; irreversible damage may occur if sustained for more than one second.
4. SCSI RESET/ pin has 10 kΩ pull-up resistor.

Figure 3.7 Rise and Fall Time Test Conditions

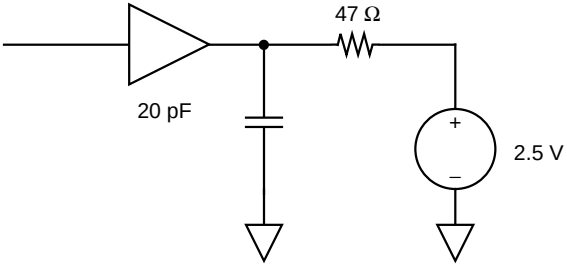
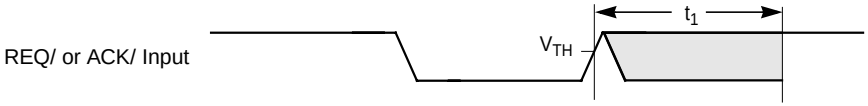


Figure 3.8 SCSI Input Filtering



Note: t_1 is the input filtering period.

Figure 3.9 Hysteresis of SCSI Receivers

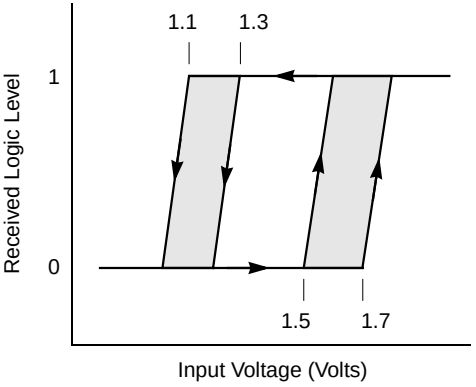


Figure 3.10 Input Current as a Function of Input Voltage

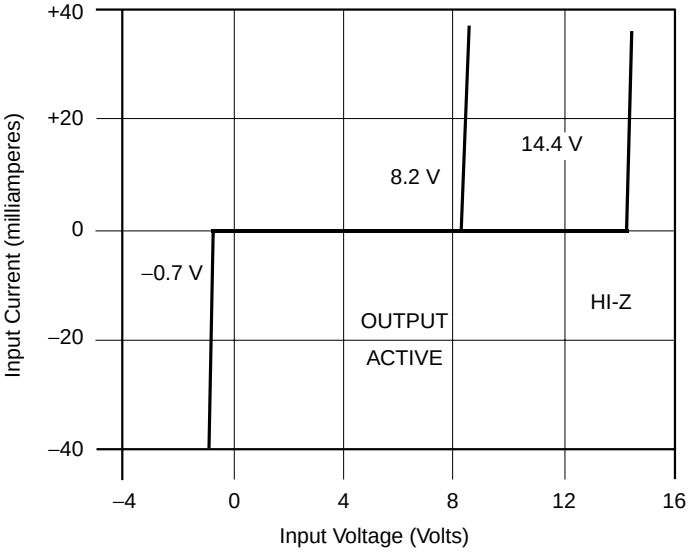
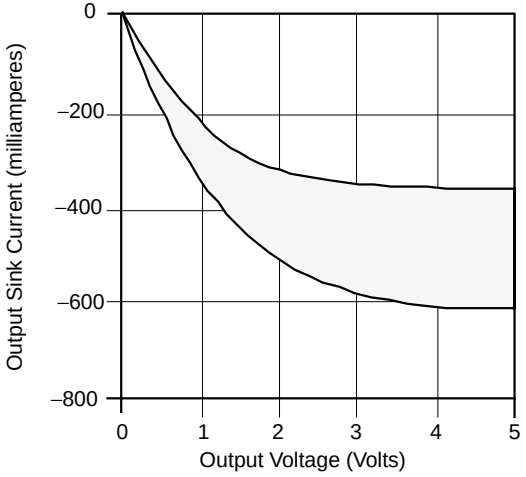
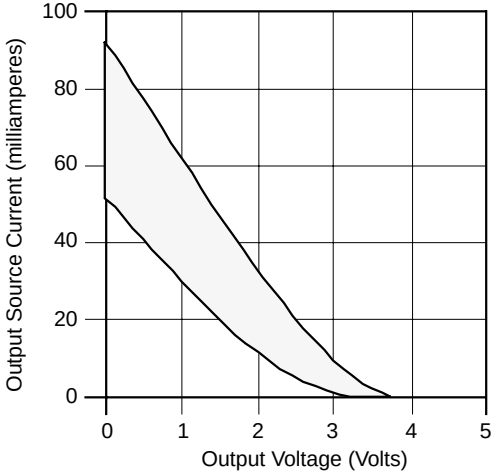


Figure 3.11 Output Current as a Function of Output Voltage





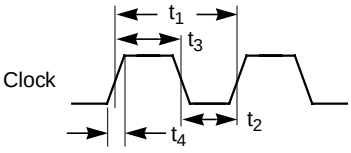
3.2.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to Section 3.2.1, "DC Characteristics"). Chip timing is based on simulation at worst case voltage, temperature, and processing. The LSI53C140 requires a 40 MHz clock input. Table 3.16 and Figure 3.12 provide clock timing data.

Table 3.16 Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	Clock period	24.75	25.25	ns
t_2	Clock low time	10	15	ns
t_3	Clock high time	10	15	ns
t_4	Clock rise time	1	–	V/ns

Figure 3.12 Clock Timing



3.2.4 SCSI Interface Timing

Table 3.17 provides input timing data. Table 3.18 provides output timing data. Figure 3.13 provides input/output timing data.

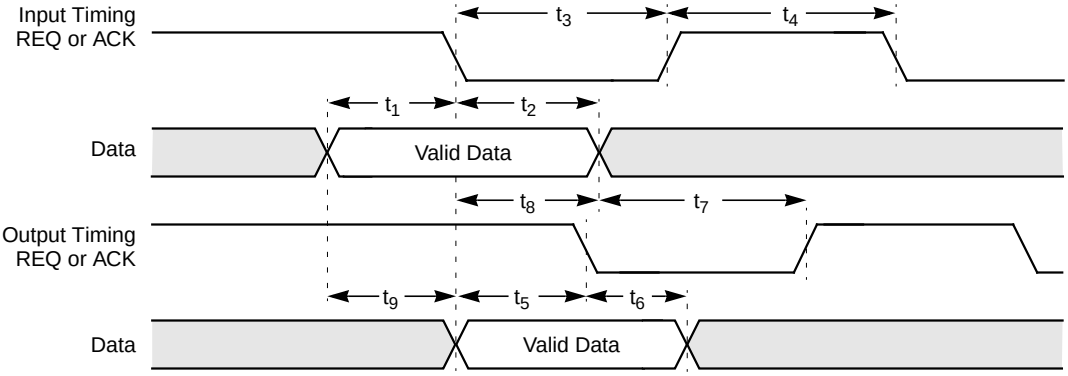
Table 3.17 Input Timing

Symbol	Parameter	Min	Max	Units
t_1	Input data setup	1	–	ns
t_2	Input data hold	4.75	–	ns
t_3	Input REQ/ACK assertion pulse width	11	–	ns
t_4	Input REQ/ACK deassertion pulse width	11	–	ns

Table 3.18 Output Timing

Symbol	Parameter	Min	Max	Units
t_5	Output data setup	Nominal: negotiated/2	–	ns
t_6	Output data hold	Nominal: negotiated/2	–	ns
t_7	Output REQ/ACK pulse width	max [negotiated ns, $t_3 - 5$]	max [negotiated ns, $t_3 + 5$]	ns
t_8	REQ/ACK transport delay	25 ns if REQ/ACK is clock for input data, 10 ns if not	50 ns if REQ/ACK is clock for input data, 30 ns if not	ns
t_9	Data transport delay	6	[$t_3 + 35$]	ns

Figure 3.13 Input/Output Timing



3.3 Mechanical Drawings

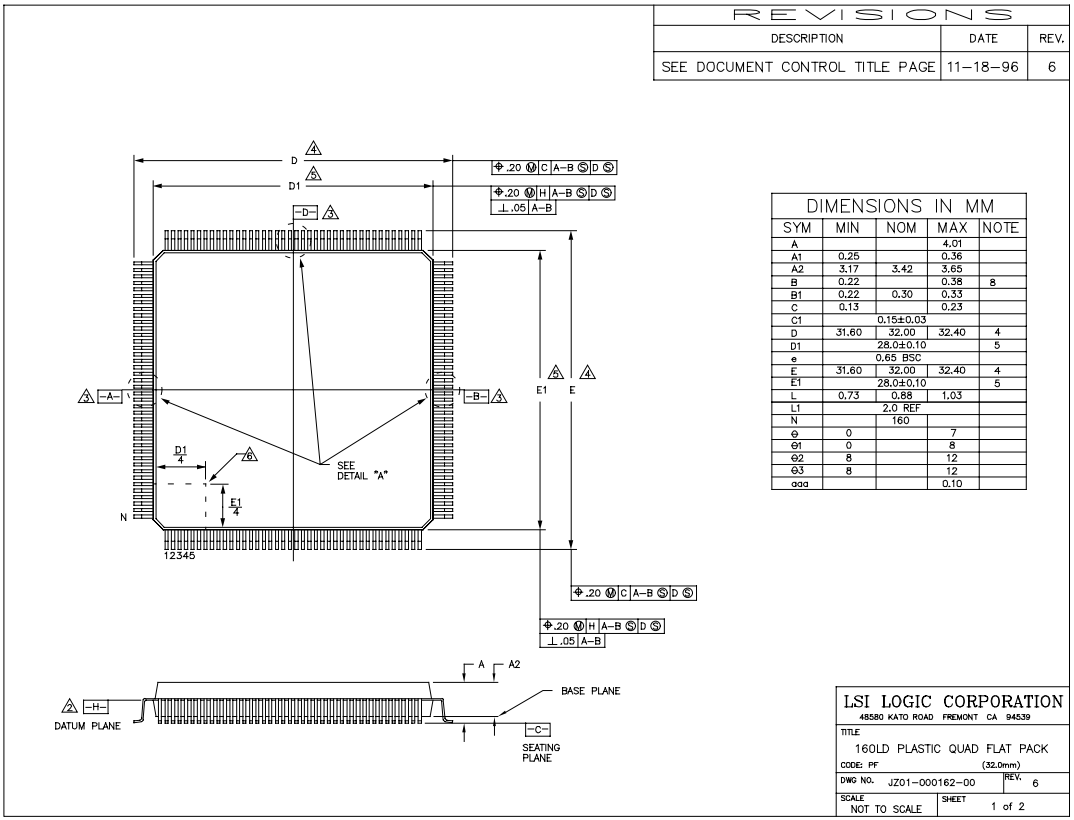
LSI Logic component dimensions conform to a current revision of the JEDEC Publication 95 standard package outline, using ANSI 14.5Y “Dimensioning and Tolerancing” interpretations. As JEDEC drawings are balloted and updated, changes may have occurred. To ensure the use of a current drawing, the JEDEC drawing revision level should be verified. Visit `www.eia.org/jedec` for review of Publication 95 drawings and revision levels.

For printed circuit board land patterns that will accept LSI Logic components, LSI Logic recommends that customers refer to the IPC standards (Institute for Interconnecting and Packaging Electronic Circuits). Specification number IPC-SM-782, “Surface Mount Design and Land Pattern Standard” is an established method of designing land patterns. Feature size and tolerances are industry standards based on IPC assumptions.

3.3.1 LSI53C140 160-Pin PQFP Mechanical Drawing

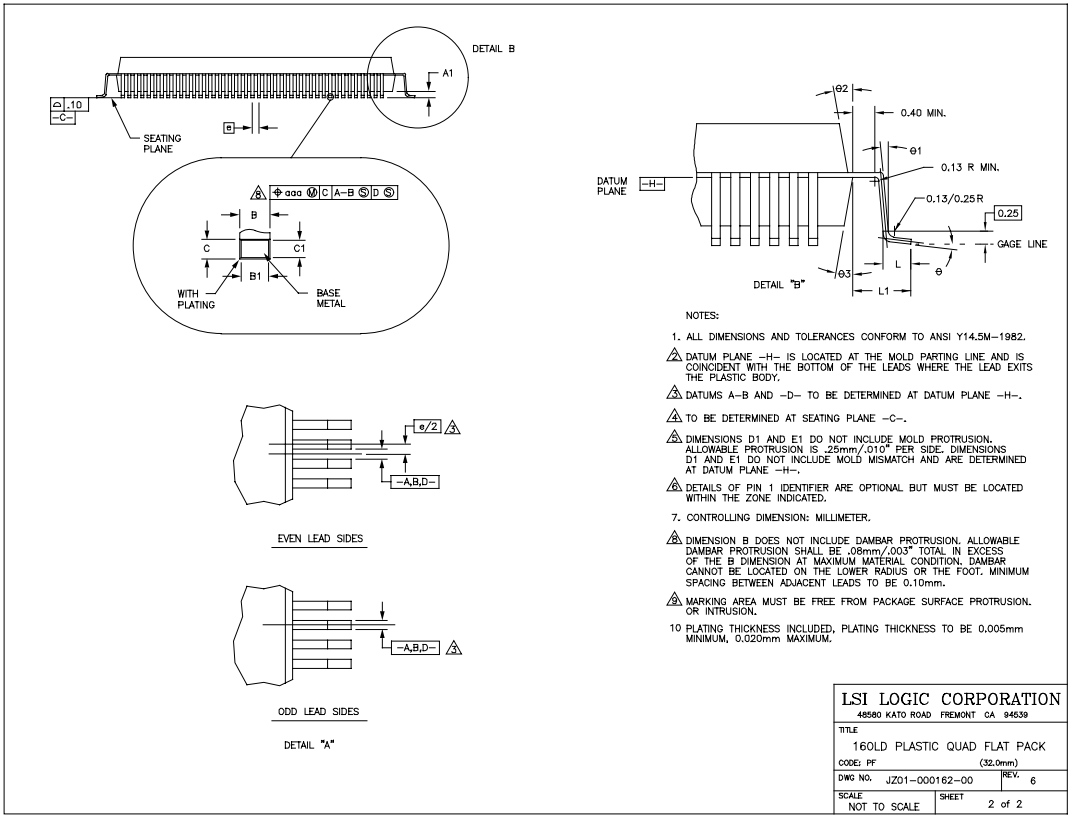
The LSI53C140 is packaged in a 160-pin metric PQFP. Figure 3.14 is the package drawing for the LSI53C140.

Figure 3.14 LSI53C140 160-Pin PQFP (PF) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PF.**

Figure 3.14 LSI53C140 160-Pin PQFP (PF) Mechanical Drawing (Cont.)

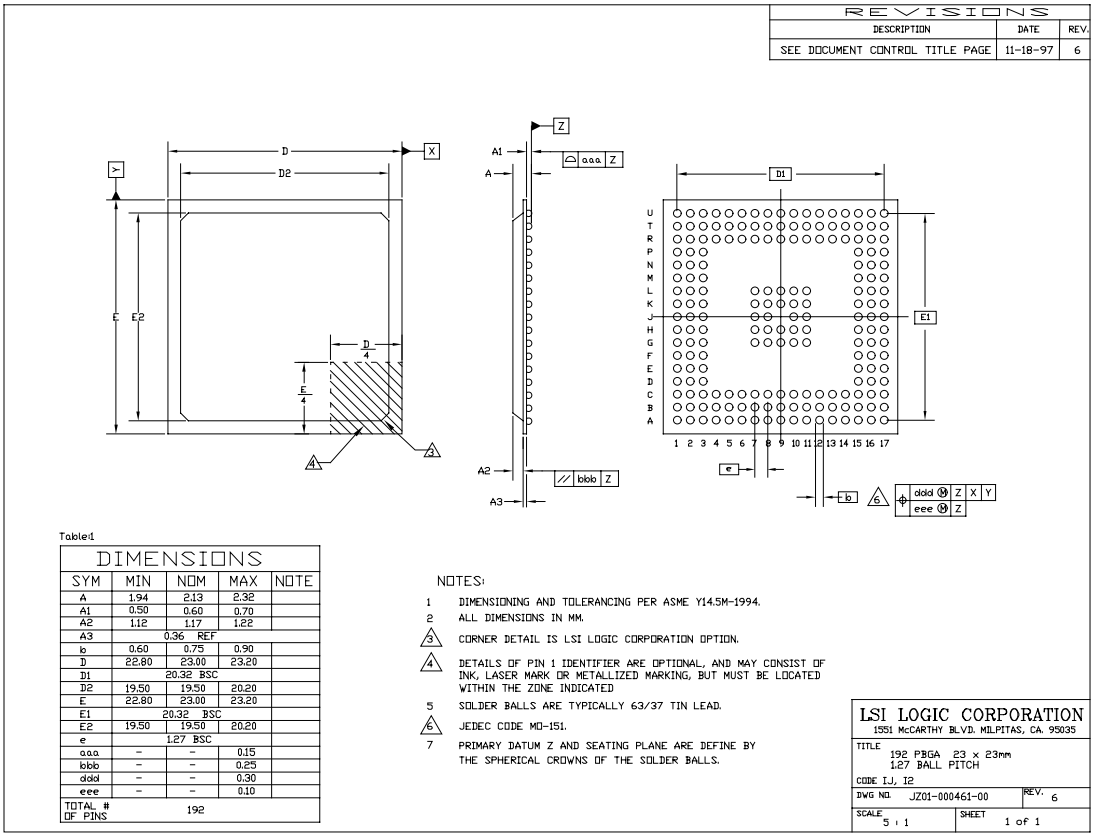


Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PF.**

3.3.2 LSI53C140 192-Ball PBGA Mechanical Drawing

The LSI53C140 is available as a 192-ball PBGA. Figure 3.15 illustrates the 192-ball PBGA mechanical drawing. Refer to Appendix B for more detailed information.

Figure 3.15 192-Ball PBGA (IJ, I2) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code IJ, I2.**

Appendix A
Wiring Diagrams

Figure A.1 illustrates a typical LSI53C140 in an evaluation test board application. Figure A.2 shows the wiring diagram for Ultra SCSI operation in the differential mode using pull-up resistors.

Figure A.1 LSI53C140 Wiring Diagram 1 of 4

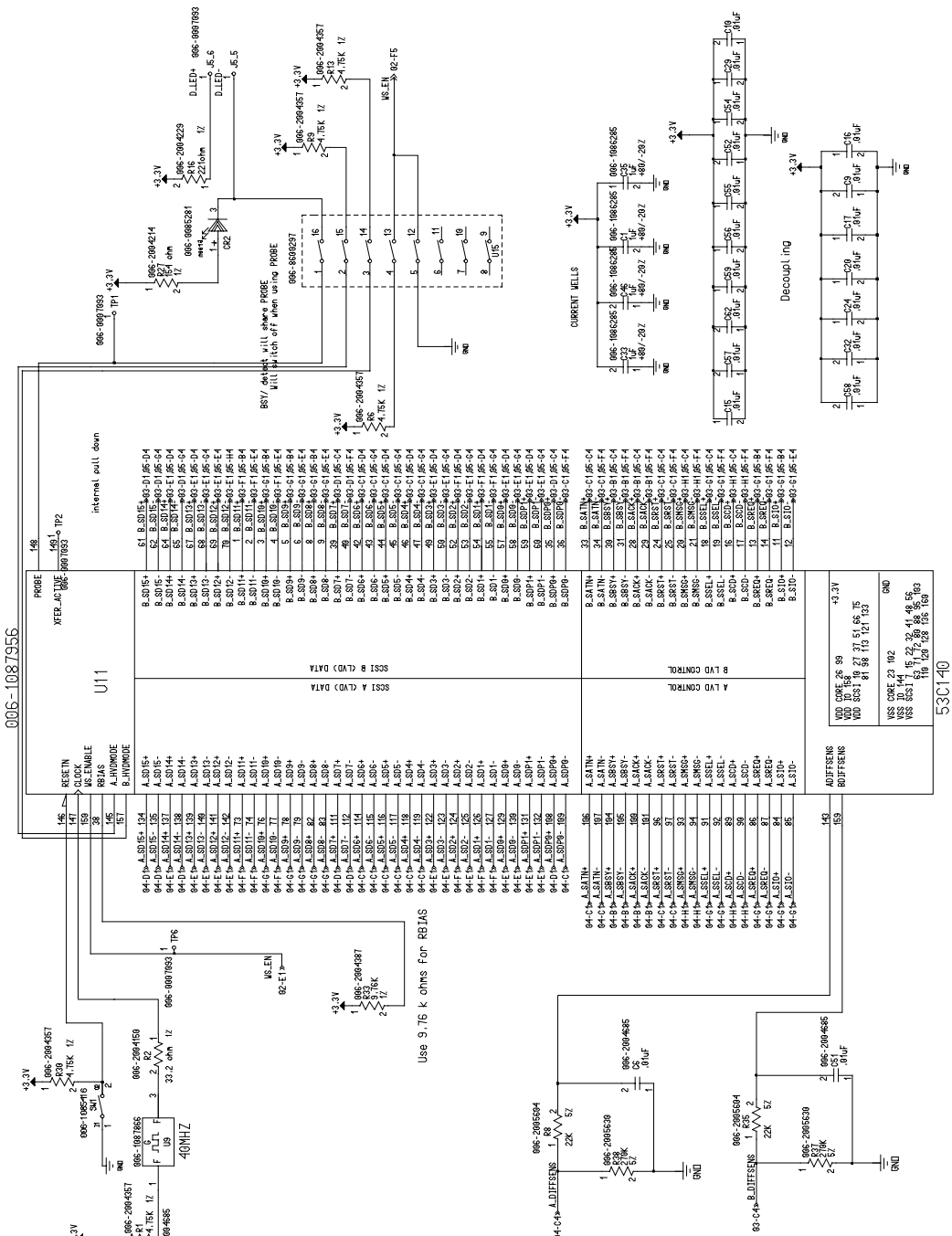


Figure A.1 LSI53C140 Wiring Diagram 2 of 4

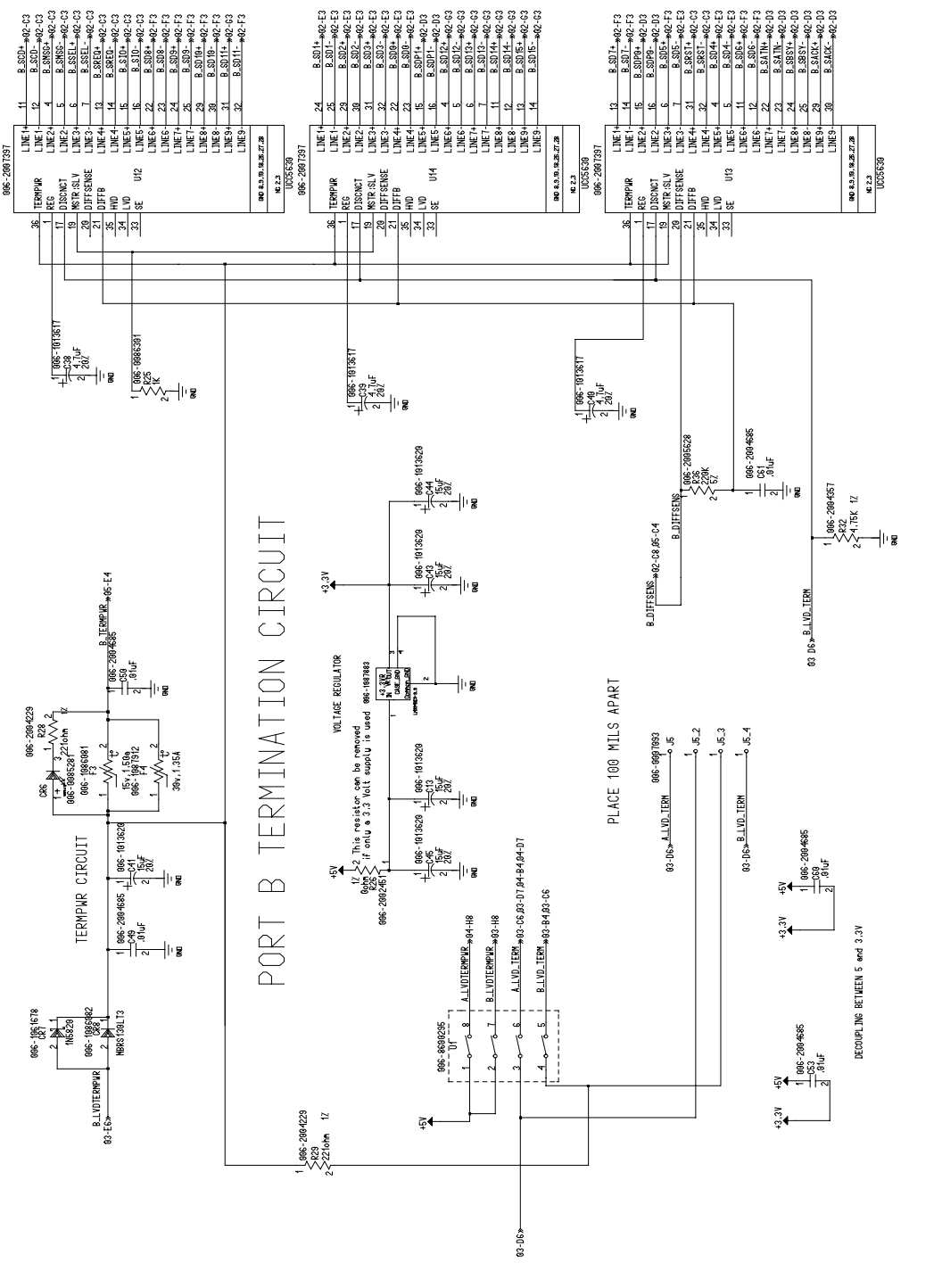


Figure A.1 LSI53C140 Wiring Diagram 3 of 4

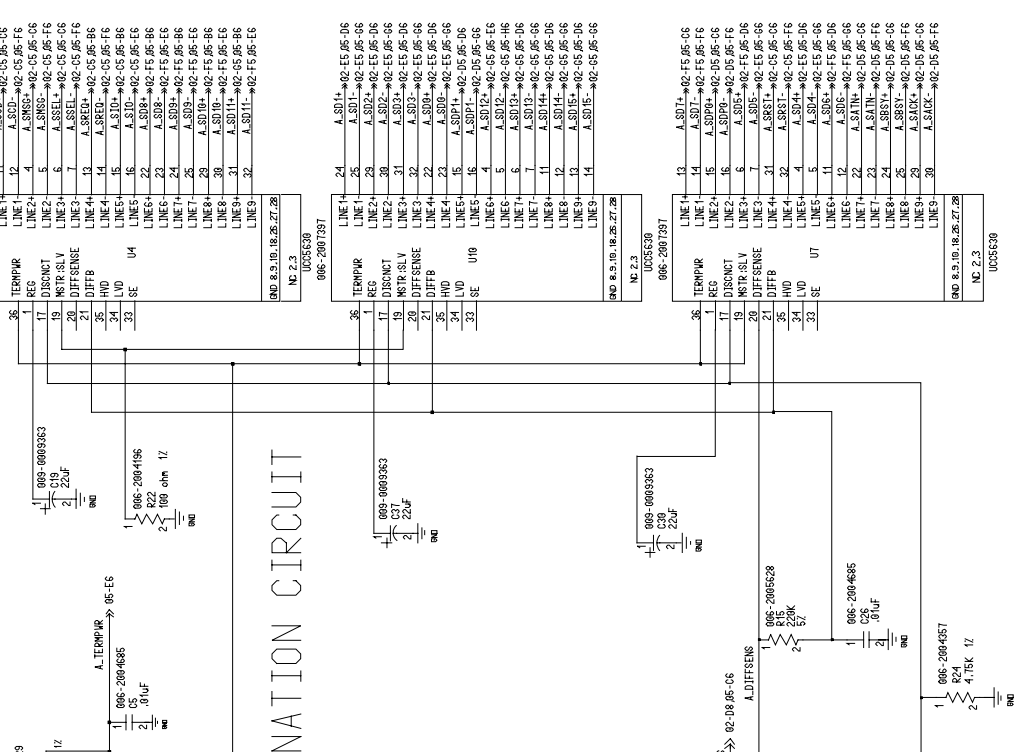


Figure A.1 LSI53C140 Wiring Diagram 4 of 4

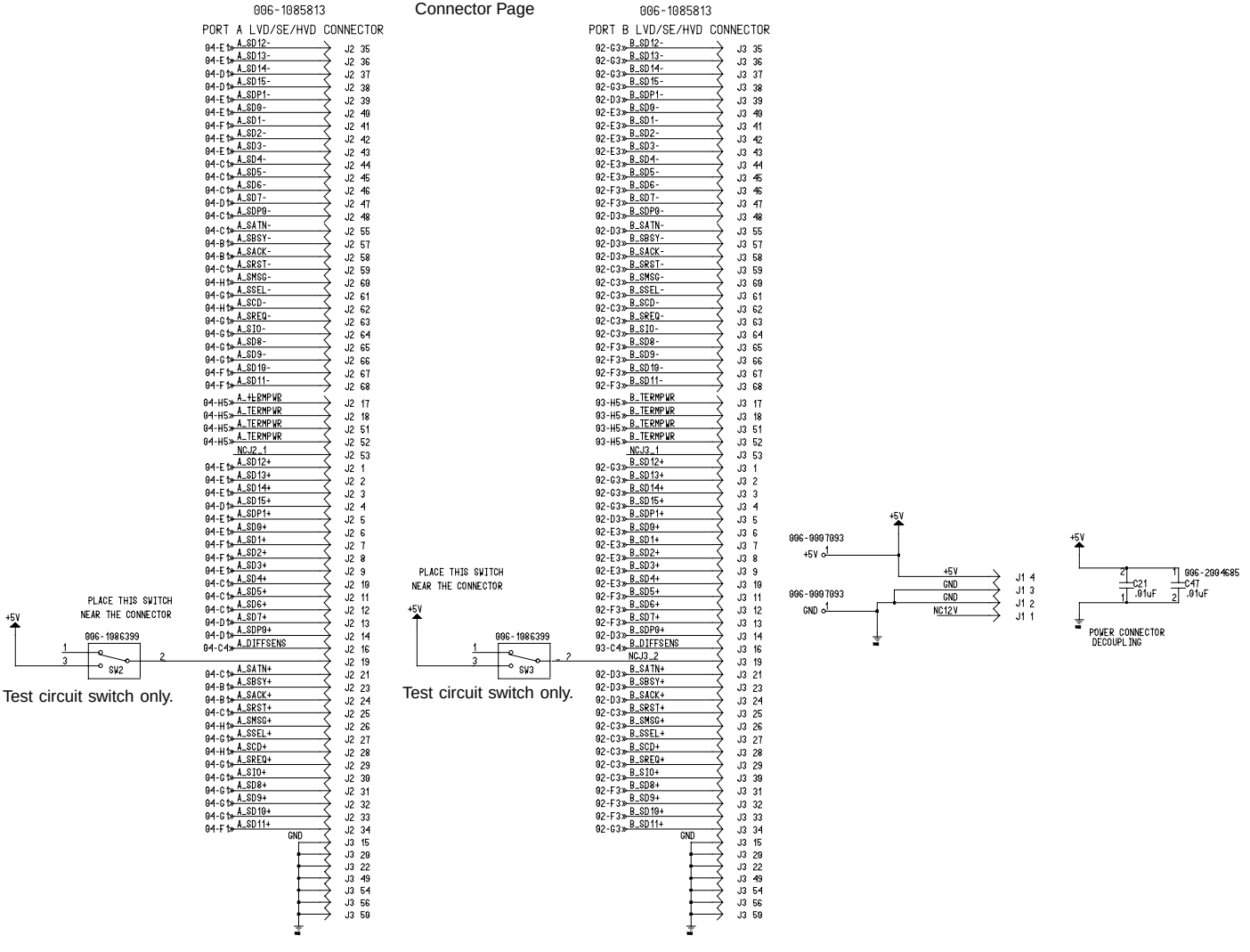
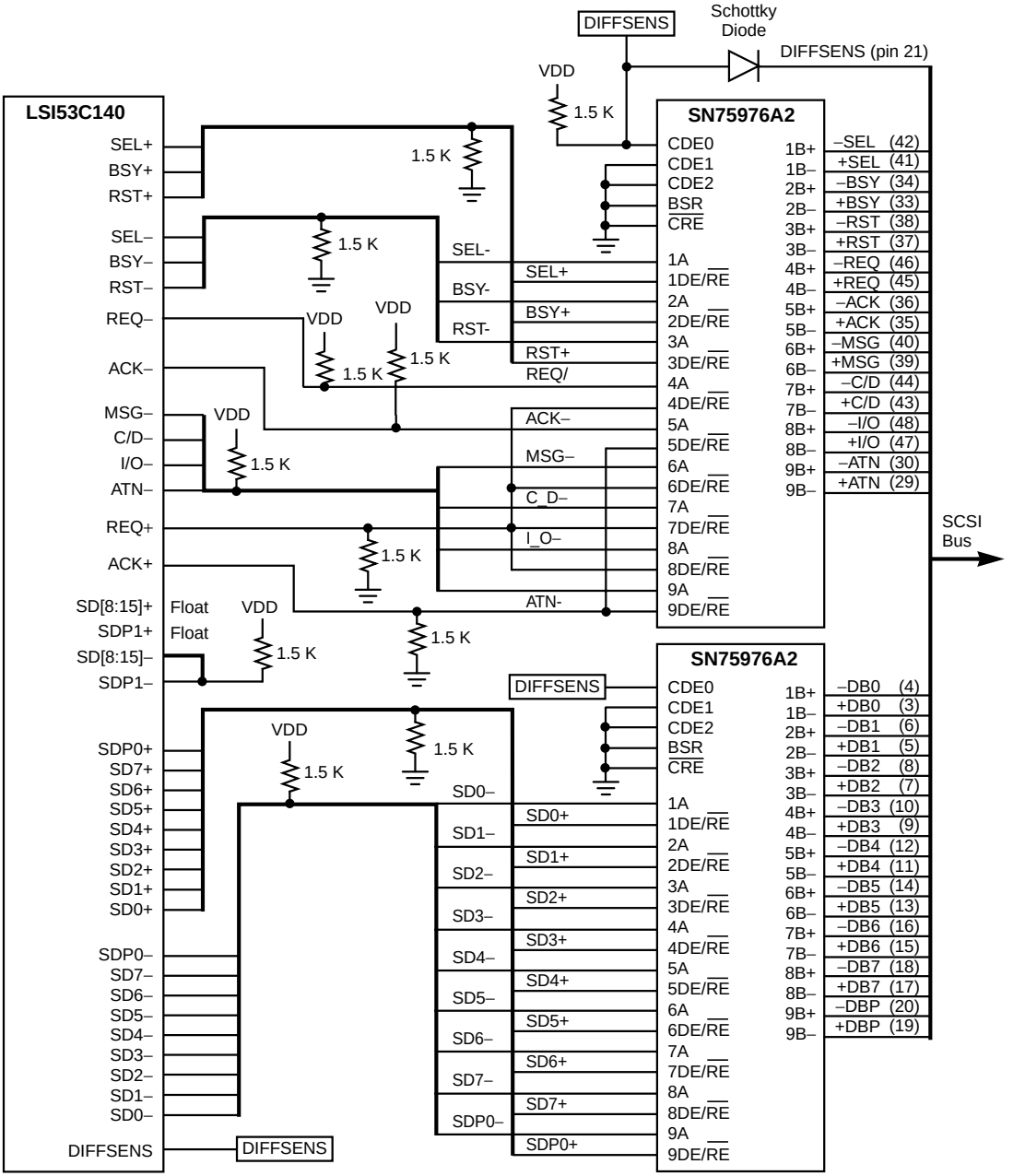


Figure A.2 LSI53C140 Differential Wiring Diagram



Appendix B
Board Design Considerations

This appenidx describes the design considerations for using the LSI53C180 as a drop in replacement for the LSI53C140. Both chips are available as a 192-ball PBGA in a 23 x 23 mm package. This appendix also describes the differences in pin configurations required for operation of the two devices.

The LSI53C180 supports Ultra160 data transfer rates for an LVD bus and Ultra data transfer rates for an SE bus. The LSI53C180 does not support HVD. Thus, HVD mode enable pins for each port are no longer present. In the LSI53C140, pins B7 and A3 should be pulled to GND to disable HVD mode when operating in SE or LVD mode. These two pins are no connects in the LSI53C180.

The LSI53C180 has an independent RBIAS pin to control margining for each bus, rather than a single pin for both buses as implemented in the LSI53C140. A 10 kΩ pull-up resistor on RBIAS is recommended to provide the correct margining. If initially designing for the LSI53C140 with the intention of upgrading to the LSI53C180 at a later time, a footprint from the pull-up resistor for the A-RBIAS signal should be implemented.

Table B.1 summarizes the information in the previous paragraphs.

Table B.1 Pin Adjustments

Pin Number	LSI53C140 Signal	LSI53C180 Signal
K17	NC	A-RBIAS
B7	A_HVD_MODE	NC
A3	B_HVD_MODE	NC

Table B.2 lists all of the no connect pins for the LSI53C140 and LSI53C180.

Table B.2 No Connect Pins

Signal	No Connect (NC) Pins
LSI53C140	D3, F3, L2, T1, U1, R4, U6, R10, R12, U16, U17, P15, H15, F15, C15, C14, A17, A5, C6, B4, A4, C4, B3
LSI53C180	D3, F3, L2, T1, U1, R4, U6, R10, R12, U16, U17, P15, H15, F15, C15, C14, A17, A5, C6, B4, A4, C4, B3, A3, B7

Appendix C
Glossary

ACK/	Acknowledge – Driven by an initiator, ACK/ indicates an acknowledgment or a SCSI data transfer. In the target mode, ACK/ is received as a response to the REQ/ Signal.
ANSI	American National Standards Institute.
Arbitration	The process of selecting one respondent from a collection of several candidates that request service concurrently.
Asserted	A signal is asserted when it is in the state that is indicated by the name of the signal. Opposite of negated or deasserted.
Assertion	The act of driving a signal to the true state.
Asynchronous Transmission	Transmission in which each byte of the information is synchronized individually through the use of Request (REQ/) and Acknowledge (ACK/) signals.
ATN/	Attention – Driven by an initiator, indicates an attention condition. In the target role, ATN/ is received and is responded to by entering the Message Out Phase.
Block	A block is the basic 512 byte size of storage that the storage media is divided into. The Logical Block Address protocol uses sequential block addresses to access the media.
BSY/	Busy – Indicates that the SCSI Bus is being used. BSY/ can be driven by the initiator or the target device.
Bus	A collection of unbroken signal lines that interconnect computer modules. The connections are made by taps on the lines.
Bus Expander	Bus expander technology permits the extension of a bus by providing some signal filtering and retiming to maintain signal skew budgets.

Cable Skew Delay Cable skew delay is the minimum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices.

C_D/ Control/Data – Driven by a target. When asserted, indicates Control or Data Information is on the SCSI Bus. This signal is received by the initiator.

Connect The function that occurs when an initiator selects a target to start an operation, or a target reselects an initiator to continue an operation.

Control Signals The set of nine lines used to put the SCSI bus into its different phases. The combinations of asserted and negated control signals define the phases.

Controller A computer module that interprets signals between a host and a peripheral device. Often, the controller is a part of the peripheral device, such as circuitry on a disk drive.

DB[7:0]/ SCSI Data Bits – These eight Data Bits (DB[7:0]/), plus a Parity Bit (DBP/), form the SCSI Bus. DB7/ is the most significant bit and has the highest priority ID during the Arbitration Phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.

Deasserted The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

A signal is deasserted or negated when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.

Device A single unit on the SCSI bus, identifiable by a SCSI address. It can be a processor unit, a storage unit (such as a disk or tape controller or drive), an output unit (such as a controller or printer), or a communications unit.

Differential A signaling alternative that employs differential drivers and receivers to improve signal-to-noise ratios and increase maximum cable lengths.

Disconnect The function that occurs when a target releases control of the SCSI bus, allowing the bus to go to the Bus Free phase.

Driver When used in the context of electrical configuration, “driver” is the circuitry that creates a signal on a line.

External Configuration	All SCSI peripheral devices are external to the host enclosure.
External Terminator	The terminator that exists on the last peripheral device that terminates the end of the external SCSI bus.
Free	In the context of Bus Free phase, “free” means that no SCSI device is actively using the SCSI bus and, therefore, the bus is available for use.
Host	A processor, usually consisting of the central processing unit and main memory. Typically, a host communicates with other devices, such as peripherals and other hosts. On the SCSI bus, a host has a SCSI address.
Host Adapter	Circuitry that translates between a processor's internal bus and a different bus, such as SCSI. On the SCSI bus, a host adapter usually acts as an initiator.
Initiator	A SCSI device that requests another SCSI device (a target) to perform an operation. Usually, a host acts as an initiator and a peripheral device acts as a target.
Internal Configuration	All SCSI peripheral devices are internal to the host enclosure.
Internal Terminator	The terminator that exists within the host that terminates the internal end of the SCSI bus.
I/O	Input/Output – Driven by a target. I/O controls the direction of data transfer on the SCSI Bus. When active, this signal indicates input to the initiator. When inactive, this signal indicates output from the initiator. This signal is also used to distinguish between the Selection and Reselection Phases.
I/O Cycle	An I/O cycle is an Input (I/O Read) operation or Output (I/O Write) operation that accesses the PC Card’s I/O address space.
Logical Unit	The logical representation of a physical or virtual device, addressable through a target. A physical device can have more than one logical unit.
Low (logical level)	A signal is at the low logic level when it is below approximately 0.5 volts.

LSB	Abbreviation for Least Significant Bit or Least Significant Byte. That portion of a number, address or field that occurs right-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the least weight in a mathematical calculation using the value.
LUN	Logical Unit Number. Used to identify a logical unit.
Mandatory	A characteristic or feature that must be present in every implementation of the standard.
MHz	MegaHertz – Measurement in millions of Hertz per second. Used as a measurement of data transfer rate.
microsecond (μs)	One millionth of a second.
MSB	Abbreviation for Most Significant Bit or Most Significant Byte. That portion of a number, address or field that occurs left-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the most weight in a mathematical calculation using the value.
MSG/	Message – Driven active by a target during the Message Phase. This signal is received by the initiator.
nanosecond (ns)	One billionth of a second.
Negated	A signal is negated or deasserted when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.
Negation	The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state.
Parity	A method of checking the accuracy of binary numbers. An extra bit, called a parity bit, is added to a number. If even parity is used, the sum of all 1s in the number and its corresponding parity is always even. If odd parity is used, the sum of the 1s and the parity bit is always odd.
Peripheral device	A device that can be attached to the SCSI bus. Typical peripheral devices are disk drives, tape drives, printers, CD ROMs, or communications units.
Phase	One of the eight states to which the SCSI bus can be set. During each phase, different communication tasks can be performed.
Port	A connection into a bus.

Priority	The ranking of the devices on the bus during arbitration.
Protocol	A convention for data transmission that encompasses timing control, formatting, and data representation.
Receiver	The circuitry that receives electrical signals on a line.
Reconnect	The function that occurs when a target reselects an initiator to continue an operation after a disconnect.
Release	The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).
REQ/	Request – Driven by a target, indicates a request for a SCSI data-transfer handshake. This signal is received by the initiator.
Reselect	A target can disconnect from an initiator in order to perform a time-consuming function, such as a disk seek. After performing the operation, the target can “reselect” the initiator.
RESET	Reset – Clears all internal registers when active. It does not assert the SCSI RST/ signal and therefore does not reset the SCSI bus.
RST	Reset – Indicates a SCSI Bus reset condition.
SCSI	Small Computer System Interface.
SCSI Address	The octal representation of the unique address ([7:0]) assigned to a SCSI device. This address is normally assigned and set in the SCSI device during system installation.
SCSI ID Identification) or SCSI Device ID	The bit-significant representation of the SCSI address referring to one of the signal lines DB7/ through DB0/.
SCAM	An acronym for SCSI Configured AutoMatically. SCAM is the new SCSI automatic ID assignment protocol. SCAM frees SCSI users from locating and setting SCSI ID switches and jumpers. SCAM is the key part of Plug and Play SCSI.
SDTR	Synchronous Data Transfer Request messages are used to negotiate a synchronous data transfer agreement between two SCSI devices. An SDTR agreement applies to all logical units of the two SCSI devices that negotiated agreement.
SEL/	Select – Used by an initiator to select a target, or by a target to reselect an initiator.

Single-Ended Configuration An electrical signal configuration that uses a single line for each signal, referenced to a ground path common to the other signal lines. The advantage of a single-ended configuration is that it uses half the pins, chips, and board area that differential/low-voltage differential configurations require. The main disadvantage of single-ended configurations is that they are vulnerable to common mode noise. Also, cable lengths are limited.

Synchronous Transmission Transmission in which the sending and receiving devices operate continuously at the same frequency and are held in a desired phase relationship by correction devices. For buses, synchronous transmission is a timing protocol that uses a master clock and has a clock period.

Target A SCSI device that performs an operation requested by an initiator.

Termination The electrical connection at each end of the SCSI bus, composed of a set of resistors.

µs Microsecond. One millionth of a second.

WDTR Wide Data Transfer Request messages are used to negotiate a wide data transfer agreement between two SCSI devices. A WDTR agreement applies to all logical units of the two SCSI devices that negotiated the agreement.

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