

TECHNICAL MANUAL

LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller

September 2003

Version 2.2

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Document DB14-000156-05, Version 2.2 (September 2003)

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Preface

This book is the primary reference and technical manual for the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller. It contains a functional description for the LSI53C1030 and the physical and electrical specifications for the LSI53C1030.

Audience

This document assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the LSI53C1030 for use in a system
 - Engineers who are designing the LSI53C1030 into a system
-

Organization

This document has the following chapters and appendixes:

- [Chapter 1, Introduction](#), provides an overview of the LSI53C1030 features and capabilities.
- [Chapter 2, Functional Description](#), provides a detailed functional description of the LSI53C1030 operation. This chapter describes how the LSI53C1030 implements the PCI, PCI-X, and SCSI bus specifications.
- [Chapter 3, Signal Description](#), provides a detailed signal description for the LSI53C1030.
- [Chapter 4, PCI Host Register Description](#), provides a bit level description of the host register set of the LSI53C1030.

- [Chapter 5, Specifications](#), provides the electrical and physical specifications for the device.
- [Appendix A, Register Summary](#), provides a register map for the LSI53C1030.

Related Publications

LSI Logic Documents

Fusion-MPT Device Management User's Guide, Version 2.0, DB15-000186-02
Integrated RAID User's Guide, Version 1.0, DB15-000292-00

LSI Logic World Wide Web Home Page

www.lsillogic.com

ANSI

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New York, NY 10036
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Global Engineering Documents

15 Inverness Way East
Englewood, CO 80112
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ENDL Publications

14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference*, *SCSI Encyclopedia*, *SCSI Tutor*

Prentice Hall

113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

SCSI Electronic Bulletin Board

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Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized*.

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end with a “/.”

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Revision History

Revision	Date	Remarks
Version 2.2	9/2003	Corrected SCSI clock period and LOW/HIGH times in Table 5.13. Updated references to Integrated RAID (IR).
Version 2.1	6/2003	Updated the external memory timing diagrams. Updated the default Subsystem ID value. Updated the ZCR behavior description. Updated the Multi-ICE test interface description.
Version 2.0	4/2002	Added register summary appendix. Updated the electrical characteristics. Updated the Index.
Preliminary Version 1.0	12/2001	Updated the description of Fusion-MPT architecture in Chapter 1. Updated External Memory Interface descriptions in Chapter 2. Added Test Interface description to Chapter 2. Added Zero Channel RAID interface description to Chapters 2 and 3. Updated the MAD Power-On Sense pin description in Chapter 3. Updated signal descriptions and lists to include the ZCR-related pins. Updated electrical and environmental characteristics in Chapter 5. Removed figures relating to SE SCSI electrical and timing characteristics from Chapter 5. Removed SCSI timing information from Chapter 5 and referred readers to the SCSI specification. Removed PSBRAM interface and all related information.

Revision	Date	Remarks
Advance Version 0.1	2/2001	Initial release of document.

Contents

Chapter 1	Introduction	
1.1	General Description	1-1
1.2	Benefits of the Fusion-MPT Architecture	1-5
1.3	Benefits of PCI-X	1-6
1.4	Benefits of Ultra320 SCSI	1-7
1.5	Benefits of SureLINK (Ultra320 SCSI Domain Validation)	1-8
1.6	Benefits of LVDlink Technology	1-8
1.7	Benefits of TolerANT® Technology	1-9
1.8	Summary of LSI53C1030 Features	1-10
1.8.1	SCSI Performance	1-10
1.8.2	PCI Performance	1-11
1.8.3	Integration	1-12
1.8.4	Flexibility	1-12
1.8.5	Reliability	1-13
1.8.6	Testability	1-13

Chapter 2	Functional Description	
2.1	Block Diagram Description	2-2
2.1.1	Host Interface Module Description	2-3
2.1.2	SCSI Channel Module Description	2-6
2.2	Fusion-MPT Architecture Overview	2-6
2.3	PCI Functional Description	2-8
2.3.1	PCI Addressing	2-8
2.3.2	PCI Commands and Functions	2-9
2.3.3	PCI Arbitration	2-15
2.3.4	PCI Cache Mode	2-15
2.3.5	PCI Interrupts	2-15
2.3.6	Power Management	2-16

2.4	Ultra320 SCSI Functional Description	2-18
2.4.1	Ultra320 SCSI Features	2-18
2.4.2	SCSI Bus Interface	2-23
2.5	External Memory Interface	2-24
2.5.1	Flash ROM Interface	2-24
2.5.2	NVSRAM Interface	2-26
2.6	Serial EEPROM Interface	2-27
2.7	Zero Channel RAID	2-28
2.8	Multi-ICE Test Interface	2-30

Chapter 3

Signal Description

3.1	Signal Organization	3-2
3.2	PCI Bus Interface Signals	3-4
3.2.1	PCI System Signals	3-4
3.2.2	PCI Address and Data Signals	3-5
3.2.3	PCI Interface Control Signals	3-6
3.2.4	PCI Arbitration Signals	3-7
3.2.5	PCI Error Reporting Signals	3-7
3.2.6	PCI Interrupt Signals	3-8
3.3	PCI-Related Signals	3-9
3.4	SCSI Interface Signals	3-10
3.4.1	SCSI Channel [0] Signals	3-10
3.4.2	SCSI Channel [1] Signals	3-13
3.5	Memory Interface	3-14
3.6	Zero Channel RAID Interface	3-16
3.7	Test Interface	3-17
3.8	GPIO and LED Signals	3-19
3.9	Power and Ground Pins	3-20
3.10	Power-On Sense Pins Description	3-21
3.11	Internal Pull-Ups and Pull-Downs	3-25

Chapter 4

PCI Host Register Description

4.1	PCI Configuration Space Register Description	4-1
4.2	PCI I/O Space and Memory Space Register Description	4-28

Chapter 5

Specifications

5.1	DC Characteristics	5-1
-----	--------------------	-----

5.2	TolerANT Technology Electrical Characteristics	5-7
5.3	AC Characteristics	5-9
5.4	External Memory Timing Diagrams	5-11
5.4.1	NVSRAM Timing	5-11
5.4.2	Flash ROM Timing	5-15
5.5	Package Drawings	5-18

Appendix A	Register Summary
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Index

Customer Feedback

Figures

1.1	Typical LSI53C1030 Board Application	1-3
1.2	Typical LSI53C1030 System Application	1-4
2.1	LSI53C1030 Block Diagram	2-3
2.2	Paced Transfer Example	2-20
2.3	Example of Precompensation	2-21
2.4	Flash ROM Block Diagram	2-25
2.5	NVSRAM Diagram	2-27
2.6	ZCR Circuit Diagram for LSI53C1030 and LSI53C1010R	2-29
3.1	LSI53C1030 Functional Signal Grouping	3-3
5.1	LVD Driver	5-3
5.2	LVD Receiver	5-4
5.3	Rise and Fall Time Test Condition	5-8
5.4	SCSI Input Filtering	5-9
5.5	External Clock	5-10
5.6	Reset Input	5-10
5.7	Interrupt Output	5-11
5.8	NVSRAM Read Cycle	5-12
5.8	NVSRAM Read Cycle (Cont.)	5-12
5.9	NVSRAM Write Cycle	5-14
5.9	NVSRAM Write Cycle (Cont.)	5-14
5.10	Flash ROM Read Cycle	5-15
5.10	Flash ROM Read Cycle (Cont.)	5-16
5.11	Flash ROM Write Cycle	5-17
5.11	Flash ROM Write Cycle (Cont.)	5-17
5.12	LSI53C1030 456-Pin BGA Top View	5-20
5.12	LSI53C1030 456-Pin BGA Top View (Cont.)	5-21
5.13	456-Pin EPBGA (KY) Mechanical Drawing	5-26

Tables

2.1	PCI/PCI-X Bus Commands and Encodings	2-10
2.2	Power States	2-16
2.3	Flash ROM Size Programming	2-24
2.4	Flash Signature Value	2-26
2.5	PCI Configuration Record in Serial EEPROM	2-28
2.6	20-Pin Multi-ICE Header Pinout	2-30
3.1	PCI System Signals	3-4
3.2	PCI Address and Data Signals	3-5
3.3	PCI Interface Control Signals	3-6
3.4	PCI Arbitration Signals	3-7
3.5	PCI Error Reporting Signals	3-7
3.6	PCI Interrupt Signals	3-8
3.7	PCI-Related Signals	3-9
3.8	SCSI Bus Clock Signal	3-10
3.9	SCSI Channel [0] Interface Signals	3-10
3.10	SCSI Channel [0] Control Signals	3-12
3.11	SCSI Channel [1] Interface Signals	3-13
3.12	SCSI Channel [1] Control Signals	3-14
3.13	Flash ROM/NVSRAM Interface Pins	3-14
3.14	Serial EEPROM Interface Pins	3-16
3.15	ZCR Configuration Pins	3-16
3.16	JTAG, ICE, and Debug Pins	3-17
3.17	LSI Logic Test Pins	3-18
3.18	GPIO and LED signals	3-19
3.19	Power and Ground Pins	3-20
3.20	MAD Power-On Sense Pin Options	3-21
3.21	PCI-X Function to SCSI Channel Configurations	3-24
3.22	Flash ROM Size Programming	3-24
3.23	Pull-Up and Pull-Down Conditions	3-25
4.1	LSI53C1030 PCI Configuration Space Address Map	4-2
4.2	Subsystem ID Register Download Conditions and Values	4-13
4.3	Multiple Message Enable Field Bit Encoding	4-22
4.4	Maximum Outstanding Split Transactions	4-25
4.5	Maximum Memory Read Count	4-25
4.6	PCI I/O Space Address Map	4-29
4.7	PCI Memory [0] Address Map	4-29

4.8	PCI Memory [1] Address Map	4-29
4.9	Interrupt Signal Routing	4-36
5.1	Absolute Maximum Stress Ratings	5-2
5.2	Operating Conditions	5-2
5.3	LVD Driver SCSI Signals— SACK \pm , SATN \pm , SBSY \pm , SCD \pm , SD[15:0] \pm , SDP[1:0] \pm , SIO \pm , SMSG \pm , SREQ \pm , SRST \pm , SSEL \pm	5-3
5.4	LVD Receiver SCSI Signals— SACK \pm , SATN \pm , SBSY \pm , SCD \pm , SD[15:0] \pm , SDP[1:0] \pm , SIO \pm , SMSG \pm , SREQ \pm , SRST \pm , SSEL \pm	5-3
5.5	A_DIFFSENS and B_DIFFSENS SCSI Signals	5-4
5.6	Input Capacitance	5-4
5.7	8 mA Bidirectional Signals — GPIO[7:0], MAD[15:0], MADP[1:0], SerialDATA	5-5
5.8	8 mA PCI Bidirectional Signals — ACK64/, AD[63:0], C_BE[7:0]/, DEVSEL/, FRAME/, IRDY/, PAR, PAR64, PERR/, REQ64/, SERR/, STOP/, TRDY/	5-5
5.9	Input Signals — CLK, CLKMODE_0, CLKMODE_1, DIS_PCI_FSN/, DIS_SCSI_FSN/, GNT/, IDDTN, IDSEL, IOPD_GNT/, PVT1, PVT2, SCANEN, SCANMODE, SCLK, TCK_CHIP, TCK_ICE, TESTACLK, TESTCLKEN, TESTHCLK, TDI_CHIP, TDI_ICE, TMS_CHIP, TMS_ICE, TN, TRST_ICE/, TST_RST/, ZCR_EN/	5-6
5.10	8 mA Output Signals — ADSC/, ADV/, ALT_INTA/, ALT_INTB/, BWE[1:0]/, FLSHALE[1:0]/, FLSHCE/, INTA/, INTB/, MCLK, MOE/, PIPESTAT[2:0], RAMCE/, REQ/, RTCK_ICE, SerialCLK, SERR/, TDO_CHIP, TDO_ICE, TRACECLK, TRACEPKT[7:0], TRACESYNC	5-6
5.11	12 mA Output Signals — A_LED/, B_LED/, HB_LED/	5-6
5.12	TolerANT Technology Electrical Characteristics for SE SCSI Signals	5-7
5.13	External Clock	5-9
5.14	Reset Input	5-10
5.15	Interrupt Output	5-10
5.16	NVSRAM Read Cycle Timing	5-11
5.17	NVSRAM Write Cycle	5-13
5.18	Flash ROM Read Cycle Timing	5-15
5.19	Flash ROM Write Cycle	5-16
A.1	LSI53C1030 PCI Registers	A-1

A.2	LSI53C1030 PCI I/O Space Registers	A-3
A.3	LSI53C1030 PCI I/O Space Registers	A-4

Chapter 1

Introduction

This chapter provides a general overview of the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller. This chapter contains the following sections:

- [Section 1.1, “General Description”](#)
- [Section 1.2, “Benefits of the Fusion-MPT Architecture”](#)
- [Section 1.3, “Benefits of PCI-X”](#)
- [Section 1.4, “Benefits of Ultra320 SCSI”](#)
- [Section 1.5, “Benefits of SureLINK \(Ultra320 SCSI Domain Validation\)”](#)
- [Section 1.6, “Benefits of LVDlink Technology”](#)
- [Section 1.7, “Benefits of TolerANT® Technology”](#)
- [Section 1.8, “Summary of LSI53C1030 Features”](#)

1.1 General Description

The LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller brings Ultra320 SCSI performance to host adapter, workstation, and server designs, making it easy to add a high-performance SCSI bus to any PCI or PCI-X system. The LSI53C1030 supports both the *PCI Local Bus Specification, Revision 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*.¹

1. In some instances, this manual references PCI-X explicitly. References to the PCI bus may be inclusive of both the PCI specification and PCI-X addendum, or they may refer only to the PCI bus depending on the operating mode of the device.

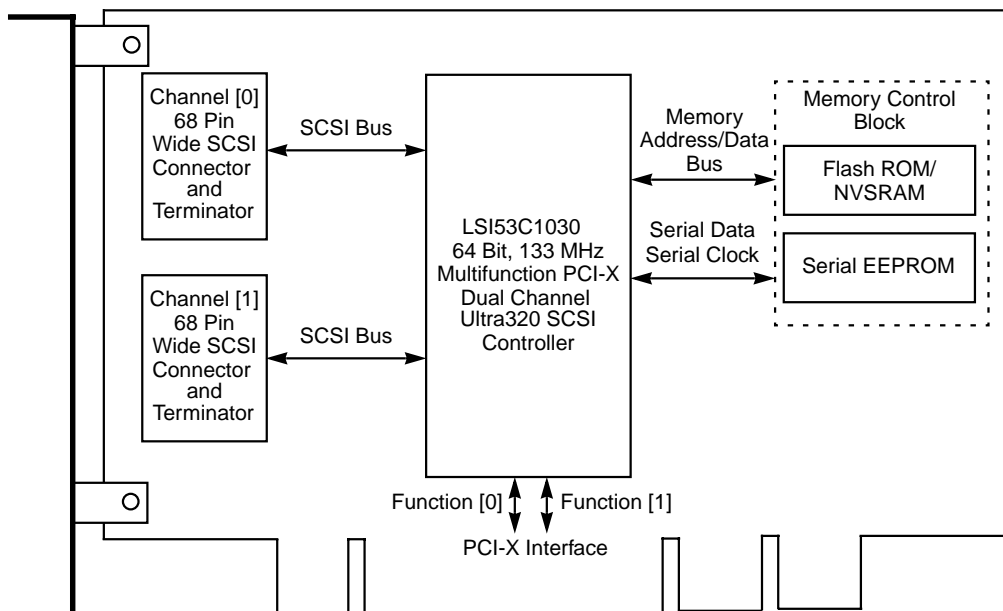
The LSI53C1030 is pin compatible with the LSI53C1010R PCI to Dual Channel Ultra160 SCSI Multifunction Controller to provide an easy and safe migration path to Ultra320 SCSI. The LSI53C1030 supports up to a 64-bit, 133 MHz PCI-X bus. The Ultra320 SCSI features for the LSI53C1030 include: double transition (DT) clocking, packetized protocol, paced transfers, quick arbitrate and select (QAS), skew compensation, intersymbol interference (ISI) compensation, cyclic redundancy check (CRC), and domain validation technology. These features comply with the American National Standard Institute (ANSI) T10 SCSI Parallel Interface-4 (SPI-4) draft specification.

DT clocking enables the LSI53C1030 to achieve data transfer rates of up to 320 megabytes per second (Mbytes/s) on each SCSI channel, for a total bandwidth of 640 Mbytes/s on both SCSI channels. Packetized protocol increases data transfer capabilities with SCSI information units. QAS minimizes SCSI bus latency by allowing the bus to directly enter the arbitration/selection bus phase after a SCSI disconnect and skip the bus free phase. Skew compensation permits the LSI53C1030 to adjust for cable and bus skew on a per-device basis. Paced transfers enable high speed data transfers during DT data phases by using the REQ/ACK transition as a free running data clock. Precompensation enables the LSI53C1030 to adjust the signal drive strength to compensate for the charge present on the cable. CRC improves the SCSI data transmission integrity through enhanced detection of communication errors.

SureLINK™ Domain Validation detects the SCSI bus configuration and adjusts the SCSI transfer rate to optimize bus interoperability and SCSI data transfer rates. SureLINK Domain Validation provides three levels of domain validation, assuring robust system operation.

The LSI53C1030 supports a local memory bus, which supports a standard serial EEPROM and allows local storage of the BIOS in Flash ROM memory. The LSI53C1030 supports programming of local Flash ROM memory for BIOS updates. Figure 1.1 shows a typical LSI53C1030 board application connected to external ROM memory.

Figure 1.1 Typical LSI53C1030 Board Application

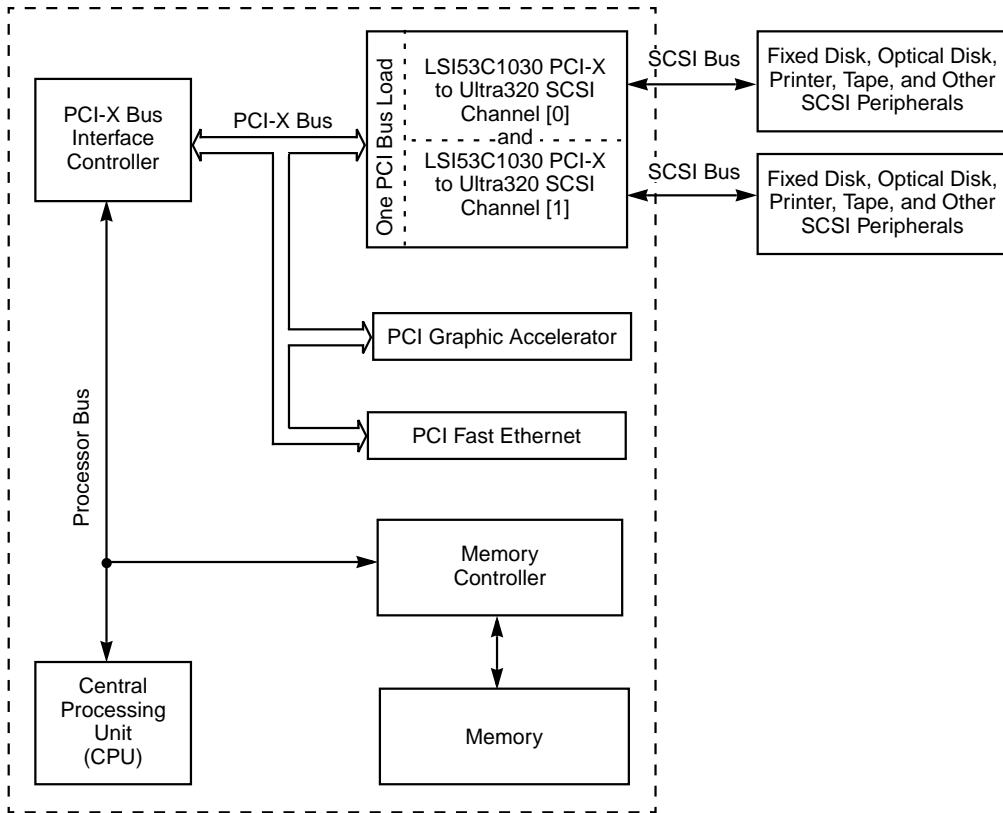


The LSI53C1030 integrates two high-performance SCSI Ultra320 cores and a 64-bit, 133 MHz PCI-X bus master DMA core. The LSI53C1030 employs three ARM966E-S processors to meet the data transfer flexibility requirements of the Ultra320 SCSI, PCI, and PCI-X specifications. Separate ARM[®] processors support each SCSI channel and the PCI/PCI-X interface.

These processors implement the LSI Logic Fusion-MPT™ architecture, a multithreaded I/O algorithm that supports data transfers between the host system and SCSI devices with minimal host processor intervention. Fusion-MPT technology provides an efficient architecture that solves the protocol overhead problems of previous intelligent and nonintelligent adapter designs.

LVDlink™ technology is the LSI Logic implementation of Low Voltage Differential (LVD) SCSI. LVDlink transceivers allow the LSI53C1030 to perform either Single-Ended (SE) or LVD transfers. [Figure 1.2](#) illustrates a typical LSI53C1030 system application.

Figure 1.2 Typical LSI53C1030 System Application



The LSI Logic Integrated RAID solution provides cost benefits for the server or workstation market where the extra performance, storage capacity, and/or redundancy of a RAID configuration are required. The two components of Integrated RAID are:

- **Integrated Mirroring™ (IM)**, which provides features of RAID 1 and RAID 1E. IM provides physical mirroring of the boot volume through LSI53C1030 firmware. This feature provides extra reliability for the system's boot volume without burdening the host CPU. The runtime mirroring of the boot drive is transparent to the BIOS, drivers, and operating system.
- **Integrated Striping™ (IS)**, which provides features of RAID 0. The IS feature writes data across multiple disks instead of onto one disk. This is accomplished by partitioning each disk's storage space into

64 Kbyte stripes. These stripes are interleaved round-robin, so that the combined storage space is composed alternately of stripes from each disk.

The LSI Logic Fusion-MPT architecture provides the interface to the SCSI chip/firmware to enable Integrated Striping and Integrated Mirroring. LSI Logic's CIM interface software is used to continuously monitor IM volumes and IS volumes and to report status and error conditions as they arise.

A BIOS-based configuration utility is provided to create the IM and IS volumes. A DOS-based configuration utility is also provided for use on the manufacturing floor.

For more information about the LSI Logic Integrated RAID solution, see the *Integrated RAID User's Guide*, DB15-000292-00.

1.2 Benefits of the Fusion-MPT Architecture

The Fusion-MPT architecture provides an open architecture that is ideal for SCSI, Fibre Channel, and other emerging interfaces. The I/O interface is interchangeable at the system and application level; embedded software uses the same device interface for SCSI and Fibre Channel implementations just as application software uses the same storage management interfaces for SCSI and Fibre Channel implementations. LSI Logic provides Fusion-MPT device drivers that are binary compatible between Fibre Channel and Ultra320 SCSI interfaces.

The Fusion-MPT architecture improves overall system performance by requiring only a thin device driver, which off loads the intensive work of managing SCSI I/Os from the system processor to the LSI53C1030. Developed from the proven LSI Logic SDMS™ solution, the Fusion-MPT architecture delivers unmatched performance of up to 100,000 Ultra320 SCSI I/Os per second with minimal system overhead or device maintenance. The use of thin, easy to develop, common OS device drivers accelerates time to market by reducing device driver development and certification times.

The Fusion-MPT architecture provides an *interrupt coalescing* feature. Interrupt coalescing allows an I/O controller to send multiple reply messages in a single interrupt to the host processor. Sending multiple

reply messages per interrupt reduces context switching of the host processor and maximizes the host processor efficiency, which results in a significant improvement of system performance. To use the interrupt coalescing feature, the host processor must be able to accept and manage multiple replies per interrupt.

The Fusion-MPT architecture also provides built-in device driver stability since the device driver need not change for each revision of the LSI53C1030 silicon or firmware. This architecture is a reliable, constant interface between the host device driver and the LSI53C1030. Changes within the LSI53C1030 are transparent to the host device driver, operating system, and user. The Fusion-MPT architecture also saves the user significant development and maintenance effort since it is not necessary to alter or redevelop the device driver when a revision of the LSI53C1030 device or firmware occurs.

1.3 Benefits of PCI-X

PCI-X doubles the maximum clock frequency of the conventional PCI bus. The *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*, defines enhancements to the proven *PCI Local Bus Specification, Revision 2.2*. PCI-X provides more efficient data transfers by enabling registered inputs and outputs, improves buffer management by including transaction information with each data transfer, and reduces bus overhead by restricting the use of wait states and disconnects. PCI-X also reduces host processor overhead by providing a wide range of error recovery implementations.

The LSI53C1030 supports up to a 133 MHz, 64-bit PCI-X bus and is backward compatible with previous versions of the PCI/PCI-X specification. The LSI53C1030 is a true multifunction PCI-X device and presents a single electrical load to the PCI bus. The LSI53C1030 uses a single REQ/-GNT/ pair to arbitrate for PCI bus mastership. Separate interrupt signals for PCI Function [0] and PCI Function [1] allow independent control of the two PCI functions.

Per the PCI-X addendum, the LSI53C1030 includes transaction information with all PCI-X transactions to enable more efficient buffer management schemes. Each PCI-X transaction contains a transaction sequence identifier (Tag), the identity of the initiator, and the number of

bytes in the sequence. The LSI53C1030 clocks PCI-X data directly into and out of registers, which creates a more efficient data path. The LSI53C1030 increases bus efficiency since it does not insert wait states after the initial data phase when acting as a PCI-X target and never inserts wait states when acting as a PCI-X initiator.

1.4 Benefits of Ultra320 SCSI

Ultra320 SCSI is an extension of the SPI-4 draft specification that allows faster synchronous SCSI data transfer rates than Ultra160 SCSI. When enabled, Ultra320 SCSI performs 160 megatransfers per second resulting in approximately double the synchronous data transfer rates of Ultra160 SCSI. The LSI53C1030 performs 16-bit, Ultra320 SCSI synchronous data transfers as fast as 320 Mbytes/s on each SCSI channel. This advantage is most noticeable in heavily loaded systems or large block size applications, such as video on-demand and image processing.

Ultra320 SCSI doubles both the data and clock frequencies from Ultra160 SCSI. Due to the increased data and clock speeds, Ultra320 SCSI introduces skew compensation and intersymbol interference (ISI) compensation. These new features simplify system design by resolving timing issues at the chip level. Skew compensation adjusts for timing differences between data and clock signals caused by cabling, board traces, etc. ISI compensation enhances the first pulse after a change in state to ensure data integrity.

Ultra320 SCSI includes CRC, which offers higher levels of data reliability by ensuring complete integrity of transferred data. CRC is a 32-bit scheme, referred to as CRC-32. CRC guarantees detection of all single or double bit errors, as well as any combination of bit errors within a single 32-bit range.

1.5 Benefits of SureLINK (Ultra320 SCSI Domain Validation)

SureLINK Domain Validation software ensures robust SCSI interconnect management and low risk Ultra320 SCSI implementations by extending the domain validation guidelines documented in the SPI-4 specifications. Domain validation verifies that the system is capable of transferring data at Ultra320 SCSI speeds, allowing the LSI53C1030 to renegotiate to a lower data transfer speed and bus width if necessary. SureLINK Domain Validation is the software control for the domain validation manageability enhancements in the LSI53C1030. SureLINK Domain Validation software provides domain validation management at boot time as well as during system operation.

SureLINK Domain Validation ensures robust system operation by providing 3 levels of integrity checking on a per-device basis: Basic (Level 1) with inquiry command, Enhanced (Level 2) with read/write buffer and Margined (Level 3) with margining of drive strength and slew rates.

1.6 Benefits of LVDlink Technology

The LSI53C1030 supports Low Voltage Differential (LVD) through LVDlink technology. This signalling technology increases the reliability of SCSI data transfers over longer distances than are supported by SE (Single Ended) SCSI. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. To allow the use of the LSI53C1030 in both legacy and Ultra320 SCSI applications, this device features universal LVDlink transceivers that support LVD SCSI and SE SCSI.

1.7 Benefits of TolerANT[®] Technology

The LSI53C1030 features TolerANT technology, which provides active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven high rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps ensure correct clocking of data. TolerANT input signal filtering is a built-in feature of the LSI53C1030 and all LSI Logic Fast SCSI, Ultra SCSI, Ultra2 SCSI, Ultra160 SCSI, and Ultra320 SCSI devices.

TolerANT technology increases noise immunity, balances duty cycles, and improves SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power-up or power-down, which protects other devices on the bus from data corruption. When used with the LVDSLink transceivers, TolerANT technology provides excellent signal quality and data reliability in real world cabling environments. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

1.8 Summary of LSI53C1030 Features

This section provides a summary of the LSI53C1030 features and benefits. It contains information on [SCSI Performance](#), [PCI Performance](#), [Integration](#), [Flexibility](#), [Reliability](#), and [Testability](#).

1.8.1 SCSI Performance

The LSI53C1030 contains the following SCSI performance features:

- Supports Ultra320 SCSI
 - Paced transfers using a free running clock
 - 320 Mbyte/s data transfer rate on each SCSI channel
 - Mandatory packetized protocol
 - Quick arbitrate and select (QAS)
 - Skew compensation with bus training
 - Transmitter precompensation to overcome ISI effects for SCSI data signals
 - Retained training information (RTI)
- Offers a performance optimized architecture
 - Three ARM966E-S processors provide high performance with low latency
 - Two independent Ultra320 SCSI channels
 - Designed for optimal packetized performance
- Uses proven integrated LVDlink transceivers for direct attach to either LVD or SE SCSI buses with precision-controlled slew rates
- Supports expander communication protocol (ECP)
- Uses the Fusion-MPT (Message Passing Technology) drivers to provide support for Windows, Linux, Solaris, SCO Openserver, UnixWare, OpenUnix 8, and NetWare operating systems

1.8.2 PCI Performance

The LSI53C1030 supports these PCI features:

- Has a 133 MHz, 64-bit PCI/PCI-X interface that:
 - Operates at 33 MHz or 66 MHz PCI
 - Operates at up to 133 MHz PCI-X
 - Supports 32-bit or 64-bit data
 - Supports 32-bit or 64-bit addressing through Dual Address Cycles (DAC)
 - Provides a theoretical 1066 Mbytes/s zero wait state transfer rate
 - Complies with the *PCI Local Bus Specification, Revision 2.2*
 - Complies with the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*
 - Complies with *PCI Power Management Interface Specification, Revision 1.1*
 - Complies with *PC2001 System Design Guide*
- Offers unmatched performance through the Fusion-MPT architecture
- Provides high throughput and low CPU utilization to off load the host processor
- Presents a single electrical load to the PCI Bus (True PCI Multifunction Device)
- Uses SCSI Interrupt Steering Logic (SISL) to provide alternate interrupt routing for RAID applications
- Reduces Interrupt Service Routine (ISR) overhead with interrupt coalescing
- Supports 32-bit or 64-bit data bursts with variable burst lengths
- Supports the PCI Cache Line Size register
- Supports the PCI Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands
- Supports the PCI-X Memory Read Dword, Split Completion, Memory Read Block, and Memory Write Block commands
- Supports up to 8 PCI-X outstanding split transactions
- Supports Message Signalled Interrupts (MSI)

1.8.3 Integration

These features make the LSI53C1030 easy to integrate:

- Is backward compatible with previous revisions of the PCI and SCSI specifications
- Is pin compatible with the LSI53C1010R PCI to Dual Channel Ultra160 SCSI Multifunction Controller
- Provides a low-risk migration path to Ultra320 SCSI from the LSI53C1010R
- Is a dual channel Ultra320 SCSI to PCI/PCI-X multifunction controller
- Supports a 32-bit or 64-bit PCI/PCI-X DMA bus master
- Reduces time to market with the Fusion-MPT architecture
 - Single driver binary for SCSI and Fibre Channel products
 - Thin, easy to develop drivers
 - Reduced integration and certification effort
- Provides integrated LVDlink transceivers

1.8.4 Flexibility

These features increase the flexibility of the LSI53C1030:

- Universal LVD transceivers are backward compatible with SE devices
- Provides a flexible programming interface to tune I/O performance or to adapt to unique SCSI devices
- Supports MSI or pin-based (INTx/ or ALT_INTx/) interrupt signalling
- Can respond with multiple SCSI IDs
- Is compatible with 3.3 V and 5.0 V PCI signalling
 - Drives and receives 3.3 V PCI signals
 - Receives 5.0 V PCI if the PCI5VBIAS pin connects to 5 V, but does not drive 5.0 V signals on the PCI bus

1.8.5 Reliability

These features enhance the reliability of the LSI53C1030:

- Supports intersymbol interference (ISI) compensation
- Provides 2 kV ESD protection on SCSI signals
- Provides latch-up protection greater than 150 mA
- Provides voltage feed-through protection
- Supports LSI Logic Integrated RAID (IR) solution to provide physical mirroring or striping of the boot volume
- Has a high proportion of power and ground pins
- Provides power and ground isolation of I/O pads and internal chip logic
- Supports CRC checking and generation in Double Transition (DT) phases
- Provides comprehensive SureLINK Domain Validation technology:
 - Basic (Level 1) with inquiry command
 - Enhanced (Level 2) with read/write buffer
 - Margined (Level 3) with margining of drive strength and slew rates
- Supports TolerANT technology, which provides:
 - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved SCSI transfer rates
 - Input signal filtering on SCSI receivers for improved data integrity, even in noisy cabling environments

1.8.6 Testability

These features enhance the testability of the LSI53C1030:

- Allows all SCSI signals to be accessed through programmed I/O
- Supports JTAG boundary scan
- Provides ARM Multi-ICE[®] for debugging purposes

Chapter 2

Functional Description

This chapter provides a subsystem level overview of the LSI53C1030, a discussion of the Fusion-MPT architecture, and a functional description of the LSI53C1030 interfaces. This chapter contains the following sections:

- [Section 2.1, “Block Diagram Description”](#)
- [Section 2.2, “Fusion-MPT Architecture Overview”](#)
- [Section 2.3, “PCI Functional Description”](#)
- [Section 2.4, “Ultra320 SCSI Functional Description”](#)
- [Section 2.5, “External Memory Interface”](#)
- [Section 2.6, “Serial EEPROM Interface”](#)
- [Section 2.7, “Zero Channel RAID”](#)
- [Section 2.8, “Multi-ICE Test Interface”](#)

The LSI53C1030 is a high performance, intelligent PCI-X to Dual Channel Ultra320 SCSI Multifunction Controller. The LSI53C1030 supports the *PCI Local Bus Specification, Revision 2.2*, the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*, and the proposed *SCSI Parallel Interface-4 (SPI-4)* draft standard.

The LSI53C1030 employs the LSI Logic Fusion-MPT architecture to ensure robust system performance, to support binary compatibility of host software between the LSI Logic SCSI and Fibre Channel products, and to significantly reduce software development time. Refer to the *Fusion-MPT Device Management User's Guide* for more information on the Fusion-MPT architecture.

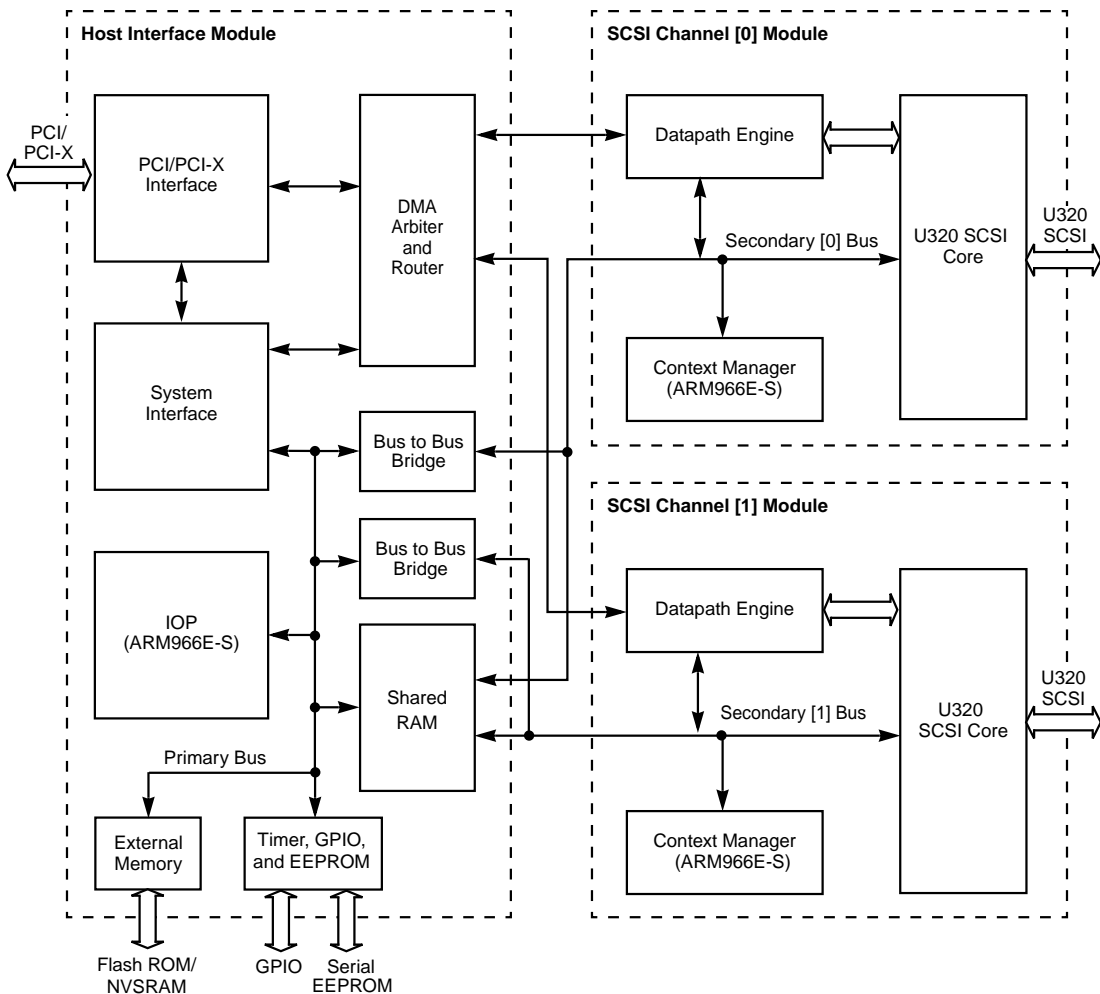
2.1 Block Diagram Description

The LSI53C1030 consists of three major modules: a host interface module and two independent Ultra320 SCSI channel modules. The modules consist of the following components:

- Host Interface Module
 - Up to a 64-bit, 133 MHz PCI/PCI-X Interface
 - System Interface
 - I/O Processor (IOP)
 - DMA Arbiter and Router
 - Shared RAM
 - External Memory Interface
 - ◊ Flash ROM Memory Controller
 - ◊ NVSRAM
 - Timer and Configuration Control
 - ◊ Device Configuration Controller
 - ◊ Serial EEPROM Interface Controller
 - ◊ GPIO Interface
 - ◊ Chip Timer
- Two independent Ultra320 SCSI Channel Modules
 - Datapath Engine
 - Context Manager
 - Ultra320 SCSI Core

[Figure 2.1](#) illustrates the relationship between these modules.

Figure 2.1 LSI53C1030 Block Diagram



2.1.1 Host Interface Module Description

The host interface module provides an interface between the host driver and the two SCSI channels. The host interface module controls system DMA transfers and the host side of the LSI Logic Fusion-MPT architecture. It also supports the external memory, serial EEPROM, and General Purpose I/O (GPIO) interfaces. This section provides a detailed explanation of the host interface submodules.

2.1.1.1 PCI Interface

The LSI53C1030 provides a PCI-X interface that supports up to a 64-bit, 133 MHz PCI-X bus. The interface is compatible with all previous implementations of the PCI specification. For more information on the PCI interface, refer to [Section 2.3, “PCI Functional Description.”](#)

2.1.1.2 System Interface

The system interface efficiently passes messages between the LSI53C1030 and other I/O agents using a high performance, packetized, mailbox architecture. The system interface coalesces PCI interrupts to minimize traffic on the PCI bus and maximize system performance.

All host accesses to the IOP, external memory, and timer and configuration subsystems pass through the system interface and use the primary bus. The host system initiates data transactions on the primary bus with the system interface registers. PCI Memory Space [0] and the PCI I/O Base Address registers identify the location of the system interface register set. [Chapter 4, “PCI Host Register Description,”](#) provides a bit level description of the system interface register set.

2.1.1.3 I/O Processor (IOP)

The LSI53C1030 I/O processor (IOP) is a 32-bit ARM966E-S RISC processor. The IOP controls the system interface and uses the LSI Logic Fusion-MPT architecture to manage the host side of non-DMA accesses to the Ultra320 SCSI bus. The context manager uses the Fusion-MPT architecture to control the SCSI side of data transfers. The IOP and Context Manager completely manage all SCSI I/Os without host intervention. Refer to [Section 2.2, “Fusion-MPT Architecture Overview,”](#) for more information on the Fusion-MPT architecture.

2.1.1.4 DMA Arbiter and Router

The descriptor based DMA Arbiter and Router subsystem manages the transfer of memory blocks between local memory and the host system. The DMA channel includes PCI bus master interface logic, the internal bus interface logic, and a 256-byte system DMA FIFO.

2.1.1.5 Shared RAM

The host interface module physically contains the 96 Kbyte shared RAM. However, both the host interface module and the SCSI channel modules access the shared RAM. The shared RAM holds a portion of the IOP and context manager firmware, as well as the request message queue and reply message queue. All non-DMA data transfers that use the request and reply message queues pass through the shared RAM.

2.1.1.6 External Memory Controller

The external memory control subsystem provides a direct interface between the primary bus and the external memory subsystem. MAD[7:0] and MADP[0] comprise the external memory bus. The LSI53C1030 supports the Flash ROM and NVSRAM interfaces through the external memory controller. The Flash ROM is optional if the LSI53C1030 is not the boot device and a suitable driver exists to initialize the device. The LSI53C1030 uses the NVSRAM for write journaling when an Integrated Mirroring (IM) volume is defined. Write journaling is used to verify that the mirrored disks in the IM volume are synchronized with each other. For a detailed description of this block refer to [Section 2.5, “External Memory Interface.”](#)

During power up or reset the LSI53C1030 uses the MAD[15:0] and MADP[1:0] signals as Power-On Sense pins, which configure the LSI53C1030 through their pull-up or pull-down settings. Refer to [Section 3.10, “Power-On Sense Pins Description,”](#) for a description of the Power-On Sense pin configuration options.

2.1.1.7 Timer, GPIO, and Configuration

This subsystem provides a free running timer to allow event time stamping and also controls the general purpose I/O (GPIO), LED, and serial EEPROM interfaces. The LSI53C1030 uses the free running timer to aid in tracking and managing SCSI I/Os. The LSI53C1030 generates the free running timer's microsecond time base by dividing the SCSI reference clock by 40.

The LSI53C1030 provides eight GPIO pins (GPIO[7:0]). These pins are under the control of the LSI53C1030 and default to the input mode upon PCI reset. The LSI53C1030 also provides three LED pins: A_LED/, B_LED/, and HB_LED/. Either firmware or hardware control A_LED/ and

B_LED/. The LSI53C1030 firmware controls HB_LED/ (heartbeat LED), which indicates that the IOP is operational.

A 2-wire serial interface provides a connection to a nonvolatile external serial EEPROM. The serial EEPROM stores PCI configuration parameters for the LSI53C1030. Refer to [Section 2.6, “Serial EEPROM Interface,”](#) for more information concerning the serial EEPROM.

2.1.2 SCSI Channel Module Description

The LSI53C1030 provides two independent Ultra320 SCSI bus channels. Separate Ultra320 SCSI cores, datapath engines, and context managers support each SCSI channel. Refer to [Section 2.4, “Ultra320 SCSI Functional Description,”](#) for an operational description of the LSI53C1030 SCSI bus channels.

2.1.2.1 Ultra320 SCSI Cores

The Ultra320 SCSI cores control their individual SCSI bus interface.

2.1.2.2 Datapath Engines

The datapath engines manage the SCSI side of DMA transactions between their individual SCSI bus and the host system.

2.1.2.3 Context Managers

The context managers are ARM966E-S processors. Each context manager controls the SCSI channel side of the LSI53C1030 Fusion-MPT architecture for their individual SCSI bus. The context managers control the outbound queues, target mode I/O mapping, disconnect and reselect sequences, scatter/gather lists, and status reports.

2.2 Fusion-MPT Architecture Overview

The Fusion-MPT architecture provides two I/O methods for the host system to communicate with the IOP: the system interface doorbell and the message queues.

The system interface doorbell is a simple message passing mechanism that allows the PCI host system and IOP to exchange single 32-bit Dword

messages. When the host system writes to the doorbell, the LSI53C1030 hardware generates a maskable interrupt to the IOP, which can then read the doorbell value and take the appropriate action. When the IOP writes a value to the doorbell, the LSI53C1030 hardware generates a maskable interrupt to the host system. The host system can then read the doorbell value and take the appropriate action.

There are two 32-bit message queues: the request message queue and the reply message queue. The host uses the request queue to request an action by the LSI53C1030, and the LSI53C1030 uses the reply queue to return status information to the host. The request message queue consists of only the request post FIFO. The reply message queue consists of both the reply post FIFO and the reply free FIFO. The shared RAM contains the message queues.

Communication using the message queues occurs through request messages and reply messages. Request message frame descriptors are pointers to the request message frames and are passed through the request post FIFO. The request message frame data structure is up to 128 bytes in length and includes a message header and a payload. The header uniquely identifies the message. The payload contains information that is specific to the request. Reply message frame descriptors have one of two formats and are passed through the reply post FIFO. When indicating the successful completion of a SCSI I/O, the IOP writes the reply message frame descriptor using the Context Reply format, which is a message context. If a SCSI I/O does not complete successfully, the IOP uses the Address Reply format. In this case, the IOP pops a reply message frame from the reply free FIFO, generates a reply message describing the error, writes the reply message to system memory, and writes the address of the reply message frame to the reply post FIFO. The host can then read the reply message and take the appropriate action.

The doorbell mechanism provides both a high-priority communication path that interrupts the host system device driver and an alternative communication path to the message queues. Since data transport through the system doorbell occurs a single Dword at a time, use the LSI53C1030 message queues for normal operation and data transport.

2.3 PCI Functional Description

The host PCI interface complies with the *PCI Local Bus Specification, Revision 2.2*, and the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*. The LSI53C1030 supports up to a 133 MHz, 64-bit PCI-X bus. The LSI53C1030 provides support for 64-bit addressing with Dual Address Cycle (DAC).

The LSI53C1030 is a true multifunction PCI-X device and presents a single electrical load to the PCI bus. The LSI53C1030 uses a single REQ/-GNT/ pair to arbitrate for PCI bus mastership. Separate interrupt signals for PCI Function [0] and PCI Function [1] allow independent control of the two PCI functions.

2.3.1 PCI Addressing

The three physical address spaces the PCI specification defines are:

- PCI Configuration Space
- PCI I/O Space for operating registers
- PCI Memory Space for operating registers

The following sections describe the PCI address spaces.

2.3.1.1 PCI Configuration Space

The LSI53C1030 defines an independent set of PCI Configuration Space registers for each PCI function. Each configuration space is a contiguous 256 x 8-bit set of addresses. The system BIOS initializes the configuration registers using PCI configuration cycles. The LSI53C1030 decodes C_BE[3:0]/ to determine if a PCI cycle intends to access the configuration register space. The IDSEL signal behaves as a chip select signal that enables access to the configuration register space only. The LSI53C1030 ignores configuration read/write cycles when IDSEL is not asserted.

Since the LSI53C1030 is a multifunction PCI device, bits AD[10:8] decode either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1030 does not respond to any other encodings of AD[10:8].

Bits AD[7:2] select one of the sixty-four Dword registers in the device's PCI Configuration Space. Bits AD[1:0] determine if the configuration command is a Type 0 Configuration Command (AD[1:0] = 0b00) or a Type 1 Configuration Command (AD[1:0] = 0b01). Since the LSI53C1030 is not a PCI Bridge device, all PCI Configuration Commands designated for the LSI53C1030 must be Type 0. C_BE[3:0]/ address the individual bytes within each Dword and determine the type of access to perform.

2.3.1.2 PCI I/O Space

The PCI specification defines I/O Space as a contiguous 32-bit I/O address that all system resources share, including the LSI53C1030. The [I/O Base Address](#) register determines the 256-byte PCI I/O area that the PCI device occupies.

2.3.1.3 PCI Memory Space

The LSI53C1030 contains two PCI memory spaces: PCI Memory Space [0] and PCI Memory Space [1]. PCI Memory Space [0] supports normal memory accesses, while PCI Memory Space [1] supports diagnostic memory accesses. The LSI53C1030 requires 64 Kbytes of memory space.

The PCI specification defines memory space as a contiguous 64-bit memory address that all system resources share. The [Memory \[0\] Low](#) and [Memory \[0\] High](#) registers determine which 64 Kbyte memory area PCI Memory Space [0] occupies. The [Memory \[1\] Low](#) and [Memory \[1\] High](#) registers determine which 64 Kbyte memory area PCI Memory Space [1] occupies.

2.3.2 PCI Commands and Functions

Bus commands indicate to the target the type of transaction the master is requesting. The master encodes the bus commands on the C_BE[3:0]/ lines during the address phase. The PCI bus command encodings appear in [Table 2.1](#).

Table 2.1 PCI/PCI-X Bus Commands and Encodings¹

C_BE[3:0]/	PCI Command	PCI-X Command	Supports as Master	Supports as Slave
0b0000	Interrupt Acknowledge	Interrupt Acknowledge	No	No
0b0001	Special Cycle	Special Cycle	No	No
0b0010	I/O Read	I/O Read	Yes	Yes
0b0011	I/O Write	I/O Write	Yes	Yes
0b0100	Reserved	Reserved	N/A	N/A
0b0101	Reserved	Reserved	N/A	N/A
0b0110	Memory Read	Memory Read Dword	Yes	Yes
0b0111	Memory Write	Memory Write	Yes	Yes
0b1000	Reserved	Alias to Memory Read Block	PCI: N/A PCI-X: No	PCI: N/A PCI-X: Yes
0b1001	Reserved	Alias to Memory Write Block	PCI: N/A PCI-X: No	PCI: N/A PCI-X: Yes
0b1010	Configuration Read	Configuration Read	No	Yes
0b1011	Configuration Write	Configuration Write	No	Yes
0b1100	Memory Read Multiple	Split Completion	Yes	Yes ²
0b1101	Dual Address Cycle	Dual Address Cycle	Yes	Yes
0b1110	Memory Read Line	Memory Read Block	Yes	Yes ²
0b1111	Memory Write and Invalidate	Memory Write Block	Yes	Yes ³

1. The LSI53C1030 ignores reserved commands as a slave and never generates them as a master.
2. When acting as a slave in the PCI mode, the LSI53C1030 supports this command as the PCI Memory Read command.
3. When acting as a slave in the PCI mode, the LSI53C1030 supports this command as the PCI Memory Write command.

The following sections describe how the LSI53C1030 implements these commands.

2.3.2.1 Interrupt Acknowledge Command

The LSI53C1030 ignores this command as a slave and never generates it as a master.

2.3.2.2 Special Cycle Command

The LSI53C1030 ignores this command as a slave and never generates it as a master.

2.3.2.3 I/O Read Command

The I/O Read command reads data from an agent mapped in the I/O address space. When decoding I/O commands, the LSI53C1030 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.4 I/O Write Command

The I/O Write command writes data to an agent mapped in the I/O address space. When decoding I/O commands, the LSI53C1030 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.5 Memory Read Command

The LSI53C1030 uses the Memory Read command to read data from an agent mapped in the memory address space. The target can perform an anticipatory read if such a read produces no side effects. The LSI53C1030 supports this command when operating in the PCI bus mode.

2.3.2.6 Memory Read Dword Command

The Memory Read Dword command reads up to a single Dword of data from an agent mapped in the memory address space and can only be initiated as a 32-bit transaction. The target can perform an anticipatory read if such a read produces no side effects. The LSI53C1030 supports this command when operating in the PCI-X bus mode.

2.3.2.7 Memory Write Command

The Memory Write command writes data to an agent mapped in the memory address space. The target assumes responsibility for data coherency when it returns "ready." The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.8 Alias to Memory Read Block Command

This command is reserved for future implementations of the PCI specification. The LSI53C1030 never generates this command as a master. When a slave, the LSI53C1030 supports this command using the Memory Read Block command.

2.3.2.9 Alias to Memory Write Block Command

This command is reserved for future implementations of the PCI specification. The LSI53C1030 never generates this command as a master. When a slave, the LSI53C1030 supports this command using the Memory Write Block command.

2.3.2.10 Configuration Read Command

The Configuration Read command reads the configuration space of a device. The LSI53C1030 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the LSI53C1030 by asserting its IDSEL signal when AD[1:0] equal 0b00. During the address phase of a configuration cycle, AD[7:2] address one of the 64 Dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each Dword register and determine the type of access to perform. Bits AD[10:8] address either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1030 treats AD[63:11] as logical don't cares.

2.3.2.11 Configuration Write Command

The Configuration Write command writes the configuration space of a device. The LSI53C1030 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the LSI53C1030 by asserting its IDSEL signal when bits AD[1:0] equal 0b00. During the address phase of a configuration cycle, bits AD[7:2] address one of the 64 Dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each Dword register and determine the type of access to perform. Bits AD[10:8] decode either the PCI Function [0] Configuration Space (AD[10:8] = 0b000) or the PCI Function [1] Configuration Space (AD[10:8] = 0b001). The LSI53C1030 treats AD[63:11] as logical don't cares.

2.3.2.12 Memory Read Multiple Command

The Memory Read Multiple command is identical to the Memory Read command, except it additionally indicates that the master intends to fetch multiple cache lines before disconnecting. The LSI53C1030 supports PCI Memory Read Multiple functionality when operating in the PCI mode and determines when to issue a Memory Read Multiple command instead of a Memory Read command.

Burst Size Selection – The Read Multiple command reads multiple cache lines of data during a single bus ownership. The number of cache lines the LSI53C1030 reads is a multiple of the cache line size, which Revision 2.2 of the PCI specification provides. The LSI53C1030 selects the largest multiple of the cache line size based on the amount of data to transfer.

2.3.2.13 Split Completion Command

Split transactions in PCI-X replace the delayed transactions in conventional PCI. The LSI53C1030 supports up to eight outstanding split transactions when operating in the PCI-X mode. A split transaction consists of at least two separate bus transactions: a split request, which the requester initiates, and one or more split completion commands, which the completer initiates. Revision 1.0a of the PCI-X addendum permits split transaction completion for the Memory Read Block, Alias to Memory Read Block, Memory Read Dword, Interrupt Acknowledge, I/O Read, I/O Write, Configuration Read, and Configuration Write commands. When operating in the PCI-X mode, the LSI53C1030 supports the Split Completion command for all of these commands except the Interrupt Acknowledge command, which the LSI53C1030 neither responds to nor generates.

2.3.2.14 Dual Address Cycles (DAC) Command

The LSI53C1030 performs Dual Address Cycles (DAC), per the *PCI Local Bus Specification, Revision 2.2*. The LSI53C1030 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.15 Memory Read Line Command

This command is identical to the Memory Read command except it additionally indicates that the master intends to fetch a complete cache line. The LSI53C1030 supports this command when operating in the PCI mode.

2.3.2.16 Memory Read Block Command

The LSI53C1030 uses this command to read from memory. The LSI53C1030 supports this command when operating in the PCI-X mode.

2.3.2.17 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except it additionally guarantees a minimum transfer of one complete cache line. The master uses this command when it intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI [Cache Line Size](#) register. The LSI53C1030 determines when to issue a Write and Invalidate command instead of a Memory Write command and supports this command when operating in the PCI bus mode.

Alignment – The LSI53C1030 uses the calculated line size value to determine if the current address aligns to the cache line size. If the address does not align, the LSI53C1030 bursts data using a noncache command. If the starting address aligns, the LSI53C1030 issues a Memory Write and Invalidate command using the cache line size as the burst size.

Multiple Cache Line Transfers – The Memory Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The LSI53C1030 issues a burst transfer as soon as it reaches a cache line boundary. The PCI Local Bus specification states that the transfer size must be a multiple of the cache line size. The LSI53C1030 selects the largest multiple of the cache line size based on the transfer size. When the DMA buffer contains less data than the value [Cache Line Size](#) register specifies, the LSI53C1030 issues a Memory Write command on the next cache boundary to complete the data transfer.

2.3.2.18 Memory Write Block Command

The LSI53C1030 uses this command to burst data to memory. The LSI53C1030 supports this command when operating in the PCI-X bus mode.

2.3.3 PCI Arbitration

The LSI53C1030 contains independent bus mastering functions for each of the SCSI functions and for the system interface. The system interface bus mastering function manages DMA operations as well as the request and reply message frames. The SCSI channel bus mastering functions manage data transfers across the SCSI channels.

The LSI53C1030 uses a single REQ/-GNT/ signal pair to arbitrate for access to the PCI bus. To ensure fair access to the PCI bus, the internal arbiter uses a round robin arbitration scheme to decide which of the three internal bus mastering functions can arbitrate for access to the PCI bus.

2.3.4 PCI Cache Mode

The LSI53C1030 supports an 8-bit [Cache Line Size](#) register. The [Cache Line Size](#) register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. The LSI53C1030 determines when to issue a PCI cache command (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate), or PCI noncache command (Memory Read or Memory Write command).

2.3.5 PCI Interrupts

The LSI53C1030 signals an interrupt to the host processor either using PCI interrupt pins, INTx/ and ALT_INTx/, or using Message Signalled Interrupts (MSI). If using the PCI interrupt pins, the Interrupt Request Routing Mode bits in the [Host Interrupt Mask](#) register configure the routing of each interrupt to either the INTx/ and/or the ALT_INTx/ pin. The [Interrupt Pin](#) register configures the routing of each PCI function's interrupt signals to either the interrupt A pins (INTA/, ALT_INTA/) or the interrupt B pins (INTB/ or ALT_INTB/).

If using MSI, the LSI53C1030 does not signal interrupts on INTx/ or ALT_INTx/. Note that enabling MSI to mask PCI interrupts is a violation of the PCI specification. Each PCI function of the LSI53C1030

implements its own MSI register set. The LSI53C1030 supports one requested message and disables MSI after the chip powers-up or resets.

The [Host Interrupt Mask](#) register also prevents the assertion of a PCI interrupt to the host processor by selectively masking reply interrupts and system doorbell interrupts. This register masks both pin-based and MSI-based interrupts.

2.3.6 Power Management

The LSI53C1030 complies with the *PCI Power Management Interface Specification, Revision 1.1*, and the *PC2001 System Design Guide*. The LSI53C1030 supports the D0, D1, D2, D3_{hot}, and D3_{cold} power states. D0 is the maximum power state, and D3 is the minimum power state. Power State D3 is further categorized as D3_{hot} or D3_{cold}. Powering a function off places it in the D3_{cold} Power State.

Bits [1:0] of the [Power Management Control/Status](#) register independently control the power state of each PCI device on the LSI53C1030. [Table 2.2](#) provides the power state bit settings.

Table 2.2 Power States

Power Management Control and Status Register, Bits [1:0]	Power State	Function
0b00	D0	Maximum Power
0b01	D1	Snooze Mode
0b10	D2	Coma Mode
0b11	D3	Minimum Power

The following sections describe the PCI Function Power States D0, D1, D2, and D3. As the device transitions from one power level to a lower one, the attributes that occur in the higher power state level carry into the lower power state level. For example, Power State D2 includes the attributes for Power State D1, as well as the attributes defined for Power State D2. The following sections describe the PCI Function power states in conjunction with each SCSI function. Power state actions are separate for each SCSI function.

2.3.6.1 Power State D0

Power State D0 is the maximum power state and is the power-up default state for each function. The LSI53C1030 is fully functional in this state.

2.3.6.2 Power State D1

Per the *PCI Power Management Interface Specification*, Power State D1 must have an equal or lower power level than Power State D0. A function in Power State D1 places the SCSI core in the snooze mode. In the snooze mode, a SCSI reset does not generate an IRQ/ signal.

2.3.6.3 Power State D2

Per the *PCI Power Management Interface Specification*, Power State D2 must have an equal or lower power level than Power State D1. A function in this state places the SCSI core in the coma mode. Placing the PCI Function in Power State D2 disables the SCSI and DMA interrupts, and suppresses the following PCI Configuration Space [Command](#) register enable bits:

- I/O Space Enable
- Memory Space Enable
- Bus Mastering Enable
- SERR/Enable
- Enable Parity Error Response

Therefore, the function's memory and I/O spaces cannot be accessed, and the PCI function cannot be a PCI bus master.

If the PCI function is changed from Power State D2 to Power State D1 or D0, the PCI function restores the previous values of the PCI [Command](#) register and asserts any interrupts that were pending before the function entered Power State D2.

2.3.6.4 Power State D3

Per the *PCI Power Management Interface Specification*, Power State D3 must have an equal or lower power level than Power State D2. Power State D3 is the minimum power state and includes the D3_{hot} and D3_{cold} settings. D3_{hot} allows the device to transition to D0 using software. D3_{cold}

removes power from the LSI53C1030. D3_{cold} can transition to D0 by applying VCC and resetting the device.

Placing a function in Power State D3 puts the LSI53C1030 core in the coma mode, clears the function's PCI [Command](#) register, and continually asserts the function's soft reset. Asserting soft reset clears all pending interrupts and 3-states the SCSI bus.

2.4 Ultra320 SCSI Functional Description

The LSI53C1030 provides two independent Ultra320 SCSI channels on a single chip. Each channel supports wide SCSI synchronous transfer rates up to 320 Mbytes/s across an SE or LVD SCSI bus. The integrated LVDlink transceivers support both LVD and SE signals and do not require external transceivers. The LSI53C1030 controller supports the Ultra320 SCSI, Ultra160 SCSI, Ultra2 SCSI, Ultra SCSI, and Fast SCSI interfaces.

2.4.1 Ultra320 SCSI Features

This section describes how the LSI53C1030 implements the features in the SPI-4 draft specification.

2.4.1.1 Parallel Protocol Request (PPR)

A SCSI extended message negotiates the PPR parameters. The PPR parameters include the (1) transfer period, (2) maximum REQ/ACK offset, (3) QAS, (4) margin control settings (MCS), (5) transfer width, (6) IU_Request, (7) write flow, (8) read streaming, (9) RTI, (10) precompensation enable, (11) information unit transfers, and the (12) DT data phases between an initiator and a target.

2.4.1.2 Double Transition (DT) Clocking

Ultra160 SCSI and Ultra320 SCSI implement DT clocking to provide speeds up to 80 megatransfers per second (megatransfers/s) for Ultra160 SCSI, and up to 160 megatransfers/s for Ultra320 SCSI. When implementing DT clocking, a SCSI device samples data on both the asserting and deasserting edge of REQ/ACK. DT clocking is only valid using an LVD SCSI bus.

2.4.1.3 Intersymbol Interference (ISI) Compensation

ISI Compensation uses paced transfers and precompensation to enable high data transfer rates. Ultra320 SCSI data transfers require the use of ISI Compensation.

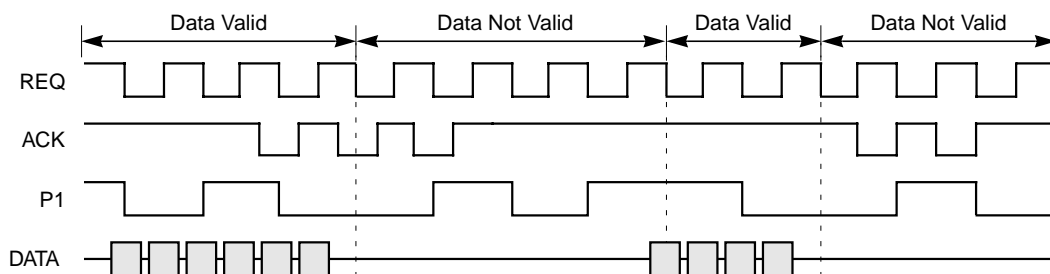
Paced Transfers – The initiator and target must establish a paced transfer agreement that specifies the REQ/ACK offset and the transfer period before using this feature. Devices can only perform paced transfers during Ultra320 SCSI DT data phases. In paced transfers, the device sourcing the data drives the REQ/ACK signal as a free running clock. The transition of the REQ/ACK signal, either the assertion or the negation, clocks data across the bus. For successful completion of a paced transfer, the number of ACK transitions must equal the number of REQ transitions and both the REQ and ACK lines must be negated.

The P1 line indicates valid data in 4-byte quantities by using its phase. The transmitting device indicates the start of valid data state by holding the state of the P1 line for the first two data transfer periods. Beginning on the third data transfer period, the transmitting device continues the valid data state by toggling the state of the P1 line every two data transfer periods for as long as the data is valid. The transmitting device must toggle the P1 line coincident with the REQ/ACK assertion. The method provides a minimum data valid period of two transfer periods.

To pause the data transfer, the transmitting device reverses the phase of P1 by withholding the next transition of P1 at the start of the first two invalid data transfer periods. Beginning with the third invalid data transfer period, the transmitting device toggles the P1 line every two invalid data transfer periods until it sends valid data. The transmitting device returns to the valid data state by reversing the phase of the P1 line. The invalid data state must experience at least one P1 transition before returning to the valid data state. This method provides a minimum data invalid period of four transfer periods.

[Figure 2.2](#) provides a waveform diagram of paced data transfers and illustrates the use of the P1 line.

Figure 2.2 Paced Transfer Example

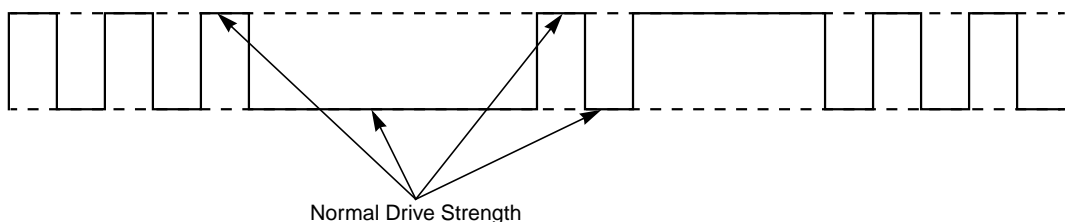


The LSI53C1030 uses the PPR negotiation that the SPI-4 draft standard describes to establish a paced transfer agreement for each initiator-target pair.

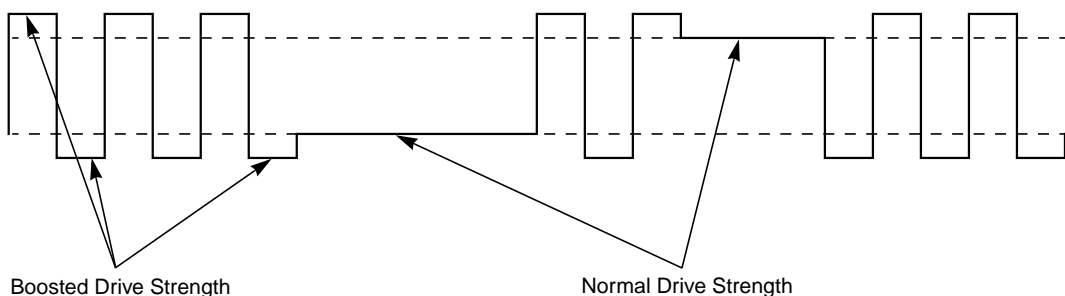
Precompensation – When transmitting in the Ultra320 SCSI mode, the LSI53C1030 uses precompensation to adjust the strength of the REQ, ACK, parity, and data signals. When a signal transitions to HIGH or LOW, the LSI53C1030 boosts the signal drive strength for the first data transfer period, and then lowers the signal drive strength on the second data transfer period if the signal remains in the same state. The LSI53C1030 maintains the lower signal drive strength until the signal again transitions HIGH or LOW. [Figure 2.3](#) illustrates the drivers performance with precompensation enabled and disabled.

Figure 2.3 Example of Precompensation

a. Drivers with Precompensation Disabled



b. Drivers with Precompensation Enabled



2.4.1.4 Packetized Transfers

Packetized transfers are also referred to as *information unit transfers*. They reduce overhead on the SCSI bus by merging several of the SCSI bus phases. Packetized transfers can only occur in DT Data phases. The initiator and target must establish either a DT synchronous transfer agreement or a paced transfer agreement before performing packetized transfers.

The number of bytes in an information unit transfer is always a multiple of four. If the number of bytes to transfer in the information unit is not a multiple of four, the LSI53C1030 transmits pad bytes to bring the byte count to a multiple of four.

2.4.1.5 Quick Arbitration and Selection (QAS)

When using packetized transfers, QAS allows devices to arbitrate for the bus immediately after the message phase. QAS reduces the bus

overhead and maximizes bus bandwidth by skipping the bus free phase that normally follows a SCSI connection.

To perform QAS, the target sends a QAS request message to the initiator during the message phase of the bus. QAS capable devices snoop the SCSI bus for the QAS request message. If a QAS request message is seen, devices can immediately move to the arbitration phase without going to the bus free phase. The LSI53C1030 employs a fairness algorithm to ensure that all devices have equal bus access.

2.4.1.6 Skew Compensation

The LSI53C1030 provides a method to account for and control system skew between the clock and data signals. Skew compensation is only available when the device operates in the Ultra320 SCSI mode. The initiator-target pair uses the training sequences in the SPI-4 draft standard to determine the skew compensation. Depending on the state of the RTI bit in the PPR negotiation, the LSI53C1030 can either execute this training pattern during each connection, or can execute the training pattern, store the adjustment parameters, and recall them on subsequent connections with the given device. The target determines when to execute the training pattern.

2.4.1.7 Cyclic Redundancy Check (CRC)

Ultra320 SCSI and Ultra160 SCSI devices employ CRC as an error detection code during the DT Data phases. These devices transfer four CRC bytes during the DT Data phases to ensure reliable data transfers.

2.4.1.8 SureLINK Domain Validation

SureLINK Domain Validation establishes the integrity of a SCSI bus connection between an initiator and a target. Under the SureLINK Domain Validation procedure, a host queries a device to determine its ability to communicate at the negotiated data transfer rate.

SureLINK Domain Validation provides 3 levels of integrity checking: Basic (Level 1) with inquiry command, Enhanced (Level 2) with read/write buffer, and Margined (Level 3) with drive strength margining and slew rate control. The basic check consists of an inquiry command to detect gross problems. The enhanced check sends a known data pattern using the read and write buffer commands to detect additional problems. The

margin check verifies that the physical parameters have a reasonable operating margin. Use SureLINK Domain Validation only during the diagnostic system checks and not during normal system operation. If transmission errors occur during any of these checks, the system can reduce the transmission rate on a per-target basis to ensure robust system operation.

2.4.2 SCSI Bus Interface

This section describes the SCSI bus modes that the LSI53C1030 supports and the SCSI bus termination methods necessary to operate a high speed SCSI bus.

2.4.2.1 SCSI Bus Modes

The LSI53C1030 supports SE and LVD transfers. To increase device connectivity and SCSI cable length, the LSI53C1030 features LVDlink technology, which is the LSI Logic implementation of LVD SCSI. LVDlink transceivers provide the inherent reliability of differential SCSI and a long-term migration path for faster SCSI transfer rates.

The A_DIFFSENS or B_DIFFSENS signals detect the different input voltages for HVD, LVD, and SE. The LSI53C1030 drivers are tolerant of HVD signal strengths, but do not support the HVD bus mode. The LSI53C1030 SCSI device 3-states its SCSI drivers when it detects an HVD signal level.

2.4.2.2 SCSI Termination

The terminator networks pull signals to an inactive voltage level and match the impedance seen at the end of the cable to the characteristic impedance of the cable. Install terminators at the extreme ends of the SCSI chain, and only at the ends; all SCSI buses must have exactly two terminators.

Note: If using the LSI53C1030 in a design with an 8-bit SCSI bus, designers must terminate all 16 data lines.

2.5 External Memory Interface

The LSI53C1030 provides Flash ROM, NVSRAM, and serial EEPROM interfaces. The Flash ROM interface stores the SCSI BIOS and firmware image. The Flash ROM is optional if the LSI53C1030 is not the boot device and a suitable driver exists to initialize the LSI53C1030. Integrated Mirroring (IM) technology requires an NVSRAM for write journaling. The nonvolatile external serial EEPROM stores configuration parameters for the LSI53C1030.

2.5.1 Flash ROM Interface

The Flash ROM interface multiplexes the 8-bit address and data buses on the MAD[7:0] pins. The interface latches the address into three 8-bit latches to support up to 1 Mbyte of address space. The interface supports byte, word, and Dword accesses. The LSI53C1030 Dword aligns Dword reads, word aligns word reads, and byte aligns byte reads. The remaining bits from word and byte reads are meaningless.

The MAD[2:1] Power-On sense pin configurations define the size of the Flash ROM address space. [Table 2.3](#) provides the pin encoding for these pins. By default, internal logic pulls these pins down to indicate that no Flash ROM is present.

Table 2.3 Flash ROM Size Programming

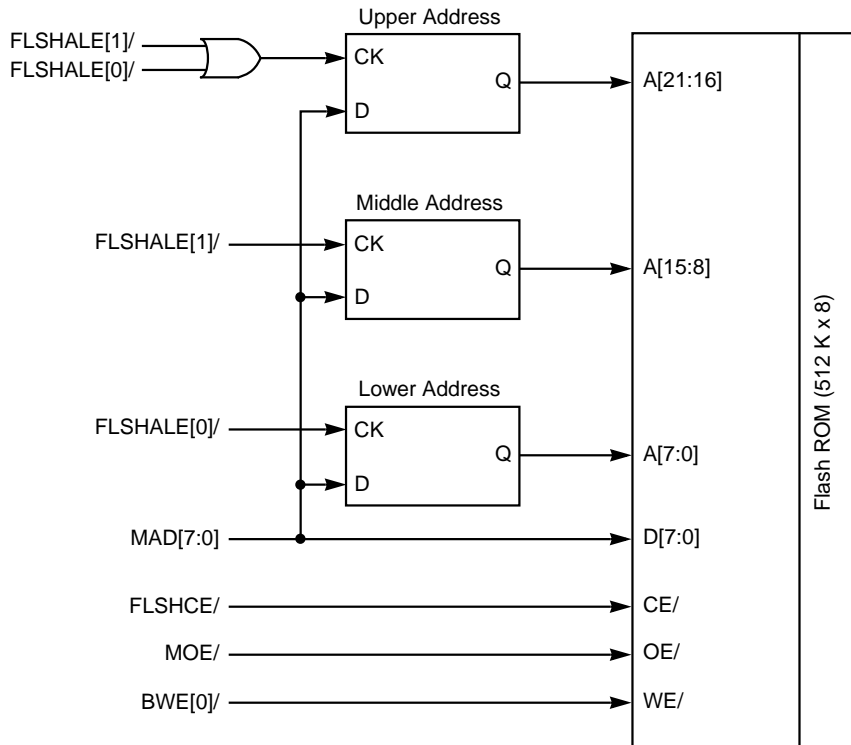
MAD[2:1] Options	Flash ROM Size
0b00	No Flash ROM present (Default)
0b01	Up to 1024 Kbytes ¹
0b10	Reserved
0b11	

1. Choose this setting for a 128 Kbyte or 512 Kbyte Flash ROM.

The LSI53C1030 defines only the middle (MA[15:8]) and lower (MA[7:0]) address ranges if the Flash ROM addressable space is 64 Kbytes or less. The LSI53C1030 defines the upper (MA[21:16]), middle (MA[15:8]), and lower (MA[7:0]) address ranges if the Flash ROM addressable space

is 128 Kbytes or more. [Figure 2.4](#) provides an example of a Flash ROM configuration.

Figure 2.4 Flash ROM Block Diagram



The LSI53C1030 implements a Flash signature recognition mechanism to determine if the Flash contains a valid image. The Flash can be present and not contain a valid image either before its initial programming or during board testing. The first access to the Flash is a 16-byte burst read beginning at Flash address 0x000000. The LSI53C1030 compares the values read to the Flash signature values that [Table 2.4](#) provides. If the signature values match, the LSI53C1030 performs the instruction located at Flash address 0x000000. If the signature values do not match, the LSI53C1030 records an error and ignores the Flash instruction. The Flash signature does not include the first three bytes of Flash memory as these bytes contain a branch offset instruction.

Table 2.4 Flash Signature Value

Flash Address	Flash Signature Values			
Bytes [3:0]	0xEA	XX	XX	XX
Bytes [7:4]	0x5A	0xEA	0xA5	0x5A
Bytes [11:8]	0xA5	0x5A	0xEA	0xA5
Bytes [15:12]	0x5A	0xA5	0x5A	0xEA

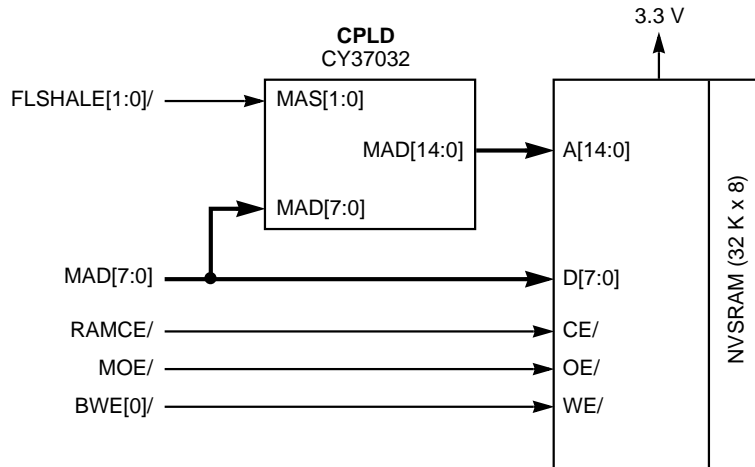
2.5.2 NVSRAM Interface

The LSI53C1030 Fusion-MPT firmware is capable of maintaining an Integrated Mirroring (IM) volume of the boot drive. IM firmware requires a 32 Kbyte NVSRAM in order to perform write journaling. Write journaling is used to verify that the mirrored disks in the IM volume are synchronized with each other. The NVSRAM also stores additional code and data used for error and exception handling, and it stores IM configuration information during serial EEPROM updates. The disk write log uses approximately 4 Kbytes of the NVSRAM.

[Figure 2.5](#) provides a block diagram illustrating how to connect the NVSRAM. This design employs the CPLD to latch the address instead of using separate address latches.

When using an NVSRAM, pull the MAD[3] Power-On Sense pin HIGH during board boot-up. This configures the external memory interface as an NVSRAM interface. During operation, RAMCE/ selects the NVSRAM when MAD[3] is pulled HIGH.

Figure 2.5 NVSRAM Diagram



2.6 Serial EEPROM Interface

The nonvolatile external serial EEPROM stores configuration fields for the LSI53C1030. The serial EEPROM contains fields for the Subsystem ID(s), Subsystem Vendor ID(s), and the size of the PCI Diagnostic Memory Space. The LSI53C1030 must establish each of these parameters prior to reading system BIOS and loading the PCI Configuration Space registers. The power-on option settings enable the download of PCI configuration data from the serial EEPROM. For more information on the setting of the power-on options, refer to [Section 3.10, "Power-On Sense Pins Description."](#)

A 2-wire serial interface provides the connection to the serial EEPROM. During initialization, the firmware checks if a serial EEPROM exists. Firmware uses the checksum byte to determine if the configuration held in the serial EEPROM is valid. If the checksum fails the firmware checks for a valid NVData signature. If a valid NVData signature is found the firmware individually checksums each persistent configuration page to find the invalid page or pages. [Table 2.5](#) provides the structure of the configuration record in the serial EEPROM.

Table 2.5 PCI Configuration Record in Serial EEPROM

EEPROM Address	Configuration Data
0x00	PCI Function [0] Subsystem ID , bits [7:0]
0x01	PCI Function [0] Subsystem ID , bits [15:8]
0x02	PCI Function [0] Subsystem Vendor ID , bits [7:0]
0x03	PCI Function [0] Subsystem Vendor ID , bits [15:8]
0x04	PCI Diagnostic Memory Size
0x05	Reserved
0x06	PCI Function [1] Subsystem ID , bits [7:0]
0x07	PCI Function [1] Subsystem ID , bits [15:8]
0x08	PCI Function [1] Subsystem Vendor ID , bits [7:0]
0x09	PCI Function [1] Subsystem Vendor ID , bits [15:8]
0x0A	Checksum

2.7 Zero Channel RAID

Zero channel RAID (ZCR) capabilities enable the LSI53C1030 to respond to accesses from a PCI RAID controller card or chip that is able to generate ZCR cycles. The LSI53C1030's ZCR functionality is controlled through the ZCR_EN/ and the IOPD_GNT/ signals. Both of these signals have internal pull-ups and are active LOW.

The ZCR_EN/ signal enables ZCR support on the LSI53C1030. Pulling ZCR_EN/ HIGH disables ZCR support on the LSI53C1030 and causes the LSI53C1030 to behave as a normal PCI-X to Ultra320 SCSI controller. When ZCR is disabled, the IOPD_GNT/ signal has no effect on the LSI53C1030 operation.

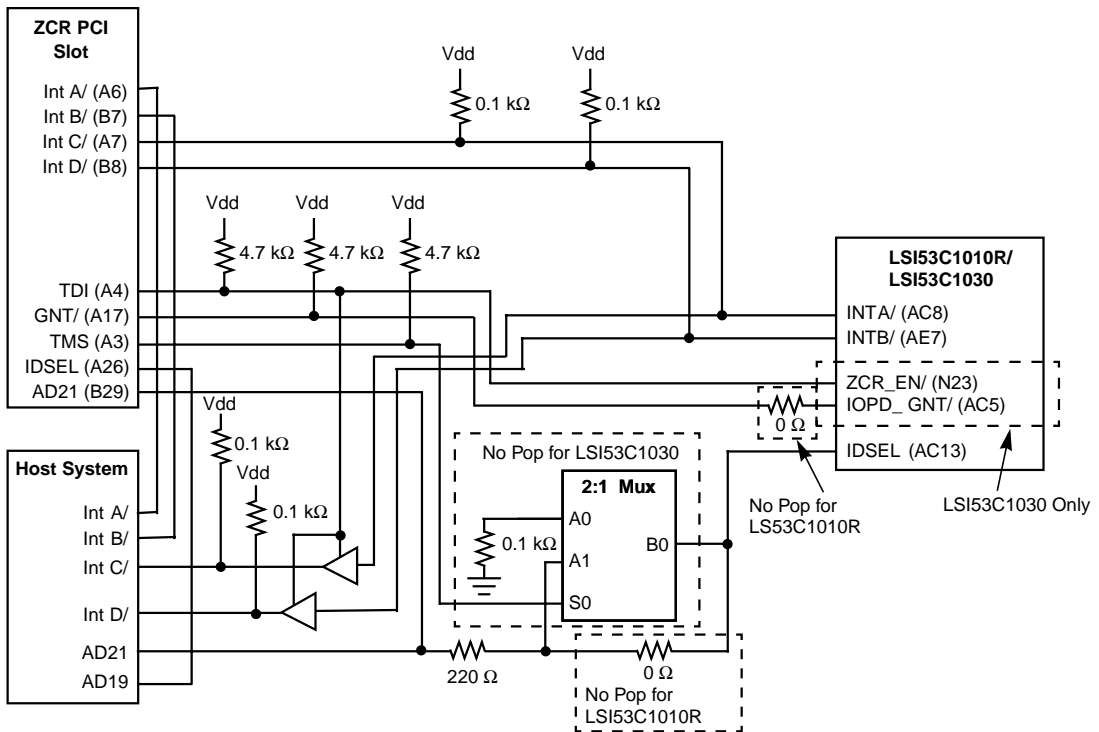
Pulling ZCR_EN/ LOW enables ZCR operation. When ZCR is enabled, the LSI53C1030 responds to PCI configuration cycles when the IOPD_GNT/ and IDSEL signal are asserted. Connect the IOPD_GNT/ pin on the LSI53C1030 to the PCI GNT/ signal of the external I/O processor. This allows the I/O processor to perform PCI configuration

cycles to the LSI53C1030 when the I/O processor is granted the PCI bus. This configuration also prevents the system processor from accessing the LSI53C1030 PCI configuration registers.

LSI53C1030 based designs do not use the M66EN pin to determine the PCI bus speed.

Figure 2.6 illustrates how to connect the LSI53C1030 to enable ZCR. This figure also contains information for connecting the LSI53C1010R based designs to a ZCR design and migrating from LSI53C1010R based designs to LSI53C1030 based designs. Notice that the LSI53C1030 does not require the 2:1 mux.

Figure 2.6 ZCR Circuit Diagram for LSI53C1030 and LSI53C1010R



Note: To maintain proper interrupt mapping, select the address line for use as IDSEL on the LSI53C1010R/LSI53C1030 to be +2 address lines above IDSEL on ZCR slot.

2.8 Multi-ICE Test Interface

This section describes the LSI Logic requirements for the Multi-ICE test interface. LSI Logic recommends that all test signals be routed to a header on the board.

The Multi-ICE test interface header is a 20-pin header for Multi-ICE debugging through the ICE JTAG port. This header is essential for debugging both the firmware and the design functionality and must be included in board designs. The connector is a 20-pin header that mates with the IDC sockets mounted on a ribbon cable. [Table 2.6](#) details the pinout of the 20 pin header.

Table 2.6 20-Pin Multi-ICE Header Pinout

Pin Number	Signal	Pin Number	Signal
1	VDD	2	VDD
3	TRST_ICE ¹	4	VSS
5	TDI_ICE ¹	6	VSS
7	TMS_ICE ¹	8	VSS
9	TCK_ICE ¹	10	VSS
11	RTCK_ICE	12	VSS
13	TDO_ICE	14	VSS
15	No Connect	16	VSS
17	No Connect	18	VSS
19	No Connect	20	VSS

1. The designer must connect a 4.7 k Ω resistor from this signal to 3.3 V.

Chapter 3

Signal Description

This chapter describes the input and output signals of the LSI53C1030. The chapter consists of the following sections:

- [Section 3.1, “Signal Organization”](#)
- [Section 3.2, “PCI Bus Interface Signals”](#)
- [Section 3.3, “PCI-Related Signals”](#)
- [Section 3.4, “SCSI Interface Signals”](#)
- [Section 3.5, “Memory Interface”](#)
- [Section 3.6, “Zero Channel RAID Interface”](#)
- [Section 3.7, “Test Interface”](#)
- [Section 3.8, “GPIO and LED Signals”](#)
- [Section 3.9, “Power and Ground Pins”](#)
- [Section 3.10, “Power-On Sense Pins Description”](#)
- [Section 3.11, “Internal Pull-Ups and Pull-Downs”](#)

A slash (/) at the end of a signal indicates that the signal is active LOW. When the slash is absent, the signal is active HIGH. NC designates a No Connect signal.

3.1 Signal Organization

The LSI53C1030 has six major interfaces:

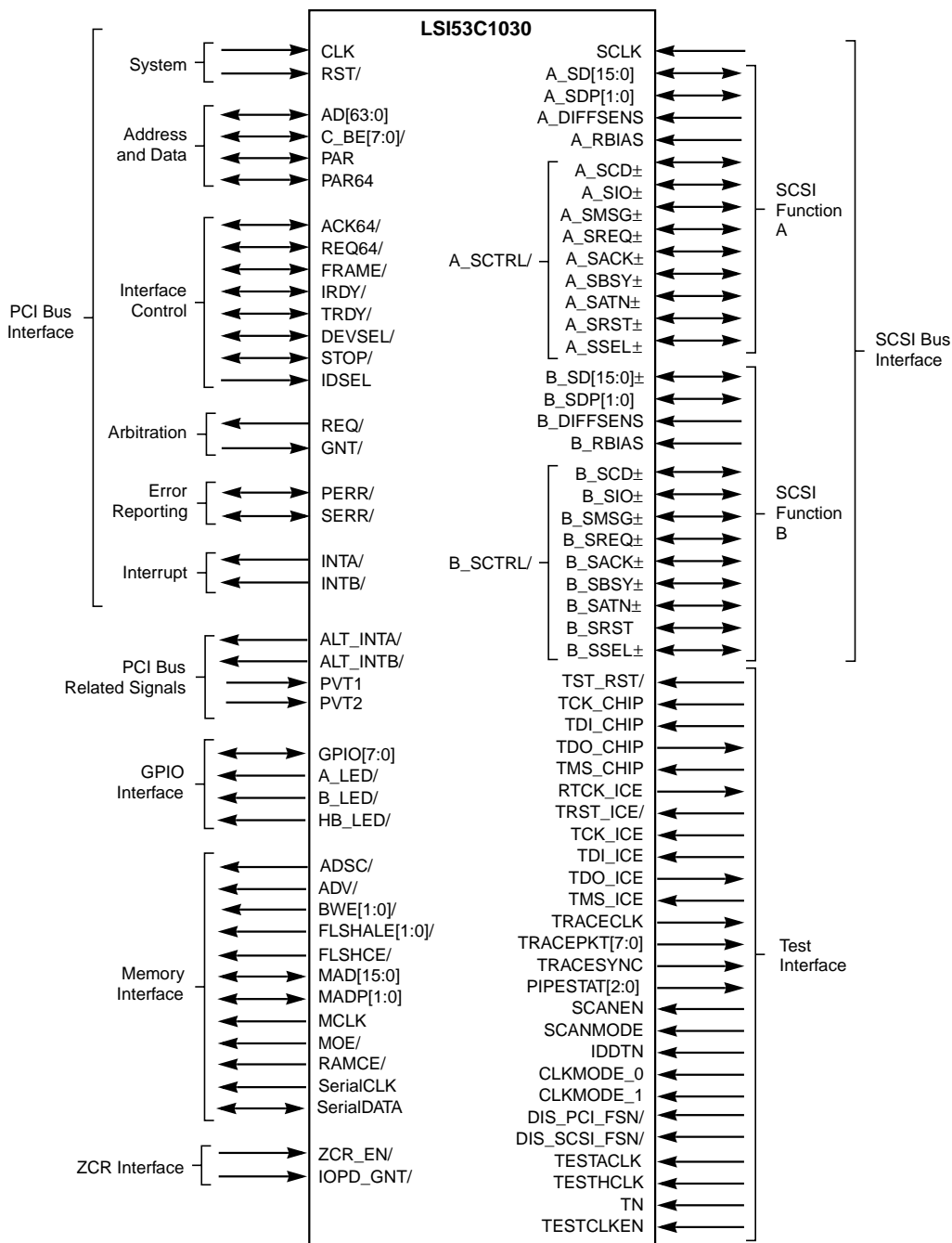
- PCI Bus Interface
- SCSI Bus Interface
- Memory Bus Interface
- ZCR Interface
- Test Interface
- General Purpose I/O (GPIO) Interface

There are five signal types:

I	Input, a standard input-only signal
O	Output, a standard output driver (typically a Totem Pole output)
I/O	Input and output (bidirectional)
P	Power
G	Ground

[Figure 3.1](#) contains the functional signal groupings of the LSI53C1030. [Figure 5.12](#) on [page 5-20](#) provides a diagram of the LSI53C1030 456 Ball Grid Array (BGA). [Table 5.20](#) and [Table 5.21](#) on [page 5-22](#) and [page 5-24](#) provide pinout listings for the LSI53C1030.

Figure 3.1 LSI53C1030 Functional Signal Grouping



3.2 PCI Bus Interface Signals

This section describes the PCI interface. The PCI interface consists of the System, Address and Data, Interface Control, Arbitration, Error Reporting, and Interrupt signal groups.

3.2.1 PCI System Signals

[Table 3.1](#) describes the PCI System signals group.

Table 3.1 PCI System Signals

Signal Name	BGA Position	Type	Strength	Description
CLK	AC22	I	N/A	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
RST/	AB10	I	N/A	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.

3.2.2 PCI Address and Data Signals

Table 3.2 describes the PCI Address and Data signals group.

Table 3.2 PCI Address and Data Signals

Signal Name	BGA Position	Type	Strength	Description
AD[63:0]	W22, AB25, AC26, AA25, W23, Y25, Y26, V22, U22, V24, V23, U24, V25, W26, U23, U25, T22, T23, T25, R25, R22, P22, P23, R23, P24, P25, T26, R26, M26, L26, N25, N24, AE9, AF8, AE10, AB11, AC11, AE11, AE12, AB12, AC12, AD13, AE13, AF11, AF16, AE14, AC15, AC14, AD17, AE19, AC18, AB17, AB18, AF20, AE20, AC19, AF23, AE22, AB19, AD21, AF24, AC20, AE23, AC21	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
C_BE[7:0]/	AA23, AC25, Y23, AD26, AB13, AB14, AE18, AE21	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
PAR	AF19	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
PAR64	AA24	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.

3.2.3 PCI Interface Control Signals

Table 3.3 describes the PCI Interface Control signals group.

Table 3.3 PCI Interface Control Signals

Signal Name	BGA Position	Type	Strength	Description
ACK64/	AB20	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
REQ64/	AD22	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
FRAME/	AB15	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
IRDY/	AE15	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
TRDY/	AE16	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
DEVSEL/	AC16	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
STOP/	AB16	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
IDSEL	AC13	I	N/A	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.

3.2.4 PCI Arbitration Signals

Table 3.4 describes the PCI Arbitration signals group.

Table 3.4 PCI Arbitration Signals

Signal Name	BGA Position	Type	Strength	Description
REQ/	AD10	O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
GNT/	AE8	I	N/A	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.

3.2.5 PCI Error Reporting Signals

Table 3.5 describes the PCI Error Reporting signals group.

Table 3.5 PCI Error Reporting Signals

Signal Name	BGA Position	Type	Strength	Description
PERR/	AE17	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.
SERR/	AC17	I/O	8 mA PCI	Refer to the <i>PCI Local Bus Specification, Version 2.2</i> , and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i> , for this signal description.

3.2.6 PCI Interrupt Signals

Table 3.6 describes the PCI Interrupt signals group.

Table 3.6 PCI Interrupt Signals

Signal Name	BGA Position	Type	Strength	Description
INTA/	AC8	O	8 mA PCI	<p>Refer to the <i>PCI Local Bus Specification, Version 2.2</i>, and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i>, for this signal description.</p> <p>The LSI53C1030 can route interrupts to INTA/ and/or ALT_INTA/. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTA/ and/or ALT_INTA/.</p>
INTB/	AE7	O	8 mA PCI	<p>Refer to the <i>PCI Local Bus Specification, Version 2.2</i>, and the <i>PCI-X Addendum to the PCI Local Bus Specification, Version 1.0a</i>, for this signal description.</p> <p>The LSI53C1030 can route interrupts to INTB/ and/or ALT_INTB/. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTB/ and/or ALT_INTB/.</p>

3.3 PCI-Related Signals

Table 3.7 describes the PCI-related signals.

Table 3.7 PCI-Related Signals

Signal Name	BGA Position	Type	Strength	Description
ALT_INTA/	AF7	O	8 mA PCI	Active LOW Alternate Interrupt A indicates that PCI Function [0] is requesting service from its host device driver. ALT_INTA/ is an open drain signal. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTA/ and/or ALT_INTA/.
ALT_INTB/	AB9	O	8 mA PCI	Active LOW Alternate Interrupt B indicates that PCI Function [1] is requesting service from its host device driver. ALT_INTB/ is an open drain signal. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTB/ and/or ALT_INTB/.
PVT2, PVT1	AF4, AE5	I	N/A	PVT2 and PVT1 provide biasing for PCI signals. Connect a 49.9 Ω , 1% resistor between PVT2 and PVT1.

3.4 SCSI Interface Signals

The SCSI Interface signals section describes the signals for the SCSI Channel [0] and SCSI Channel [1] interfaces. [Table 3.8](#) describes the SCSI bus clock signal that is common to both SCSI Channel [0] and SCSI Channel [1].

In the LVD mode, the negative and positive signals form the differential pair. In the SE mode, the negative signals represent the signal pin and the positive signals are a virtual ground. The LSI53C1030 does not support the HVD mode. If HVD signalling is present, the SCSI channel 3-states its drivers.

Table 3.8 SCSI Bus Clock Signal

Signal Name	BGA Position	Type	Strength	Description
SCLK	F3	I	N/A	SCSI Clock provides the 80 MHz reference clock source for the ARM966E-S processors and all SCSI-related timings.

3.4.1 SCSI Channel [0] Signals

[Table 3.9](#) describes the SCSI Channel [0] Interface signals.

Table 3.9 SCSI Channel [0] Interface Signals

Signal Name	BGA Position	Type	Strength	Description
A_SD[15:0]- A_SD[15:0]+	Y1, AA2, AB2, AD1, F2, G2, J4, H1, R4, T5, T2, U2, U5, V2, V4, W4 W5, Y2, AA3, AC1, D1, G1, H4, H2, P3, R5, R2, T4, U4, U3, V5, V3	I/O	SE: 48 mA LVD: 12 mA	SCSI Channel [0] Data signals.
A_SDP[1:0]- A_SDP[1:0]+	W2, P4 W1, P5	I/O	SE: 48 mA LVD: 12 mA	SCSI Channel [0] Data Parity signals.

Table 3.9 SCSI Channel [0] Interface Signals (Cont.)

Signal Name	BGA Position	Type	Strength	Description
A_VDDBIAS	T1	O	N/A	A_VDDBIAS provides power for the A_RBIAS circuit.
A_RBIAS	R1	I	N/A	Connect a 9.76 k Ω or 10.0 k Ω resistor between the A_VDDBIAS and A_RBIAS pins to generate the LVD signalling pad bias current.
A_DIFFSENS	E2	I	N/A	<p>The SCSI Channel [0] Differential Sense pin detects the present mode of the SCSI bus. This signal is 5 V tolerant and must connect to the DIFFSENS signal on the physical SCSI bus.</p> <p>SE Mode: Driving this pin below 0.5 V (LOW) indicates an SE bus and places SCSI Channel [0] in the SE bus mode.</p> <p>LVD Mode: Driving this signal between 0.7 V and 1.9 V (intermediate) indicates an LVD mode and places SCSI Channel [0] in the LVD bus mode.</p> <p>HVD Mode: Driving this pin above 2.0 V (HIGH) indicates an HVD bus and causes SCSI Channel [0] to 3-state its SCSI drivers.</p>

Table 3.10 describes the SCSI Channel [0] Control signals.

Table 3.10 SCSI Channel [0] Control Signals

Signal Name	BGA Position	Type	Strength	Description
A_SCD– A_SCD+	K3 K4	I/O	SE: 48 mA	SCSI Channel [0] Command/Data .
A_SIO– A_SIO+	K5 J5		LVD: 12 mA	SCSI Channel [0] Input/Output .
A_SMSG– A_SMSG+	L2 L1			SCSI Channel [0] Message .
A_SREQ– A_SREQ+	J2 J3			SCSI Channel [0] Request .
A_SACK– A_SACK+	M5 L5			SCSI Channel [0] Acknowledge .
A_SBSY– A_SBSY+	N3 N4			SCSI Channel [0] Busy .
A_SATN– A_SATN+	M4 N5			SCSI Channel [0] Attention .
A_SRST– A_SRST+	M1 M2			SCSI Channel [0] Bus Reset .
A_SSEL– A_SSEL+	L4 K2			SCSI Channel [0] Select .

3.4.2 SCSI Channel [1] Signals

Table 3.11 describes the SCSI Channel [1] Interface signals.

Table 3.11 SCSI Channel [1] Interface Signals

Signal Name	BGA Position	Type	Strength	Description
B_SD[15:0]- B_SD[15:0]+	D8, E8, C6, A3, B21, D19, E18, A19, E13, A12, B11, B10, D10, C9, D9, B8 B7, B6, B5, A4, A23, B20, A20, B19, E12, B12, D11, C10, E11, E10, B9, A8	I/O	SE: 48 mA LVD: 12 mA	SCSI Channel [1] Data signals.
B_SDP[1:0]- B_SDP[1:0]+	A7, D12 E9, C13	I/O	SE: 48 mA LVD: 12 mA	SCSI Channel [1] Data Parity signals.
B_VDDBIAS	B13	O	N/A	B_VDDBIAS provides power for the B_RBIAS circuit.
B_RBIAS	A11	I	N/A	Connect a 9.76 k Ω or 10.0 k Ω resistor between the B_VVDDBIAS and B_RBIAS pins to generate the LVD signalling pad bias current.
B_DIFFSENS	B22	I	N/A	<p>The SCSI Channel [1] Differential Sense pin detects the present mode of the SCSI bus. This signal is 5 V tolerant and must connect to the DIFFSENS signal on the physical SCSI bus.</p> <p>SE Mode: Driving this pin below 0.5 V (low) indicates an SE bus and places SCSI Channel [1] in the SE mode.</p> <p>LVD Mode: Driving this signal between 0.7 V and 1.9 V (intermediate) indicates an LVD bus and places SCSI Channel [1] in the LVD mode.</p> <p>HVD Mode: Driving this pin above 2.0 V (high) indicates an HVD bus and causes SCSI Channel [1] to 3-state its SCSI drivers.</p>

Table 3.12 describes the SCSI Channel [1] Control signals.

Table 3.12 SCSI Channel [1] Control Signals

Signal Name	BGA Position	Type	Strength	Description
B_SCD- B_SCD+	E16 D17	I/O	SE: 48 mA	SCSI Channel [1] Command/Data .
B_SIO- B_SIO+	E17 D18		LVD: 12 mA	SCSI Channel [1] Input/Output .
B_SMSG- B_SMSG+	B16 D16			SCSI Channel [1] Message .
B_SREQ- B_SREQ+	B18 C18			SCSI Channel [1] Request .
B_SACK- B_SACK+	D14 E14			SCSI Channel [1] Acknowledge .
B_SBSY- B_SBSY+	A15 B15			SCSI Channel [1] Busy .
B_SATN- B_SATN+	B14 D13			SCSI Channel [1] Attention .
B_SRST- B_SRST+	E15 A16			SCSI Channel [1] Bus Reset .
B_SSEL- B_SSEL+	B17 C17			SCSI Channel [1] Select .

3.5 Memory Interface

Table 3.13 describes the Flash ROM/NVSRAM Interface signals.

Table 3.13 Flash ROM/NVSRAM Interface Pins

Signal Name	BGA Position	Type	Strength	Description
MCLK	E20	O	4 mA	Reserved.
ADSC/	D21	O	4 mA	Reserved.
ADV/	B23	O	4 mA	Reserved.

Table 3.13 Flash ROM/NVSRAM Interface Pins (Cont.)

Signal Name	BGA Position	Type	Strength	Description
MAD[15:0]	D22, E21, B25, D23, E22, C24, F22, E23, D26, E25, H22, F24, G23, D25, F23, G22	I/O	8 mA	The Memory Address and Data Bus carries the memory and address signals for the Flash ROM and NVSRAM interfaces on MAD[7:0]. These pins also provide the Power-On Sense options that configure operating parameters during chip power up or reset.
MADP[1:0]	C22, B24	I/O	8 mA	The Memory Address and Data Parity signals provide parity checking for MAD[15:0]. By default, the LSI53C1030 uses even parity. The user can enable odd parity through the Fusion-MPT architecture. These pins also provide the Power-On Sense options that configure operating parameters during chip power up or reset.
MOE/	G26	O	4 mA	The LSI53C1030 asserts active LOW Memory Output Enable to indicate that the selected NVSRAM or Flash ROM device can drive data. This signal is typically an asynchronous input to NVSRAM and/or Flash ROM devices.
BWE[1:0]/	E24, H23	O	8 mA	The LSI53C1030 asserts active LOW Memory Byte Write Enables to allow single byte writes to the NVSRAM. BWE0/ enables writes on MAD[7:0].
RAMCE/	D20	O	8 mA	When MAD[3] is pulled HIGH, the LSI53C1030 asserts active LOW synchronous RAM Chip Enable to select the NVSRAM.
FLSHCE/	G25	O	8 mA	The LSI53C1030 asserts active LOW Flash Chip Enable to enable data transfers with a single 8-bit device.
FLSHALE[1:0]/	J24, K22	O	8 mA	The Flash ROM and NVSRAM interfaces use active LOW Flash Address Latch Enable . For the Flash ROM, these signals provide clocks for address latches. For the NVSRAM, these signals provide the memory address strobe.

Table 3.14 describes the serial EEPROM Interface signals.

Table 3.14 Serial EEPROM Interface Pins

Signal Name	BGA Position	Type	Strength	Description
SerialCLK	J25	O	8 mA	Serial EEPROM clock. This signal requires a 4.7 k Ω external pull up resistor when an EEPROM is present.
SerialDATA	H26	I/O	8 mA	Serial EEPROM data. This signal requires a 4.7 k Ω external pull up resistor when an EEPROM is present.

3.6 Zero Channel RAID Interface

Table 3.15 describes the zero channel RAID (ZCR) configuration signals.

Table 3.15 ZCR Configuration Pins

Signal Name	BGA Position	Type	Strength	Description
ZCR_EN/	N23	I	N/A	This signal enables and disables ZCR support on the LSI53C1030. By default, this signal is internally pulled HIGH to disable ZCR operation. Pull this signal LOW to enable ZCR operation.
IOPD_GNT/	AC5	I	N/A	When ZCR is enabled on the LSI53C1030 the device only responds to PCI configuration cycles if IOPD_GNT/ or IDSEL is asserted. Connect IOPD_GNT/ to PCI GNT/ on the external I/O processor.

3.7 Test Interface

Table 3.16 describes the JTAG and ICE debug signals.

Table 3.16 JTAG, ICE, and Debug Pins

Signal Name	BGA Position	Type	Strength	Description
TST_RST/	AD5	I	N/A	Active low Test Reset is for test purposes.
TCK_CHIP	AC6	I	N/A	Chip Test Clock provides a JTAG test clock signal.
TDI_CHIP	AF3	I	N/A	Chip Test Data In provides the JTAG test data in signal.
TDO_CHIP	AD6	O	8 mA	Chip Test Data Out provides the JTAG test data out signal.
TMS_CHIP	AE4	I	N/A	Chip Test Mode Select provides the JTAG test mode select signal.
RTCK_ICE	AA5	O	8 mA	Test Clock Acknowledge provides the JTAG test clock acknowledge signal for the In-Circuit Emulator (ICE) debug logic.
TRST_ICE/	AB4	I	N/A	Test Reset provides the JTAG test reset signal for the ICE debug logic.
TCK_ICE	AA4	I	N/A	Test Clock provides the JTAG test clock signal for the ICE debug logic.
TDI_ICE	AB3	I	N/A	Test Data In provides the JTAG test data in signal for the ICE debug logic.
TDO_ICE	AD2	O	8 mA	Test Data Out provides the JTAG test data out signal for the ICE debug logic.
TMS_ICE	Y5	I	N/A	Test Mode Select provides the test mode select signal for the ICE debug logic.
TRACECLK	B3	O	8 mA	Reserved.
TRACEPKT[7:0]	F4, G5, E3, C2, E4, F5, B2, D4	O	8 mA	Reserved.
TRACESYNC	E5	O	8 mA	Reserved.
PIPESTAT[2:0]	C3, E6, D5	O	8 mA	Reserved.

Table 3.17 lists the LSI Logic test signals.

Table 3.17 LSI Logic Test Pins

Signal Name	BGA Position	Type	Strength	Description
SCANEN	N22	I	N/A	SCANEN is for use only by LSI Logic.
SCANMODE	E7	I	N/A	SCANMODE is for use only by LSI Logic.
IDDTN	Y4	I	N/A	IDDTN is for use only by LSI Logic.
CLKMODE_0	AA22	I	N/A	CLKMODE_0 is for use only by LSI Logic.
CLKMODE_1	AC2	I	N/A	CLKMODE_1 is for use only by LSI Logic.
DIS_PCI_FSN/	A24	I	N/A	Pulling DIS_PCI_FSN/ LOW disables the PCI FSN. Pulling this pin HIGH allows the chip to enable the PCI FSN when operating in PCI-X mode, or to disable the PCI FSN when operating in PCI mode. The LSI53C1030 controls the PCI FSN.
DIS SCSI_FSN/	AC4	I	N/A	DIS SCSI_FSN/ is for use only by LSI Logic.
TESTACLK	AB6	I	N/A	TESTACLK is for use only by LSI Logic.
TESTHCLK	AE2	I	N/A	TESTHCLK is for use only by LSI Logic.
TN	C5	I	N/A	TN is for use only by LSI Logic.
TESTCLKEN	D7	I	N/A	TESTCLKEN is for use only by LSI Logic.

3.8 GPIO and LED Signals

Table 3.18 describes the GPIO and LED signals group.

Table 3.18 GPIO and LED signals

Signal Name	BGA Position	Type	Strength	Description
GPIO[7:0]	K25, L23, L25, M25, H25, K24, AE25, AC23	I/O	8 mA	General purpose I/O pins. The LSI53C1030 controls these signals and can configure them as inputs or as outputs. These pins default to input mode after chip initialization.
A_LED/	J23	O	12 mA	A_LED/ either drives the SCSI Channel [0] activity LED or provides a General Purpose I/O pin. A_LED can be controlled by firmware or driven by chip activity.
B_LED/	K23	O	12 mA	B_LED/ either drives the SCSI Channel [1] activity LED or provides a General Purpose I/O pin. B_LED/ can be controlled by firmware or driven by chip activity.
HB_LED/	C25	O	12 mA	Firmware blinks Heart Beat LED at a 1.0 second interval when the IOP is operational.

3.9 Power and Ground Pins

Table 3.19 describes the Power and Ground signals.

Table 3.19 Power and Ground Pins

Signal Name	BGA Position	Type	Strength	Description
VDD_IO	A1, A2, A6, A10, A14, A18, A22, A26, C7, C11, C15, C19, C23, D3, E26, F1, G24, H3, J26, K1, L24, M3, N26, P1, R24, T3, U26, V1, W24, Y3, AA26, AB1, AC24, AD4, AD8, AD12, AD16, AD20, AE26, AF1, AF5, AF9, AF13, AF17, AF21, AF25	P	N/A	VDD_IO provides power for the PCI bus drivers/receivers, SCSI bus drivers/receivers, local memory interface drivers/receivers, and other I/O pins.
VSS_IO	A5, A9, A13, A17, A21, A25, B1, B26, C4, C8, C12, C16, C20, D24, E1, F26, G3, H24, J1, K26, L3, L11-L16, M11-M16, M24, N1, N11-N16, P11-P16, P26, R3, R11-R16, T11-T16, T24, U1, V26, W3, Y24, AA1, AB26, AC3, AD7, AD11, AD15, AD19, AD23, AE1, AF2, AF6, AF10, AF14, AF18, AF22, AF26	G	N/A	VSS_IO provides ground for the PCI bus drivers/receivers, SCSI bus drivers/receivers, local memory interface drivers/receivers, and other I/O pins.
VDDA ¹	AB21, C1	P	N/A	VDDA provides the analog circuit power for the PLL circuit.
VSSA ¹	AD24, H5	G	N/A	VSSA provides the analog circuit ground for the PLL circuit.
VDDC	D2, D6, D15, E19, J22, M22, N2, AC7, AD3, AD25, AE3, AE24, AF15	P	N/A	VDDC provides power for the core logic.
VSSC	B4, C14, C21, C26, F25, G4, L22, P2, AB5, AB7, AB8, AB23, AB24, AD14	G	N/A	VSSC provides ground for the core logic.
PCI5VBIAS	M23, W25, Y22, AB22, AC10, AD9, AD18, AE6, AF12	I	N/A	Connects the PCI 5V Tolerant pins to 5 V in a 5 V system or to 3.3 V in a 3.3 V system.
NC	AC9	—	N/A	No Connect.

1. To reduce signal noise that can affect FSN functionality, place a ferrite bead in series with the VDDA and VSSA pins. LSI Logic recommends a bead with a rating of 150 Ω at 100 MHz.

3.10 Power-On Sense Pins Description

In addition to providing the address/data bus for the external memory interface, MAD[15:0] and MADP[1:0] provide eighteen Power-On Sense pins that configure global operating conditions within the LSI53C1030. The MAD[15:0] and MADP[1:0] pins have internal pull-down current sinks and sense a logical 0 if no pull-up resistor is present on the pin. To program a particular option, allow the internal pull-down to pull the pin LOW or connect a 4.7 k Ω resistor between the appropriate pin and VDD to pull the pin HIGH. The LSI53C1030 samples these pins during PCI reset and holds their values upon the removal of PCI reset. [Table 3.20](#) provides the MAD Power-On Sense pin configuration options. LSI Logic expects most configurations to employ the default settings. Provide pull-up options for all MAD pins.

Table 3.20 MAD Power-On Sense Pin Options

MAD Pin	Function	Pulled-Down (Default)	Pulled-Up
MADP[1]	Reserved		
MADP[0]	PCI-X Mode	Enables the PCI-X Mode.	Disables the PCI-X Mode.
MAD[15]	133 MHz PCI-X	Enables 133 MHz PCI-X Mode.	Disables 133 MHz PCI-X Mode.
MAD[14]	64-bit PCI	Configures a 64-bit PCI Bus.	Configures a 32-bit PCI Bus.
MAD[13]	66 MHz PCI	Enables the 66 MHz PCI Mode.	Disables the 66 MHz PCI Mode.
MAD[12]	Reserved		
MAD[11]	ID Control [1]	Has no effect.	Sets bit [15] of the PCI Function [1] Subsystem ID register to 0b1.
MAD[10]	ID Control [0]	Has no effect.	Sets bit [15] of the PCI Function [0] Subsystem ID register to 0b1.
MAD[9:8]	Reserved		
MAD[7]	Serial EEPROM Download Enable	Enables the download of the PCI configuration information from the serial EEPROM.	Disables the download of the PCI configuration information from the serial EEPROM.
MAD[6]	IOP Boot Enable	Enables the IOP boot process.	Disables the IOP boot process.
MAD[5:4]	PCI/SCSI Configuration	Configures the LSI53C1030 according to Table 3.21 .	

Table 3.20 MAD Power-On Sense Pin Options (Cont.)

MAD Pin	Function	Pulled-Down (Default)	Pulled-Up
MAD[3]	NVSRAM Select	Has no effect.	Configures the LSI53C1030 to support an NVSRAM.
MAD[2:1]	Flash ROM Size	Configures the Flash ROM size according to Table 3.22 .	
MAD[0]	Reserved		

- **MADP[1], Reserved.**
- **MADP[0], PCI-X Mode** – By default, internal logic pulls this pin LOW to enable the PCI-X mode on the LSI53C1030. Pulling this pin HIGH disables the PCI-X mode on the LSI53C1030. Pull this pin HIGH when the host board does not support the PCI-X mode. The setting of this pin must coincide with the setting of the PCI_CAP pin on the host board. When the PCI-X mode is disabled, the PCI-X extended capabilities register structure is not visible in PCI Configuration Space.
- **MAD[15], 133 MHz PCI-X** – By default, internal logic pulls this pin LOW to enable 133 MHz PCI-X operation and to set the 133 MHz Capable bit in the [PCI-X Status](#) register. Pulling this pin HIGH disables 133 MHz PCI-X operation and clears the 133 MHz Capable bit in the [PCI-X Status](#) register.
- **MAD[14], 64-bit PCI** – By default, internal logic pulls this pin LOW to enable 64-bit PCI operation and to set the 64-bit Enable bit in the [PCI-X Status](#) register. Pulling this pin HIGH configures the PCI connection as a 32-bit connection and clears the 64-bit Enable bit in the [PCI-X Status](#) register.
- **MAD[13], 66 MHz PCI** – By default, internal logic pulls this pin LOW to enable 66 MHz PCI operation on the LSI53C1030 and to set the 66 MHz Capable bit in the [PCI Status](#) register. Pulling this pin HIGH disables 66 MHz PCI operation and clears the 66 MHz Capable bit in the [PCI Status](#) register.
- **MAD[12], Reserved.**
- **MAD[11], ID Control [1]** – By default, internal logic pulls this pin LOW. Pulling this signal LOW either allows the serial EEPROM to program bit 15 of the PCI Function [1] [Subsystem ID](#) register or allows this bit to default to 0b0. Pulling this pin HIGH sets this bit to 0b1.

- **MAD[10], ID Control [0]** – By default, internal logic pulls this pin LOW. Pulling this signal LOW either allows the serial EEPROM to program bit 15 of the PCI Function [0] [Subsystem ID](#) register or allows this bit to default to 0b0. Pulling this pin HIGH sets this bit to 0b1.
- **MAD[9:8], Reserved.**
- **MAD[7], Serial EEPROM Download Enable** – By default, internal logic pulls this pin LOW to enable the download of PCI configuration information from the serial EEPROM. Pulling this pin HIGH disables the download of the PCI configuration information from the serial EEPROM. Disabling the download of PCI configuration information defaults the [Subsystem Vendor ID](#) register to 0x1000 and defaults [Subsystem ID](#) register for the respective PCI Function to either 0x1000 if MAD[11:10] are pulled LOW or to 0x8000 if MAD[11:10] are pulled HIGH.
- **MAD[6], IOP Boot Enable** – By default, internal logic pulls this pin LOW. In the default mode, the IOP starts the boot process and downloads firmware from the Flash ROM. Pulling this pin HIGH causes the IOP to await a firmware download from the host system.
- **MAD[5:4], PCI Single/Multifunction and SCSI Single/Dual Channel Configuration** – These pins work in conjunction with each other to configure the LSI53C1030 as a single function PCI-X to single channel SCSI controller or a multifunction PCI-X to dual channel SCSI controller. By default, hardware internally pulls MAD[5:4] down to configure the LSI53C1030 as multifunction PCI-X to dual channel SCSI controller. The user may pull MAD[5:4] HIGH to configure the LSI53C1030 as a single function PCI-X to single channel SCSI controller. This configuration enables PCI Function [0] and SCSI Channel [0], disables PCI Function [1] and SCSI Channel [1], and programs the PCI Function [0] [Header Type](#) register to indicate a single function PCI device. LSI Logic does not support multifunction PCI-X to single channel SCSI or single function PCI-X to dual channel SCSI configurations. [Table 3.21](#) provides the MAD[5:4] pin encoding definitions.

Table 3.21 PCI-X Function to SCSI Channel Configurations

MAD[5:4] Options	LSI53C1030 Configuration
0b00	Multifunction PCI-X to Dual Channel SCSI Controller
0b01	Reserved
0b10	Reserved
0b11	Single Function PCI-X to Single Channel SCSI Controller

- **MAD[3], NVSRAM Select** – By default, internal logic pulls this pin LOW, which has no effect on the LSI53C1030. Pulling this pin HIGH configures the external memory interface as an NVSRAM interface.
- **MAD[2:1], ROM Size** – These pins program the size of the Flash ROM memory. Refer to [Table 3.22](#) for the pin encoding. By default, internal logic pulls these pins LOW to indicate that a Flash ROM is not present in the system.

Table 3.22 Flash ROM Size Programming

MAD[2:1] Options	Flash ROM Size
0b00	Flash ROM not present (Default)
0b01	Up to 1024 Kbytes ¹
0b10	Reserved
0b11	

1. Choose this setting for a 128 Kbyte or 512 Kbyte Flash ROM.

- **MAD[0], Reserved.**

3.11 Internal Pull-Ups and Pull-Downs

Table 3.23 describes the pull-up and pull-down signals for the LSI53C1030.

Table 3.23 Pull-Up and Pull-Down Conditions

Signal Name	BGA Position	Pull Type
MAD[15:0], MADP[1:0]	D22, E21, B25, D23, E22, C24, F22, E23, D26, E25, H22, F24, G23, D25, F23, G22, C22, B24	Internal Pull-down.
SerialDATA, SerialCLK	H26, J25	Internal Pull-down. Pull-up externally when connected to a serial EEPROM.
GPIO[7:0]	K25, L23, L25, M25, H25, K24, AE25, AC23	Internal Pull-down.
TST_RST/	AD5	Internal Pull-up.
TCK_CHIP, TDI_CHIP, TMS_CHIP	AC6, AF3, AE4	Internal Pull-down.
TRST_ICE/, TCK_ICE, TDI_ICE, TMS_ICE	AB4, AA4, AB3, Y5	Internal Pull-down.
SCANEN, SCANMODE, IDDTN, CLKMODE_0, CLKMODE_1, TESTACLK, TESTCLKEN	N22, E7, Y4, AA22, AC2, AB6, D7	Internal Pull-down.
DIS_SCSI_FSN/, TESTHCLK, TN	AC4, AE2, C5	Internal Pull-up.
DIS_PCI_FSN/	A24	Internal Pull-down. Pull up externally to enable correct operation of the PCI FSN.
ZCR_EN/, IOPD_GNT/	N23, AC5	Internal Pull-up.

Chapter 4

PCI Host Register Description

This chapter describes the PCI host register space. This chapter consists of the following sections:

- [Section 4.1, “PCI Configuration Space Register Description”](#)
- [Section 4.2, “PCI I/O Space and Memory Space Register Description”](#)

The register map at the beginning of each register description provides the default bit settings for the register. Shading indicates a reserved bit or register. Do not access the reserved address areas.

There are two PCI functions on the LSI53C1030. Each PCI function has its own independent interrupt pin and its own PCI Address space. The PCI System Address space consists of three regions: Configuration Space, Memory Space, and I/O Space. PCI Configuration Space supports the identification, configuration, initialization and error management functions for the LSI53C1030 PCI devices.

PCI Memory Space [0] and Memory Space [1] form the PCI Memory Space. PCI Memory Space [0] provides normal system accesses to memory and PCI Memory Space [1] provides diagnostic memory accesses. PCI I/O Space provides normal system access to memory.

4.1 PCI Configuration Space Register Description

This section provides bit level descriptions of the PCI Configuration Space registers. [Table 4.1](#) defines the PCI Configuration Space registers. A separate set of PCI Configuration Space registers exists for each PCI function.

The LSI53C1030 enables, orders, and locates the PCI extended capability register structures (Power Management, Messaged Signalled

Interrupts, and PCI-X) to optimize device performance. The LSI53C1030 does not hard code the location and order of the PCI extended capability structures. The address and location of the PCI extended capability structures are subject to change. To access a PCI extended capability structure, follow the pointers held in the Capability Pointer registers and identify the extended capability structure with the Capability ID register for the given structure.

Table 4.1 LSI53C1030 PCI Configuration Space Address Map

31	16 15			0	Offset	Page
Device ID			Vendor ID		0x00	4-3
Status			Command		0x04	4-3
Class Code				Revision ID	0x08	4-7
Reserved	Header Type	Latency Timer	Cache Line Size		0x0C	4-7
I/O Base Address					0x10	4-9
Memory [0] Low					0x14	4-9
Memory [0] High					0x18	4-10
Memory [1] Low					0x1C	4-10
Memory [1] High					0x20	4-11
Reserved					0x24	–
					0x28	–
Subsystem ID		Subsystem Vendor ID			0x2C	4-12
Expansion ROM Base Address					0x30	4-14
Reserved				Capabilities Pointer	0x34	4-14
					0x38	–
Maximum Latency	Minimum Grant	Interrupt Pin	Interrupt Line		0x3C	4-15
Reserved					0x40– 0x7F	–
Power Management Capabilities		PM Next Pointer	PM Capability ID			4-17
PM Data	PM BSE	Power Management Control/Status				4-19
Reserved						–
Message Control		MSI Next Pointer	MSI Capability ID			4-21
Message Address						4-22
Message Upper Address						4-23
		Message Data				4-23
Reserved						–
PCI-X Command		PCI-X Next Pointer	PCI-X Capability ID			4-24
PCI-X Status						4-26
Reserved						–

Register: 0x00–0x01**Vendor ID****Read Only**

15															0
Vendor ID															
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Vendor ID [15:0]

This 16-bit register identifies the manufacturer of the device. The Vendor ID is 0x1000.

Register: 0x02–0x03**Device ID****Read Only**

15															0
Device ID															
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Device ID [15:0]

This 16-bit register identifies the particular device. The default Device ID for the LSI53C1030 is 0x0030.

Register: 0x04–0x05**Command****Read/Write**

15							9	8	7	6	5	4	3	2	1	0
Command																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Command register provides coarse control over the PCI function's ability to generate and respond to PCI cycles. Writing a zero to this register logically disconnects the LSI53C1030 PCI function from the PCI bus for all accesses except configuration accesses.

Reserved [15:9]

This field is reserved.

SERR/ Enable	8
Setting this bit enables the LSI53C1030 to activate the SERR/ driver. Clearing this bit disables the SERR/ driver.	
Reserved	7
This bit is reserved.	
Enable Parity Error Response	6
Setting this bit enables the LSI53C1030 PCI function to detect parity errors on the PCI bus and report these errors to the system. Clearing this bit causes the LSI53C1030 PCI function to set the Detected Parity Error bit, bit 15 in the PCI Status register, but not assert PERR/ when the PCI function detects a parity error. This bit only affects parity checking. The PCI function always generates parity for the PCI bus.	
Reserved	5
This bit is reserved.	
Write and Invalidate Enable	4
Setting this bit enables the PCI function to generate write and invalidate commands on the PCI bus when operating in the conventional PCI mode.	
Reserved	3
This bit is reserved.	
Enable Bus Mastering	2
Setting this bit allows the PCI function to behave as a PCI bus master. Clearing this bit disables the PCI function from generating PCI bus master accesses.	
Enable Memory Space	1
This bit controls the ability of the PCI function to respond to Memory Space accesses. Setting this bit allows the LSI53C1030 to respond to Memory Space accesses at the address range specified by the Memory [0] Low , Memory [0] High , Memory [1] Low , Memory [1] High , and Expansion ROM Base Address registers. Clearing this bit disables the PCI function's response to PCI Memory Space accesses.	

Enable I/O Space **0**

This bit controls the LSI53C1030 PCI function's response to I/O Space accesses. Setting this bit enables the PCI function to respond to I/O Space accesses at the address range the PCI Configuration Space [I/O Base Address](#) register specifies. Clearing this bit disables the PCI function's response to I/O Space accesses.

Register: 0x06–0x07**Status****Read/Write**

15	14	13	12	11	10	9	8	7	6	5	4	3				0
Status																
0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0

Reads to this register behave normally. To clear a bit location that is currently set, write the bit to one (1). For example, to clear bit 15 when it is set, without affecting any other bits, write 0x8000 to the register.

Detected Parity Error (from Slave) **15**

This bit is set per the *PCI Local Bus Specification, Revision 2.2*, and *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*.

Signalled System Error **14**

The LSI53C1030 PCI function sets this bit when asserting the SERR/ signal.

Received Master Abort (from Master) **13**

A master device sets this bit when a Master Abort command terminates its transaction (except for Special Cycle).

Received Target Abort (from Master) **12**

A master device sets this bit when a Target Abort command terminates its transaction.

Reserved **11**

This bit is reserved.

DEVSEL/ Timing **[10:9]**

These two read only bits encode the timing of DEVSEL/ and indicate the slowest time that a device asserts

DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSI53C1030 only supports medium DEVSEL/ timing. The possible timing values are:

0b00	Fast
0b01	Medium
0b10	Slow
0b11	Reserved

Data Parity Error Reported 8

This bit is set per the *PCI Local Bus Specification, Revision 2.2*, and *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*. Refer to bit 0 of the [PCI-X Command](#) register for more information.

Reserved [7:6]

This field is reserved.

66 MHz Capable 5

The MAD[13] Power-On Sense pin controls this bit. Allowing the internal pull-down to pull MAD[13] LOW sets this bit and indicates to the host system that the LSI53C1030 PCI function is capable of operating at 66 MHz. Pulling MAD[13] HIGH clears this bit and indicates to the host system that the LSI53C1030 PCI function is not configured to operate at 66 MHz. Refer to [Section 3.10, "Power-On Sense Pins Description,"](#) for more information.

New Capabilities 4

The LSI53C1030 PCI function sets this read only bit to indicate a list of PCI extended capabilities such as PCI Power Management, MSI, and PCI-X support.

Reserved [3:0]

This field is reserved.

Register: 0x08**Revision ID****Read/Write**

7							0
Revision ID							
X	X	X	X	X	X	X	X

Revision ID**[7:0]**

This register indicates the current revision level of the device.

Register: 0x09–0x0B**Class Code****Read Only**

23																							0
Class Code																							
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Class Code**[23:0]**

This 24-bit register identifies the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface. The value of this register is 0x010000, which identifies a SCSI controller.

Register: 0x0C**Cache Line Size****Read/Write**

7				3		2		0	
Cache Line Size									
0	0	0	0	0	0	0	0	0	0

Cache Line Size**[7:3]**

This register specifies the system cache line size in units of 32-bit words. In the conventional PCI mode, the LSI53C1030 PCI function uses this register to determine whether to use Write and Invalidate or Write commands

for performing write cycles. Programming this register to a number other than a nonzero power of two disables the use of the PCI performance commands to execute data transfers. The PCI function ignores this register when operating in the PCI-X mode.

Reserved [2:0]
This field is reserved.

Register: 0x0D

Latency Timer

Read/Write

7			4		3		0
Latency Timer							
0	X	0	0	0	0	0	0

Latency Timer [7:4]

The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. If the LSI53C1030 initializes in the PCI mode, the default value of this register is 0x00. If the LSI53C1030 initializes in the PCI-X mode, the default value of this register is 0x40.

Reserved [3:0]
This field is reserved.

Register: 0x0E

Header Type

Read Only

7							0
Header Type							
X	0	0	0	0	0	0	0

Header Type [7:0]

This 8-bit register identifies the layout of bytes 0x10 through 0x3F in configuration space and also indicates if the device is a single function or multifunction PCI device. If the LSI53C1030 is configured as a multifunction PCI device, bit 7 is set. If the LSI53C1030 is configured as a single function PCI device, bit 7 is cleared.

Register: 0x0F
Reserved

7								0
Reserved								
0	0	0	0	0	0	0	0	

Reserved [7:0]
This register is reserved.

Register: 0x10–0x13
I/O Base Address
Read/Write

31																														2	1	0
I/O Base Address																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The I/O Base Address register maps the operating register set into I/O Space. The LSI53C1030 requires 256 bytes of I/O Space for this base address register. Hardware sets bit 0 to 0b1. Bit 1 is reserved and returns 0b0 on all reads.

I/O Base Address [31:2]
This field contains the I/O Base address.

Reserved [1:0]
This field is reserved.

Register: 0x14–0x17
Memory [0] Low
Read/Write

31	Memory [0] Low																														0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

The [Memory \[0\] Low](#) register and the [Memory \[0\] High](#) register map SCSI operating registers into Memory Space [0]. This register contains the lower 32 bits of the Memory Space [0] base address. Hardware programs bits [9:0] to 0b0000000100, which indicates that the Memory

Space [0] base address is 64 bits wide and that the memory data is not prefetchable. The LSI53C1030 requires 1024 bytes of memory space.

Memory [0] Low [31:0]

This field contains the Memory [0] Low address.

Register: 0x18–0x1B

Memory [0] High

Read/Write

31	Memory [0] High																																0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The [Memory \[0\] High](#) register and the [Memory \[0\] Low](#) register map SCSI operating registers into Memory Space [0]. This register contains the upper 32 bits of the Memory Space [0] base address. The LSI53C1030 requires 1024 bytes of memory space.

Memory [0] High [31:0]

This field contains the Memory [0] High address.

Register: 0x1C–0x1F

Memory [1] Low

Read/Write

31	Memory [1] Low																																0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

The [Memory \[1\] Low](#) register and the [Memory \[1\] High](#) register map the RAM into Memory Space [1]. This register contains the lower 32 bits of the Memory Space [1] base address. Hardware programs bits [12:0] to 0b00000000000100, which indicates that the Memory Space [1] base address is 64 bits wide and that the memory data is not prefetchable. The LSI53C1030 requires 64 Kbytes of memory for Memory Space [1].

Memory [1] Low [31:0]

This field contains the Memory [1] Low address.

Register: 0x20–0x23**Memory [1] High****Read/Write**

31	Memory [1] High																														0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The [Memory \[1\] High](#) register and the [Memory \[1\] Low](#) register map the RAM into Memory Space [1]. This register contains the upper 32 bits of the Memory Space [1] base address. The LSI53C1030 requires 64 Kbytes of memory for Memory Space [1].

Memory [1] High**[31:0]**

This field contains the Memory [1] High address.

Register: 0x24–0x27**Reserved**

31	Reserved																														0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved**[31:0]**

This register is reserved.

Register: 0x28–0x2B**Reserved**

31	Reserved																														0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved**[31:0]**

This register is reserved.

Register: 0x2C–0x2D
Subsystem Vendor ID
Read Only

15	Subsystem Vendor ID														0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Subsystem Vendor ID [15:0]

This 16-bit register uniquely identifies the vendor that manufactures the add-in board or subsystem where the LSI53C1030 resides. This register provides a mechanism for an add-in card vendor to distinguish their cards from another vendor's cards, even if the cards use the same PCI controller (and have the same Vendor ID and Device ID).

The external serial EEPROM can hold a vendor-specific, 16-bit value for this register, which the board designer must obtain from the PCI Special Interest Group (PCI-SIG). By default, an internal pull-down on the MAD[7] Power-On Sense pin enables the serial EEPROM interface so that the LSI53C1030 can load this register from the serial EEPROM at power-up. If the download from the EEPROM fails, this register contains 0x0000.

If the board designer disables the EEPROM interface by pulling the MAD[7] Power-On Sense pin HIGH, this register returns a value of 0x1000. Refer to [Section 3.10, "Power-On Sense Pins Description," page 3-21](#), for more information.

Register: 0x2E–0x2F
Subsystem ID
Read Only

15	Subsystem ID														0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Subsystem ID [15:0]

This 16-bit register uniquely identifies the add-in board or subsystem where this PCI device resides. This register provides a mechanism for an add-in card vendor to dis-

tinguish their cards from one another even if the cards use the same PCI controller (and have the same Vendor ID and Device ID). The board designer can store a vendor specific, 16-bit value in an external serial EEPROM.

The ID Control Power-On Sense pins (MAD[11] for PCI Function [1]; MAD[10] for PCI Function [0]) and the serial EEPROM enable Power-On Sense pin (MAD[7]) control the value of this register. These pins have internal pull downs. Allowing MAD[7] to remain internally pulled down enables the serial EEPROM interface and permits the LSI53C1030 to load this register from the serial EEPROM at power up. Pulling MAD[7] HIGH disables the serial EEPROM interface. Allowing the ID Control pins to remain internally pulled LOW has no effect on this register. Pulling the ID Control pins HIGH sets bit [15] of this register for the given PCI function. Pulling the ID Control pins HIGH takes precedence over all other settings for bit [15].

Table 4.2 lists the configuration options for the Power-On Sense pins and settings for this register. If the serial EEPROM interface is disabled and the ID Control pins are internally pulled LOW, this register contains 0x1000. If the serial EEPROM interface is disabled and the ID Control pins are pulled HIGH, this register contains 0x8000. If a download from the serial EEPROM fails and the ID Control pins are internally pulled LOW, this register contains 0x0000. If a download from the serial EEPROM fails and the ID Control pins are pulled HIGH, this register contains 0x8000. Refer to [Section 3.10, “Power-On Sense Pins Description,”](#) for additional information.

Table 4.2 Subsystem ID Register Download Conditions and Values

MAD[7] State	MAD[11] or MAD[10] LOW	MAD[11] or MAD[10] HIGH
MAD[7] LOW	Subsystem ID = 0XXXXX Bits [15:0] are downloaded. ¹ (Default)	Subsystem ID = 0b1XXXXXXXXXXXXXXXXX Bits [14:0] are downloaded with Bit [15] set. ²
MAD[7] HIGH	Subsystem ID register = 0x1000.	Subsystem ID = 0x8000.

1. The Subsystem ID register returns 0x0000 if the serial EEPROM download fails.

2. The Subsystem ID register returns 0x8000 if the serial EEPROM download fails.

Register: 0x30–0x33
Expansion ROM Base Address
Read/Write

[illegible]

This four-byte register contains the base address and size information for the expansion ROM.

Expansion ROM Base Address	[31:11]
-----------------------------------	----------------

These bits correspond to the upper 21 bits of the expansion ROM base address. The host system detects the size of the external memory by first writing 0xFFFFFFFF to this register and then reading the register back. The LSI53C1030 responds with zeros in all don't care locations. The least significant one (1) that remains represents the binary version of the external memory size. For example, to indicate an external memory size of 32 Kbytes, this register returns ones in the upper 17 bits when written with 0xFFFFFFFF and read back.

Reserved **[10:1]**

This field is reserved.

Expansion ROM Enable	0
----------------------	---

This bit controls if the device accepts accesses to its expansion ROM. Setting this bit enables address decoding. Depending on the system configuration, the device can optionally use an expansion ROM. Note that to access the expansion ROM, the user must also set bit 1 in the PCI **Command** register.

Register: 0x34
Capabilities Pointer
Read Only

7							0
Capabilities Pointer							
X	X	X	X	X	X	X	X

Capabilities Pointer [7:0]

This register indicates the location of the first extended capabilities register in PCI Configuration Space. The value of this register varies according to system configuration.

Register: 0x35–0x37

Reserved

23	Reserved																											0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved [23:0]

This register is reserved.

Register: 0x38–0x3B

Reserved

31	Reserved																												0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reserved [31:0]

This register is reserved.

Register: 0x3C

Interrupt Line

Read/Write

7								0
Interrupt Line								
0	0	0	0	0	0	0	0	

Interrupt Line [7:0]

This register communicates interrupt line routing information. Power-On-Self-Test (POST) software writes the routing information into this register as it configures the system. This register indicates the system interrupt controller input to which this PCI function's interrupt pin connects. System architecture determines the values in this register.

Register: 0x3D

Interrupt Pin

Read Only

7							0
Function [0] Interrupt Pin							
0	0	0	0	0	0	0	1
Function [1] Interrupt Pin							
0	0	0	0	0	0	1	0

Interrupt Pin

[7:0]

The encoding of this read only register is unique to each function on the LSI53C1030. It indicates which interrupt pin the function uses. The value for Function [0] is 0x01, which indicates that Function [0] presents interrupts on the INTA/ or ALT_INTA pins. The value for Function [1] is 0x02, which indicates that Function [1] presents interrupts on the INTB/ or ALT_INTB/ pins. The Interrupt Request Routing Mode bits, bits [9:8] in the [Host Interrupt Mask](#) register, determine if the function presents interrupts on INTx/, ALT_INTx/, or both.

Register: 0x3E

Minimum Grant

Read Only

7							0
Minimum Grant							
0	0	0	1	0	0	0	0

Min_Gnt

[7:0]

This register specifies the desired settings for the latency timer values in units of 0.25 μ s. This register specifies how long of a burst period the device needs. The LSI53C1030 sets this register to 0x10, indicating a burst period of 4.0 μ s.

Register: 0x3F**Maximum Latency****Read Only**

7							0
Maximum Latency							
0	0	0	0	0	1	1	0

Max_Lat**[7:0]**

This register specifies the desired settings for the latency timer values in units of 0.25 μ s. Max_Lat specifies how often the device needs to gain access to the PCI bus.

The LSI53C1030 SCSI function sets this register to 0x06 since it requires the PCI bus every 1.5 μ s to maintain a data transfer rate of 320 Mbytes/s.

Register: 0xXX**Power Management Capability ID****Read Only**

7								0
Power Management Capability ID								
0	0	0	0	0	0	0	0	1

Power Management Capability ID**[7:0]**

This register indicates the type of the current data structure. It is set to 0x01 to indicate the Power Management Data Structure.

Register: 0xXX**Power Management Next Pointer****Read Only**

7							0
Power Management Next Pointer							
X	X	X	X	X	X	X	X

Power Management Next Pointer**[7:0]**

This register contains the pointer to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

Register: 0xXX
Power Management Capabilities
Read Only

15						11	10	9	8	7	6	5	4	3	2		0
Power Management Capabilities																	
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0

PME_Support [15:11]

These bits define the power management states in which the device asserts the Power Management Event (PME) pin. The LSI53C1030 clears these bits since the LSI53C1030 does not provide a PME signal.

D2_Support 10

The PCI function sets this bit since the LSI53C1030 supports power management state D2.

D1_Support 9

The PCI function sets this bit since the LSI53C1030 supports power management state D1.

Aux_Current [8:6]

The PCI function clears this field since the LSI53C1030 does not support Aux_Current.

Device Specific Initialization 5

The PCI function clears this bit since no special initialization is required before a generic class device driver can use it.

Reserved 4

This bit is reserved.

PME Clock 3

The LSI53C1030 clears this bit since the chip does not provide a PME pin.

Version [2:0]

The PCI function programs these bits to 0b010 to indicate that the LSI53C1030 complies with the *PCI Power Management Interface Specification, Revision 1.1*.

Register: 0xXX
Power Management Control/Status
Read/Write

15	14	13					9	8	7					2	1	0
Power Management Control/Status																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PME_Status **15**

The PCI function clears this bit since the LSI53C1030 does not support PME signal generation from D3_{cold}.

Data_Scale **[14:13]**

The PCI function clears these bits since the LSI53C1030 does not support the Power Management Data register.

Data_Select **[12:9]**

The PCI function clears these bits since the LSI53C1030 does not support the Power Management Data register.

PME_Enable **8**

The PCI function clears this bit since the LSI53C1030 does not provide a PME signal and disables PME assertion.

Reserved **[7:2]**

This field is reserved.

Power State **[1:0]**

These bits determine the current power state of the LSI53C1030. Power states are:

0b00	D0
0b01	D1
0b10	D2
0b11	D3 _{hot}

Register: 0xXX**Power Management Bridge Support Extensions****Read Only**

7							0
Power Management Bridge Support Extensions							
0	0	0	0	0	0	0	0

Power Management Bridge Support Extensions [7:0]

This register indicates PCI Bridge specific functionality.

The LSI53C1030 always returns 0x00 in this register.

Register: 0xXX**Power Management Data****Read Only**

7							0
Power Management Data							
0	0	0	0	0	0	0	0

Power Management Data [7:0]

This register provides an optional mechanism for the PCI function to report state-dependent operating data. The LSI53C1030 always returns 0x00 in this register.

Register: 0xXX**MSI Capability ID****Read Only**

7							0
MSI Capability ID							
0	0	0	0	0	1	0	1

MSI Capability ID [7:0]

This register indicates the type of the current data structure. This register always returns 0x05, indicating Message Signalled Interrupts (MSI).

Register: 0xXX
MSI Next Pointer
Read Only

7							0
MSI Next Pointer							
X	X	X	X	X	X	X	X

MSI Next Pointer [7:0]
This register points to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

Register: 0xXX
Message Control
Read/Write

15					8	7	6					4	3					1	0
Message Control																			
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0		

Reserved [15:8]
This field is reserved.

64-bit Address Capable 7
The PCI function sets this read only bit to indicate support of a 64-bit message address.

Multiple Message Enable [6:4]
These read/write bits indicate the number of messages that the host allocates to the LSI53C1030. The host system software allocates all or a subset of the requested messages by writing to this field. The number of allocated request messages must align to a power of two. [Table 4.3](#) provides the bit encoding of this field.

Table 4.3 Multiple Message Enable Field Bit Encoding

Bits [6:4] Encoding	Number of Allocated Messages
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	Reserved
0b111	Reserved

Multiple Message Capable [3:1]

These read only bits indicate the number of messages that the LSI53C1030 requests from the host. The host system software reads this field to determine the number of requested messages. The number of requested messages must align to a power of two. The LSI53C1030 sets this field to 0b000 to request one message. All other encodings of this field are reserved.

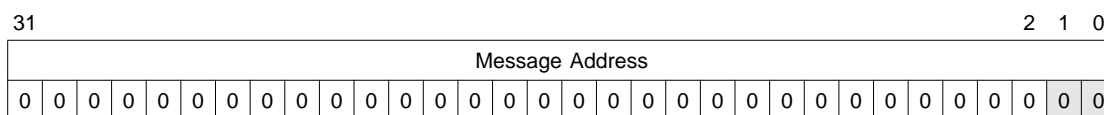
MSI Enable	0
------------	---

System software sets this bit to enable MSI. Setting this bit enables the device to use MSI to interrupt the host and request service. Setting this bit also prohibits the device from using the INTx_/ or ALT_INTx_/ pins to request service from the host. Setting this bit to mask interrupts on the INTx_/ or ALT_INTx_/ pins is a violation of the PCI specification.

Register: 0xXX

Message Address

Read/Write



Message Address [31:2]

This register contains message address bits [31:2] for the MSI memory write transaction. The host system specifies and Dword aligns the message address. During the address phase, the LSI53C1030 drives Message Address[1:0] to 0b00.

Reserved [1:0]

This field is reserved.

Register: 0xXX
Message Upper Address
Read/Write

31	Message Upper Address																												0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Message Upper Address [31:0]

The LSI53C1030 supports 64-bit MSI. This register contains the upper 32 bits of the 64-bit message address, which the system specifies. The host system software can program this register to 0x0000 to force the PCI function to generate 32-bit message addresses.

Register: 0xXX
Message Data
Read/Write

15	Message Data														0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Message Data [15:0]

System software initializes this register by writing to it. The LSI53C1030 sends an interrupt message by writing a Dword to the address held in the [Message Address](#) and [Message Upper Address](#) registers. This register forms bits [15:0] of the Dword message that the PCI function passes to the host. The PCI function drives bits [31:16] of this message to 0x0000.

Register: 0xXX
PCI-X Capability ID
Read Only

7							0
PCI-X Capability ID							
0	0	0	0	0	1	1	1

PCI-X Capability ID [7:0]

This register indicates the type of the current data structure. This register returns 0x07, indicating the PCI-X Data Structure.

Register: 0xXX
PCI-X Next Pointer
Read Only

7							0
PCI-X Next Pointer							
X	X	X	X	X	X	X	X

PCI-X Next Capabilities Pointer [7:0]

This register points to the next item in the device's capabilities list. The value of this register varies according to system configuration.

Register: 0xXX
PCI-X Command
Read/Write

15								7	6					4	3	2	1	0
PCI-X Command																		
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Reserved [15:7]

This field is reserved.

Maximum Outstanding Split Transactions [6:4]

These bits indicate the maximum number of split transactions the LSI53C1030 can have outstanding at one time. The LSI53C1030 uses the most recent value of this register each time it prepares a new sequence. Note that if

the LSI53C1030 prepares a sequence before the setting of this field changes, the PCI function initiates the prepared sequence with the previous setting. [Table 4.4](#) provides the bit encodings for this field.

Table 4.4 Maximum Outstanding Split Transactions

Bits [6:4] Encoding	Maximum Outstanding Split Transactions
0b000	1
0b001	2
0b010	3
0b011	4
0b100	8
0b101	Reserved
0b110	Reserved
0b111	Reserved

Maximum Memory Read Byte Count [3:2]

These bits indicate the maximum byte count the LSI53C1030 uses when initiating a sequence with one of the burst memory read commands. [Table 4.5](#) provides the bit encodings for this field.

Table 4.5 Maximum Memory Read Count

Bits [3:2] Encoding	Maximum Memory Read Byte Count
0b00	512
0b01	1024
0b10	2048
0b11	Reserved

Reserved

This bit is reserved.

1

Data Parity Error Recovery Enable 0

The host device driver sets this bit to allow the LSI53C1030 to attempt to recover from data parity errors. If the user clears this bit and the LSI53C1030 is operating in the PCI-X mode, the LSI53C1030 asserts SERR/ whenever the Master Data Parity Error bit in the PCI Status register is set.

Register: 0xXX

PCI-X Status

Read/Write

31	30	29	28	27	26	25	23	22	21	20	19	18	17	16	15	8	7	3	2	0
PCI-X Status																				
0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	1	X	X	X	X	X

Reserved [31:30]

This field is reserved.

Received Split Completion Error Message 29

The LSI53C1030 sets this bit upon receipt of a split completion message if the split completion error attribute bit is set. Write a one (1) to this bit to clear it.

Designed Maximum Cumulative Read Size [28:26]

These read only bits indicate a number greater than or equal to the maximum cumulative size of all outstanding burst memory read transactions for the LSI53C1030 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1030 reports 0b001 in this field to indicate a designed maximum cumulative read size of 2 Kbytes.

Designed Maximum Outstanding Split Transactions [25:23]

These read only bits indicate a number greater than or equal to the maximum number of all outstanding split transactions for the LSI53C1030 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1030 reports 0b100 in this field to indicate that the designed maximum number of outstanding split transactions is eight.

Designed Maximum Memory Read

Byte Count

[22:21]

These read only bits indicate a number greater than or equal to the maximum byte count for the LSI53C1030 device. The PCI function uses this count to initiate a sequence with one of the burst memory read commands. The PCI function must report the smallest value that correctly indicates its capability. The LSI53C1030 reports 0b10 in this field to indicate that the designed maximum memory read bytes count is 2048.

Device Complexity

20

The PCI function clears this read only bit to indicate that the LSI53C1030 is a simple device.

Unexpected Split Completion

19

The PCI function sets this read only bit when it receives an unexpected split completion. Once set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

Split Completion Discarded

18

The PCI function sets this read only bit when it discards a split completion. Once set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

133 MHz Capable

17

The MAD[15] Power-On Sense pin controls this read only bit. Allowing the internal pull-downs to pull MAD[15] LOW sets this bit and enables 133 MHz operation of the PCI bus. Pulling MAD[15] HIGH clears this bit and disables 133 MHz operation of the PCI bus. Refer to [Section 3.10, "Power-On Sense Pins Description,"](#) for more information concerning the Power-On Sense pins.

64-bit Device

16

The MAD[14] Power-On Sense pin controls this read only bit. Allowing the internal pull-downs to pull MAD[14] LOW sets this bit and indicates a 64-bit PCI Address/Data bus. Pulling MAD[14] HIGH clears this bit and indicates a 32-bit PCI Address/Data bus. If using the LSI53C1030 on an add-in card, this bit must indicate the size of the card's PCI Address/Data bus. Refer to [Section 3.10, "Power-On Sense Pins Description,"](#) for more information concerning the Power-On Sense pins.

Bus Number [15:8]

These read only bits indicate the number of the LSI53C1030 bus segment. This PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

Device Number [7:3]

These read only bits indicate the device number of the LSI53C1030. This PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

Function Number [2:0]

These read only bits indicate the number in the Function Number field (AD[10:8]) of a Type 0 PCI configuration transaction. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

4.2 PCI I/O Space and Memory Space Register Description

This section describes the host interface registers in the PCI I/O Space and PCI Memory Space. These address spaces contain the Fusion-MPT interface register set. PCI Memory Space [0] and PCI Memory Space [1] form the PCI Memory Space. PCI Memory [0] supports normal memory accesses while PCI Memory Space [1] supports diagnostic memory accesses. For all registers except the [Diagnostic Read/Write Data](#) and [Diagnostic Read/Write Address](#) registers, access the address offset through either PCI I/O Space or PCI Memory Space [0]. Access to the [Diagnostic Read/Write Data](#) and [Diagnostic Read/Write Address](#) registers is only through PCI I/O Space.

When the LSI53C1030 operates as a multifunction PCI device, the entire PCI Memory and PCI I/O Space register sets are visible to both PCI functions. When the LSI53C1030 operates as a single function PCI device, only PCI Function [0] register sets are accessible. Refer to [Section 3.10, “Power-On Sense Pins Description,”](#) for information on how to configure the LSI53C1030 as a single or multifunction PCI device.

[Table 4.6](#) defines the PCI I/O Space address map.

Table 4.6 PCI I/O Space Address Map

31	0	Offset	Page
		System Doorbell	0x00004-30
		Write Sequence	0x00044-30
		Host Diagnostic	0x00084-31
		Test Base Address	0x000C4-33
		Diagnostic Read/Write Data	0x00104-33
		Diagnostic Read/Write Address	0x00144-34
		Reserved	0x0018–0x002F–
		Host Interrupt Status	0x00304-35
		Host Interrupt Mask	0x00344-36
		Reserved	0x0038–0x003F–
		Request FIFO	0x00404-37
		Reply FIFO	0x00444-37
		Reserved	0x0048–0x007F–

Table 4.7 defines the PCI Memory Space [0] address map.

Table 4.7 PCI Memory [0] Address Map

31	0	Offset	Page
	System Doorbell	0x0000	4-30
	Write Sequence	0x0004	4-30
	Host Diagnostic	0x0008	4-31
	Test Base Address	0x000C	4-33
	Reserved	0x0010–0x002F	–
	Host Interrupt Status	0x0030	4-35
	Host Interrupt Mask	0x0034	4-36
	Reserved	0x0038–0x003F	–
	Request FIFO	0x0040	4-37
	Reply FIFO	0x0044	4-37
	Reserved	0x0048–0x007F	–
	Shared Memory	0x0080– 0x(Sizeof(Mem0)–1)	–

Table 4.8 defines the PCI Memory Space [1] address map.

Table 4.8 PCI Memory [1] Address Map

31	0
Diagnostic Memory	0x0000– 0x(Sizeof(Mem1)–1)

A bit level description of the PCI Memory and PCI I/O Spaces follows.

Register: 0x00
System Doorbell
Read/Write

31	System Doorbell																												0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The System Doorbell register is a simple message passing mechanism that allows the system to pass single word messages to the embedded IOP processor and vice-versa. There is a unique system doorbell for each PCI function.

When a host system PCI master writes to the Host Registers->Doorbell register, the LSI53C1030 generates a maskable interrupt to the IOP. The value written by the host system is available for the IOP to read in the System Interface Registers->Doorbell register. The IOP clears the interrupt status after reading the value.

Conversely, when the IOP processor writes to the System Interface Registers->Doorbell register, the LSI53C1030 generates a maskable interrupt to the PCI system. The host system can read the value written by the IOP in the Host Registers->Doorbell register. The host system clears the interrupt status bit and interrupt pin by writing any value to the Host Registers->Interrupt Status register.

Host Doorbell Value **[31:0]**

During a write, this register contains the doorbell value that the host system passes to the IOP. During a read, this register contains the doorbell value that the IOP passes to the host system.

Register: 0x04
Write Sequence
Read/Write

31																										4	3	0	
Write Sequence																													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

The Write Sequence register provides a protection mechanism against inadvertent writes to the [Host Diagnostic](#) register. There is one Write

Sequence register that is visible to both PCI functions. The two PCI functions physically share this register.

Reserved

[31:4]

This field is reserved.

Write I/O Key

[3:0]

To enable write access to the [Diagnostic Read/Write Data](#), [Diagnostic Read/Write Address](#), and [Host Diagnostic](#) registers, perform five data-specific writes to the Write I/O Key. Writing an incorrect value to the Write I/O Key invalidates the key sequence and the host must rewrite the entire sequence. The Write I/O Key sequence is: 0x0004, 0x000B, 0x0002, 0x0007, and 0x000D. To disable write access to the [Diagnostic Read/Write Data](#), [Diagnostic Read/Write Address](#), and [Host Diagnostic](#) registers, perform a write of any value, except the Write I/O Key sequence, to the Write Sequence register. The Diagnostic Write Enable bit, bit 7 in the [Host Diagnostic](#) register, indicates the write access status.

Register: 0x08

**Host Diagnostic
Read/Write**

[illegible]

The Host Diagnostic register contains diagnostic controls and status information. There is one [Host Diagnostic](#) register that is visible to both PCI functions. The two PCI functions physically share this register. However, the Reset History bit operates independently for each PCI function. This register can only be written when bit 7 of this register is set.

Reserved

[31:8]

This field is reserved.

Diagnostic Write Enable

7

The LSI53C1030 sets this read only bit when the host writes the correct Write I/O Key to the [Write Sequence](#) register. The LSI53C1030 clears this bit when the host

writes a value other than the Write I/O Key to the [Write Sequence](#) register.

Flash Bad Signature **6**

The LSI53C1030 sets this bit if the IOP ARM966E-S processor encounters a bad Flash signature when booting from Flash ROM. The LSI53C1030 also sets the DisARM bit (bit 1 in this register) to hold the IOP ARM processor in a reset state. The LSI53C1030 maintains this state until the PCI host clears both the Flash Bad Signature and DisARM bits.

Reset History **5**

The LSI53C1030 sets this bit if it experiences a Power On Reset (POR), PCI Reset, or TestReset/. A host driver can clear this bit to help coordinate recovery between multiple driver instances in a multifunction PCI implementation.

Diagnostic Read/Write Enable **4**

Setting this bit enables access to the [Diagnostic Read/Write Data](#) and [Diagnostic Read/Write Address](#) registers.

TTL Interrupt **3**

Setting this bit configures PCI INTA/ as a TTL output. Clearing this bit configures PCI INTA/ as an open-drain output. Use this bit for test purposes only.

Reset Adapter **2**

Setting this write only bit causes a hard reset within the LSI53C1030. The bit self-clears after eight PCI clock periods. After deasserting this bit, the IOP ARM processor executes from its default reset vector.

DisARM **1**

Setting this bit disables the ARM processor.

Diagnostic Memory Enable **0**

Setting this bit enables diagnostic memory accesses through PCI Memory Space [1]. Clearing this bit disables diagnostic memory accesses to PCI Memory Space [1] and returns 0xFFFF on reads.

Register: 0x0C
Test Base Address
Read/Write

31	16 15																												0	
Test Base Address																														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Test Base Address register specifies the base address for Memory Space [1] accesses. There is one Test Base Address register that is visible to both PCI functions. The two PCI functions physically share this register. Because Diagnostic Memory is visible only to PCI Function [0], PCI Function [1] cannot write to this register.

Test Base Address **[31:16]**

The number of significant bits is determined by the size of the PCI Memory Space [1] in the serial EEPROM.

Reserved **[15:0]**

This field is reserved.

Register: 0x10
Diagnostic Read/Write Data
Read/Write

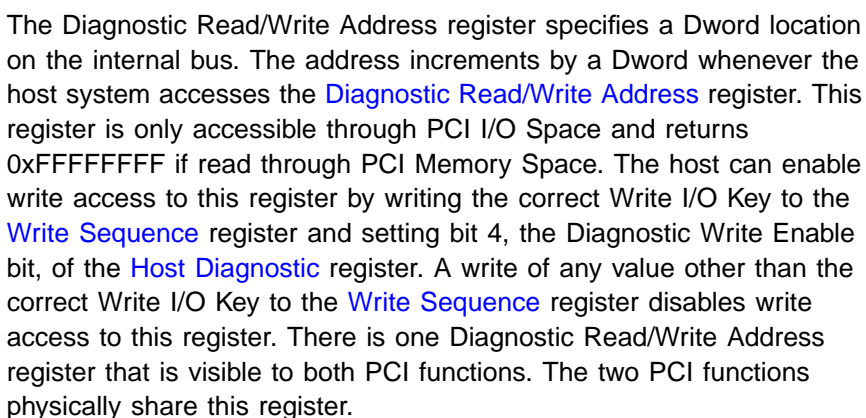
31																															0	
Diagnostic Read/Write Data																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register reads or writes Dword locations on the LSI53C1030 internal bus. This register is only accessible through PCI I/O Space and returns 0xFFFFFFFF if read through PCI Memory Space. The host can enable write access to this register by writing the correct Write I/O Key to the [Write Sequence](#) register and setting bit 4, the Diagnostic Write Enable bit, of the [Host Diagnostic](#) register. A write of any value other than the correct Write I/O Key to the [Write Sequence](#) register disables write access to this register. There is one [Diagnostic Read/Write Data](#) register that is visible to both PCI functions. The two PCI functions physically share this register.

[31:0]

Register: 0x14

Read/Write



[31:0]

This register holds the address that the **Diagnostic Read/Write Data** register writes data to or reads data from.

Register: 0x30
Host Interrupt Status
Read/Write

31 30																												4 3 2 1 0				
Host Interrupt Status																																
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	0	

The Host Interrupt Status register provides read only interrupt status information to the PCI Host. A write to this register of any value clears the associated System Doorbell interrupt. There is a unique Host Interrupt Status register for each PCI function.

IOP Doorbell Status **31**

The LSI53C1030 sets this bit when the IOP receives a message from the system doorbell but has yet to process it. The IOP processes the System Doorbell message by clearing the corresponding system request interrupt.

Reserved **[30:4]**

This field is reserved.

Reply Interrupt **3**

The LSI53C1030 sets this bit when the Reply Post FIFO is not empty. The LSI53C1030 generates a PCI interrupt when this bit is set and the corresponding mask bit in the [Host Interrupt Mask](#) register is cleared.

Reserved **[2:1]**

This field is reserved.

System Doorbell Interrupt **0**

The LSI53C1030 sets this bit when the IOP writes a value to the System Doorbell. The host can clear this bit by writing any value to this register. The LSI53C1030 generates a PCI interrupt when this bit is set and the corresponding mask bit in the [Host Interrupt Mask](#) register is cleared.

Register: 0x34
Host Interrupt Mask
Read/Write

31																10 9 8 7				4 3 2 1 0								
Host Interrupt Mask																												
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X	X	1	X	X	1

The Host Interrupt Mask register masks and/or routes the interrupt conditions that the [Host Interrupt Status](#) register reports. There is a unique Host Interrupt Mask register for each PCI function.

Reserved **[31:10]**

This field is reserved.

Interrupt Request Routing Mode [9:8]

This field routes PCI interrupts to the INTx/ or ALT_INTx/ pins according to the bit encodings in [Table 4.9](#). If the host system enables MSI, the LSI53C1030 does not signal PCI interrupts on the INTx/ or ALT_INTx/ pins.

Table 4.9 Interrupt Signal Routing

Bits [9:8] Encodings	Interrupt Signal Routing
0b00	INTx/ and ALT_INTx/
0b01	INTx/ only
0b10	ALT_INTx/ only
0b11	INTx/ only

Reserved **[7:4]**

This field is reserved.

Reply Interrupt Mask 3

Setting this bit masks reply interrupts and prevents the assertion of a PCI interrupt for all reply interrupt conditions.

Reserved **[2:1]**

This field is reserved.

Doorbell Interrupt Mask

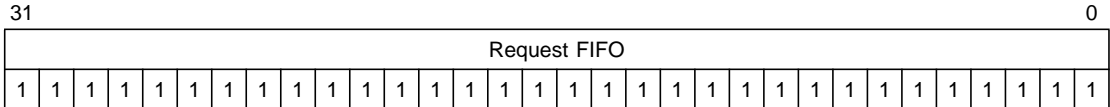
0

Setting this bit masks System Doorbell interrupts and prevents the assertion of a PCI interrupt for all System Doorbell interrupt conditions.

Register: 0x40

Request FIFO

Read/Write



The Request FIFO provides Request Free Message Frame Addresses (MFAs) to the host system on reads and accepts Request Post MFAs from the host system on writes. There is one Request FIFO register that is visible to both PCI functions. The two PCI functions physically share this register.

Request FIFO

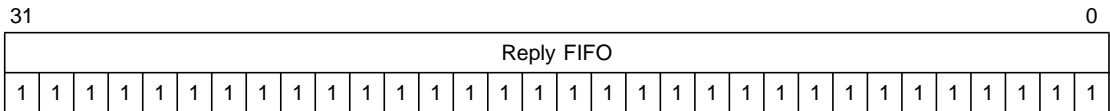
[31:0]

For reads, the Request Free MFA is empty and this register contains 0xFFFFFFFF. For writes, the register contains the Request Post MFA.

Register: 0x44

Reply FIFO

Read/Write



The Reply FIFO provides Reply Post MFAs to the host system on reads and accepts Reply Free MFAs from the host system on writes. There is a unique Reply FIFO register for each PCI function.

Reply FIFO

[31:0]

For reads, the Request Free MFA is empty and this register contains 0xFFFFFFFF. For writes, the register contains the Reply Free MFA.

Chapter 5

Specifications

This chapter specifies the LSI53C1030 electrical and mechanical characteristics. It is divided into the following sections:

- [Section 5.1, “DC Characteristics”](#)
- [Section 5.2, “TolerANT Technology Electrical Characteristics”](#)
- [Section 5.3, “AC Characteristics”](#)
- [Section 5.4, “External Memory Timing Diagrams”](#)
- [Section 5.5, “Package Drawings”](#)

Please refer to the *PCI Local Bus Specification*, the *PCI-X Addendum to the PCI Local Bus Specification*, and the *SCSI Parallel Interface-4 Draft Specification* for PCI, PCI-X, and SCSI timings and timing diagrams. The LSI53C1030 timings conform to the timings these specifications provide.

5.1 DC Characteristics

This section of the manual describes the LSI53C1030 DC characteristics. Tables [5.1](#) through [5.11](#) give current and voltage specifications. Figures [5.1](#) and [5.2](#) are LVD transceiver schematics.

Table 5.1 Absolute Maximum Stress Ratings¹

Symbol	Parameter	Min	Max	Unit	Test Conditions
T _{STG}	Storage temperature	−40	125	°C	—
V _{DD-Core}	Supply voltage	−0.3	2.2	V	—
V _{DD-IO}	I/O Supply voltage	−0.3	3.9	V	—
V _{IN}	Input voltage	−0.5	V _{DD} + 0.5	V	—
I _{LP} ²	Latch-up current	±150	—	mA	−2 V < V _{PIN} < 8 V
T ²	Lead temperature	—	125	°C	—
ESD ²	Electrostatic discharge	—	2000	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed above can damage the device. These are stress ratings only; functional operation of the device at or beyond these values is not implied.
2. SCSI pins only.

Table 5.2 Operating Conditions¹

Symbol	Parameter	Min	Nominal	Max	Unit	Test Conditions
V _{DD-Core}	Core and analog supply voltage	1.71	1.80	1.89	V	—
V _{DD-IO}	I/O supply voltage	2.97	3.30	3.63	V	—
I _{DD-Core}	Core and analog supply current (dynamic) ²	—	1.50	1.80	A	—
I _{DD-I/O}	I/O supply current (dynamic)	—	0.50	1.00	A	—
T _j	Junction temperature	—	—	115	°C	—
T _A	Operating free air	0	—	70.0	°C	—
θ _{JA}	Thermal resistance (junction to ambient air)	—	—	15.0	°C/W	0 Linear Feet/Minute

1. Conditions that exceed the operating limits can cause the device to function incorrectly.
2. Core and analog supply only.

The core voltage must come up before I/O voltage. The following equation must hold at all times: $V_{DD_I/O} \leq (V_{DD_CORE} + 2 \text{ V})$.

Table 5.3 LVD Driver SCSI Signals¹— SACK \pm , SATN \pm , SBSY \pm , SCD \pm , SD[15:0] \pm , SDP[1:0] \pm , SIO \pm , SMSG \pm , SREQ \pm , SRST \pm , SSEL \pm

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{O+}	Source (+) current	-6.5	-13.5	mA	Asserted state
I_{O-}	Sink (-) current	6.5	13.5	mA	Asserted state
I_{O+}	Source (+) current	2.5	9.5	mA	Negated state
I_{O-}	Sink (-) current	-2.5	-9.5	mA	Negated state
I_{OZ}	3-state leakage	-	20	μA	-

1. $V_{CM} = 0.7\text{--}1.8 \text{ V}$ (Common Mode, nominal $\sim 1.2 \text{ V}$), $R_{bias} = 10.0 \text{ k}\Omega$.

Figure 5.1 LVD Driver

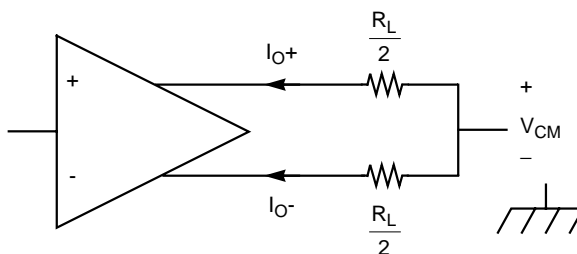


Table 5.4 LVD Receiver SCSI Signals¹— SACK \pm , SATN \pm , SBSY \pm , SCD \pm , SD[15:0] \pm , SDP[1:0] \pm , SIO \pm , SMSG \pm , SREQ \pm , SRST \pm , SSEL \pm

Symbol	Parameter	Min	Max	Units	Test Conditions
V_I	LVD receiver voltage asserting	30	-	mV	Differential voltage
V_I	LVD receiver voltage negating		30	mV	Differential voltage

1. $V_{CM} = 0.7\text{--}1.8 \text{ V}$ (Common Mode Voltage, nominal $\sim 1.2 \text{ V}$.)

Figure 5.2 LVD Receiver

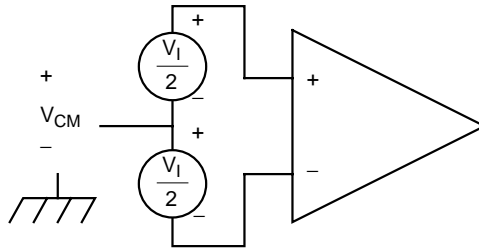


Table 5.5 A_DIFFSENS and B_DIFFSENS SCSI Signals

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	HVD sense voltage	2.4	3.6	V	Note 1
V_S	LVD sense voltage	0.7	1.9	V	Note 1
V_{IL}	SE sense voltage	$V_{SS} - 0.35$	0.5	V	Note 1
I_{OZ}	3-state leakage	-10	10	μA	$V_{PIN} = 0\text{ V}, 3.6\text{ V}$

1. V_{IH} , V_{IL} , and V_S are specified in the SPI-4 draft specification.

Table 5.6 Input Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	—	7	pF	Guaranteed by design
C_{IO}	Input capacitance of I/O pads	—	15	pF	Guaranteed by design
C_{PCI}	Input capacitance of PCI pads	—	8	pF	Guaranteed by design
C_{LVD}	Input capacitance of LVD pads	—	8	pF	6.5 pF pad 1.5 pF package

Table 5.7 8 mA Bidirectional Signals — GPIO[7:0], MAD[15:0], MADP[1:0], SerialDATA

Symbol	Parameter	Min	Max	Unit	Test Conditions
V _{IH}	Input high voltage	2.0	3.6	V	—
V _{IL}	Input low voltage	−0.3	0.8	V	—
V _{OH}	Output high voltage	2.4	VDD	V	−8 mA
V _{OL}	Output low voltage	V _{SS}	0.4	V	8 mA
I _{OZ}	3-state leakage	−10	10	μA	V _{PIN} = 0 V, 5.25 V
I _{PULL}	Pull up current	25	—	μA	—

Table 5.8 8 mA PCI Bidirectional Signals — ACK64/, AD[63:0], C_BE[7:0]/, DEVSEL/, FRAME/, IRDY/, PAR, PAR64, PERR/, REQ64/, SERR/, STOP/, TRDY/

Symbol	Parameters	Min	Max	Unit	Test Conditions
V _{IH}	Input high voltage	0.5 VDD	PCI5VBIAS ¹	V	—
V _{IL}	Input low voltage	−0.5	0.3 VDD	V	—
V _{OH}	Output high voltage	0.9 VDD	VDD	V	−500 μA
V _{OL}	Output low voltage	VSS	0.1 VDD	V	1500 μA
I _{OZ}	3-state leakage	−10	10	μA	V _{PIN} = 0 V, 5.25 V
I _{PULL-DOWN}	Pull-down current ²	25	—	μA	—

1. The maximum PCI input voltage depends upon the operating mode of the PCI bus, which PCI5VBIAS determines. The maximum input voltage in a 5 V PCI system is 5 V. The maximum input voltage in a 3.3 V PCI system is VDD. Refer to the signal description in [Section 3.9, “Power and Ground Pins,”](#) for more information concerning PCI5VBIAS.
2. Pull-down text does not apply to AD[31:0] and C_BE[3:0]/.

Table 5.9 Input Signals¹ — CLK, CLKMODE_0, CLKMODE_1, DIS_PCI_FSN/, DIS_SCSI_FSN/, GNT/, IDDTN, IDSEL, IOPD_GNT/, PVT1, PVT2, SCANEN, SCANMODE, SCLK, TCK_CHIP, TCK_ICE, TESTACLK, TESTCLKEN, TESTHCLK, TDI_CHIP, TDI_ICE, TMS_CHIP, TMS_ICE, TN, TRST_ICE/, TST_RST/, ZCR_EN/

Symbol	Parameters	Min	Max	Unit	Test Conditions
V _{IH}	Input high voltage	2.0	VDD + 0.5	V	—
V _{IL}	Input low voltage	−0.3	0.8	V	—
I _{IN}	3-state leakage	−10	10	μA	V _{PIN} = 0 V, VDD + 0.5 V
I _{PULL-UP}	Pull current	25	—	μA	—

1. Do not place pulls on CLK, GNT/, IDSEL, RST/, and SCLK. The pull information given does not apply to these signals.

Table 5.10 8 mA Output Signals¹ — ADSC/, ADV/, ALT_INTA/, ALT_INTB/, BWE[1:0]/, FL SHALE[1:0]/, FL SHCE/, INTA/, INTB/, MCLK, MOE/, PIPESTAT[2:0], RAMCE/, REQ/, RTCK_ICE, SerialCLK, SERR/, TDO_CHIP, TDO_ICE, TRACECLK, TRACEPKT[7:0], TRACESYNC

Symbol	Parameters	Min	Max	Unit	Test Conditions
V _{OH}	Output high voltage	2.4	VDD	V	−8 mA
V _{OL}	Output low voltage	VSS	0.4 VDD	V	8 mA
I _{OZ}	3-state leakage	−10	10	μA	V _{PIN} = 0 V, 3.6 V
I _{PULL-UP}	Pull current	25	—	μA	—

1. Do not place pulls on REQ/ and SERR/. The pull information given does not apply to these signals.

Table 5.11 12 mA Output Signals — A_LED/, B_LED/, HB_LED/

Symbol	Parameters	Min	Max	Unit	Test Conditions
V _{OH}	Output high voltage	2.4	VDD	V	−12 mA
V _{OL}	Output low voltage	VSS	0.4 VDD	V	12 mA
I _{OZ}	3-state leakage	−10	10	μA	V _{PIN} = 0 V, 3.6 V
I _{PULL-UP}	Pull current	25	—	μA	—

5.2 TolerANT Technology Electrical Characteristics

The LSI53C1030 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators.

Table 5.12 provides electrical characteristics for SE SCSI signals. Figure 5.3 and Figure 5.4 provide the reference information for testing SCSI signals.

Table 5.12 TolerANT Technology Electrical Characteristics for SE SCSI Signals¹

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}^2	Output high voltage	2.5	3.7	V	$I_{OH} = 0$ mA
V_{OL}	Output low voltage	0.0	0.5	V	$I_{OL} = 48$ mA
V_{IH}	Input high voltage	1.9	5.50	V	Signal FALSE State
V_{IL}	Input low voltage	-0.5	1.0	V	Referenced to V_{SS} Signal TRUE State
V_{IK}	Input clamp voltage	—	-0.75	V	$V_{pp} = \text{Min};$ $I_1 = -20$ mA
V_{TH}	Threshold, HIGH to LOW	1.00	—	V	—
V_{TL}	Threshold, LOW to HIGH	—	1.90	V	—
$V_{TH}-V_{TL}$	Hysteresis	375	—	mV	—
$I_{ih.hp}$	Hot Plug High Level Current Peak	—	1.5	mA	Transient duration of 10% of peak equals 20 μ s. This applies during physical insertion only.
I_{OH2}	Output high current	0	7	mA	$V_{OH} = 2.2$ V
I_{OL}	Output low current	48	—	mA	$V_{OL} = 0.5$ V
I_{OSH2}	Short-circuit output high current	48	—	mA	Short to V_{DD}^3
I_{OSL}	Short-circuit output low current	22	—	mA	Short to V_{SS}

Table 5.12 TolerANT Technology Electrical Characteristics for SE SCSI Signals¹ (Cont.)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{LH}	Input high leakage	–	20	μA	$-0.5 < V_{DD} < 5.25$ $V_{PIN} = 2.7 V$
I_{LL}	Input low leakage	–	20	μA	$-0.5 < V_{DD} < 5.25$ $V_{PIN} = 0.5 V$
R_I	Input resistance	20	–	$M\Omega$	Receivers disabled
C_P	Capacitance per pin	–	8	pF	PQFP
dV_H/dt	Slew rate LOW to HIGH	110	540	mV/ns	Figure 5.3
dV_L/dt	Slew rate HIGH to LOW	110	540	mV/ns	Figure 5.3
ESD_{HBM}	Electrostatic discharge (HBM)	2	–	kV	MIL-STD-883C; Method 3015-7; 100 pF at 1.5 k Ω
ESD_{CDM}	Electrostatic discharge (CDM)	0.5	–	kV	ESD DS5.3.1-1996
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	Figure 5.4
	Ultra filter delay	10	15	ns	Figure 5.4
	Ultra2 filter delay	5	8	ns	Figure 5.4
	Extended filter delay	40	60	ns	Figure 5.4

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, and SACK/. SCSI SE mode only (minus pins).
3. Single pin only; irreversible damage can occur if sustained for longer than one second.

Figure 5.3 Rise and Fall Time Test Condition

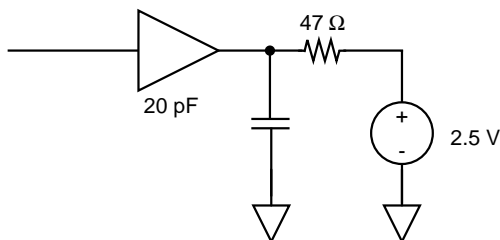


Figure 5.4 SCSI Input Filtering



Note: t_1 is the input filtering period.

5.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to [Section 5.1, “DC Characteristics”](#)). Chip timing is based on simulation at worst case voltage, temperature, and processing. Timing was developed with a load capacitance of 50 pF. [Table 5.13](#) and [Figure 5.5](#) provide external clock timing data.

Table 5.13 External Clock

Symbol	Parameter	133 MHz PCI-X		66 MHz PCI-X		66 MHz PCI		33 MHz PCI		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_1	PCI Bus clock period ¹	7.5	20	15	20	15	30	30	250	ns
	SCSI clock period	12.5	12.5	12.5	12.5	12.5	12.5	12.5	12.5	ns
t_2	PCI CLK LOW time ²	3	—	6	—	6	—	11	—	ns
	SCLK LOW time	5	7.5	5	7.5	5	7.5	5	7.5	ns
t_3	PCI CLK HIGH time	3	—	6	—	6	—	11	—	ns
	SCLK HIGH time	5	7.5	5	7.5	5	7.5	5	7.5	ns
t_4	PCI CLK slew rate	1.5	4	1.5	4	1.5	4	1	4	V/ns

1. For frequencies above 33 MHz, the clock frequency can not be changed beyond the spread spectrum limits except while RST/ is asserted.
2. Duty cycle not to exceed 60/40.

Figure 5.5 External Clock

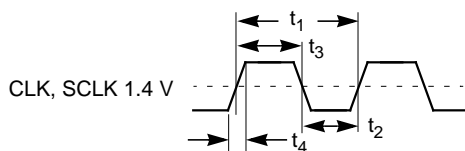


Table 5.14 and Figure 5.6 provide reset input timing data.

Table 5.14 Reset Input

Symbol	Parameter	Min	Max	Units
t_1	Reset pulse width	10	—	ns
t_2	Reset deasserted setup to CLK HIGH	0	—	ns
t_3	MAD setup time to CLK HIGH (for configuring the MAD bus only)	20	—	ns
t_4	MAD hold time from CLK HIGH (for configuring the MAD bus only)	20	—	ns

Figure 5.6 Reset Input

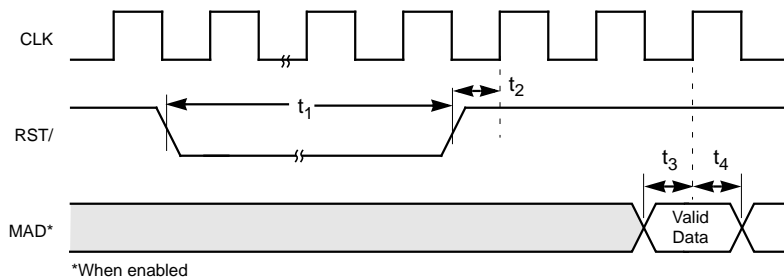
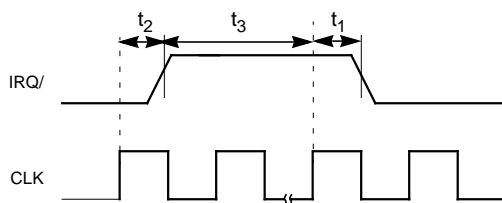


Table 5.15 and Figure 5.7 provide Interrupt Output timing data.

Table 5.15 Interrupt Output

Symbol	Parameter	Min	Max	Units
t_1	CLK HIGH to IRQ/ LOW	2	11	ns
t_2	CLK HIGH to IRQ/ HIGH	2	11	ns
t_3	IRQ/ deassertion time	3	—	CLK

Figure 5.7 Interrupt Output



5.4 External Memory Timing Diagrams

This section provides timing diagrams and data for NVSRAM and Flash ROM timings.

5.4.1 NVSRAM Timing

[Table 5.16](#) and [Figure 5.8](#) provide the timing information for the Memory Address and Data (MAD) bus NVSRAM read accesses.

Table 5.16 NVSRAM Read Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_1	Address setup to FL SHALE/ HIGH	25	—	ns
t_2	Address hold from FL SHALE/ HIGH	25	—	ns
t_3	FL SHALE/ pulse width	25	—	ns
t_4	Address valid to data clocked in	135	—	ns
t_5	RAMCE/ LOW to data clocked in	85	—	ns
t_6	MOE/ LOW to data clocked in	75	—	ns
t_7	Data setup to MOE/ HIGH	10	—	ns
t_8	Data setup to RAMCE/ HIGH	10	—	ns
t_9	Data hold from RAMCE/ HIGH	0	—	ns

Figure 5.8 NVSRAM Read Cycle

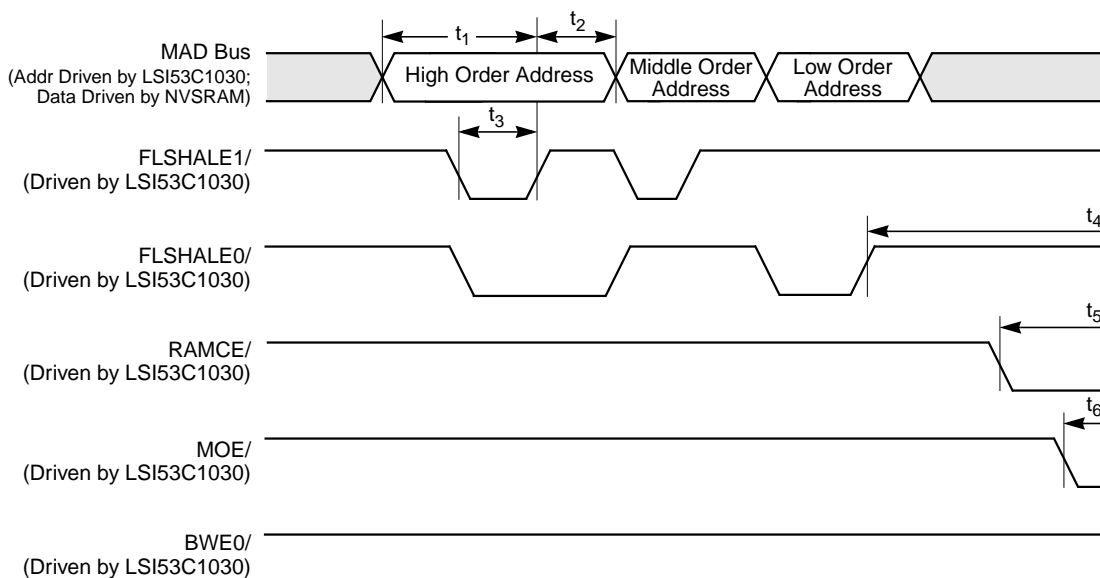


Figure 5.8 NVSRAM Read Cycle (Cont.)

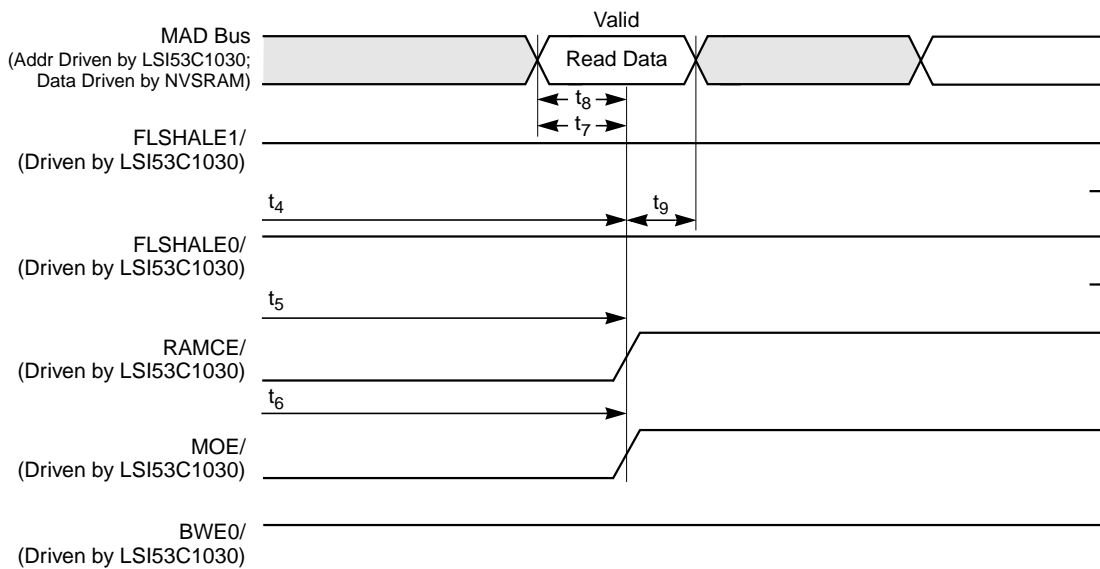


Table 5.17 and Figure 5.9 provide the timing information for NVSRAM write accesses.

Table 5.17 NVSRAM Write Cycle

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to FLSHALE/ HIGH	25	—	ns
t_{12}	Address hold from FLSHALE/ HIGH	25	—	ns
t_{13}	FLSHALE/ pulse width	25	—	ns
t_{20}	Data setup to BWE0/ LOW	40	—	ns
t_{21}	Data hold from BWE0/ HIGH	30	—	ns
t_{22}	BWE0/ pulse width	20	—	ns
t_{23}	Address setup to BWE0/ LOW	75	—	ns
t_{24}	RAMCE/ LOW to BWE0/ HIGH	60	—	ns
t_{25}	RAMCE/ LOW to BWE0/ LOW	25	—	ns
t_{26}	BWE0/ HIGH to RAMCE/ HIGH	25	—	ns
t_{27}	RAMCE/ pulse width	100	—	ns

Figure 5.9 NVSRAM Write Cycle

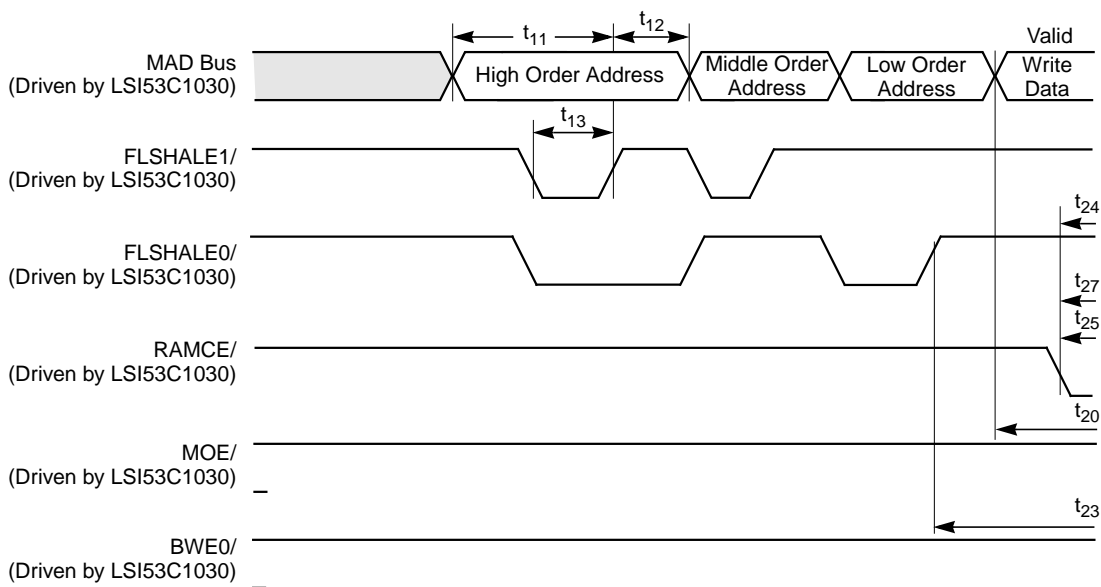
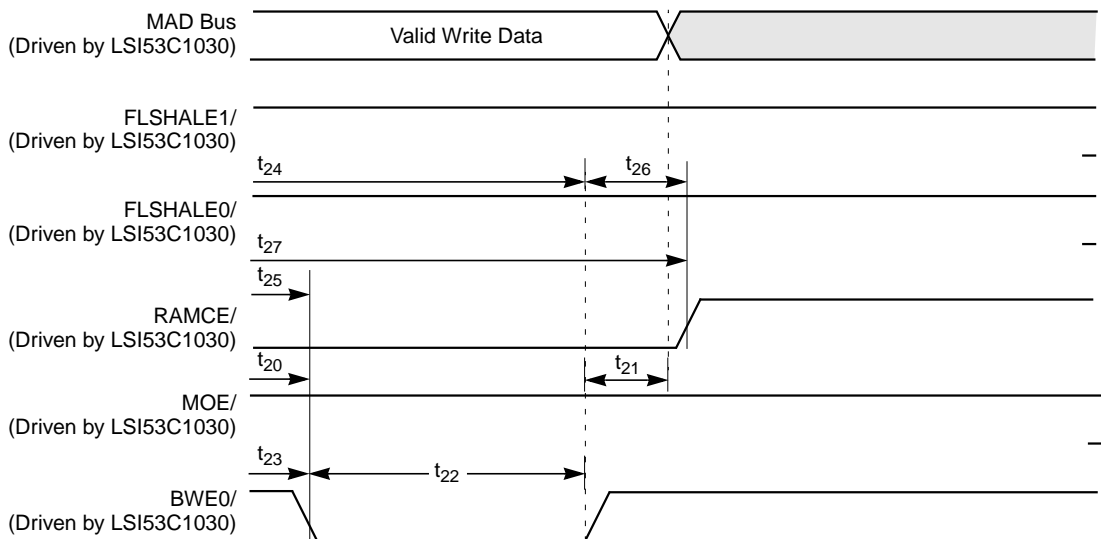


Figure 5.9 NVSRAM Write Cycle (Cont.)



5.4.2 Flash ROM Timing

Table 5.18 and Figure 5.10 provide the timing information for Flash ROM read accesses.

Table 5.18 Flash ROM Read Cycle Timing

Symbol	Parameter	Min	Max	Unit
t_1	Address setup to FLSHALE/ HIGH	25	—	ns
t_2	Address hold from FLSHALE/ HIGH	25	—	ns
t_3	FLSHALE/ pulse width	25	—	ns
t_4	Address valid to data clocked in	135	—	ns
t_5	FLSHCE/ LOW to data clocked in	85	—	ns
t_6	MOE/ LOW to data clocked in	75	—	ns
t_7	Data setup to MOE/ HIGH	10	—	ns
t_8	Data setup to FLSHCE/ HIGH	10	—	ns
t_9	Data hold from FLSHCE/ HIGH	0	—	ns

Figure 5.10 Flash ROM Read Cycle

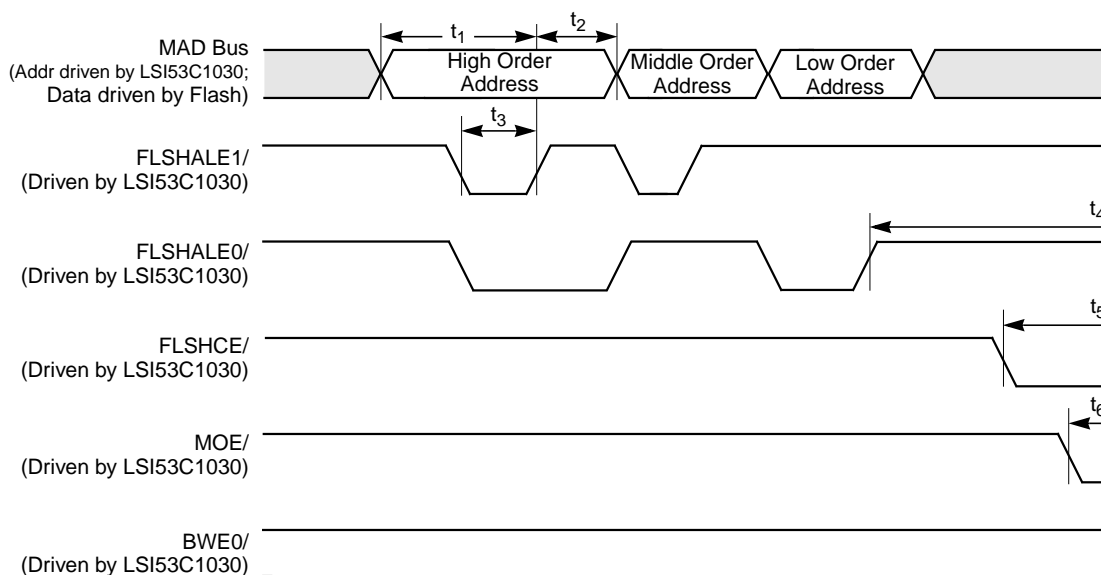


Figure 5.10 Flash ROM Read Cycle (Cont.)

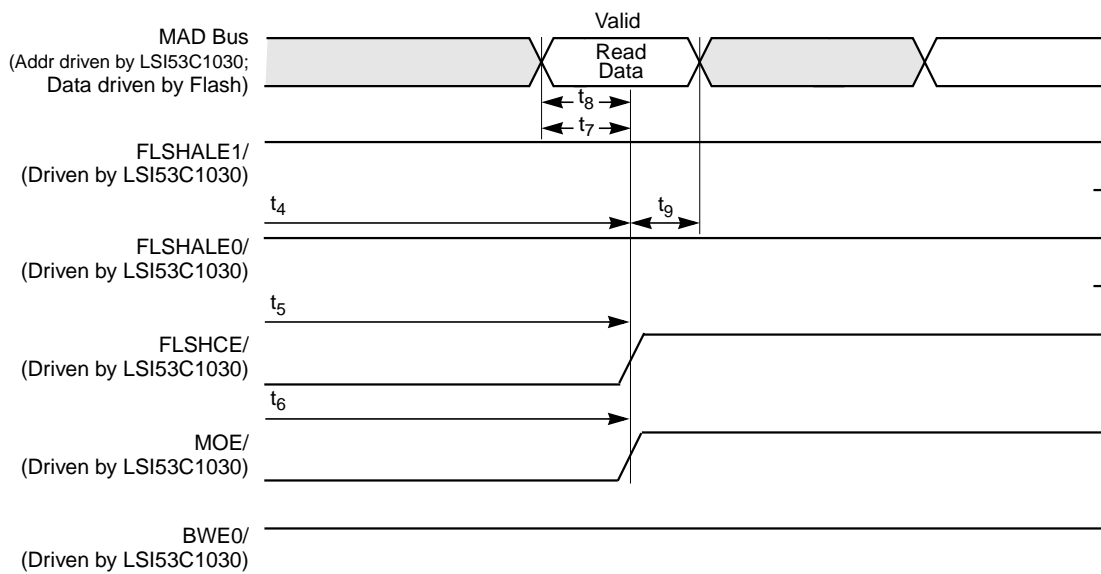


Table 5.19 and Figure 5.11 provide the timing information for Flash ROM write accesses.

Table 5.19 Flash ROM Write Cycle

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to FL SHALE/ HIGH	25	—	ns
t_{12}	Address hold from FL SHALE/ HIGH	25	—	ns
t_{13}	FL SHALE/ pulse width	25	—	ns
t_{20}	Data setup to BWE0/ LOW	40	—	ns
t_{21}	Data hold from BWE0/ HIGH	30	—	ns
t_{22}	BWE0/ pulse width	20	—	ns
t_{23}	Address setup to BWE0/ LOW	75	—	ns
t_{24}	FL SHCE/ LOW to BWE0/ HIGH	60	—	ns
t_{25}	FL SHCE/ LOW to BWE0/ LOW	25	—	ns
t_{26}	BWE0/ HIGH to RAMCE/ HIGH	25	—	ns
t_{27}	FL SHCE/ pulse width	100	—	ns

Figure 5.11 Flash ROM Write Cycle

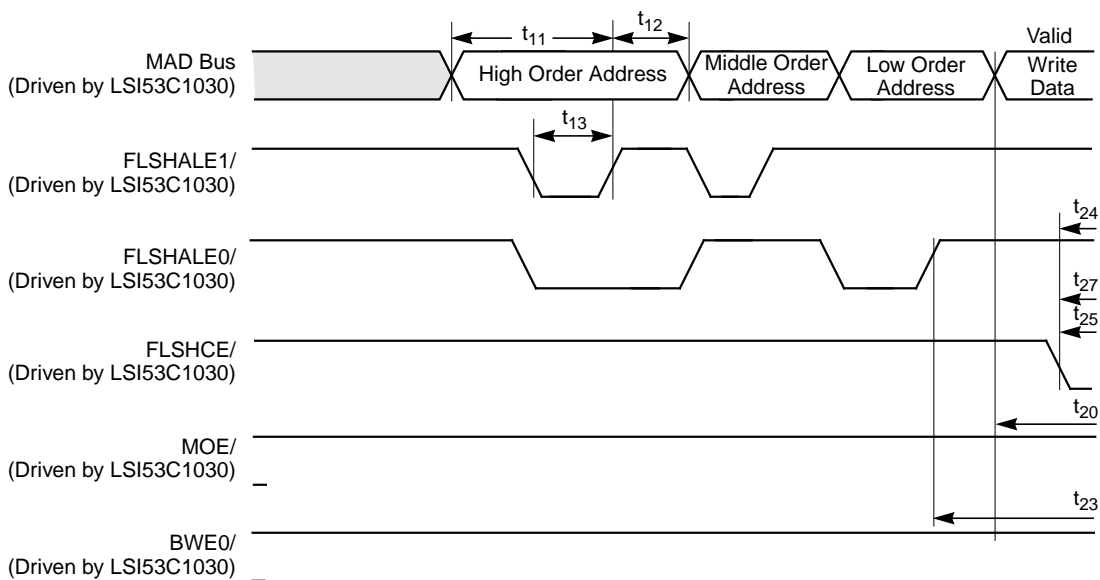
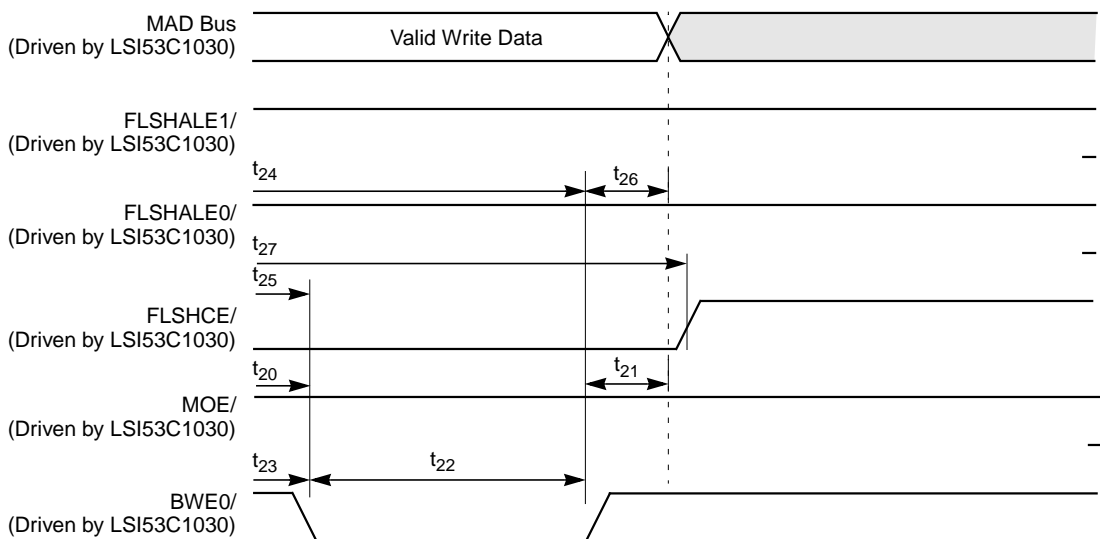


Figure 5.11 Flash ROM Write Cycle (Cont.)



5.5 Package Drawings

Figure 5.12 illustrates the signal locations on the Ball Grid Array (BGA).

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Figure 5.12 LSI53C1030 456-Pin BGA Top View

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13
VDD_IO	VDD_IO	B_SD12-	B_SD12+	VSS_IO	VDD_IO	B_SDP1-	B_SD0+	VSS_IO	VDD_IO	B_RBIA	B_SD6-	VSS_IO
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13
VSS_IO	TRACE PKT1	TRACECLK	VSSC	B_SD13+	B_SD14+	B_SD15+	B_SD0-	B_SD1+	B_SD4-	B_SD5-	B_SD6+	B_VDDBIAS
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13
VDDA	TRACE PKT4	PIPESTAT2	VSS_IO	TN	B_SD13-	VDD_IO	VSS_IO	B_SD2-	B_SD4+	VDD_IO	VSS_IO	B_SDP0+
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
A_SD11+	VDDC	VDD_IO	TRACE PKT0	PIPESTAT0	VDDC	TESTCLKEN	B_SD15-	B_SD1-	B_SD3-	B_SD5+	B_SDP0-	B_SATN+
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13
VSS_IO	A_ DIFFSENS	TRACE PKT5	TRACE PKT3	TRACSYNC	PIPESTAT1	SCANMODE	B_SD14-	B_SDP1+	B_SD2+	B_SD3+	B_SD7+	B_SD7-
F1	F2	F3	F4	F5								
VDD_IO	A_SD11-	SCLK	TRACE PKT7	TRACE PKT2								
G1	G2	G3	G4	G5								
A_SD10+	A_SD10-	VSS_IO	VSSC	TRACE PKT6								
H1	H2	H3	H4	H5								
A_SD8-	A_SD8+	VDD_IO	A_SD9+	VSSA								
J1	J2	J3	J4	J5								
VSS_IO	A_SREQ-	A_SREQ+	A_SD9-	A_SIO+								
K1	K2	K3	K4	K5								
VDD_IO	A_SSEL+	A_SCD-	A_SCD+	A_SIO-								
L1	L2	L3	L4	L5								
A_SMSG+	A_SMSG-	VSS_IO	A_SSEL-	A_SACK+								
M1	M2	M3	M4	M5								
A_SRST-	A_SRST+	VDD_IO	A_SATN-	A_SACK-								
N1	N2	N3	N4	N5								
VSS_IO	VDDC	A_SBSY-	A_SBSY+	A_SATN+								
P1	P2	P3	P4	P5								
VDD_IO	VSSC	A_SD7+	A_SDP0-	A_SDP0+								
R1	R2	R3	R4	R5								
A_RBIA	A_SD5+	VSS_IO	A_SD7-	A_SD6+								
T1	T2	T3	T4	T5								
A_VDDBIAS	A_SD5-	VDD_IO	A_SD4+	A_SD6-								
U1	U2	U3	U4	U5								
VSS_IO	A_SD4-	A_SD2+	A_SD3+	A_SD3-								
V1	V2	V3	V4	V5								
VDD_IO	A_SD2-	A_SD0+	A_SD1-	A_SD1+								
W1	W2	W3	W4	W5								
A_SDP1+	A_SDP1-	VSS_IO	A_SD0-	ASD15+								
Y1	Y2	Y3	Y4	Y5								
A_SD15-	A_SD14+	VDD_IO	IDDTN	TMS_ICE								
AA1	AA2	AA3	AA4	AA5								
VSS_IO	A_SD14-	A_SD13+	TCK_ICE	RTCK_ICE								
AB1	AB2	AB3	AB4	AB5	AB6	AB7	AB8	AB9	AB10	AB11	AB12	AB13
VDD_IO	A_SD13-	TDI_ICE	TRST_ICE/	VSSC	TESTACLK	VSSC	VSSC	ALT_INTB/	RST/	AD28	AD24	C_BE3/
AC1	AC2	AC3	AC4	AC5	AC6	AC7	AC8	AC9	AC10	AC11	AC12	AC13
A_SD12+	CLK MODE_1	VSS_IO	DIS_SCSL_	IOPD_GNT/	TCK_CHIP	VDDC	INTA/	NC	PCI5VBIAS	AD27	AD23	IDSEL
AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13
A_SD12-	TDO_ICE	VDDC	VDD_IO	TST_RST/	TDO_CHIP	VSS_IO	VDD_IO	PCI5VBIAS	REQ/	VSS_IO	VDD_IO	AD22
AE1	AE2	AE3	AE4	AE5	AE6	AE7	AE8	AE9	AE10	AE11	AE12	AE13
VSS_IO	TESTHCLK	VDDC	TMS_CHIP	PVT1	PCI5VBIAS	INTB/	GNT/	AD31	AD29	AD26	AD25	AD21
AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13
VDD_IO	VSS_IO	TDI_CHIP	PVT2	VDD_IO	VSS_IO	ALT_INTA/	AD30	VDD_IO	VSS_IO	AD20	PCI5VBIAS	VDD_IO

L11	L12	L13
VSS_IO	VSS_IO	VSS_IO
M11	M12	M13
VSS_IO	VSS_IO	VSS_IO
N11	N12	N13
VSS_IO	VSS_IO	VSS_IO
P11	P12	P13
VSS_IO	VSS_IO	VSS_IO
R11	R12	R13
VSS_IO	VSS_IO	VSS_IO
T11	T12	T13
VSS_IO	VSS_IO	VSS_IO

Figure 5.12 LSI53C1030 456-Pin BGA Top View (Cont.)

A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26
VDD_IO	B_SBSY-	B_SRST+	VSS_IO	VDD_IO	B_SD8-	B_SD9+	VSS_IO	VDD_IO	B_SD11+	DIS_PCL_FSN/	VSS_IO	VDD_IO
B14	B15	B16	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26
B_SATN-	B_SBSY+	B_SMSG-	B_SSEL-	B_SREQ-	B_SD8+	B_SD10+	B_SD11-	B_DIFFSENS	ADV/	MADP0	MAD13	VSS_IO
C14	C15	C16	C17	C18	C19	C20	C21	C22	C23	C24	C25	C26
VSSC	VDD_IO	VSS_IO	B_SSEL+	B_SREQ+	VDD_IO	VSS_IO	VSSC	MADP1	VDD_IO	MAD10	HB_LED/	VSSC
D14	D15	D16	D17	D18	D19	D20	D21	D22	D23	D24	D25	D26
B_SACK-	VDDC	B_SMSG+	B_SCD+	B_SIO+	B_SD10-	RAMCE/	ADSC/	MAD15	MAD12	VSS_IO	MAD2	MAD7
E14	E15	E16	E17	E18	E19	E20	E21	E22	E23	E24	E25	E26
B_SACK+	B_SRST-	B_SCD-	B_SIO-	B_SD9-	VDDC	MCLK	MAD14	MAD11	MAD8	BWE1/	MAD6	VDD_IO
								F22	F23	F24	F25	F26
								MAD9	MAD1	MAD4	VSSC	VSS_IO
								G22	G23	G24	G25	G26
								MAD0	MAD3	VDD_IO	FLSHCE/	MOE/
								H22	H23	H24	H25	H26
								MAD5	BWE0/	VSS_IO	GPIO3	SerialDATA
								J22	J23	J24	J25	J26
								VDDC	A_LED/	FLSHALE1/	SerialCLK	VDD_IO
								K22	K23	K24	K25	K26
								FLSHALE0/	B_LED/	GPIO2	GPIO7	VSS_IO
								L22	L23	L24	L25	L26
								VSSC	GPIO6	VDD_IO	GPIO5	AD34
								M22	M23	M24	M25	M26
								VDDC	PCI5VBIAS	VSS_IO	GPIO4	AD35
								N22	N23	N24	N25	N26
								SCANEN	ZCR_EN/	AD32	AD33	VDD_IO
P22	P23	P24	P25	P26								
AD42	AD41	AD39	AD38	VSS_IO								
R22	R23	R24	R25	R26								
AD43	AD40	VDD_IO	AD44	AD36								
T22	T23	T24	T25	T26								
AD47	AD46	VSS_IO	AD45	AD37								
U22	U23	U24	U25	U26								
AD55	AD49	AD52	AD48	VDD_IO								
V22	V23	V24	V25	V26								
AD56	AD53	AD54	AD51	VSS_IO								
W22	W23	W24	W25	W26								
AD63	AD59	VDD_IO	PCI5VBIAS	AD50								
Y22	Y23	Y24	Y25	Y26								
PCI5VBIAS	C_BE5/	VSS_IO	AD58	AD57								
AA22	AA23	AA24	AA25	AA26								
CLK MODE_0	C_BE7/	PAR64	AD60	VDD_IO								

AB14	AB15	AB16	AB17	AB18	AB19	AB20	AB21	AB22	AB23	AB24	AB25	AB26
C_BE2/	FRAME/	STOP/	AD12	AD11	AD5	ACK64/	VDDA	PCI5VBIAS	VSSC	VSSC	AD62	VSS_IO
AC14	AC15	AC16	AC17	AC18	AC19	AC20	AC21	AC22	AC23	AC24	AC25	AC26
AD16	AD17	DEVSEL/	SERR/	AD13	AD8	AD2	AD0	CLK	GPI00	VDD_IO	C_BE6/	AD61
AD14	AD15	AD16	AD17	AD18	AD19	AD20	AD21	AD22	AD23	AD24	AD25	AD26
VSSC	VSS_IO	VDD_IO	AD15	PCI5VBIAS	VSS_IO	VDD_IO	AD4	REQ64/	VSS_IO	VSSA	VDDC	C_BE4/
AE14	AE15	AE16	AE17	AE18	AE19	AE20	AE21	AE22	AE23	AE24	AE25	AE26
AD18	IRDY/	TRDY/	PERR/	C_BE1/	AD14	AD9	C_BE0/	AD6	AD1	VDDC	GPIO1	VDD_IO
AF14	AF15	AF16	AF17	AF18	AF19	AF20	AF21	AF22	AF23	AF24	AF25	AF26
VSS_IO	VDDC	AD19	VDD_IO	VSS_IO	PAR	AD10	VDD_IO	VSS_IO	AD7	AD3	VDD_IO	VSS_IO

Table 5.20 contains the pinout for the LSI53C1030.

Table 5.20 LSI53C1030 Signal List by Signal Name

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
ACK64/	AB20	AD45	T25	A_SD6-	T5	B_SD0-	B8	B_VDDBIAS	B13
AD0	AC21	AD46	T23	A_SD6+	R5	B_SD0+	A8	BWE0/	H23
AD1	AE23	AD47	T22	A_SD7-	R4	B_SD1-	D9	BWE1/	E24
AD2	AC20	AD48	U25	A_SD7+	P3	B_SD1+	B9	C_BE0/	AE21
AD3	AF24	AD49	U23	A_SD8-	H1	B_SD2-	C9	C_BE1/	AE18
AD4	AD21	AD50	W26	A_SD8+	H2	B_SD2+	E10	C_BE2/	AB14
AD5	AB19	AD51	V25	A_SD9-	J4	B_SD3-	D10	C_BE3/	AB13
AD6	AE22	AD52	U24	A_SD9+	H4	B_SD3+	E11	C_BE4/	AD26
AD7	AF23	AD53	V23	A_SD10-	G2	B_SD4-	B10	C_BE5/	Y23
AD8	AC19	AD54	V24	A_SD10+	G1	B_SD4+	C10	C_BE6/	AC25
AD9	AE20	AD55	U22	A_SD11-	F2	B_SD5-	B11	C_BE7/	AA23
AD10	AF20	AD56	V22	A_SD11+	D1	B_SD5+	D11	CLK	AC22
AD11	AB18	AD57	Y26	A_SD12-	AD1	B_SD6-	A12	CLK	
AD12	AB17	AD58	Y25	A_SD12+	AC1	B_SD6+	B12	MODE_0	AA22
AD13	AC18	AD59	W23	A_SD13-	AB2	B_SD7-	E13	CLK	
AD14	AE19	AD60	AA25	A_SD13+	AA3	B_SD7+	E12	MODE_1	AC2
AD15	AD17	AD61	AC26	A_SD14-	AA2	B_SD8-	A19	DIS	
AD16	AC14	AD62	AB25	A_SD14+	Y2	B_SD8+	B19	PCI_FSN/	A24
AD17	AC15	AD63	W22	A_SD15-	Y1	B_SD9-	E18	DIS	
AD18	AE14	A_DIFFSENS	E2	A_SD15+	W5	B_SD9+	A20	SCSI_FSN/	AC4
AD19	AF16	ADSC/	D21	A_SDP0-	P4	B_SD10-	D19	DEVSEL/	AC16
AD20	AF11	ADV/	B23	A_SDP0+	P5	B_SD10+	B20	FLSHALE0/	K22
AD21	AE13	A_LED/	J23	A_SDP1-	W2	B_SD11-	B21	FLSHALE1/	J24
AD22	AD13	ALT_INTA/	AF7	A_SDP1+	W1	B_SD11+	A23	FLSHCE/	G25
AD23	AC12	ALT_INTB/	AB9	A_SIO-	K5	B_SD12-	A3	FRAME/	AB15
AD24	AB12	A_RBIA	R1	A_SIO+	J5	B_SD12+	A4	GNT/	AE8
AD25	AE12	A_SACK-	M5	A_SMSG-	L2	B_SD13-	C6	GPIO0	AC23
AD26	AE11	A_SACK+	L5	A_SMSG+	L1	B_SD13+	B5	GPIO1	AE25
AD27	AC11	A_SATN-	M4	A_SREQ-	J2	B_SD14-	E8	GPIO2	K24
AD28	AB11	A_SATN+	N5	A_SREQ+	J3	B_SD14+	B6	GPIO3	H25
AD29	AE10	A_SBSY-	N3	A_SRST-	M1	B_SD15-	D8	GPIO4	M25
AD30	AF8	A_SBSY+	N4	A_SRST+	M2	B_SD15+	B7	GPIO5	L25
AD31	AE9	A_SCD-	K3	A_SSEL-	L4	B_SDP0-	D12	GPIO6	L23
AD32	N24	A_SCD+	K4	A_SSEL+	K2	B_SDP0+	C13	GPIO7	K25
AD33	N25	A_SD0-	W4	A_VDDBIAS	T1	B_SDP1-	A7	HB_LED/	C25
AD34	L26	A_SD0+	V3	B_DIFFSENS	B22	B_SDP1+	E9	IDDTN	Y4
AD35	M26	A_SD1-	V4	B_LED/	K23	B_SIO-	E17	IDSEL	AC13
AD36	R26	A_SD1+	V5	B_RBIA	A11	B_SIO+	D18	INTA/	AC8
AD37	T26	A_SD2-	V2	B_SACK-	D14	B_SMSG-	B16	INTB/	AE7
AD38	P25	A_SD2+	U3	B_SACK+	E14	B_SMSG+	D16	IOPD_GNT/	AC5
AD39	P24	A_SD3-	U5	B_SATN-	B14	B_SREQ-	B18	IRDY/	AE15
AD40	R23	A_SD3+	U4	B_SATN+	D13	B_SREQ+	C18	MAD0	G22
AD41	P23	A_SD4-	U2	B_SBSY-	A15	B_SRST-	E15	MAD1	F23
AD42	P22	A_SD4+	T4	B_SBSY+	B15	B_SRST+	A16	MAD2	D25
AD43	R22	A_SD5-	T2	B_SCD-	E16	B_SSEL-	B17	MAD3	G23
AD44	R25	A_SD5+	R2	B_SCD+	D17	B_SSEL+	C17	MAD4	F24

Table 5.20 LSI53C1030 Signal List by Signal Name (Cont.)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
MAD5	H22	TCK_ICE	AA4	VDD_IO	N26	VSS_IO	B26	VSS_IO	R15
MAD6	E25	TDI_CHIP	AF3	VDD_IO	P1	VSS_IO	C4	VSS_IO	R16
MAD7	D26	TDI_ICE	AB3	VDD_IO	R24	VSS_IO	C8	VSS_IO	T11
MAD8	E23	TDO_CHIP	AD6	VDD_IO	T3	VSS_IO	C12	VSS_IO	T12
MAD9	F22	TDO_ICE	AD2	VDD_IO	U26	VSS_IO	C16	VSS_IO	T13
MAD10	C24	TESTCLKEN	D7	VDD_IO	V1	VSS_IO	C20	VSS_IO	T14
MAD11	E22	TESTACLK	AB6	VDD_IO	W24	VSS_IO	D24	VSS_IO	T15
MAD12	D23	TESTHCLK	AE2	VDD_IO	Y3	VSS_IO	E1	VSS_IO	T16
MAD13	B25	TMS_CHIP	AE4	VDD_IO	AA26	VSS_IO	F26	VSS_IO	T24
MAD14	E21	TMS_ICE	Y5	VDD_IO	AB1	VSS_IO	G3	VSS_IO	U1
MAD15	D22	TN	C5	VDD_IO	AC24	VSS_IO	H24	VSS_IO	V26
MADP0	B24	TRACECLK	B3	VDD_IO	AD4	VSS_IO	J1	VSS_IO	W3
MADP1	C22	TRACEPKT0	D4	VDD_IO	AD8	VSS_IO	K26	VSS_IO	Y24
MCLK	E20	TRACEPKT1	B2	VDD_IO	AD12	VSS_IO	L3	VSS_IO	AA1
MOE/	G26	TRACEPKT2	F5	VDD_IO	AD16	VSS_IO	L11	VSS_IO	AB26
NC	AC9	TRACEPKT3	E4	VDD_IO	AD20	VSS_IO	L12	VSS_IO	AC3
PAR	AF19	TRACEPKT4	C2	VDD_IO	AE26	VSS_IO	L13	VSS_IO	AD7
PAR64	AA24	TRACEPKT5	E3	VDD_IO	AF1	VSS_IO	L14	VSS_IO	AD11
PCI5VBIAS	AD9	TRACEPKT6	G5	VDD_IO	AF5	VSS_IO	L15	VSS_IO	AD15
PCI5VBIAS	AE6	TRACEPKT7	F4	VDD_IO	AF9	VSS_IO	L16	VSS_IO	AD19
PCI5VBIAS	AC10	TRACESYNC	E5	VDD_IO	AF13	VSS_IO	M11	VSS_IO	AD23
PCI5VBIAS	AF12	TRDY/	AE16	VDD_IO	AF17	VSS_IO	M12	VSS_IO	AE1
PCI5VBIAS	AD18	TRST_ICE/	AB4	VDD_IO	AF21	VSS_IO	M13	VSS_IO	AF2
PCI5VBIAS	AB22	TST_RST/	AD5	VDD_IO	AF25	VSS_IO	M14	VSS_IO	AF6
PCI5VBIAS	Y22	VDD_IO	A1	VDDA	C1	VSS_IO	M15	VSS_IO	AF10
PCI5VBIAS	W25	VDD_IO	A2	VDDA	AB21	VSS_IO	M16	VSS_IO	AF14
PCI5VBIAS	M23	VDD_IO	A6	VDDC	D2	VSS_IO	M24	VSS_IO	AF18
PERR/	AE17	VDD_IO	A10	VDDC	N2	VSS_IO	N1	VSS_IO	AF22
PIPESTAT0	D5	VDD_IO	A14	VDDC	AD3	VSS_IO	N11	VSS_IO	AF26
PIPESTAT1	E6	VDD_IO	A18	VDDC	AE3	VSS_IO	N12	VSSA	H5
PIPESTAT2	C3	VDD_IO	A22	VDDC	AC7	VSS_IO	N13	VSSA	AD24
PVT1	AE5	VDD_IO	A26	VDDC	AF15	VSS_IO	N14	VSSC	G4
PVT2	AF4	VDD_IO	C7	VDDC	AE24	VSS_IO	N15	VSSC	P2
RAMCE/	D20	VDD_IO	C11	VDDC	AD25	VSS_IO	N16	VSSC	AB5
REQ/	AD10	VDD_IO	C15	VDDC	M22	VSS_IO	P11	VSSC	AB7
REQ64/	AD22	VDD_IO	C19	VDDC	J22	VSS_IO	P12	VSSC	AB8
RST/	AB10	VDD_IO	C23	VDDC	E19	VSS_IO	P13	VSSC	AD14
RTCK_ICE	AA5	VDD_IO	D3	VDDC	D15	VSS_IO	P14	VSSC	AB23
SCANEN	N22	VDD_IO	E26	VDDC	D6	VSS_IO	P15	VSSC	AB24
SCANMODE	E7	VDD_IO	F1	VSS_IO	A5	VSS_IO	P16	VSSC	L22
SCLK	F3	VDD_IO	G24	VSS_IO	A9	VSS_IO	P26	VSSC	F25
SerialCLK	J25	VDD_IO	H3	VSS_IO	A13	VSS_IO	R3	VSSC	C26
SerialDATA	H26	VDD_IO	J26	VSS_IO	A17	VSS_IO	R11	VSSC	C21
SERR/	AC17	VDD_IO	K1	VSS_IO	A21	VSS_IO	R12	VSSC	C14
STOP/	AB16	VDD_IO	L24	VSS_IO	A25	VSS_IO	R13	VSSC	B4
TCK_CHIP	AC6	VDD_IO	M3	VSS_IO	B1	VSS_IO	R14	ZCR_EN/	N23

Table 5.21 contains the pinout for the LSI53C1030.

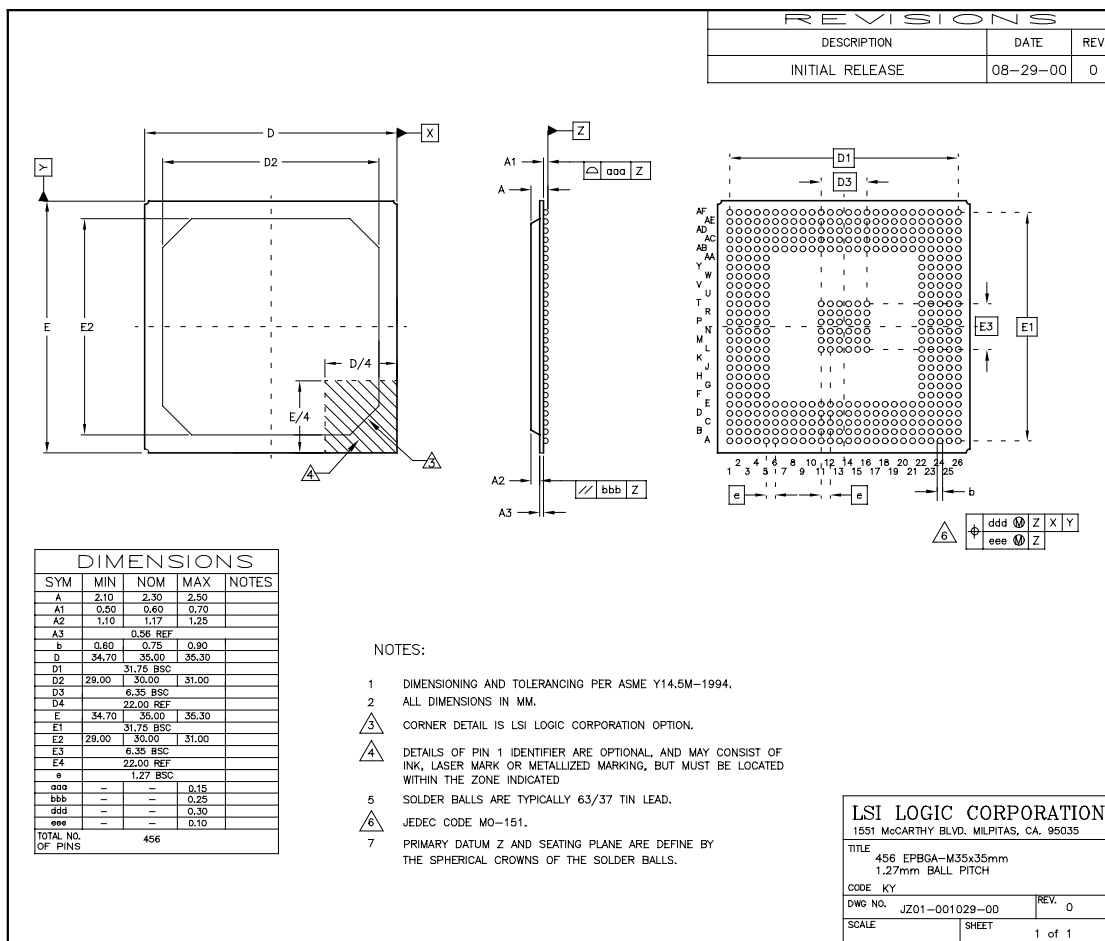
Table 5.21 LSI53C1030 Signal List by BGA Position

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
A1	VDD_IO	B20	B_SD10+	D14	B_SACK-	F24	MAD4	L4	A_SSEL-
A2	VDD_IO	B21	B_SD11-	D15	VDDC	F25	VSSC	L5	A_SACK+
A3	B_SD12-	B22	B_DIFFSENS	D16	B_SMSG+	F26	VSS_IO	L11	VSS_IO
A4	B_SD12+	B23	ADV/	D17	B_SCD+	G1	A_SD10+	L12	VSS_IO
A5	VSS_IO	B24	MADP0	D18	B_SIO+	G2	A_SD10-	L13	VSS_IO
A6	VDD_IO	B25	MAD13	D19	B_SD10-	G3	VSS_IO	L14	VSS_IO
A7	B_SDP1-	B26	VSS_IO	D20	RAMCE/	G4	VSSC	L15	VSS_IO
A8	B_SD0+	C1	VDDA	D21	ADSC/	G5	TRACEPKT6	L16	VSS_IO
A9	VSS_IO	C2	TRACEPKT4	D22	MAD15	G22	MAD0	L22	VSSC
A10	VDD_IO	C3	PIPESTAT2	D23	MAD12	G23	MAD3	L23	GPIO6
A11	B_RBIA5	C4	VSS_IO	D24	VSS_IO	G24	VDD_IO	L24	VDD_IO
A12	B_SD6-	C5	TN	D25	MAD2	G25	FLSHCE/	L25	GPIO5
A13	VSS_IO	C6	B_SD13-	D26	MAD7	G26	MOE/	L26	AD34
A14	VDD_IO	C7	VDD_IO	E1	VSS_IO	H1	A_SD8-	M1	A_SRST-
A15	B_SBSY-	C8	VSS_IO	E2	A_DIFFSENS	H2	A_SD8+	M2	A_SRST+
A16	B_SRST+	C9	B_SD2-	E3	TRACEPKT5	H3	VDD_IO	M3	VDD_IO
A17	VSS_IO	C10	B_SD4+	E4	TRACEPKT3	H4	A_SD9+	M4	A_SATN-
A18	VDD_IO	C11	VDD_IO	E5	TRACESYNC	H5	VSSA	M5	A_SACK-
A19	B_SD8-	C12	VSS_IO	E6	PIPESTAT1	H22	MAD5	M11	VSS_IO
A20	B_SD9+	C13	B_SDP0+	E7	SCANMODE	H23	BWE0/	M12	VSS_IO
A21	VSS_IO	C14	VSSC	E8	B_SD14-	H24	VSS_IO	M13	VSS_IO
A22	VDD_IO	C15	VDD_IO	E9	B_SDP1+	H25	GPIO3	M14	VSS_IO
A23	B_SD11+	C16	VSS_IO	E10	B_SP2+	H26	SerialDATA	M15	VSS_IO
A24	DIS_	C17	B_SSEL+	E11	B_SD3+	J1	VSS_IO	M16	VSS_IO
	PCI_FSN/	C18	B_SREQ+	E12	B_SD7+	J2	A_SREQ-	M22	VDDC
A25	VSS_IO	C19	VDD_IO	E13	B_SD7-	J3	A_SREQ+	M23	PCI5VBIAS
A26	VDD_IO	C20	VSS_IO	E14	B_SACK+	J4	A_SD9-	M24	VSS_IO
B1	VSS_IO	C21	VSSC	E15	B_SRST-	J5	A_SIO+	M25	GPIO4
B2	TRACEPKT1	C22	MADP1	E16	B_SCD-	J22	VDDC	M26	AD35
B3	TRACECLK	C23	VDD_IO	E17	B_SIO-	J23	A_LED/	N1	VSS_IO
B4	VSSC	C24	MAD10	E18	B_SD9-	J24	FLSHALE1/	N2	VDDC
B5	B_SD13+	C25	HB_LED/	E19	VDDC	J25	SerialCLK	N3	A_SBSY-
B6	B_SD14+	C26	VSSC	E20	MCLK	J26	VDD_IO	N4	A_SBSY+
B7	B_SD15+	D1	A_SD11+	E21	MAD14	K1	VDD_IO	N5	A_SATN+
B8	B_SD0-	D2	VDDC	E22	MAD11	K2	A_SSEL+	N11	VSS_IO
B9	B_SD1+	D3	VDD_IO	E23	MAD8	K3	A_SCD-	N12	VSS_IO
B10	B_SD4-	D4	TRACEPKT0	E24	BWE1/	K4	A_SCD+	N13	VSS_IO
B11	B_SD5-	D5	PIPESTAT0	E25	MAD6	K5	A_SIO-	N14	VSS_IO
B12	B_SD6+	D6	VDDC	E26	VDD_IO	K22	FLSHALE0/	N15	VSS_IO
B13	B_VDDBIAS	D7	TESTCLKEN	F1	VDD_IO	K23	B_LED/	N16	VSS_IO
B14	B_SATN-	D8	B_SD15-	F2	A_SD11-	K24	GPIO2	N22	SCANEN
B15	B_SBSY+	D9	B_SD1-	F3	SCLK	K25	GPIO7	N23	ZCR_EN/
B16	B_SMSG-	D10	B_SD3-	F4	TRACEPKT7	K26	VSS_IO	N24	AD32
B17	B_SSEL-	D11	B_SD5+	F5	TRACEPKT2	L1	A_SMSG+	N25	AD33
B18	B_SREQ-	D12	B_SDP0-	F22	MAD9	L2	A_SMSG-	N26	VDD_IO
B19	B_SD8+	D13	B_SATN+	F23	MAD1	L3	VSS_IO		

Table 5.21 LSI53C1030 Signal List by BGA Position (Cont.)

Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal
P1	VDD_IO	T25	AD45	AA5	RTCK_ICE	AC14	AD16	AE8	GNT/
P2	VSSC	T26	AD37	AA22	CLKMODE_0	AC15	AD17	AE9	AD31
P3	A_SD7+	U1	VSS_IO	AA23	C_BE7/	AC16	DEVSEL/	AE10	AD29
P4	A_SDP0-	U2	A_SD4-	AA24	PAR64	AC17	SERR/	AE11	AD26
P5	A_SDP0+	U3	A_SD2+	AA25	AD60	AC18	AD13	AE12	AD25
P11	VSS_IO	U4	A_SD3+	AA26	VDD_IO	AC19	AD8	AE13	AD21
P12	VSS_IO	U5	A_SD3-	AB1	VDD_IO	AC20	AD2	AE14	AD18
P13	VSS_IO	U22	AD55	AB2	A_SD13-	AC21	AD0	AE15	IRDY/
P14	VSS_IO	U23	AD49	AB3	TDI_ICE	AC22	CLK	AE16	TRDY/
P15	VSS_IO	U24	AD52	AB4	TRST_ICE/	AC23	GPIO0	AE17	PERR/
P16	VSS_IO	U25	AD48	AB5	VSSC	AC24	VDD_IO	AE18	C_BE1/
P22	AD42	U26	VDD_IO	AB6	TESTACLK	AC25	C_BE6/	AE19	AD14
P23	AD41	V1	VDD_IO	AB7	VSSC	AC26	AD61	AE20	AD9
P24	AD39	V2	A_SD2-	AB8	VSSC	AD1	A_SD12-	AE21	C_BE0/
P25	AD38	V3	A_SD0+	AB9	ALT_INTB/	AD2	TDO_ICE	AE22	AD6
P26	VSS_IO	V4	A_SD1-	AB10	RST/	AD3	VDDC	AE23	AD1
R1	A_RBIA5	V5	A_SD1+	AB11	AD28	AD4	VDD_IO	AE24	VDDC
R2	A_SD5+	V22	AD56	AB12	AD24	AD5	TST_RST/	AE25	GPIO1
R3	VSS_IO	V23	AD53	AB13	C_BE3/	AD6	TDO_CHIP	AE26	VDD_IO
R4	A_SD7-	V24	AD54	AB14	C_BE2/	AD7	VSS_IO	AF1	VDD_IO
R5	A_SD6+	V25	AD51	AB15	FRAME/	AD8	VDD_IO	AF2	VSS_IO
R11	VSS_IO	V26	VSS_IO	AB16	STOP/	AD9	PCI5VBIAS	AF3	TDI_CHIP
R12	VSS_IO	W1	A_SDP1+	AB17	AD12	AD10	REQ/	AF4	PVT2
R13	VSS_IO	W2	A_SDP1-	AB18	AD11	AD11	VSS_IO	AF5	VDD_IO
R14	VSS_IO	W3	VSS_IO	AB19	AD5	AD12	VDD_IO	AF6	VSS_IO
R15	VSS_IO	W4	A_SD0-	AB20	ACK64/	AD13	AD22	AF7	ALT_INTA/
R16	VSS_IO	W5	A_SD15+	AB21	VDDA	AD14	VSSC	AF8	AD30
R22	AD43	W22	AD63	AB22	PCI5VBIAS	AD15	VSS_IO	AF9	VDD_IO
R23	AD40	W23	AD59	AB23	VSSC	AD16	VDD_IO	AF10	VSS_IO
R24	VDD_IO	W24	VDD_IO	AB24	VSSC	AD17	AD15	AF11	AD20
R25	AD44	W25	PCI5VBIAS	AB25	AD62	AD18	PCI5VBIAS	AF12	PCI5VBIAS
R26	AD36	W26	AD50	AB26	VSS_IO	AD19	VSS_IO	AF13	VDD_IO
T1	A_VDDBIAS	Y1	A_SD15-	AC1	A_SD12+	AD20	VDD_IO	AF14	VSS_IO
T2	A_SD5-	Y2	A_SD14+	AC2	CLKMODE_1	AD21	AD4	AF15	VDDC
T3	VDD_IO	Y3	VDD_IO	AC3	VSS_IO	AD22	REQ64/	AF16	AD19
T4	A_SD4+	Y4	IDDTN	AC4	DIS_	AD23	VSS_IO	AF17	VDD_IO
T5	A_SD6-	Y5	TMS_ICE		SCSI_FSN/	AD24	VSSA	AF18	VSS_IO
T11	VSS_IO	Y22	PCI5VBIAS	AC5	IOPD_GNT/	AD25	VDDC	AF19	PAR
T12	VSS_IO	Y23	C_BE5/	AC6	TCK_CHIP	AD26	C_BE4/	AF20	AD10
T13	VSS_IO	Y24	VSS_IO	AC7	VDDC	AE1	VSS_IO	AF21	VDD_IO
T14	VSS_IO	Y25	AD58	AC8	INTA/	AE2	TESTHCLK	AF22	VSS_IO
T15	VSS_IO	Y26	AD57	AC9	NC	AE3	VDDC	AF23	AD7
T16	VSS_IO	AA1	VSS_IO	AC10	PCI5VBIAS	AE4	TMS_CHIP	AF24	AD3
T22	AD47	AA2	A_SD14-	AC11	AD27	AE5	PVT1	AF25	VDD_IO
T23	AD46	AA3	A_SD13+	AC12	AD23	AE6	PCI5VBIAS	AF26	VSS_IO
T24	VSS_IO	AA4	TCK_ICE	AC13	IDSEL	AE7	INTB/		

Figure 5.13 456-Pin EPBGA (KY) Mechanical Drawing



Important: This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code KY.

Appendix A

Register Summary

Tables [A.1](#), [A.2](#), and [A.3](#) provide a register summary.

Table A.1 LSI53C1030 PCI Registers

Register Name	Offset ¹	Read/Write	Page
Vendor ID	0x00–0x01	Read Only	4-3
Device ID	0x02–0x03	Read Only	4-3
Command	0x04–0x05	Read/Write	4-3
Status	0x06–0x07	Read/Write	4-5
Revision ID	0x08	Read/Write	4-7
Class Code	0x09–0x0B	Read Only	4-7
Cache Line Size	0x0C	Read/Write	4-7
Latency Timer	0x0D	Read/Write	4-8
Header Type	0x0E	Read Only	4-8
Reserved	0x0F	Reserved	4-9
I/O Base Address	0x10–0x13	Read/Write	4-9
Memory [0] Low	0x14–0x17	Read/Write	4-9
Memory [0] High	0x18–0x1B	Read/Write	4-10
Memory [1] Low	0x1C–0x1F	Read/Write	4-10
Memory [1] High	0x20–0x23	Read/Write	4-11
Reserved	0x24–0x27; 0x28–0x2B	Reserved	4-11
Subsystem Vendor ID	0x2C–0x2D	Read Only	4-12
Subsystem ID	0x2E–0x2F	Read Only	4-12

Table A.1 LSI53C1030 PCI Registers (Cont.)

Register Name	Offset ¹	Read/Write	Page
Expansion ROM Base Address	0x30–0x33	Read/Write	4-14
Capabilities Pointer	0x34	Read Only	4-14
Reserved	0x35–0x37; 0x38–0x3B	Reserved	4-15
Interrupt Line	0x3C	Read/Write	4-15
Interrupt Pin	0x3D	Read Only	4-16
Minimum Grant	0x3E	Read Only	4-16
Maximum Latency	0x3F	Read Only	4-17
Power Management Capability ID	—	Read Only	4-17
Power Management Next Pointer	—	Read Only	4-17
Power Management Capabilities	—	Read Only	4-18
Power Management Control/Status	—	Read/Write	4-19
Power Management Bridge Support Extensions	—	Read Only	4-20
Power Management Data	—	Read Only	4-20
MSI Capability ID	—	Read Only	4-20
MSI Next Pointer	—	Read Only	4-21
Message Control	—	Read/Write	4-21
Message Address	—	Read/Write	4-22
Message Upper Address	—	Read/Write	4-23
Message Data	—	Read/Write	4-23
PCI-X Capability ID	—	Read Only	4-24
PCI-X Next Pointer	—	Read Only	4-24
PCI-X Command	—	Read/Write	4-24
PCI-X Status	—	Read/Write	4-26

1. The offset of the PCI extended capabilities registers can vary. Access these registers through the Next Pointer and Capability ID registers.

Table A.2 LSI53C1030 PCI I/O Space Registers

Register Name	Offset	Read/Write	Page
System Doorbell	0x00	Read/Write	4-30
Write Sequence	0x04	Read/Write	4-30
Host Diagnostic	0x08	Read/Write	4-31
Test Base Address	0x0C	Read/Write	4-33
Diagnostic Read/Write Data	0x10	Read/Write	4-33
Diagnostic Read/Write Address	0x14	Read/Write	4-34
Reserved	0x18–0x2F	Reserved	–
Host Interrupt Status	0x30	Read/Write	4-35
Host Interrupt Mask	0x34	Read/Write	4-36
Reserved	0x38–0x3F	Reserved	–
Request FIFO	0x40	Read/Write	4-37
Reply FIFO	0x44	Read/Write	4-37

Table A.3 LSI53C1030 PCI I/O Space Registers

Register Name	Offset	Read/Write	Page
System Doorbell	0x00	Read/Write	4-30
Write Sequence	0x04	Read/Write	4-30
Host Diagnostic	0x08	Read/Write	4-31
Test Base Address	0x0C	Read/Write	4-33
Reserved	0x10–0x2F	Reserved	–
Host Interrupt Status	0x30	Read/Write	4-35
Host Interrupt Mask	0x34	Read/Write	4-36
Reserved	0x38–0x3F	Reserved	–
Request FIFO	0x40	Read/Write	4-37
Reply FIFO	0x44	Read/Write	4-37

Index

Numerics

12 mA output signals 5-6
133 MHz 1-11
133 MHz capable bit 4-27
133 MHz PCI-X 1-3, 3-21, 3-22, 5-9
133 MHz PCI-X bit 4-27
33 MHz PCI 5-9
64-bit address capable bit 4-21
64-bit device bit 4-27
64-bit enable bit 3-22
64-bit PCI 1-3, 1-11, 3-21, 3-22
66 MHz capable bit 3-22, 4-6
66 MHz PCI 3-21, 3-22, 5-9
66 MHz PCI-X 5-9
8 mA output signals 5-6

A

A_DIFFSENS 2-23, 3-11, 5-4
A_LED/ 2-5, 3-19, 5-6
A_RBIAS 3-11
A_SACK+- 3-12
A_SATN+- 3-12
A_SBSY+- 3-12
A_SCD+- 3-12
A_SD[15:0]+- 3-10
A_SDP[1:0]+- 3-10
A_SIO+- 3-12
A_SMSG+- 3-12
A_SREQ+- 3-12
A_SRST+- 3-12
A_SSEL+- 3-12
A_VDDBIAS 3-11
absolute maximum stress ratings 5-2
AC characteristics 5-9
ACK64/ 3-6, 5-5
active LOW 3-1
active termination 2-23
AD[31:0] 5-5
AD[63:0] 3-5, 5-5
address

diagnostic read/write 4-34
latches 3-15
address reply 2-7
address/data bus 3-21, 4-27
ADSC/ 3-14, 5-6
ADV/ 3-14, 5-6
air temperature 5-2
alias to memory read block 2-10, 2-12, 2-13
alias to memory write block 2-10, 2-12
alignment 2-14
ALT_INTA/ 2-15, 3-8, 3-9, 4-22, 4-36, 5-6
ALT_INTB/ 2-15, 3-8, 3-9, 4-22, 4-36, 5-6
analog voltage 5-2
arbitration 2-15
ARM Multi-ICE 1-13
ARM966E-S 1-3, 1-10, 2-4, 2-6, 3-10, 4-32
aux_current bit 4-18

B

B_DIFFSENS 2-23, 3-13, 5-4
B_LED/ 2-5, 3-19, 5-6
B_RBIAS 3-13
B_SACK+- 3-14
B_SATN+- 3-14
B_SBSY+- 3-14
B_SCD+- 3-14
B_SD[15:0]+- 3-13
B_SDP[1:0]+- 3-13
B_SIO+- 3-14
B_SMSG+- 3-14
B_SREQ+- 3-14
B_SRST+- 3-14
B_SSEL+- 3-14
B_VDDBIAS 3-13
ball grid array 5-18, 5-20
base address register
I/O 2-4, 4-9
memory [0] 4-9
memory [1] 4-10
BGA top view 5-20
bidirectional signals 5-5

BIOS 2-8, 2-27

bit

- 133 MHz capable 4-27
- 64-bit address capable 4-21
- 64-bit device 4-27
- 66 MHz capable 4-6
- aux current 4-18
- bus number 4-28
- D1 support 4-18
- D2 support 4-18
- data parity error recovery enable 4-26
- data parity error reported 4-6
- data scale 4-19
- data select 4-19
- designed maximum cumulative read size 4-26
- designed maximum memory read byte count 4-27
- designed maximum outstanding split transactions 4-26
- detected parity error (from slave) 4-5
- device complexity 4-27
- device number 4-28
- device specific initialization 4-18
- DEVSEL/ timing 4-5
- diagnostic memory enable 4-32
- diagnostic read/write enable 4-32
- diagnostic write enable 4-31, 4-34
- DisARM 4-32
- doorbell interrupt mask 4-37
- enable bus mastering 4-4
- enable I/O 4-5
- enable memory space 4-4
- enable parity error response 4-4
- expansion ROM enable 4-14
- flash ROM bad signature 4-32
- function number 4-28
- interrupt request routing mode 4-36
- IOP doorbell status 4-35
- MSI enable 4-22
- multiple message 4-22
- new capabilities 4-6
- PME clock 4-18
- PME enable 4-19
- PME status 4-19
- PME support 4-18
- power management version 4-18
- power state 4-19
- received master abort (from master) 4-5
- received split completion error message 4-26
- received target abort (from master) 4-5
- reply interrupt 4-35
- reply interrupt mask 4-36
- reset adapter 4-32
- reset history 4-31, 4-32

SERR/ enable 4-4

signalled system error 4-5

system doorbell interrupt 4-35

TTL interrupt 4-32

unexpected split completion 4-27

write and invalidate enable 4-4

block diagram 2-3

board application 1-3

boot device 2-5, 2-24

boundary scan 1-13

burst size selection 2-13

bus

- mastering 2-15, 2-17

- number 4-28

- PCI commands 2-10

- training 1-10

BWE[1:0]/ 3-15, 5-6

C

C_BE[3:0]/ 2-8, 2-9, 2-10, 2-12, 5-5

C_BE[7:0]/ 3-5, 5-5

cache line size 1-11, 2-13, 2-14, 4-7

- alignment 2-14

- register 2-15, 4-7

capabilities pointer register 4-14

capability ID 4-2

- MSI 4-20

- PCI-X 4-24

- power management 4-17

capacitance

- input 5-4

checksum 2-27, 2-28

class code register 4-7

CLK 3-4, 5-6

CLKMODE_0 3-18, 3-25, 5-6

CLKMODE_1 3-18, 3-25, 5-6

clock

- EEPROM 3-16, 3-25

- external 5-9

- PCI 5-9

- PME 4-18

- SCLK 3-10, 5-9

- SCSI 3-10

- skew control 2-22

CLS 4-7

CLS alignment 2-14

command register 2-18, 4-3

common mode voltage 5-3

completer ID 4-28

configuration

- parameters 2-24

- read command 2-8, 2-10, 2-12, 2-13, 4-6

- record 2-27, 2-28
- space 2-8, 4-1
- write command 2-8, 2-10, 2-12, 2-13, 4-6
- configuration space 2-8, 4-1
 - C_BE[3:0]/ 2-10
- context manager 2-5, 2-6
- core voltage 5-2, 5-3
- CRC 1-2, 1-7, 1-13, 2-22
- CRC-32 1-7
- current
 - I/O supply 5-2
 - latch-up 5-2, 5-8
- cyclic redundancy check 1-2, 2-22

D

- D0 2-16, 2-17, 4-19
- D1 2-16, 2-17, 4-19
- D1 support bit 4-18
- D2 2-16, 2-17, 4-19
- D2 support bit 4-18
- D3 2-16, 2-17, 2-18, 4-19
- DAC 1-11, 2-8, 2-10, 2-13
- data
 - diagnostic read/write 4-33
 - EEPROM 3-16
 - parity error recovery enable bit 4-26
 - parity error reported bit 4-6
 - scale bit 4-19
 - select bit 4-19
- datapath engine 2-6
- DC characteristics 5-1
- debug signals 3-17
- delay filter 5-8
- designed maximum cumulative read size bit 4-26
- designed maximum memory read byte count bit 4-27
- designed maximum outstanding split transactions bit 4-26
- detected parity error (from slave) bit 4-5
- device complexity bit 4-27
- device driver stability 1-6
- device ID register 4-3
- device number bit 4-28
- device specific initialization bit 4-18
- DEVSEL/ 3-6, 5-5
- DEVSEL/ timing bit 4-5
- diagnostic memory 4-28
- diagnostic memory enable bit 4-32
- diagnostic read/write address register 4-31, 4-32, 4-34
- diagnostic read/write data register 4-31, 4-32, 4-33, 4-34
- diagnostic read/write enable bit 4-32
- diagnostic write enable bit 4-31, 4-34

- DIS_PCI_FSN/ 3-18, 3-25, 5-6
- DIS_SCSI_FSN/ 3-18, 3-25, 5-6
- DisARM bit 4-32
- DMA 1-12, 2-4, 2-6, 2-15
 - arbiter and router 2-4
- domain validation 1-2, 1-8, 1-13, 2-22
- doorbell 2-6, 2-7
 - host 4-30
 - interrupt mask bit 4-37
 - status bit 4-35
 - system 4-30, 4-35
 - system interface 2-6
 - system interrupt bit 4-35
- double transition clocking 1-2, 2-18
- drawing
 - mechanical 5-26
 - package 5-18, 5-20
- drive strength 1-8, 2-20, 2-22
- driver
 - LVD 5-3
- DT clocking 1-2, 2-18
- DT data phase 2-18
- dual address cycles command 1-11, 2-8, 2-10, 2-13

E

- EEPROM 2-5, 2-6, 2-27, 3-16, 3-23, 3-25
 - configuration record 2-27
 - download enable 3-21
 - interface 2-27, 3-16
- electrostatic discharge 5-2
- enable
 - bus mastering bit 4-4
 - diagnostic memory bit 4-32
 - diagnostic write bit 4-31
 - I/O space bit 4-5
 - memory space bit 4-4
 - MSI bit 4-22
 - parity error response bit 4-4
 - write and invalidate bit 4-4
- ESD 1-13, 5-2, 5-8
- expansion ROM base address 4-4
- expansion ROM base address register 4-14
- expansion ROM enable bit 4-14
- external
 - clock 5-9
 - memory controller 2-5
 - memory interface 2-24
 - memory interface timing diagrams 5-11

F

- ferrite bead 3-20
- fibre channel 1-5, 1-12

FIFO

- DMA 2-4
 - reply 4-37
 - reply free 2-7
 - reply post 2-7, 4-35
 - request 4-37
 - request post 2-7
- filter delay 5-8
- filtering 5-9
- flash ROM 1-3, 2-5, 2-24, 3-15, 3-23
- address space 2-24
 - bad signature bit 4-32
 - block diagram 2-25
 - configurations 2-25
 - interface 2-24, 3-14
 - signature recognition 2-25, 2-26
 - size 3-22, 3-24
- flexibility 1-12
- FLSHALE[1:0]/ 2-25, 3-15, 5-6
- FLSHCE/ 2-25, 3-15, 5-6
- FRAME/ 3-6, 5-5
- frames
- reply message 2-7, 2-15
 - request message 2-7, 2-15
- free running timer 2-5
- frequency synthesizer 3-18, 3-20, 3-25
- function number bit 4-28
- Fusion-MPT 1-3, 1-5, 1-10, 1-11, 1-12, 2-1, 2-3, 2-4, 2-6, 2-26, 3-15, 4-28

G

- general description 1-1
- GNT/ 2-15, 2-28, 3-7, 5-6
- GPIO[7:0] 2-5, 3-19, 3-25, 5-5
- grant 2-15
- ground signals 3-20

H

- HB_LED/ 2-5, 3-19, 5-6
- header type register 4-8
- host diagnostic register 4-31, 4-34
- host doorbell value 4-30
- host interface module 2-2, 2-3, 2-5
- host interrupt mask register 2-16, 3-8, 3-9, 4-35, 4-36
- host interrupt status register 4-35, 4-36
- host system 2-6
- hot plug 5-7
- HVD 2-23, 3-10, 3-11, 3-13
- sense voltage 5-4
- hysteresis 5-7

I

I/O

- base address 4-5
 - base address register 2-4, 2-9, 4-9
 - key 4-31, 4-34
 - processor 2-4, 2-28
 - read command 2-10, 2-11, 2-13
 - space 2-9, 4-1, 4-28
 - supply voltage 5-2
 - write command 2-10, 2-11, 2-13
- I/O supply current 5-2
- ICE 3-17
- ID control 3-21, 3-22, 3-23, 4-13
- IDC socket 2-30
- IDD-Core 5-2
- IDD-I/O 5-2
- IDDTN 3-18, 3-25, 5-6
- IDSEL 2-8, 2-28, 3-6, 3-16, 5-6
- IM 1-4, 1-13, 2-5, 2-24, 2-26
- in-circuit emulator 3-17
- information unit 2-18, 2-21
- input
- capacitance 5-4
 - filtering 5-9
 - reset 5-10
 - signals 5-6
 - voltage 5-2
- INTA/ 2-15, 3-8, 4-22, 4-32, 4-36, 5-6
- INTB/ 2-15, 3-8, 4-22, 4-36, 5-6
- Integrated Mirroring 1-4, 1-13, 2-5, 2-24, 2-26
- Integrated Striping 1-4
- integration 1-12
- interface
- EEPROM 2-27
 - external memory 2-24
 - flash ROM 2-24, 3-14, 3-15
 - ICE 3-17
 - JTAG 3-17
 - memory 3-14
 - NVSRAM 3-14, 3-15
 - PCI bus 3-4
 - SCSI channel [0] 3-10
 - SCSI channel [1] 3-13
 - serial EEPROM 2-6, 2-27, 3-16
 - test 3-17
- interrupt 2-16
- acknowledge command 2-10, 2-13
 - ALT_INTA/ 2-15
 - ALT_INTB/ 2-15
 - coalescing 1-11
 - doorbell mask bit 4-37
 - INTA/ 2-15

- INTB/ 2-15
- line register 4-15
- message signalled 2-15, 2-16
- message signalled 2-16
- MSI 1-12
- output 5-10
- PCI 2-15
- pin register 4-16
- pins 2-15
- reply 2-16
- reply bit 4-35
- reply mask bit 4-36
- request routing mode bits 4-36
- service routine 1-11
- signal routing 4-36
- system doorbell 2-16, 4-35
- system doorbell bit 4-35
- TTL bit 4-32
- intersymbol interference 1-7, 1-13
- IOP 2-4, 2-5, 2-6, 2-7, 3-21, 4-30, 4-32, 4-35
 - boot 3-21, 3-23
- IOP doorbell status bit 4-35
- IOPD_GNT/ 2-28, 3-16, 3-25, 5-6
- IRDY/ 3-6, 5-5
- IS 1-4
- ISI 1-7, 1-13, 2-19
- ISR 1-11
- IU_Request 2-18

J

- JTAG 1-13, 3-17
- junction temperature 5-2

K

- key
 - I/O 4-31, 4-34

L

- latch-up current 5-2, 5-8
- latch-up protection 1-13
- latency timer 4-8
- latency timer register 4-8
- lead temperature 5-2
- LED 2-5, 3-19
- low voltage differential 2-23
- LSI53C1010R 1-12, 2-29
- LVD 1-12, 2-23, 3-10, 3-11, 3-13
 - driver 5-3
 - driver SCSI signals 5-3
 - receiver SCSI signals 5-3
 - receiver voltage 5-3

- sense voltage 5-4
- LVDlink 1-3, 1-8, 1-12, 2-18, 2-23

M

- MAD[10] 4-13
- MAD[11] 4-13
- MAD[13] 4-6
- MAD[14] 4-27
- MAD[15:0] 2-5, 3-15, 3-21, 3-25, 5-5
- MAD[15] 4-27
- MAD[2:1] 2-24
- MAD[3] 2-26
- MAD[7:0] 2-5, 2-24, 3-15
- MAD[7] 4-12, 4-13
- MADP[0] 2-5
- MADP[1:0] 2-5, 3-15, 3-21, 3-25, 5-5
- margin control settings 2-18
- master abort 4-5
- master data parity error 4-26
- max_lat 4-17
- maximum latency register 4-17
- maximum memory read byte count bits 4-25
- maximum outstanding split transactions bits 4-24
- maximum stress ratings 5-2
- MCLK 3-14, 5-6
- MCS 2-18
- mechanical drawing 5-26
- memory
 - alias to read block 2-12, 2-13
 - alias to write block 2-10, 2-12
 - controller 2-5
 - flash ROM size 3-24
 - read block command 1-11, 2-10, 2-12, 2-13, 2-14
 - read command 2-10, 2-11, 2-13, 2-14, 2-15
 - read dword command 1-11, 2-10, 2-11, 2-13
 - read line command 1-11, 2-10, 2-14, 2-15
 - read multiple command 1-11, 2-10, 2-13, 2-15
 - signal interface 3-14
 - space 2-9, 4-1, 4-28
 - space description 4-28
 - write and invalidate command 1-11, 2-10, 2-14, 2-15
 - write block command 1-11, 2-10, 2-12, 2-15
 - write command 2-10, 2-11, 2-14, 2-15
- memory [0] high 4-4, 4-10
- memory [0] low 4-4, 4-9
- memory [1] high 4-4, 4-11
- memory [1] low 4-4, 4-10
- memory read 4-27
- memory space 2-9, 4-28
- message address register 4-22
- message control register 4-21

message data register 4-23
message frame address 4-37
message passing technology 1-10, 2-1
message queues 2-6, 2-7
message signalled interrupts 2-15, 2-16
message upper address register 4-23

MFA

reply 4-37
request 4-37
request free 4-37
minimum grant register 4-16
MOE/ 3-15, 5-6
MSI 1-11, 1-12, 2-15, 2-16, 4-36
capability ID register 4-20
enable bit 4-22
message address 4-22
message data 4-23
message upper address register 4-23
multiple message 4-22
next pointer register 4-21
multifunction PCI 2-8, 3-23, 4-32
multi-ICE 2-30
multiple cache line transfers 2-14
multiple message capable 4-22
multiple message enable 4-21

N

NC 3-1, 3-20
new capabilities bit 4-6
no connect 3-1
normal/fast memory (128 Kbytes)
single byte access read cycle 5-11, 5-15
single byte access write cycle 5-13, 5-16
NVSRAM 1-3, 2-5, 2-24, 2-26, 3-15
block diagram 2-27
integrated mirroring 2-26
interface 3-14
select 3-24
sense 3-22
write journaling 2-26

O

operating conditions 5-2
operating free air temperature 5-2
output signals 5-6

P

P1 line 2-19
paced transfers 1-2, 2-19
package drawing 5-18, 5-20
packetized protocol 1-2, 1-10, 2-21

packetized transfers 2-21
PAR 3-5, 5-5
PAR64 3-5, 5-5
parallel protocol request 2-18, 2-22
parity error 4-6
passive termination 2-23
PC2001 system design guide 1-11, 2-16
PCI 1-12, 2-6
33 MHz 5-9
64-bit 3-21, 3-22
66 MHz 3-21, 3-22, 5-9
66 MHz capable bit 4-6
address and data signals 3-5
address/data bus 3-21, 4-27
addressing 2-8
alias to memory read block command 2-12, 2-13
alias to memory write block command 2-12
arbitration 2-15
arbitration signals 3-7
benefits 1-6
bidirectional signals 5-5
bus commands 2-9, 2-10
bus interface 3-4
cache line size register 2-14
cache mode 2-15
CLK 5-9
command 2-10
configuration read 2-8, 2-10, 2-12
configuration write 2-8, 2-10, 2-12
dual address cycle 2-13
dual address cycles 1-11, 2-8
I/O read 2-10, 2-11
I/O write 2-10
I/O write command 2-11
interrupt acknowledge 2-10
memory read 2-10
memory read block 1-11, 2-10, 2-12, 2-14
memory read command 2-11
memory read dword 1-11, 2-10
memory read dword command 2-11
memory read line 1-11, 2-10, 2-14
memory read multiple 1-11, 2-10, 2-13
memory write 2-10, 2-11
memory write and invalidate 1-11, 2-10, 2-14
memory write block 1-11, 2-10, 2-15
memory write command 2-11
register 4-14
special cycle 2-10, 2-11
split completion 1-11, 2-10, 2-13
command register 4-3
configuration read command 2-10, 2-12, 2-13, 4-6
configuration record 2-28
configuration space 2-8, 2-27, 4-1
address map 4-2
C_BE[3:0]/ 2-8, 2-9, 2-10
configuration write command 2-10, 2-12, 2-13, 4-6
DAC 1-11, 2-8, 2-10, 2-13
device complexity bit 4-27

- dual address cycles command 2-10, 2-13
- dual function 3-21
- encoding 2-10
- error reporting signals 3-7
- frequency synthesizer 3-18, 3-20, 3-25
- FSN 3-18, 3-20, 3-25
- functional description 2-8
- I/O read command 2-10, 2-11, 2-13
- I/O space 2-8, 2-9, 4-1, 4-28
- I/O space address map 4-29
- I/O space and memory space 4-28
- I/O write command 2-10, 2-11, 2-13
- interface 2-4
- interface control signals 3-6
- interrupt acknowledge command 2-10, 2-13
- interrupt signals 3-8
- interrupts 2-15, 4-36, 4-37
- memory [0] address map 4-29
- memory [1] address map 4-29
- memory read block command 2-13, 2-14
- memory read command 2-10, 2-11, 2-13, 2-14, 2-15
- memory read dword command 2-11, 2-13
- memory read line command 2-10, 2-14, 2-15
- memory read multiple command 2-10, 2-13, 2-15
- memory space 2-8, 2-9, 4-1
- memory space [0] 2-4, 2-9, 2-27, 4-1
- memory space [1] 2-9, 4-1
- memory write and invalidate command 2-10, 2-14, 2-15
- memory write block command 2-12, 2-15
- memory write command 2-10, 2-14, 2-15
- multifunction 2-8, 4-32
- new capabilities bit 4-6
- performance 1-11
- power management 2-16
- power management interface specification 2-16
- related signals 3-9
- reset 4-32
- single function 3-21, 3-23
- special cycle command 2-10, 2-11, 4-5
- split completion command 2-13
- status 3-22
- system address space 4-1
- system signals 3-4
- PCI_CAP 3-22
- PCI_GNT/ 3-16
- PCI5VBIAS 1-12, 3-20, 5-5
- PCI-SIG 4-12
- PCI-X 1-11, 1-12, 2-8
 - 133 MHz 3-21, 5-9
 - 133 MHz capable bit 4-27
 - 64-bit device bit 4-27
 - 66 MHz 5-9
 - alias to memory read block command 2-10
 - alias to memory write block command 2-10
 - benefits 1-6
 - bus commands 2-10
 - bus number 4-28
 - capability ID register 4-24
 - command register 4-24
 - commands 2-10
 - data parity error recovery enable bit 4-26
 - designed maximum cumulative read size bit 4-26
 - designed maximum memory read byte count bit 4-27
 - designed maximum outstanding split transactions bit 4-26
 - device complexity bit 4-27
 - device number bit 4-28
 - function number bit 4-28
 - maximum memory read byte count bits 4-25
 - maximum outstanding split transactions bits 4-24
 - memory read block command 2-10
 - memory read dword command 2-10
 - memory write block command 2-10
 - mode 3-21, 3-22
 - next pointer register 4-24
 - received split completion error message bit 4-26
 - split completion command 2-10
 - split completion discarded bit 4-27
 - status 3-22
 - status register 4-26
 - unexpected split completion bit 4-27
- PERR/ 3-7, 5-5
- pinout 5-22, 5-24
- PIPESTAT[2:0] 3-17, 5-6
- PME 4-18, 4-19
 - clock bit 4-18
 - enable bit 4-19
 - status bit 4-19
 - support bits 4-18
- POR 4-32
- POST 4-15
- power management 2-16
 - aux_current bit 4-18
 - bridge support extensions register 4-20
 - capabilities register 4-18
 - capability ID register 4-17
 - control/status register 2-16, 4-19
 - D0 4-19
 - D1 4-19
 - D1 support bit 4-18
 - D2 4-19
 - D2 support bit 4-18
 - D3 2-17, 4-19
 - data register 4-20

- data scale bit 4-19
- data select bit 4-19
- device specific initialization bit 4-18
- event 4-18
- interface 1-11
- next pointer register 4-17
- PME clock bit 4-18
- PME enable bit 4-19
- PME status bit 4-19
- power state bit 4-19
- support bits 4-18
- version bit 4-18

power signals 3-20

power state

- D0 2-16, 2-17

- D1 2-16, 2-17

- D2 2-16, 2-17

- D3 2-16, 2-17, 2-18, 4-19

power state bit 4-19

power-on reset 4-32

power-on sense pins 3-21

PPR 2-18, 2-20, 2-22

precompensation 1-2, 2-18, 2-20

pull-ups and pull-downs 3-25

PVT1, PVT2 3-9, 5-6

Q

QAS 1-2, 1-10, 2-18, 2-21

queue

- message 2-7

- reply message 2-5, 2-7

- request message 2-5, 2-7

quick arbitration and selection 1-2, 1-10, 2-18, 2-21

R

RAID 2-28, 3-16

RAMCE/ 2-26, 3-15, 5-6

read streaming 2-18

received master abort (from master) bit 4-5

received split completion error message bit 4-26

received target abort (from master) bit 4-5

register

- cache line size 4-7

- capabilities pointer 4-14

- class code 4-7

- command 2-18, 4-3

- device ID 4-3

- diagnostic read/write address 4-34

- diagnostic read/write data 4-33

- expansion ROM base address 4-14

- header type 4-8

- host diagnostic 4-31

- host interrupt mask 2-16, 3-8, 3-9, 4-36

- host interrupt status 4-35

- I/O base address 4-9

- interrupt line 4-15

- interrupt pin 4-16

- latency timer 4-8

- maximum latency 4-17

- memory [0] high 4-10

- memory [0] low 4-9

- memory [1] high 4-11

- memory [1] low 4-10

- message address 4-22

- message control 4-21

- message data 4-23

- message upper address 4-23

- minimum grant 4-16

- MSI capability ID 4-20

- MSI next pointer 4-21

- PCI memory [0] address map 4-29

- PCI memory [1] address map 4-29

- PCI-X capability ID 4-24

- PCI-X command 4-24

- PCI-X next pointer 4-24

- PCI-X status 4-26

- power management bridge support extensions 4-20

- power management capabilities 4-18

- power management capability ID 4-17

- power management control/status 2-16, 4-19

- power management data 4-20

- power management next pointer 4-17

- reply FIFO 4-37

- request FIFO 4-37

- revision ID 4-7

- status 4-5

- subsystem ID 4-12

- subsystem vendor ID 4-12

- system doorbell 4-30

- test base address 4-33

- vendor ID 4-3

- write sequence 4-30

register map A-1

- PCI configuration space 4-2

- PCI I/O space 4-29

reliability 1-13

reply FIFO register 4-37

reply free FIFO 2-7

reply interrupt 2-16

reply interrupt bit 4-35

reply interrupt mask bit 4-36

reply message 2-5, 2-7, 2-15, 4-37

reply message queue 2-7

reply MFA 4-37

reply post FIFO 2-7, 4-35

- reply queue 2-7
- REQ/ 2-15, 3-7, 5-6
- REQ/ACK offset, 2-18
- REQ64/ 3-6, 5-5
- request 2-15
- request FIFO register 4-37
- request free MFA 4-37
- request message 2-5
- request message frames 2-7, 2-15
- request message queue 2-7
- request messages 2-7
- request MFA 4-37
- request post FIFO 2-7
- request post MFA 4-37
- requester ID 4-28
- reset adapter bit 4-32
- reset history bit 4-31, 4-32
- reset input 5-10
- revision ID register 4-7
- rise and fall time test condition 5-8
- ROM 2-5, 2-24
- ROM expansion enable bit 4-14
- ROM size 3-22, 3-24
- RST/ 3-4, 5-9
- RTCK_ICE 2-30, 3-17, 5-6
- RTI 2-18
- RTI bit 2-22

S

- SACK+- 5-3
- SATN+- 5-3
- SBSY+- 5-3
- SCANEN 3-18, 3-25, 5-6
- SCANMODE 3-18, 3-25, 5-6
- SCD+- 5-3
- SCLK 3-10, 5-6, 5-9
- SCSI
 - A_DIFFSENS signal 5-4
 - B_DIFFSENS signal 5-4
 - bus interface 2-6
 - bus mastering functions 2-15
 - channel [0] interface 3-10
 - channel [1] interface 3-13
 - channel module 2-5, 2-6
 - CLK 3-10
 - clock 3-10
 - core 2-6
 - CRC 2-22
 - datapath engine 2-6
 - domain validation 2-22
 - driver signals 5-3
 - DT clocking 1-2, 2-18

- dual channel 3-21
- functions 2-15
- information unit transfers 2-21
- input filtering 5-9
- interface signals 3-10
- interrupt steering logic 1-11
- ISI 2-19
- LVD 2-23
- paced transfers 2-19
- packetized transfers 2-21
- parallel protocol request 2-18, 2-22
- performance 1-10
- PPR 2-18, 2-22
- precompensation 2-20
- QAS 2-18, 2-21
- quick arbitration and selection 2-21
- receiver signals 5-3
- SE 2-23
- single channel 3-21
- single ended 2-23
- skew compensation 2-22
- synchronous transfer 2-18
- termination 2-23
- TolerANT technology 1-9
- Ultra320 features 2-19
- SD[15:0]+- 5-3
- SDP[1:0]+- 5-3
- SE 2-23, 3-10, 3-11, 3-13
 - sense voltage 5-4
- sense voltage 5-4
- serial EEPROM 2-5, 2-6, 2-24, 2-27, 3-22, 3-23, 3-25, 4-12, 4-13, 4-33
 - configuration record 2-27
 - download enable 3-21, 3-23
 - interface 2-27
- SerialCLK 3-16, 3-25
- SerialDATA 3-16, 3-25, 5-5
- SERR/ 3-7, 4-26, 5-5, 5-6
- SERR/ enable bit 4-4
- shared RAM 2-5, 2-7
- signal
 - grouping 3-3
 - list 5-22, 5-24
 - no connect 3-1
 - types 3-2
- signal descriptions
 - A_DIFFSENS 3-11
 - A_LED/ 3-19
 - A_RBIAS 3-11
 - A_SACK+- 3-12
 - A_SATN+- 3-12
 - A_SBSY+- 3-12
 - A_SCD+- 3-12

A_SD[15:0]+- 3-10
 A_SDP[1:0]+- 3-10
 A_SIO+- 3-12
 A_SMSG+- 3-12
 A_SREQ+- 3-12
 A_SRST+- 3-12
 A_SSEL+- 3-12
 A_VDDBIAS 3-11
 ACK64/ 3-6
 AD[63:0] 3-5
 ADSC/ 3-14
 ADV/ 3-14
 ALT_INTA/ 3-8, 3-9
 ALT_INTB/ 3-8, 3-9
 B_DIFFSENSE 3-13
 B_LED/ 3-19
 B_RBIAS 3-13
 B_SACK+- 3-14
 B_SATN+- 3-14
 B_SBSY+- 3-14
 B_SCD+- 3-14
 B_SD[15:0]+- 3-13
 B_SDP[1:0]+- 3-13
 B_SIO+- 3-14
 B_SMSG+- 3-14
 B_SREQ+- 3-14
 B_SRST+- 3-14
 B_SSEL+- 3-14
 B_VDDBIAS 3-13
 BWE[1:0]/ 3-15
 C_BE[7:0]/ 3-5
 CLK 3-4
 CLKMODE_0 3-18
 CLKMODE_1 3-18
 DEVSEL/ 3-6
 DIS_PCI_FSN/ 3-18
 DIS_SCSI_FSN/ 3-18
 FL SHALE[1:0]/ 3-15
 FLSHCE/ 3-15
 FRAME/ 3-6
 GNT/ 3-7
 GPIO[7:0] 3-19
 ground 3-20
 HB_LED/ 3-19
 IDDTN 3-18
 IDSEL 3-6
 INTA/ 3-8
 INTB/ 3-8
 IOPD_GNT/ 3-16
 IRDY/ 3-6
 MAD[15:0] 3-15, 3-21
 MADP[1:0] 3-15, 3-21
 MCLK 3-14
 MOE/ 3-15
 NC 3-20
 PAR 3-5
 PAR64 3-5
 PCI5VBIAS 3-20
 PERR/ 3-7
 PIPESTAT[2:0] 3-17
 power 3-20
 power-on sense 3-21
 PVT1,PVT2 3-9
 RAMCE/ 3-15
 REQ/ 3-7
 REQ64/ 3-6
 RST/ 3-4
 RTCK_ICE 3-17
 SCANEN 3-18
 SCANMODE 3-18
 SCLK 3-10
 SerialCLK 3-16
 SerialDATA 3-16
 SERR/ 3-7
 STOP/ 3-6
 TCK_CHIP 3-17
 TCK_ICE 3-17
 TDI_CHIP 3-17
 TDI_ICE 3-17
 TDO_CHIP 3-17
 TDO_ICE 3-17
 TESTACLK 3-18
 TESTCLKEN 3-18
 TESTHCLK 3-18
 TMS_CHIP 3-17
 TMS_ICE 3-17
 TN 3-18
 TRACECLK 3-17
 TRACEPKT[7:0] 3-17
 TRACESYNC 3-17
 TRDY/ 3-6
 TRST_ICE/ 3-17
 TST_RST/ 3-17
 VDD_IO 3-20
 VDDA 3-20
 VDDC 3-20
 VSS_IO 3-20
 VSSA 3-20
 VSSC 3-20
 ZCR_EN/ 3-16
 signal drive strength 2-20, 2-22
 signal list 5-22, 5-24
 signalled system error bit 4-5
 signals
 bidirectional 5-5
 debug 3-17

- flash ROM/NVSRAM interface 3-14
- GPIO 3-19
- ground 3-20
- input 5-6
- LED 3-19
- memory interface 3-14
- PCI address and data 3-5
- PCI arbitration 3-7
- PCI error reporting 3-7
- PCI interface control 3-6
- PCI interrupt 3-8
- PCI system 3-4
- PCI-related 3-9
- power 3-20
- power-on sense 3-21
- pull-ups and pull-downs 3-25
- SCSI channel [0] control 3-12
- SCSI channel [0] interface 3-10
- SCSI channel [1] control 3-14
- SCSI channel [1] interface 3-13
- SCSI interface 3-10
- serial EEPROM interface 3-16
- test interface 3-17
- zero channel RAID interface 3-16
- signature recognition 2-25
- single ended SCSI 2-23
- single ended SCSI signals 5-7
- SIO+- 5-3
- SISL 1-11
- skew compensation 1-2, 1-7, 1-10, 2-22
- slew rate 1-8, 1-10, 1-13, 2-22, 5-8, 5-9
- SMSC+- 5-3
- special cycle command 2-10, 2-11, 4-5
- split completion command 1-11, 2-10, 2-13
- split completion discarded bit 4-27
- split completion error 4-26
- split completion received error message 4-26
- split completion unexpected 4-27
- split transaction 1-11, 4-26
- SREQ+- 5-3
- SRST+- 5-3
- SSEL+- 5-3
- status
 - IOP doorbell bit 4-35
 - register 4-5, 4-26
- STOP/ 3-6, 5-5
- stress ratings 5-2
- subsystem ID 2-27, 2-28, 3-22, 3-23, 4-13
- subsystem ID register 4-12
- subsystem vendor ID 2-27, 2-28, 3-23
- subsystem vendor ID register 4-12
- supply current 5-2
- supply voltage 5-2

- SureLINK 1-2, 1-8, 1-13, 2-22, 2-23
- system address space 4-1
- system application 1-4
- system BIOS 2-8, 2-27
- system doorbell 2-16, 4-35
- system doorbell interrupt bit 4-35
- system doorbell register 4-30
- system interface 2-4, 2-15
 - bus mastering function 2-15
 - doorbell 2-6

T

- Ta 5-2
- target abort 4-5
- TCK_CHIP 3-17, 3-25, 5-6
- TCK_ICE 2-30, 3-17, 3-25, 5-6
- TDI_CHIP 3-17, 3-25, 5-6
- TDI_ICE 2-30, 3-17, 3-25, 5-6
- TDO_CHIP 3-17, 5-6
- TDO_ICE 2-30, 3-17, 5-6
- temperature
 - junction 5-2
 - lead 5-2
 - operating free air 5-2
 - storage 5-2
- termination 2-23
- test base address register 4-33
- test condition 5-8
- test interface 2-30, 3-17
- testability 1-13
- TESTACLK 3-18, 3-25, 5-6
- TESTCLKEN 3-18, 3-25, 5-6
- TESTHCLK 3-18, 3-25, 5-6
- TestReset/ 4-32
- thermal resistance 5-2
- timer 2-5
- timing
 - external memory 5-11
 - interrupt output 5-10
 - PCI and PCI-X 5-9
 - power-up 5-11
 - reset 5-10
- timing diagrams 5-11
- Tj 5-2
- TMS_CHIP 3-17, 3-25, 5-6
- TMS_ICE 2-30, 3-17, 3-25, 5-6
- TN 3-18, 3-25, 5-6
- TolerANT 1-9, 1-13, 5-7
- TRACECLK 3-17, 5-6
- TRACEPKT[7:0] 3-17, 5-6
- TRACESYNC 3-17, 5-6
- transfer period 2-18

transfer width [2-18](#)

transfers

information units [2-21](#)

packetized [2-21](#)

TRDY/ [3-6](#), [5-5](#)

TRST_ICE/ [2-30](#), [3-17](#), [3-25](#), [5-6](#)

TST_RST/ [3-17](#), [3-25](#), [5-6](#)

TTL interrupt bit [4-32](#)

U

Ultra160 SCSI

DT clocking [1-2](#), [2-18](#)

parallel protocol request [2-22](#)

PPR [2-22](#)

Ultra320 SCSI [1-5](#), [1-7](#)

benefits [1-7](#)

bus training [1-10](#)

channel modules [2-2](#)

core [2-6](#)

CRC [2-22](#)

domain validation [2-22](#)

DT clocking [1-2](#), [2-18](#)

features [1-2](#), [2-18](#), [2-19](#)

functional description [2-18](#)

information unit [2-21](#)

ISI [1-7](#), [2-19](#)

paced transfers [2-19](#)

packetized transfers [2-21](#)

parallel protocol request [2-18](#), [2-22](#)

PPR [2-18](#)

precompensation [2-20](#)

QAS [2-21](#)

quick arbitration and selection [2-21](#)

skew compensation [1-2](#), [1-7](#), [1-10](#), [2-22](#)

unexpected split completion bit [4-27](#)

V

VDD_CORE [5-3](#)

VDD_IO [3-20](#), [5-2](#)

VDDA [3-20](#)

VDDC [3-20](#), [5-2](#)

vendor ID register [4-3](#)

version bit [4-18](#)

voltage

analog [5-2](#)

common mode [5-3](#)

core [5-2](#), [5-3](#)

feed-through protection [1-13](#)

I/O [5-2](#)

input [5-2](#)

supply [5-2](#)

VSS_IO [3-20](#)

VSSA [3-20](#)

VSSC [3-20](#)

W

write and invalidate enable bit [4-4](#)

write flow [2-18](#)

write I/O key [4-31](#), [4-34](#)

write journaling [2-26](#)

write sequence register [4-30](#), [4-31](#), [4-34](#)

Z

ZCR [2-28](#), [2-29](#), [3-16](#)

ZCR_EN/ [2-28](#), [3-16](#), [3-25](#), [5-6](#)

zero channel RAID [2-28](#), [2-29](#), [3-16](#)

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