TECHNICAL MANUAL

LSI53C040 Enclosure Services Processor

Version 2.7

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LSI LOGIC®

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This document describes the LSI Logic LSI53C040 Enclosure Services Processor and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This technical manual provides reference information on the LSI53C040 Enclosure Services Processor. It contains a complete functional description for the product and includes complete physical and electrical specifications for it.

Audience

This manual assumes some prior knowledge of current and proposed SCSI, Inter-Integrated Circuit, and SFF-8067 standards, including the SAF-TE and SES standards for parallel SCSI devices, as well as a detailed understanding of serial data communication. It is intended for system designers who are using this device to manage SCSI or Fibre Channel peripheral device enclosures.

Organization

This document has the following chapters and appendix:

- Chapter 1, **Introduction**, contains general information about the LSI53C040, including an overview of its features and functions.
- Chapter 2, **Functional Description**, describes the main functions of the chip in more detail, including the major interfaces.
- Chapter 3, **Signal Descriptions**, contains the pin diagrams and descriptions of each signal.
- Chapter 4, **SCSI and DMA Registers**
- Chapter 5, **SFF-8067 Registers**
- Chapter 6, **Two-Wire Serial Registers**
- Chapter 7, **Miscellaneous Registers**
- Chapter 8, **System Registers**

- Chapter 9, **Electrical Characteristics**, contains the operating conditions and AC timings for the chip and mechanical drawings.
- Appendix A, **Register Summary**

Related Publications

For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-199X (SCSI-2)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 397-7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2); X3.253 (*SCSI-3 Parallel Interface*); or NCITS 305-199x (*SCSI-3 Enclosure Services (SES) Specification* working draft)

SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification
This document can be downloaded from www.safte.org

LSI Logic World Wide Web Home Page
www.lsilogic.com

SFF-8067 Specification
ENDL Fax Access
(408) 741-1600 (call from a FAX machine)

Inter-Integrated Circuit Bus Specification
For general information about the Inter-Integrated Circuit bus, contact Philips Semiconductors at www.semiconductors.philips.com

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end in a "/."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

Revision Record

Page No.	Date	Remarks
all	April 1998	Initial Release
all	December 1998	Preliminary, Version 2.0
all	February 2000	Version 2.5
all	April 2001	Version 2.6. All product names changed from SYM to LSI. Updated DC electrical specifications and test conditions.
Front Cover, page ii, pages 9-25 and 9-26	June 2002	Version 2.7. Replaced PZ package mechanical drawing with P3 package mechanical drawing, pages 9-25 and 9-26.

Contents

Tables

Chapter 1
Introduction

This chapter provides general overview information on the LSI53C040 Enclosure Services Processor. The chapter contains the following sections:

1.1 LSI53C040 Overview

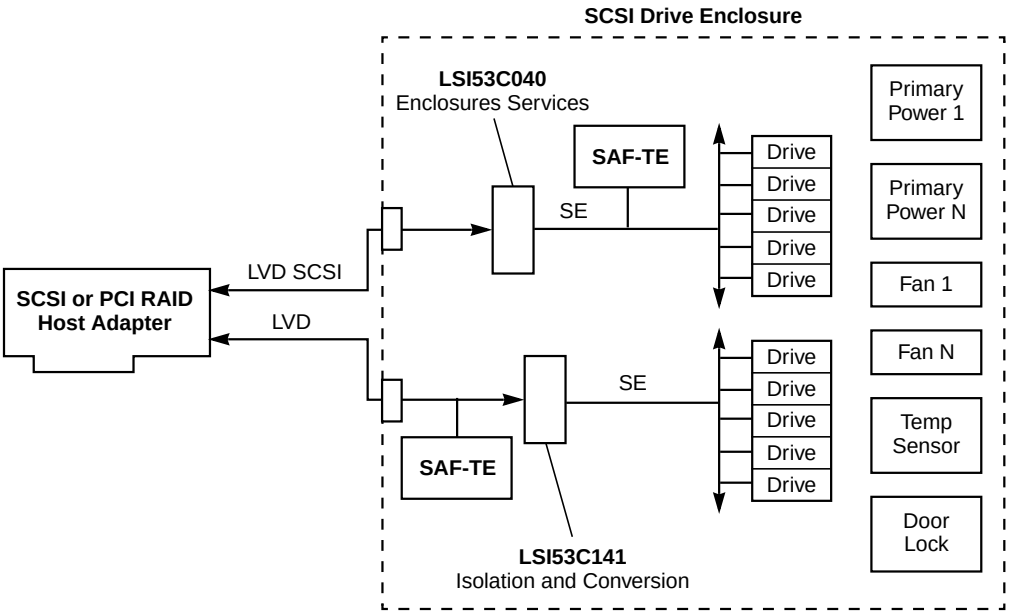
The LSI53C040 is an integrated Enclosure Services Processor (ESP) device that provides enclosure monitoring services for SCSI and Fibre Channel enclosures. It supports the SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) and SCSI-3 Enclosure Services (SES) enclosure specifications.

The enclosure monitoring services in the LSI53C040 allow a single chip solution for monitoring disk drives, power supplies, cooling systems, and other system services. Support for standard protocols such as SAF-TE and SES provide a nonproprietary way for third party disk and RAID controllers to be automatically integrated with peripheral enclosures that support status signals, hot swapping of hard drives, and monitoring of enclosure components. This decreases component cost and increases system reliability in distributed storage environments where status information on system resources, such as disk drives, must be available to multiple controllers. SCSI/SAF-TE Enclosure Implementation.

1.2 SCSI Mode

The LSI53C040 uses the SCSI bus to report system information such as enclosure temperature, power supply status, and disk slot status to the host SCSI controller. It also responds to host SCSI controller commands by generating control outputs to enable and disable disk slots, drive indicator displays, or perform other system tasks. The LSI53C040 supports Low Voltage Differential (LVD) access as well as Single-Ended (SE) SCSI access without the need for external transceivers. Figure 1.1 shows a typical SCSI enclosure implementation with the LSI53C040.

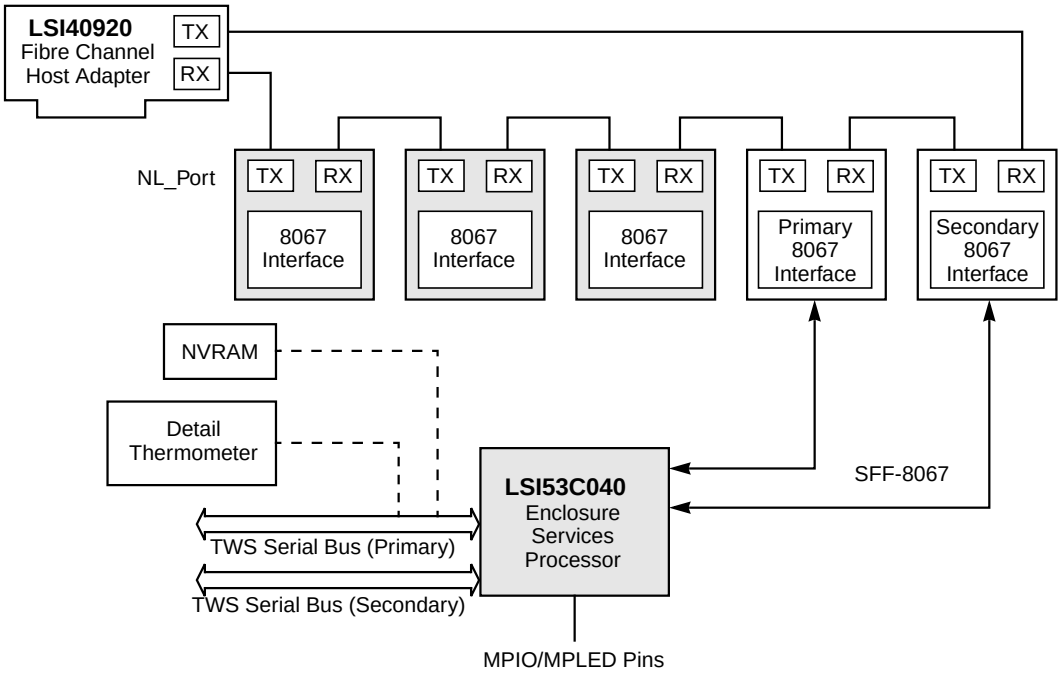
Figure 1.1 SCSI/SAF-TE Enclosure Implementation



1.3 SFF-8067 Mode

As an alternative to SCSI, the two SFF-8067 interfaces in the LSI53C040 allow it to communicate data between a Fibre Channel enclosure and the Fibre Channel host, using the SFF-8067 physical interface and the SES protocol to monitor the power supply, cooling system, and other alarms or status indicators in the enclosure. It also reports this information to the Fibre Channel host controller and generates control outputs to control system components, in response to host commands. Figure 1.2 shows a typical Fibre Channel enclosure design.

Figure 1.2 SFF-8067/SES Enclosure Implementation



1.4 Features Summary

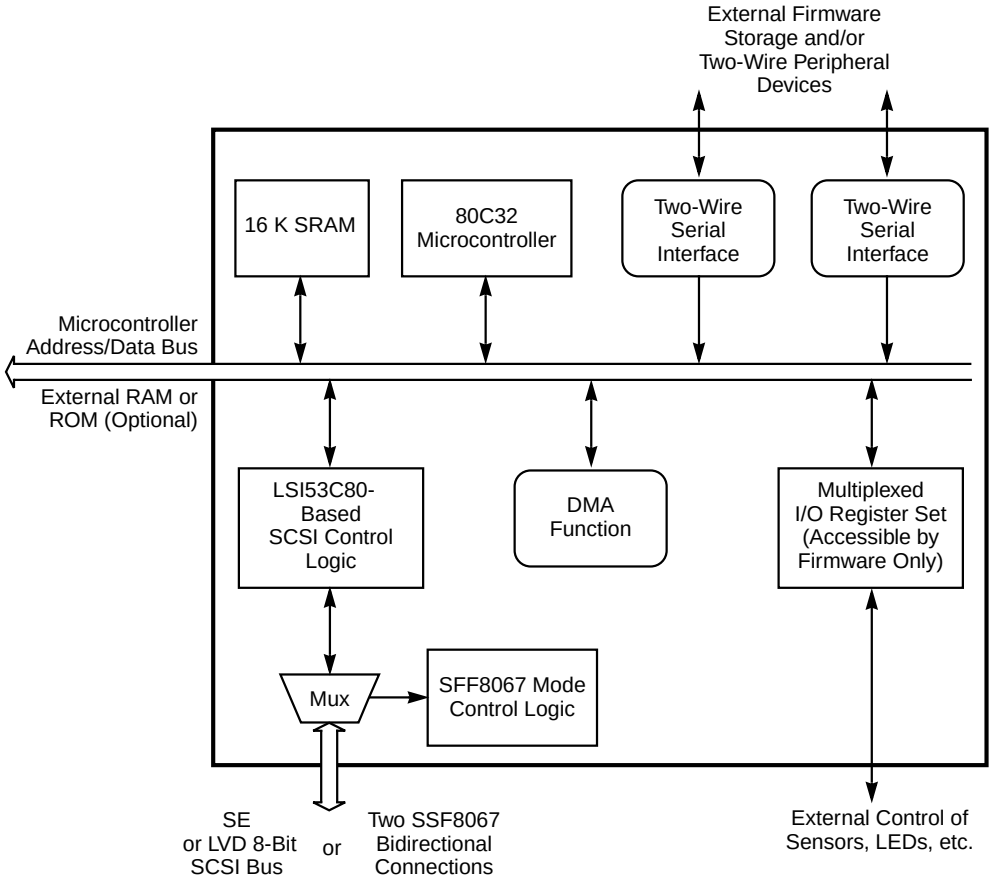
The following are the key features of the LSI53C040 as they relate to flexibility, integration, ease of use, reliability, and performance.

- Supports the SAF-TE protocol in SCSI environments, and the SES protocol in either SCSI or Fibre Channel environments
- Two SFF-8067 interfaces provided for Fibre Channel Enclosure applications
- 28 multipurpose I/O pins and 24 multipurpose LED drivers for flexible configurations
- Two programmable LED blink rates
- Watchdog timer with time-out values programmable between 20 ms and 300 ms
- Two on-chip timers external to the microcontroller
- Downloadable/upgradable firmware
- On-chip SE and LVD SCSI transceivers for direct attach to either LVD or SE SCSI bus
- 16 Kbytes of onboard static RAM
- Two multimaster, two-wire serial interfaces for automatic download of external firmware, and access to external two-wire serial peripherals
- Integrated 80C32 (MCS 51 compatible) microcontroller
- 160-pin QFP or 169-ball BGA packaging
- Two-wire serial interface for automatic download of external firmware
- Full featured SAF-TE firmware provided by LSI Logic
- Proven LSI53C80 core for basic SCSI protocol management
- 16 mA open drain LED drivers
- 5 Volt tolerant inputs (except DIFFSENS)
- IEEE 1149.1 JTAG compliant
- Hardware DMA function for increased SCSI throughput
- Support for 11 LVD SCSI IDs (0–7 plus three high IDs)

Chapter 2
Functional Description

This chapter describes the main functional blocks of the LSI53C040. Figure 2.1 is a high-level functional overview of the device, followed by a high-level description of each item. The remainder of the chapter describes these functional areas in more detail.

Figure 2.1 LSI53C040 Block Diagram



2.1 Functional Blocks

Following are brief descriptions of the main functional blocks comprising the LSI53C040.

2.1.1 LSI53C80-Based SCSI Control Logic

The SCSI core in the LSI53C040 is based on the LSI53C80 SCSI controller. The LSI53C80 is a first generation SCSI protocol controller that provides simple, register-based access to SCSI control and data signals. This core provides additional support for parity checking and a DMA function. It supports only asynchronous SCSI transfers. It supports both SE and LVD SCSI transfers. The LSI53C80 register set is mapped into the Internal Features register block as shown on the memory map in Figure 2.2. These registers are described in Chapter 4.

2.1.2 80C32 Microcontroller Core

The 80C32 microcontroller core used in the LSI53C040 is an 8-bit Intel MCS 51 family compatible device with 256 bytes of internal scratch RAM. This microcontroller uses a shared address/data bus and can address either 64 Kbytes of shared program and data memory or 16 Kbytes of internal memory and 47 Kbytes each of external program and data memory spaces. The microcontroller executes one instruction every 12 clocks. Additional functionality includes two 16-bit timers, a full-duplex UART, and two additional external interrupt sources (five interrupt sources total).

2.1.3 Two-Wire Serial Interface

The LSI53C040 has 2 Two-Wire Serial interface blocks that provide access to external serial EEPROM storage and any other user-defined, two-wire peripheral devices. The LSI53C040 can attempt to download from an external serial ROM through one interface at power-on or reset. External two-wire devices are connected to the SDA and SCL signal pins on the LSI53C040. The Two-Wire Serial interface blocks are controlled by a set of control registers in the Internal Features register block as shown on the memory map in Figure 2.2. These registers are described in Chapter 6.

2.1.4 SFF-8067 Interface

The two SFF-8067 interfaces allow the LSI53C040 to communicate with Fibre Channel SCA-2 devices to transfer SES information to/from Fibre Channel host controllers. The information is transferred across the signal pins used to provide the loop identifier to the SCSI device. Details of the protocol are provided in the SFF-8067 draft specification.

2.1.5 16 Kbytes SRAM

The LSI53C040 contains 16 Kbytes of internal static RAM for data and firmware storage. Under microcontroller control, the internal RAM may be loaded with additional firmware from an external parallel ROM, or automatically from a serial EEPROM using the Two-Wire Serial interface.

Note: The external parallel ROM must not be mapped into the first 16 Kbytes or the last 1 Kbyte of the external memory.

2.1.6 DMA Function

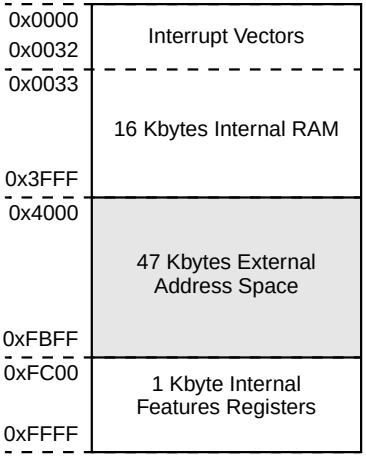
The DMA block provides memory access from and to the SCSI core. During DMA operations, the microcontroller is put in an idle state and the internal bus is driven by the DMA block. External memory access by the DMA block happens in the same way that microcontroller memory accesses occur. Control of the DMA block is achieved through a set of control registers shown on the memory map in Figure 2.2 and is described in Chapter 4.

2.2 Memory Map

All memory accesses are visible on the external microcontroller memory bus. Figure 2.2 is the memory map of the LSI53C040.

Note: It is the responsibility of the system designer to prevent other external devices from conflicting with internal memory options.

Figure 2.2 LSI53C040 Memory Map



The address decode block in the LSI53C040 decodes addresses generated by the microcontroller and multiplexes memory space accesses between the different register and memory blocks according to the memory map.

2.3 SCSI Core Operation

The LSI53C040 uses a SCSI core based on the LSI53C80 first generation SCSI architecture. The LSI53C80 architecture supports 8-bit, asynchronous only SCSI data transfers. It supports both SE and LVD SCSI transfers. The core contains support for parity generation and checking, initiator and target operation, arbitration, and interrupts to the microcontroller. The core is controlled by several registers that are described in Chapter 4.

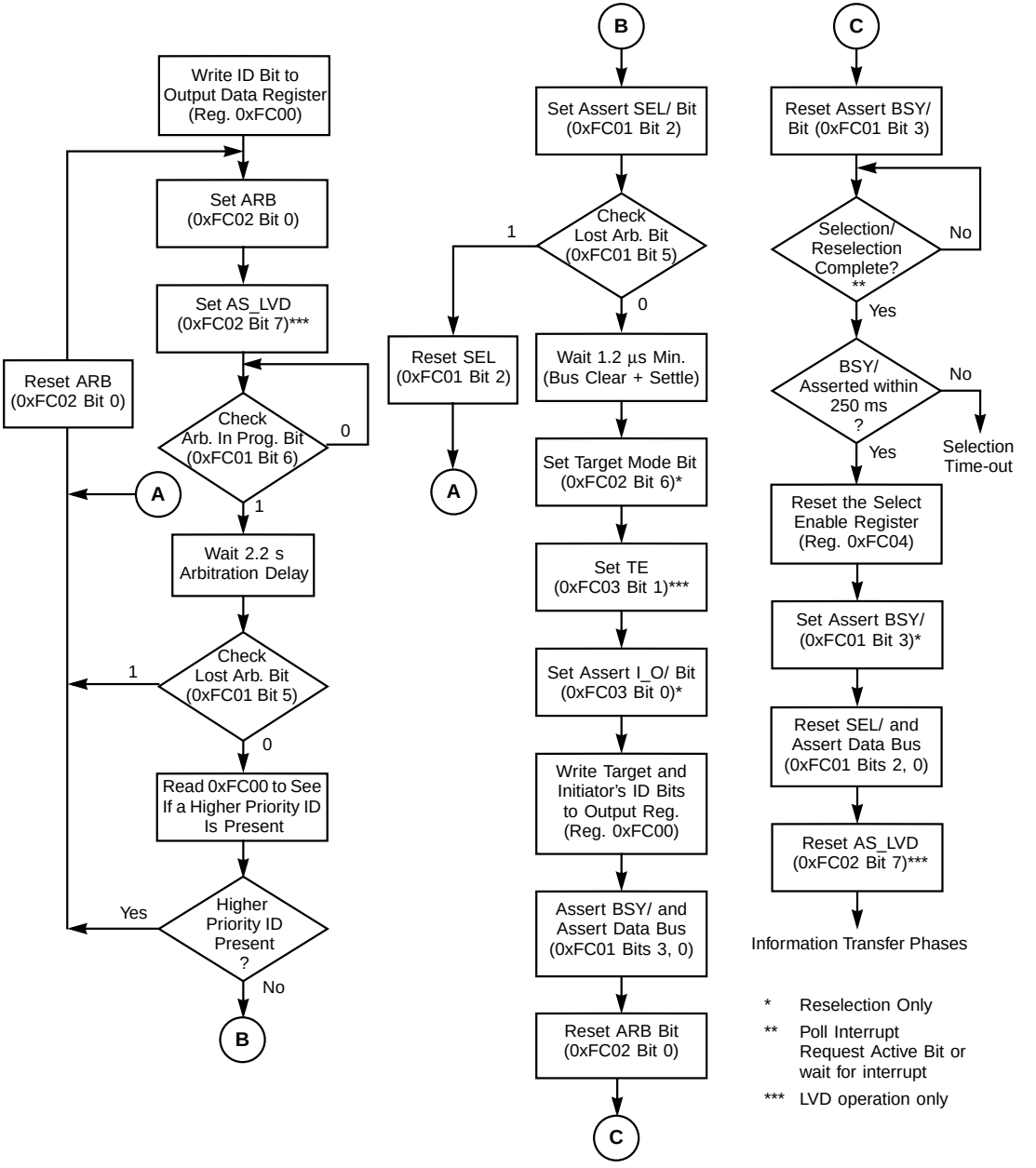
2.3.1 Recommended Use of SCSI High ID Pins

The SCSI core in the LSI53C040 is designed for 8-bit SCSI applications only. However, the LSI53C040 contains some additional logic that allows the device to have three SCSI high IDs, in addition to 0–7, so that the LSI53C040 can be given lower priority on a wide SCSI bus. However, the LSI53C040 cannot perform selection or reselection on a wide bus; parity

checking during the selection/reselection phase may be in error and should not be monitored. This limits the LSI53C040 to only target applications, with no disconnects, on a wide bus.

To select a high ID for the LSI53C040, connect any of the SCSI high data lines (8–15) to one of the SHID[2:0] pins. The user can monitor the value of the SHID[2:0] pins by reading the SHID[2:0] bits in the Current SCSI Data High (CSDHI) register (0xFC08). The Select Enable High (SENHI) register allows a bit to be set that corresponds to the device SCSI ID. This allows an interrupt to be generated if the corresponding data line is driven during selection, if the data line is connected to the appropriate SHIDx pin. Figure 2.3 on page 2-7 illustrates SCSI arbitration and selection/reselection and DMA target transfers.

Figure 2.3 Initiating Arbitration and Selection/Reselection



2.3.2 LVDlink™ Technology

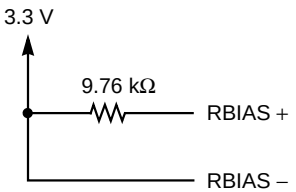
To support greater device connectivity and a longer SCSI cable, the LSI53C040 includes LVDlink technology, the LSI Logic implementation of LVD SCSI. LVDlink transceivers provide the inherent reliability of differential SCSI, and a long-term migration path for faster SCSI transfer rates.

LVDlink technology is based on current drive; its low output current reduces the power needed to drive the SCSI bus, so that the I/O drivers can be integrated directly onto the chip. This reduces cost and complexity compared to high-power differential designs. LVDlink lowers the amplitude of noise reflections and allows higher transmission frequencies.

The LSI Logic LVDlink transceivers operate in LVD and SE modes. The LSI53C040 automatically detects which type of signal is connected, based on voltage detected by the DIFFSENS pin.

The RBIAS+ and RBIAS– signals are the bias resistors for LVD operation. A resistor value of 9.76 kΩ, ± 1%, is recommended, as illustrated in Figure 2.4.

Figure 2.4 LVD Resistor Value



2.3.3 Programmed I/O Transfers

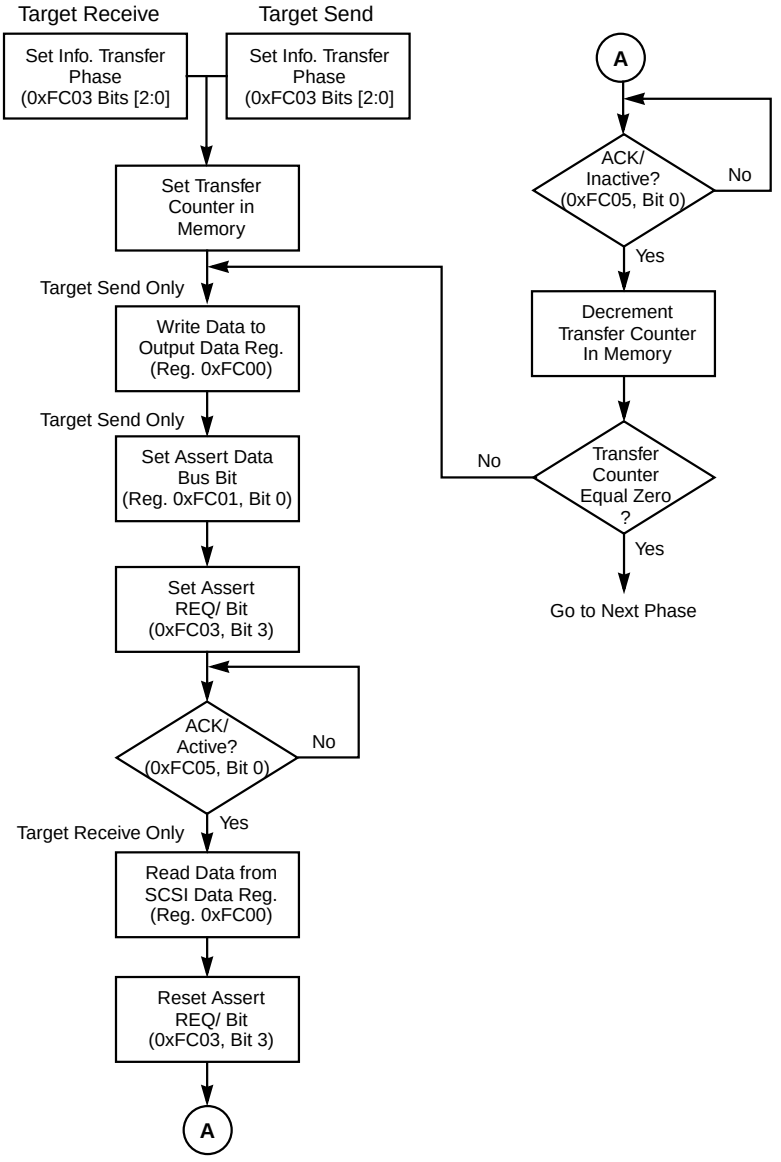
Programmed I/O is the most primitive form of data transfer. The REQ/ and ACK/ handshake signals are individually monitored and asserted by reading and writing the appropriate register bits. This type of transfer is normally used when transferring small blocks of data such as command blocks or message and status bytes. Figure 2.5 illustrates a programmed I/O transfer.

A Target Send operation begins when the ACD (Assert C_D/), AIO (Assert I_O/), and AMSG (Assert MSG/) bits in the Target Command (TC) register are set to the correct state so that a phase match exists. In addition to the phase match condition, the Assert Data Bus bit (bit 0 in register 0xFC01) must be set and the I/O signals must be deasserted for the SCSI core to send data.

For each transfer, the data is loaded into the Output Data (ODR) register (0xFC00) and the Assert REQ/ bit (0xFC03, bit 3) is set. The microcontroller must then wait for the REQ/ bit (0xFC04, bit 5) to become active. Once REQ/ goes active, the Phase Match bit (0xFC05, bit 3) is checked and the Assert ACK/ bit (0xFC01, bit 4) is set. The REQ/ bit is sampled until it becomes false and the microcontroller resets the Assert ACK/ bit to complete the transfer.

In addition to target send, programmed I/O transfers can also be used for target receive, initiator send, and initiator receive operations. Figure 2.5 illustrates target send and receive operations.

Figure 2.5 Programmed I/O Target Transfers



2.3.4 SCSI - DMA Transfers

In the LSI53C040, DMA handshaking with the SCSI core is handled automatically by the DMA function. In order to initiate a DMA transfer to the SCSI core using the DMA function in the LSI53C040, the following sequence must be performed:

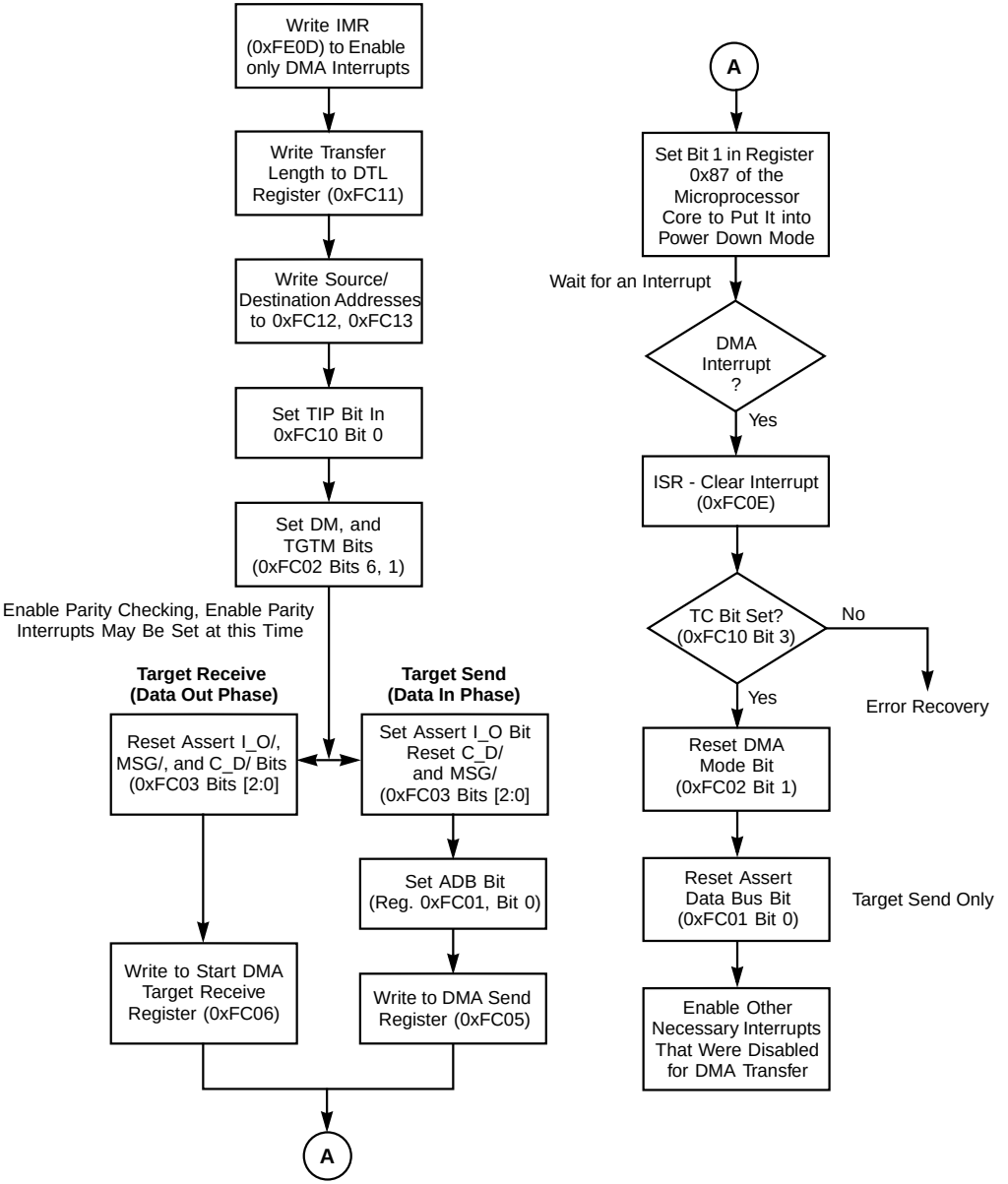
1. The DMA Transfer Length (DTL) register and the DMA Source/Destination Low (DSDL) and DMA Source/Destination High (DSDH) address registers (0xFC11–0xFC13) must be written.
2. The DMA Status (DS) register (0xFC10) is written with a 1 in the bit 0 (TIP) position.
3. The firmware sets bit 0 in register 0x87 of the microcontroller core to place the core in idle mode.
4. The DMA waits for the microcontroller to enter the idle mode before taking over the internal bus for memory reads or writes.
5. Once the DMA receives a request from the SCSI core, the transfer begins.

Figure 2.6 illustrates a target mode DMA transfer.

2.3.4.1 Halting a DMA Operation

Any SCSI or DMA interrupt, if enabled in the Interrupt Mask (IMR) register, terminates the DMA cycle for the current bus phase. It is recommended that the DMA Mode bit be reset after receiving an interrupt. The DMA Mode bit must be set before writing any of the Start DMA registers for subsequent bus phases.

Figure 2.6 DMA Target Mode Transfers



2.4 DMA Function

The LSI53C040 DMA function is designed to automatically handshake with the SCSI core for SCSI send and receive operations. For SCSI send operations, the DMA reads a byte from memory and writes it to the SCSI core when requested. For receive operations, the DMA receives a byte from the SCSI core and writes it to memory.

After setting up the transfer length and source/destination addresses, a DMA operation begins with the microcontroller setting the TIP bit in the DMA Status (DS) register. Next, the firmware sets bit 1 in register 0x87 of the microcontroller core to place the core into idle mode while the DMA waits for the microcontroller to halt. With the microcontroller halted, the DMA has control of the internal bus. For a send, the DMA first reads a byte of data from internal or external memory. After each byte transfer, the DMA Transfer Length (DTL) register will be decremented and the address register incremented.

Note: The entire address, which is a combination of two byte-wide registers, will be incremented.

This cycle repeats until the transfer length is zero, which indicates the last byte is being transferred.

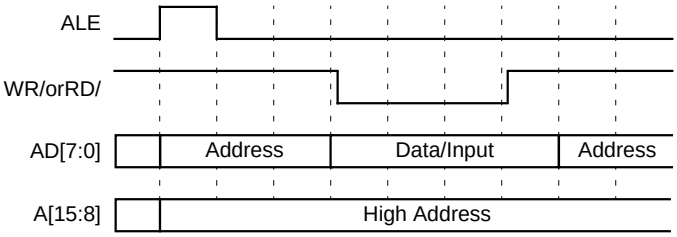
A DMA receive operation happens in much the same way. This data byte is written to the memory address pointed to by the DMA address registers. Finally, the DMA Transfer Length (DTL) register is decremented and the address pointer register is incremented.

This cycle repeats until the transfer length is zero. This indicates the last byte is being transferred.

If any interrupt not masked in the Interrupt Mask (IMR) register is generated during a DMA transfer, the microcontroller will come out of idle mode and the DMA transfer will be halted. The DMA address pointer and transfer length registers will not be cleared, so that the microcontroller can determine at what point the transfer was interrupted.

During DMA transfers, the DMA block controls the internal bus and the pins that bring these signals out to external memory. External memory accesses function as illustrated in Figure 2.7.

Figure 2.7 DMA External Memory Access



2.5 Microcontroller Operation

The 80C32 microcontroller core used in the LSI53C040 is an 8-bit Intel MCS 51 family compatible device with 256 bytes of internal scratch RAM and no internal ROM. This microcontroller uses a shared address/data bus and can address either 64 Kbytes of shared program and data memory or 16 Kbytes of internal memory and 47 Kbytes each of external program and data memory spaces. The microcontroller executes one instruction every 12 clocks. Additional functionality includes two 16-bit timers, a full-duplex UART, and two additional external interrupt sources (five interrupt sources total).

For more information on the operation of the microcontroller core, refer to documentation on the Intel MCS 51 embedded microcontroller family.

The microcontroller core has two external interrupt functions as well as the TXD and RXD serial port functions. The user can access these functions on the microcontroller core by setting the External Interrupt Enable and Serial Port Enable bits in the System Control (SYSCTRL) register (0xFF05).

2.5.1 ONCE Mode

ONCE mode is available for use as in any standard Intel 80C32 microcontroller. However, the DMA feature cannot be used when the microcontroller is in ONCE mode. This is because the DMA logic inside the LSI53C040 looks for a signal from the microcontroller to indicate that it is halted before beginning any DMA operation. ONCE mode does not provide this signal to the DMA logic.

To enter ONCE mode, hold ALE low while bringing RESET/ to low, then releasing it to high. ONCE mode should be used for testing or diagnostic purposes only, and should be disabled during normal chip operation.

2.6 Two-Wire Serial Interface Operation

The Two-Wire Serial interface performs two main functions: it automatically downloads firmware from an external serial EEPROM device, and it serves as a Two-Wire Serial port with full multimaster and slave capability that can communicate with external Two-Wire Serial devices. The Two-Wire Serial interface in the LSI53C040 provides the microcontroller an additional means to gather external system information. The Two-Wire Serial interface supported by the LSI53C040 is compliant with the Inter-Integrated Circuit bus defined by Philips Electronics. Figure 2.8 illustrates serial bus activity during a read operation. Figure 2.9 illustrates serial bus activity during a write operation.

Figure 2.8 Serial Read Operation

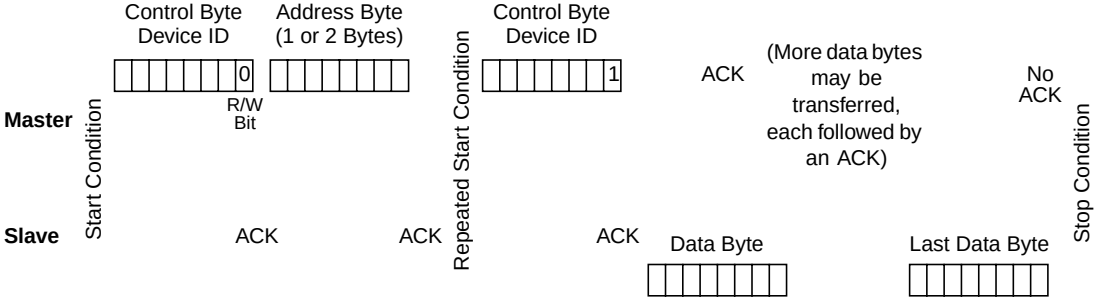
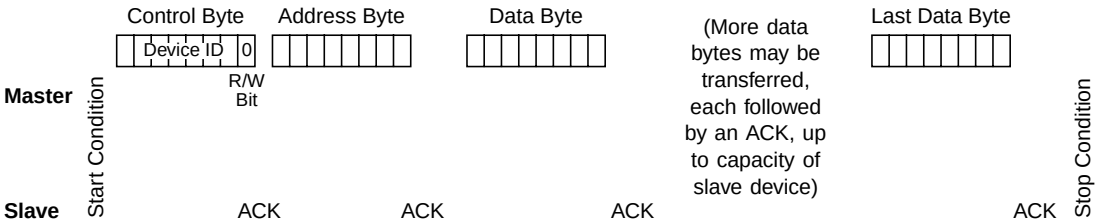


Figure 2.9 Serial Write Operation



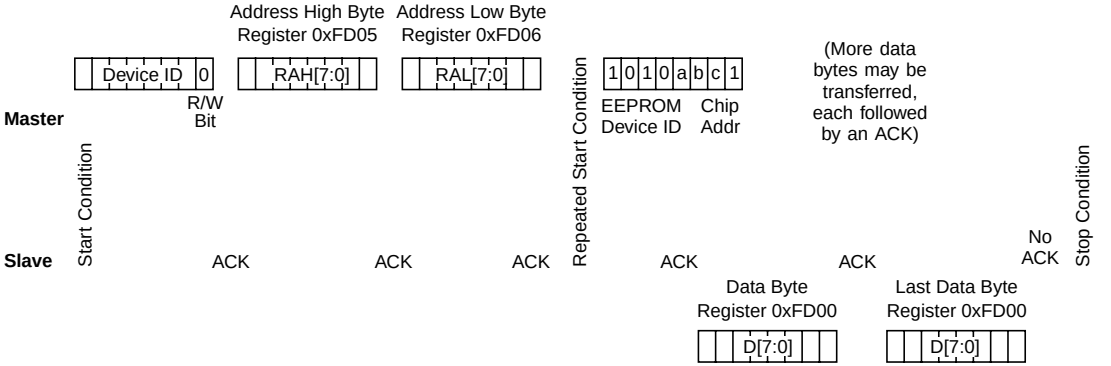
2.6.1 Two-Wire Serial Interface Transfer Rate

The Two-Wire Serial interface performs all initial downloads at a 78.125 kHz SCL clock rate (with a 40 MHz system clock). At 78.125 kHz, an entire 64 Kbit (8 Kbit x 8) serial EEPROM device can be downloaded in under 945 ms. Other SCL clock rates can be achieved by programming the Clock (ES0, ES1, ES2 = 010) register (0xFD00/0xFD02). See Chapter 6 for more information on the Clock register in the Two-Wire Serial register block.

2.6.2 Power-On Serial ROM Download

At power-on, the Two-Wire Serial interface in the LSI53C040 attempts to read from a serial EEPROM with slave address 0b1010, and a chip address defined at power-on through the use of external pull-up/pull-down options on signal pins A10, A9, and A8. These options are summarized in Table 2.4. The initial download attempt can also be skipped if no pull-up resistor is used on signal pin AD5. Signal pin A11 indicates which serial interface will perform the initial download if the AD5 signal is high. A low on pin A11 indicates the download will occur through serial port 0 while a high indicates the download will occur through serial port 1. If an initial serial ROM download is attempted, the microcontroller core will be delayed in fetching its first instruction until the download has completed, so that firmware downloaded from the serial ROM can be executed first if desired. Table 2.1 lists the contents of the initial ROM download to the LSI53C040. Figure 2.10 illustrates a typical download sequence. The device ID to download from is 1010abc. The 0b1010 denotes a ROM device, and the “abc” value is the serial ROM chip address, determined by the configuration of the A[10:8] pins as presented in Table 2.4.

Figure 2.10 Serial ROM Download



On a power-on reset or on a soft-chip reset (watchdog timer expires or the RESET/ pin toggles), the download logic will download data beginning at address 0x00 of the two-wire slave ROM device.

Table 2.1 Initial ROM Download Contents

Byte	Contents
0	Destination address low
1	Destination address high
2	Firmware length (n) low (includes checksum byte but not destination address bytes)
3	Firmware length (n) high
4 through n + 2	Firmware
n + 3	Checksum for firmware (up to maximum supported ROM size)

2.6.3 Address and Length Download Configuration

The first four bytes read from the two-wire external ROM contain the download destination address and the number of bytes to be downloaded. The first byte is the destination address low byte. The second byte is the destination address high byte. The third byte is the firmware length low byte, and the fourth byte is the firmware length high byte. The firmware length is the number of bytes of code not including the two bytes of destination address, or the two bytes of firmware length. The length does include the final checksum byte. The minimum firmware length is three bytes.

2.6.4 Firmware Download and Checksum

The first step in the download is to read in the destination address and firmware length. Then the firmware will be read in and written out starting at the destination address. Each byte is bit wise XORed with the previous checksum, starting with zeros. The final byte read is the checksum value. This byte is compared to the calculated checksum. Bit 0 of the Miscellaneous register (0xFD04) indicates a checksum error. If this bit is high after download, there was a difference between the calculated checksum and the last byte read in at download.

2.6.5 Manually Accessing External Two-Wire Serial Devices

The LSI53C040 Two-Wire Serial interface allows the microcontroller core to manually access external two-wire devices such as temperature sensors, A/D converters, memory devices or any other I/O device that adheres to the standard Two-Wire Serial protocol. The LSI53C040 Two-Wire Serial interface always performs single byte read and write operations when accessed through the register interface, so it is not intended for maximum throughput with large blocks of data. Figure 2.11 and Figure 2.12 are flowcharts of LSI53C040 serial transmit and receive operations.

Figure 2.11 Two-Wire Serial Slave Data Transmit and Receive

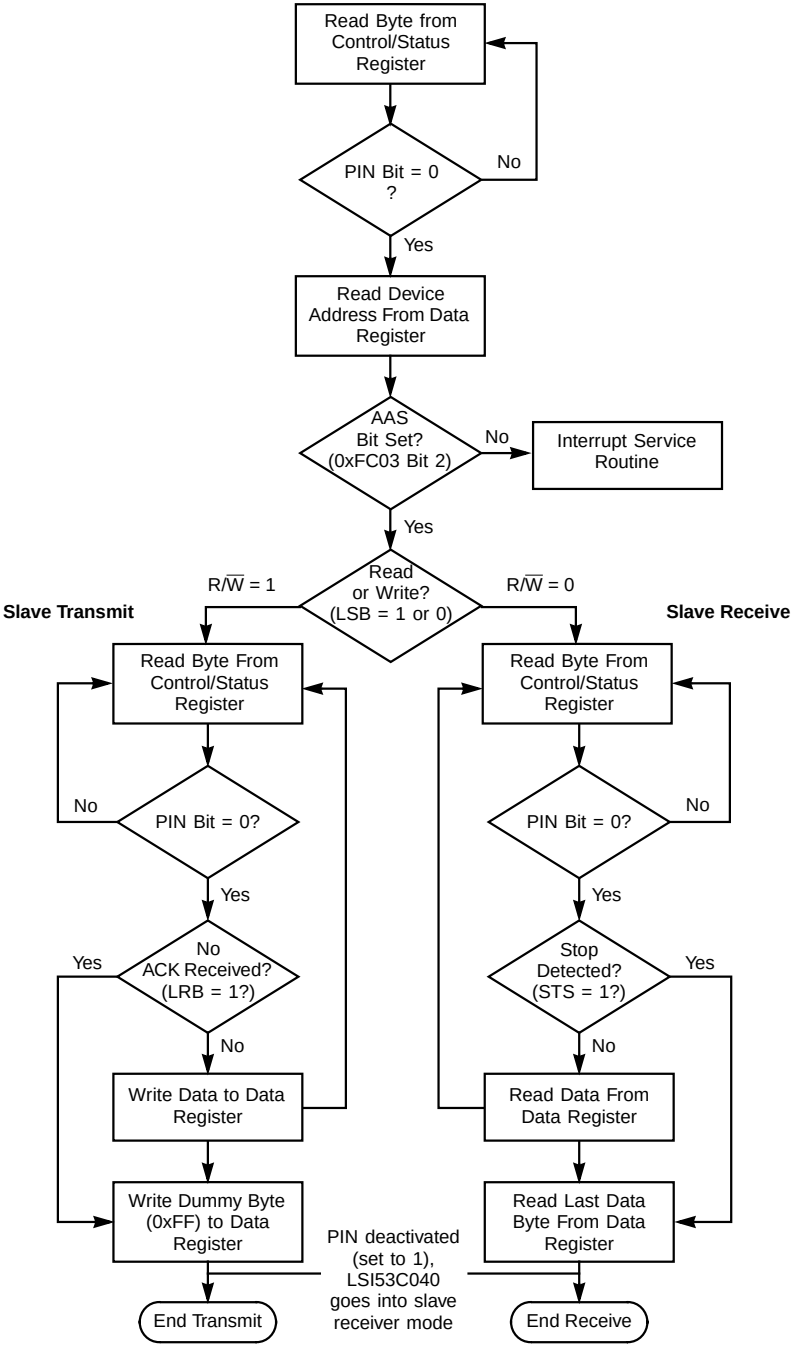
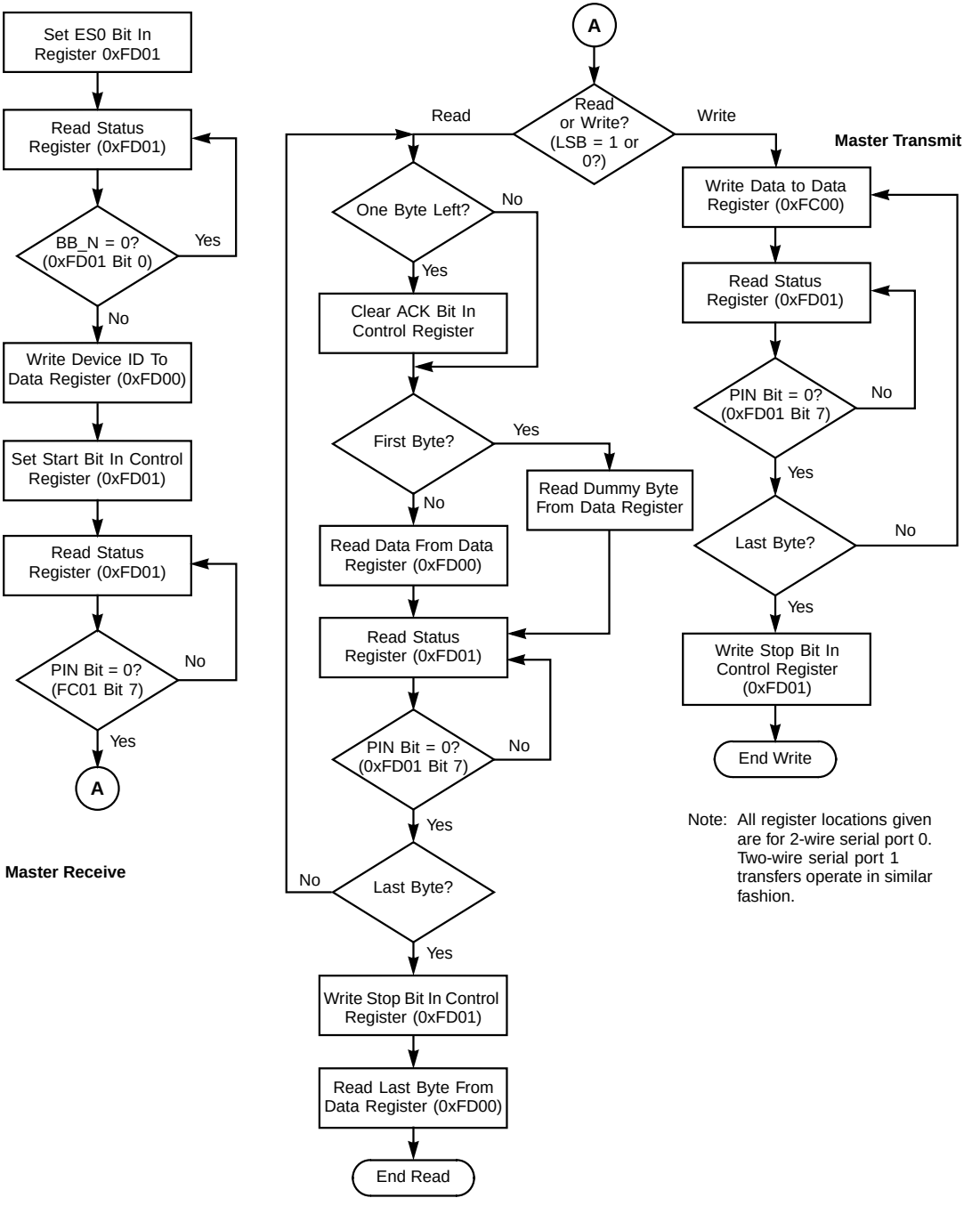


Figure 2.12 Two-Wire Serial Master Data Transmit and Receive



Note: All register locations given are for 2-wire serial port 0. Two-wire serial port 1 transfers operate in similar fashion.

2.7 Power-On Configuration Options

The power-on configuration of the LSI53C040 can be customized for different applications using the AD5, AD[1:0], and A[11:8] pins. Table 2.2 summarizes the functionality that is enabled or disabled by using pull-up resistors on these pins.

Table 2.2 Power-On Configuration Pins and Options[1]

Signal Name	Function	Pull-up Use
AD[1:0]	Automatic branch generation	See Table 2.3.
AD5	Serial ROM automatic download	Enable with external pull-up.
A[10:8]	Download configuration address	See Table 2.4.
A11[2]	Download serial port select	Pull-up resistor changes serial ROM download from Two-Wire Serial port 0 to port 1.

1. The values of these pins are latched into the Power-On Configuration Registers (System registers 0xFF01, 0xFF03).

2.7.1 Automatic Branch Generation

At reset, the microcontroller core fetches its first instruction from address 0x0000. Because the interrupt vectors are mapped to locations 0x0003 through 0x0032, an unconditional jump instruction must be issued as the first instruction fetched from address 0x0000. The LSI53C040 address decode logic automatically generates this jump instruction when the microcontroller core accesses address locations 0x0000 through 0x0002 during its initial instruction fetch, if automatic branch generation is enabled. Three address destinations are possible for this initial automatic jump, configurable by external pull-up resistors on the AD0 and AD1 pins. The states of these pins are checked on chip reset. In the LSI53C040, the AD0 and AD1 signal pins have internal pull-down resistors, so these pins power-up deasserted if no external pull-up is used. They power-up asserted with an external pull-up resistor. If an external pull-up resistor is detected on either of these pins, the internal pull-down resistor will be disabled to reduce power dissipation. The destination of the first instruction jump is determined by the power-on values of the AD0 and AD1 pins, as described in Table 2.3.

Table 2.3 External Pull-up Values for Automatic Branch Generation

External Pull-up on AD1/AD0	First Instruction Branch Destination
Pull-up/Pull-up	0x8000
Pull-up/None	0x4000
None/Pull-up	0x0033
None/None	Fetched from 0x0000

Address locations 0x0033 and 0x0000 correspond to the internal RAM. Address locations 0x8000 and 0x4000 correspond to external memory accesses. Using no external pull-up resistors on AD0 and AD1 disables the automatic branch instruction generation, and the microcontroller fetches its first instruction from address 0x0000. If automatic branch generation is disabled, a branch instruction must be downloaded into address 0x0000, using an external serial ROM. The power-on setting of AD0 and AD1 can be read in the Power-On Configuration Zero (POC0) register (0xFF01) bits 0 and 1, respectively.

2.7.2 External Serial ROM Configuration

The LSI53C040 can attempt to download firmware from a serial ROM at power-on, through the Two-Wire Serial interface. The serial ROM download is performed immediately at power-on or after a reset, and the microcontroller will hold off from fetching its first instruction until the download completes.

The initial ROM download will be skipped if no external pull-up is used on the AD5 signal pin (the pin has an internal pull-down). If a pull-up is detected on the AD5 signal pin, the download will be attempted and the internal pull-down will be disabled to reduce power dissipation.

2.7.3 Serial ROM Chip Address

The chip address of the serial ROM to be used in the power-on download can be defined by using pull-up resistors on the A8, A9, and A10 signal pins. There are eight possible chip addresses for most popular Two-Wire Serial EEPROM devices. Table 2.4 describes the address of the serial EEPROM device from which the LSI53C040 will attempt the initial

configuration download, based on the values of the A[10:8] signal pins. As indicated in the table, the serial ROM chip address mapping is equivalent to the power-on value of signal pins A[10:8].

Table 2.4 Serial ROM Chip Addresses

Serial ROM Chip Address	AD10 Pull-up	AD9 Pull-up	AD8 Pull-up
1010 000	None	None	None
1010 001	None	None	Pull-up
1010 010	None	Pull-up	None
1010 011	None	Pull-up	Pull-up
1010 100	Pull-up	None	None
1010 101	Pull-up	None	Pull-up
1010 110	Pull-up	Pull-up	None
1010 111	Pull-up	Pull-up	Pull-up

2.7.4 Download Port Select

The A11 pin selects which of the Two-Wire Serial interfaces will perform the initial download. The default for the download is Two-Wire Serial port 0. A pull-up resistor on the A11 pin starts the download from Two-Wire Serial port 1, after a reset or at power-on.

2.8 Resets

The LSI53C040 can be reset in three different ways: power-on reset, asserting the reset pin, and an internal chip reset forced by expiration of the watchdog timer. A power-on reset initializes all chip registers to their default values and returns the Two-Wire Serial port and the SCSI or SFF-8067 interfaces to idle states. A power-on reset is caused when power to the chip has been turned off and is turned back on. Manually asserting the RESET/ pin triggers a soft reset. This can be done to initiate a second configuration ROM download for the purpose of adding more firmware or changing default register values before the chip begins normal operation.

If the watchdog timer is used and it expires, it causes an internal soft reset. If the Enable Reset Output bit is also set (0xFF05, bit 7), the RESET/ pin is asserted low (0) to reset external devices. The Watchdog Reboot bit is set (0xFE00, bit 7) to indicate that the LSI53C040 has performed a soft reset due to expiration of the watchdog timer. Not all register values in the LSI53C040 are affected by a soft reset. The following bits/registers require a power-on reset to return to their default values:

- 0xFE00, Watchdog Timer Control (WDTC)
- 0xFE02, Watchdog Final Chain (WDFC)
- 0xFF03, Power-On Configuration One (POC1)
- Bit 7, Enable Reset Output, in register 0xFF05, System Control (SYSCTRL)

2.9 SFF-8067 Mode

The two SFF-8067 interfaces allow the LSI53C040 to communicate with Fibre Channel SCA-2 devices. Details of the protocol are provided in the SFF-8067 specification.

The SFF-8067 port 0 and port 1 interfaces can be controlled either manually by the microcontroller through direct control of the interface pins; or automatically by the SFF-8067 interface control logic, which has the ability to interrupt the microcontroller when input data has been received over one of the ports or when output data has been requested at one of the ports.

The SFF-8067 interface is enabled when the DIFFSENS pin is set to V_{DD}. The SCSI pins are reassigned to SFF-8067 pins, as indicated in Chapter 3.

A simple ping-pong arbitration scheme provides equal priority access between the two ports, since only one of them can be active at a time. A drive requests access to the LSI53C040 by asserting the PARALLEL ESI/ pin on its respective port. If the other port is not being used, the Discovery and Data Transfer phases can proceed as described in the

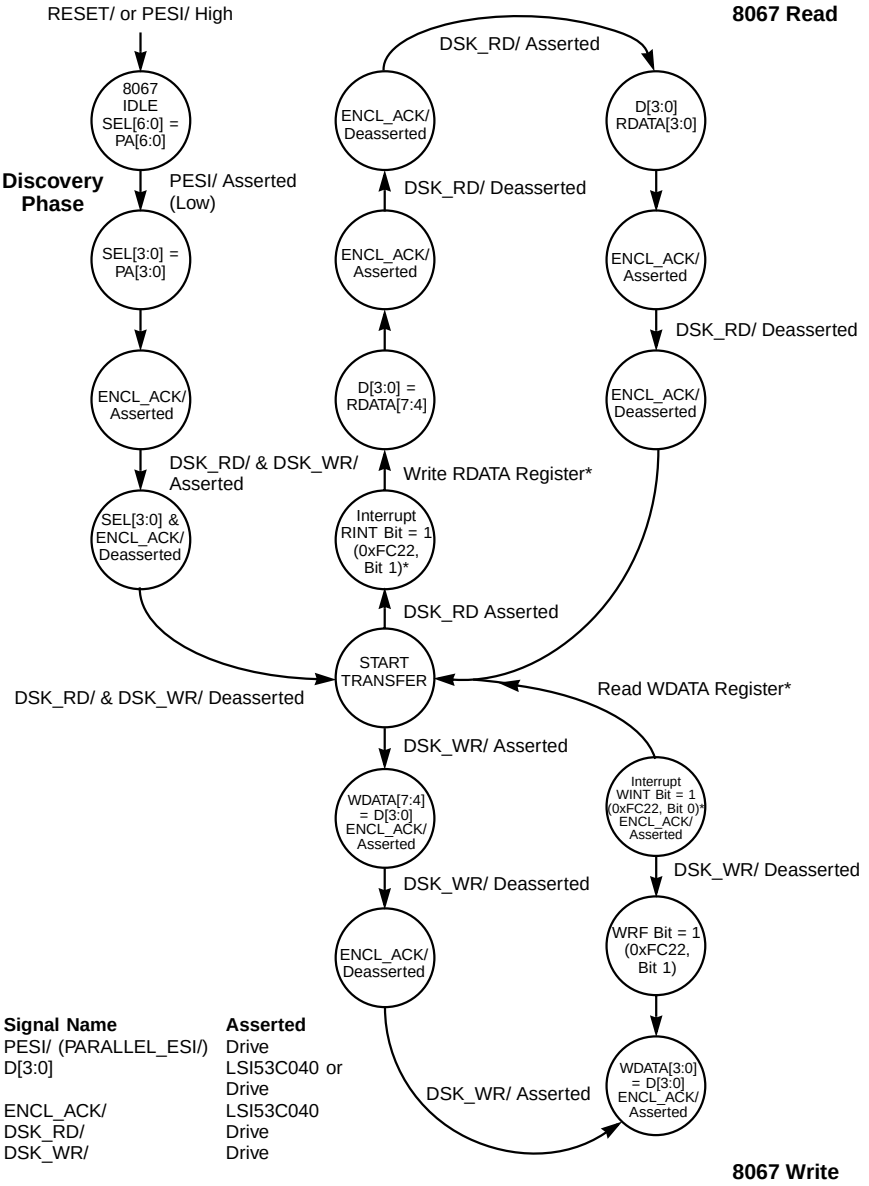
SFF-8067 specification. A request for access of the other port will not be acknowledged until the PARALLEL ESI/ pin is deasserted on the port that is currently in use.

Interrupts notify the microcontroller of port access. The Read interrupt notifies the microcontroller that the Fibre Channel device is requesting data. The microcontroller responds by clearing the interrupt and writing one byte of data to the RDATA register which will then be transferred to the requesting Fibre Channel device. The write interrupt notifies the microcontroller that the Fibre Channel device has written a byte of data to the interface. The microcontroller responds by clearing the interrupt and reading the WDATA register. The LSI53C040 SFF-8067 interface control is illustrated in a state diagram in Figure 2.13.

Port access is terminated when the PARALLEL ESI/ pin is deasserted. If the PARALLEL ESI/ pin of the other port is asserted at that time it will be granted access.

Refer to Chapter 5 for SFF-8067 interface register descriptions.

Figure 2.13 LSI53C040 SFF-8067 Interface Control State Diagram



Signal Name	Asserted
PESI/ (PARALLEL_ESI/)	Drive
D[3:0]	LSI53C040 or Drive
ENCL_ACK/	LSI53C040
DSK_RD/	Drive
DSK_WR/	Drive

*Items marked with an asterisk require action by the firmware. All other activities are part of standard SFF-8067 interface operation.

2.10 Interrupts

The LSI53C040 supports the following type of interrupts:

- Microcontroller
- DMA and SCSI
- SFF-8067
- Two-Wire Serial
- Masking and Enabling
- Polling and Hardware

2.10.1 Microcontroller Interrupts

The microcontroller core has two interrupt inputs through which interrupt requests are presented. The SCSI core, DMA core, the Two-Wire Serial cores, the two timers, the two SFF-8067 ports, and the two external interrupt ports all generate interrupts that can be individually routed to either of the two internal interrupt ports of the microcontroller core. The MPIO3_[1:0] pins are used as the external interrupt lines. Refer to these pin descriptions for additional information. The Interrupt Status (ISR) register (0xFE04), allows the LSI53C040 to quickly determine the source of an interrupt. The Interrupt Mask (IMR) register (0xFE0D), allows the corresponding interrupts in the ISR to be masked by writing a 0 to the bit location. All interrupts are disabled by default. The Interrupt Destination (IDR) register (0xFE0E), allows the corresponding interrupts of the ISR to be routed to either of the two interrupt inputs of the microcontroller core.

During DMA operation, the Two-Wire Serial interrupts and the Timer 2 interrupts should be masked from the microcontroller core so it will not be interrupted until the DMA transfer is complete or interrupted by the SCSI core or Timer 1. Other interrupts can also bring the microcontroller core out of idle mode, but only if they occur during the DMA operation. Table 2.5 summarizes the primary registers and bits that are used in detecting and handling interrupts. The DMA core will pass any SCSI interrupt along to the microcontroller.

Table 2.5 Register Bits for Interrupt Handling

Register Bit Location	Register or Bit Name	Function
0xFE04	Interrupt Status	Reports to the microcontroller which block asserted the interrupt. Individual bits in this register may be written to force an interrupt on the corresponding bit. Refer to the register description for complete information.
0xFE0D	Interrupt Mask	Clearing individual bits in this register masks the corresponding interrupts in the Interrupt Status (ISR) register from being sent to the microcontroller.
0xFE0E	Interrupt Destination	The bits in this register can be set or cleared to route interrupts to either of the two interrupt sources to the microcontroller core.
0xFC05, bit 7	End of DMA Transfer	This bit is set when the DMA transfer is complete.
0xFC02, bit 4	Enable Parity Interrupt	When set, causes an interrupt from the SCSI core to occur if a parity error is detected. The Enable Parity Checking bit must also be set.
0xFC02, bit 2	Monitor Busy	When set, causes an interrupt from the SCSI core to be generated for an unexpected loss of BSY/.
0xFC07 (Read register)	Reset Parity/Interrupt Register	Any read to this register resets the Interrupt Request Active bit (0xFC05, bit 4).
0xFC10, bit 1	DMA Interrupt Enable	When set, the DMA function will generate an interrupt whenever the TIP bit (bit 0) transitions from 1 to 0. This signifies that the transfer completed normally, or was interrupted.
0xFC14, bit 0	DMA Interrupt	This is the interrupt value for the DMA function. This interrupt will only be enabled if the IEN bit (bit 1 in register 0xFC10) is set.

2.10.1.1 Interrupt Status Register (0xFE04)

The bits in this register are set when the corresponding interrupt condition occurs. They are cleared when the interrupt is cleared by the microcontroller. The register contains interrupt bits for the two SFF-8067 ports or MPIO3_[1:0]; the two programmable timers; the DMA core; the Two-Wire Serial interfaces; and the SCSI core.

2.10.1.2 Interrupt Mask Register (0xFE0D)

Clearing the bits in this register masks the interrupts corresponding to the bits in the Interrupt Status (ISR) register.

2.10.1.3 Interrupt Destination Register (0xFE0E)

This register provides the ability to route an interrupt to either of the two external interrupt inputs of the microcontroller core. The bits correspond to the interrupts in the Interrupt Status (ISR) register. Clearing the bit routes the interrupt to external interrupt 0, and setting the bit routes it to external interrupt 1.

2.10.2 DMA and SCSI Interrupts

The SCSI core provides an interrupt output to indicate task completion or an abnormal bus occurrence. The use of interrupts is optional and may be disabled by resetting the appropriate bits in the Mode (MR) register (0xFC02) or the Select Enable (SER) register (0xFC04).

When an interrupt occurs, the Bus and Status (BSR) register and the Current SCSI Bus Status (CSBS) register must be read to determine which condition created the interrupt. The interrupt can be reset by simply reading the Reset Parity/Interrupt (RPI) register (0xFC07) or by an external chip reset.

If the SCSI core has been properly initialized, an interrupt will be generated in the following cases:

- the chip is selected/reselected
- a DMA transfer completes
- a SCSI bus reset occurs
- a parity error occurs during a data transfer
- a bus phase mismatch occurs
- a SCSI bus disconnection occurs

2.10.2.1 End of DMA Transfer Interrupt

The End of DMA bit determines when a block data transfer is complete. Receive operations are complete when there is no data left in the SCSI core and no additional handshakes occur.

For send operations, the End of DMA bit is set when the DMA finishes its transfer, but the SCSI transfer may still be in progress. If connected as a target, REQ/ and ACK/ should be sampled until both are false. In the LSI53C040 SCSI core, the Last Byte Sent (bit 7 of the Target Command (TC) register) may be sampled to determine when the last byte was transferred.

2.10.2.2 SCSI Bus Reset Interrupt

The SCSI core generates an interrupt when the RST/ signal transitions to asserted. The device releases all bus signals within a bus clear delay (800 ns) of this transition. This interrupt also occurs after setting the Assert RST/ bit (bit 7 of register 0xFC01).

Note: The RST/ signal is not latched in bit 7 of the Current SCSI Bus Status (CSBS) register and may not be active when this bit is read. For this case, the Bus Reset interrupt may be determined by default.

2.10.2.3 Parity Error Interrupt

An interrupt is generated for a received parity error if the Enable Parity Check bit (bit 5) and the Enable Parity Interrupt bit (bit 4) are set in the Mode (MR) register (0xFC02). Parity is checked during a read of the Current SCSI Data (CSD) register (0xFC00) and during a DMA receive operation. A parity error can be detected without generating an interrupt by disabling the Enable Parity Interrupt bit and checking the Parity Error flag (bit 5 in register 0xFC05).

2.10.2.4 Bus Phase Mismatch Interrupt

The SCSI phase lines are the I_O/, C_D/, and MSG/ bus signals. These signals are compared with the corresponding bits in the Target Command (TC) register: Assert I_O/ (bit 0), Assert C_D/ (bit 1), and Assert MSG/ (bit 2). The comparison occurs continually and is reflected in the Phase Mismatch bit (bit 3) of the Bus and Status (BSR) register (0xFC05). If the DMA Mode bit (bit 1 in register 0xFC02) is active and a phase mismatch occurs when REQ/ transitions from HIGH to LOW, an interrupt (IRQ) is generated.

A phase mismatch prevents the recognition of REQ/ and removes the chip from the bus during an initiator send operation. DB0/ through DB7/ and DBP/ will not be driven even though the Assert Data Bus bit is active. This interrupt is only significant when the LSI53C040 is connected as an initiator. It may be disabled by clearing the DMA Mode bit.

Note: It is possible for this interrupt to occur when connected as a target if another device is driving the phase lines to a different state.

2.10.2.5 Loss of BSY/ Interrupt

If the Monitor Busy bit (bit 2) in the Mode (MR) register (0xFC02) is active, an interrupt will be generated if the BSY/ signal is asserted for at least a bus settle delay (400 ns). This interrupt may be disabled by resetting the Monitor Busy bit.

2.10.3 SFF-8067 Interrupts

The SFF-8067 interface generates two types of interrupts: read interrupts and write interrupts. The read interrupt notifies the LSI53C040 that the Fibre Channel device is requesting data. The LSI53C040 microcontroller core should respond by clearing the interrupt and writing one byte of data to the RDATA register, which is transferred to the requesting drive. The write interrupt notifies the LSI53C040 that the drive has written a byte of data to the interface. The LSI53C040 microcontroller core should respond by clearing the interrupt and reading the WDATA register. The Port Control/Status (PCST0/PCST1) registers (0xFC22/0xFC2A), bits [1:0] indicate whether a read or write interrupt has occurred.

2.10.4 Two-Wire Serial Interrupts

An interrupt from the Two-Wire Serial block is caused by one of the following conditions:

- A byte has been transferred (Status register 0xFD01/0xFD03, bit 3)
- A Two-Wire Serial bus error (register 0xFD01/0xFD03, bit 4)
- The chip is addressed as a slave (register 0xFD01/0xFD03, bit 2)

The External Interrupt Enable bit (0xFD01/0xFD03, bit 3) enables the interrupt output to the microcontroller, while the Pending Interrupt bit (bit 7) is clear. The PIN bit is active when the Two-Wire Serial interface has completed an operation and requires processor intervention to continue.

2.10.5 Masking and Enabling Interrupts

Table 2.5 lists the registers used for masking and enabling interrupts. For testing purposes, certain types of interrupts can be forced by writing individual bits in the Interrupt Status (ISR) register (0xFE04). These interrupts can be masked by clearing the corresponding bit in the Interrupt Mask (IMR) register (0xFE0D). Even if the interrupt is masked, the corresponding bit in the ISR will be set if the interrupting condition occurs.

Masking an interrupt prevents it from being seen by the microcontroller core in the LSI53C040. You can allow hardware interrupts either by enabling them in the appropriate register bits, or by masking the interrupts and polling for them. In general, it is recommended to enable as few interrupts as possible and mask/poll for them instead. With the microcontroller and the serial transfer rates on the Two-Wire Serial bus, masking and polling for interrupts is less disruptive to the microcontroller and does not impede performance. An exception to this recommendation would be SCSI and 8067 interrupts, since the bus speeds and the need to complete transfers quickly suggest that interrupts should be enabled.

2.10.6 Polling and Hardware Interrupts

The microcontroller core is informed of an interrupt condition by polling or hardware interrupts. Polling means that the microcontroller must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but consumes microcontroller time that could be used for other tasks. The other method for detecting interrupts is hardware interrupts, where the interrupting condition asserts one of the microcontroller external interrupt signals. This interrupts the microcontroller, and causes it to execute an interrupt service routine. A hybrid approach is common, using hardware interrupts for conditions that might occur infrequently or after a long wait; and polling for interrupts that typically occur after only a short wait.

2.10.7 Interrupt Service Routine

When the microcontroller core receives an interrupt, it reads the Interrupt Status (ISR) register (0xFE04) to determine the source of the interrupt. Once it determines the source of the interrupt, it reads the appropriate bits for determining the exact cause of the interrupt. This activity is described in Table 2.6.

Table 2.6 Interrupt Handling

ISR Bit Number	Interrupt Source	Location to read to determine cause of interrupt	Description
7	SCSI core	BSR (0xFC05)	Monitors SCSI bus control signals not found in CSBS, plus six other status bits.
		CSBS (0xFC04)	Monitors SCSI bus control lines plus data parity bit.
		CSD (0xFC00), CSDHI (0xFC08)	Reads the active SCSI bus.
6	Two-wire serial port 0	Status (0xFD01)	Contains PIN bit plus other status bits.
5	Two-wire serial port 1	Status (0xFD03)	Contains PIN bit plus other status bits.
4	DMA core	DMAI (0xFC14)	Enables DMA interrupt.

Table 2.6 Interrupt Handling (Cont.)

ISR Bit Number	Interrupt Source	Location to read to determine cause of interrupt	Description
3 2	Timer 2 Timer 1	T2C (0xFE09)	Programs Timer 2, and enables an interrupt upon expiration of the timer.
		T1C (0xFE05)	Programs Timer 1, and enables an interrupt upon expiration of the timer.
1	8067 Port 1 or MPIO3_1	MPI3	Reads the values of MPIO3_[1:0] pins, which also serve as external interrupt lines to the microcontroller core.
		PCST1 (0xFC2A)	Read Interrupt and Write Interrupt status bits.
0	8067 Port 0 or MPIO3_0	MPI3	Reads the values of MPIO3_[1:0] pins, which also serve as external interrupt lines to microcontroller core.
		PCST0 (0xFC22)	Read Interrupt and Write Interrupt status bits.

2.11 JTAG Boundary Scan Testing

The LSI53C040 includes support for JTAG boundary scan testing in accordance with the IEEE 1149.1 specification. The device can accept all required boundary scan instructions, as well as the optional CLAMP, HIGH-Z, and IDCODE instructions.

The LSI53C040 uses an 8-bit instruction register to support all boundary scan instructions. The data registers included in the device are the Boundary Data register, the IDCODE register, and the Bypass register. The device can handle a 10 MHz TCK frequency for TDO and TDI.

Chapter 3
Signal Descriptions

This chapter presents the LSI53C040 pin configurations and signal definitions using tables and illustrations. Figure 3.1 through Figure 3.2 are the pin diagrams for all versions of the LSI53C040, Table 3.1 through Table 3.4 show a alphabetical listing and numerical listing for each version, and Figure 3.3 is the functional signal grouping. The pin definitions are presented in Table 3.5 through Table 3.9, organized in functional groups.

- Section 3.1, “Safety Mode Signals”
- Section 3.2, “SFF-8067 Mode”

A slash (/) at the end of a signal name indicates that the active state occurs when the signal is at a LOW voltage. When the slash is absent, the signal is active at a HIGH voltage.

Figure 3.1 LSI53C040, 160-Pin QFP Option

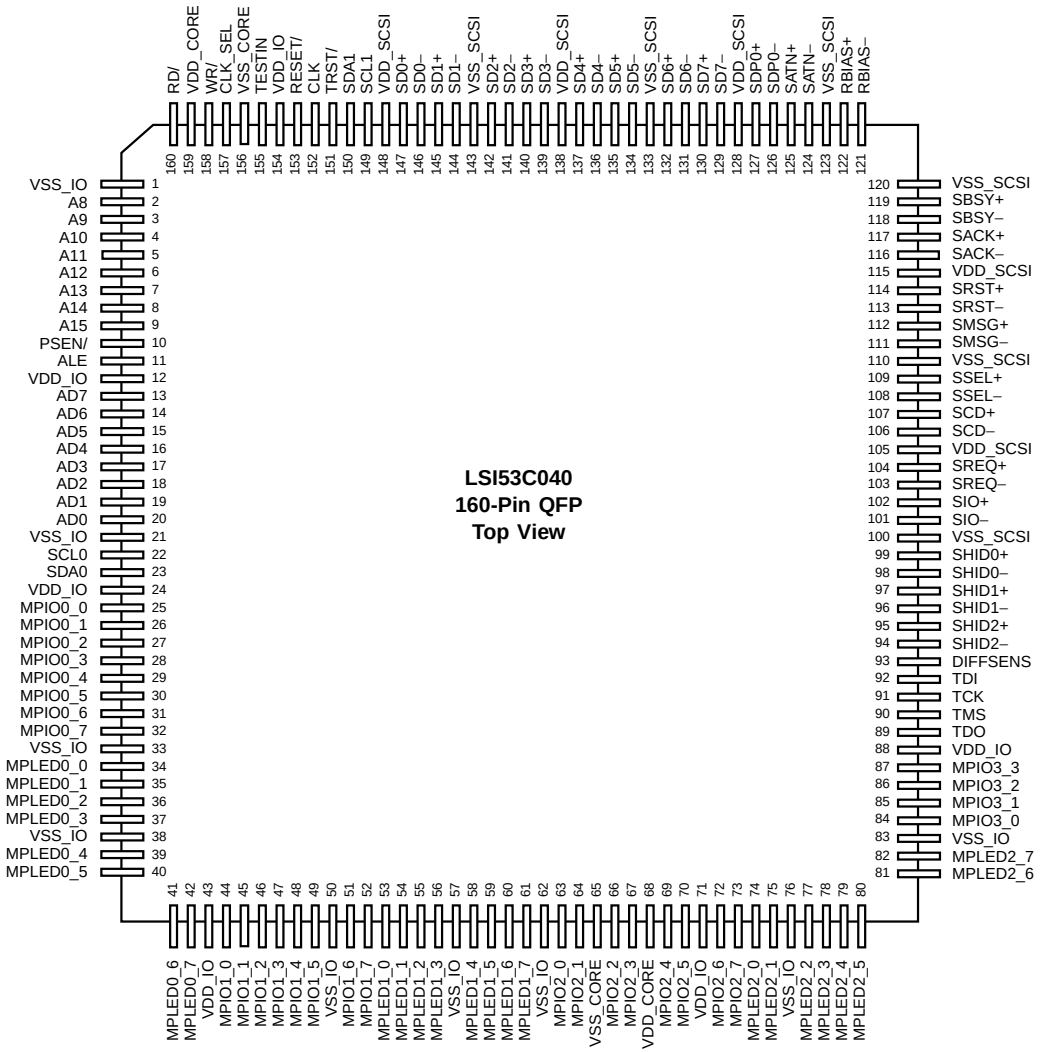


Table 3.1 LSI53C040 160-Pin QFP Pin List (Alphabetically by Signal Name)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A10	4	MPIO2_4	69	SATN–	124	SRST–	113
A11	5	MPIO2_5	70	SBSY+	119	SSEL+	109
A12	6	MPIO2_6	72	SBSY–	118	SSEL–	108
A13	7	MPIO2_7	73	SCD+	107	TCK	91
A14	8	MPIO3_0	84	SCD–	106	TDI	92
A15	9	MPIO3_1	85	SCL0	22	TDO	89
A8	2	MPIO3_2	86	SCL1	149	TESTIN	155
A9	3	MPIO3_3	87	SD0+	147	TMS	90
AD0	20	MPLED0_0	34	SD0–	146	TRST/	151
AD1	19	MPLED0_1	35	SD1+	145	VDD_CORE	68
AD2	18	MPLED0_2	36	SD1–	144	VDD_CORE	159
AD3	17	MPLED0_3	37	SD2+	142	VDD_IO	12
AD4	16	MPLED0_4	39	SD2–	141	VDD_IO	24
AD5	15	MPLED0_5	40	SD3+	140	VDD_IO	43
AD6	14	MPLED0_6	41	SD3–	139	VDD_IO	71
AD7	13	MPLED0_7	42	SD4+	137	VDD_IO	88
ALE	11	MPLED1_0	53	SD4–	136	VDD_IO	154
CLK	152	MPLED1_1	54	SD5+	135	VDD_SCSI	105
CLK_SEL	157	MPLED1_2	55	SD5–	134	VDD_SCSI	115
DIFFSENS	93	MPLED1_3	56	SD6+	132	VDD_SCSI	128
MPIO0_0	25	MPLED1_4	58	SD6–	131	VDD_SCSI	138
MPIO0_1	26	MPLED1_5	59	SD7+	130	VDD_SCSI	148
MPIO0_2	27	MPLED1_6	60	SD7–	129	VSS_CORE	65
MPIO0_3	28	MPLED1_7	61	SDA0	23	VSS_CORE	156
MPIO0_4	29	MPLED2_0	74	SDA1	150	VSS_IO	1
MPIO0_5	30	MPLED2_1	75	SDP0+	127	VSS_IO	21
MPIO0_6	31	MPLED2_2	77	SDP0–	126	VSS_IO	33
MPIO0_7	32	MPLED2_3	78	SHID0+	99	VSS_IO	38
MPIO1_0	44	MPLED2_4	79	SHID0–	98	VSS_IO	50
MPIO1_1	45	MPLED2_5	80	SHID1+	97	VSS_IO	57
MPIO1_2	46	MPLED2_6	81	SHID1–	96	VSS_IO	62
MPIO1_3	47	MPLED2_7	82	SHID2+	95	VSS_IO	76
MPIO1_4	48	PSEN/	10	SHID2–	94	VSS_IO	83
MPIO1_5	49	RBIAS+	122	SIO+	102	VSS_SCSI	100
MPIO1_6	51	RBIAS–	121	SIO–	101	VSS_SCSI	110
MPIO1_7	52	RD/	160	SMSG+	112	VSS_SCSI	120
MPIO2_0	63	RESET/	153	SMSG–	111	VSS_SCSI	123
MPIO2_1	64	SACK+	117	SREQ+	104	VSS_SCSI	133
MPIO2_2	66	SACK–	116	SREQ–	103	VSS_SCSI	143
MPIO2_3	67	SATN+	125	SRST+	114	WR/	158

Table 3.2 LSI53C040 160-Pin QFP Pin List (Numerically by Pin Number)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS_IO	41	MPLED0_6	81	MPLED2_6	121	RBIAS–
2	A8	42	MPLED0_7	82	MPLED2_7	122	RBIAS+
3	A9	43	VDD_IO	83	VSS_IO	123	VSS_SCSI
4	A10	44	MPIO1_0	84	MPIO3_0	124	SATN–
5	A11	45	MPIO1_1	85	MPIO3_1	125	SATN+
6	A12	46	MPIO1_2	86	MPIO3_2	126	SDP0–
7	A13	47	MPIO1_3	87	MPIO3_3	127	SDP0+
8	A14	48	MPIO1_4	88	VDD_IO	128	VDD_SCSI
9	A15	49	MPIO1_5	89	TDO	129	SD7–
10	PSEN/	50	VSS_IO	90	TMS	130	SD7+
11	ALE	51	MPIO1_6	91	TCK	131	SD6–
12	VDD_IO	52	MPIO1_7	92	TDI	132	SD6+
13	AD7	53	MPLED1_0	93	DIFFSENS	133	VSS_SCSI
14	AD6	54	MPLED1_1	94	SHID2–	134	SD5–
15	AD5	55	MPLED1_2	95	SHID2+	135	SD5+
16	AD4	56	MPLED1_3	96	SHID1–	136	SD4–
17	AD3	57	VSS_IO	97	SHID1+	137	SD4+
18	AD2	58	MPLED1_4	98	SHID0–	138	VDD_SCSI
19	AD1	59	MPLED1_5	99	SHID0+	139	SD3–
20	AD0	60	MPLED1_6	100	VSS_SCSI	140	SD3+
21	VSS_IO	61	MPLED1_7	101	SIO–	141	SD2–
22	SCL0	62	VSS_IO	102	SIO+	142	SD2+
23	SDA0	63	MPIO2_0	103	SREQ–	143	VSS_SCSI
24	VDD_IO	64	MPIO2_1	104	SREQ+	144	SD1–
25	MPIO0_0	65	VSS_CORE	105	VDD_SCSI	145	SD1+
26	MPIO0_1	66	MPIO2_2	106	SCD–	146	SD0–
27	MPIO0_2	67	MPIO2_3	107	SCD+	147	SD0+
28	MPIO0_3	68	VDD_CORE	108	SSEL–	148	VDD_SCSI
29	MPIO0_4	69	MPIO2_4	109	SSEL+	149	SCL1
30	MPIO0_5	70	MPIO2_5	110	VSS_SCSI	150	SDA1
31	MPIO0_6	71	VDD_IO	111	SMSG–	151	TRST/
32	MPIO0_7	72	MPIO2_6	112	SMSG+	152	CLK
33	VSS_IO	73	MPIO2_7	113	SRST–	15	3RESET/
34	MPLED0_0	74	MPLED2_0	114	SRST+	154	VDD_IO
35	MPLED0_1	75	MPLED2_1	115	VDD_SCSI	155	TESTIN
36	MPLED0_2	76	VSS_IO	116	SACK–	156	VSS_CORE
37	MPLED0_3	77	MPLED2_2	117	SACK+	157	CLK_SEL
38	VSS_IO	78	MPLED2_3	118	SBSY–	158	WR/
39	MPLED0_4	79	MPLED2_4	119	SBSY+	159	VDD_CORE
40	MPLED0_5	80	MPLED2_5	120	VSS_SCSI	160	RD/

Figure 3.2 LSI53C040 169-Ball BGA Top View

A1 NC	A2 RD/	A3 VSS_CORE	A4 RESET/	A5 SCL1	A6 SD1+	A7 SD3+	A8 SD4–	A9 SD6–	A10 VDD_SCSI	A11 SATN–	A12 NC	A13 NC
B1 NC	B2 NC	B3 WR/	B4 VDD_IO	B5 SDA1	B6 SD1–	B7 SD3–	B8 SD5+	B9 SD7+	B10 SDP0–	B11 NC	B12 NC	B13 NC
C1 A10	C2 NC	C3 A8	C4 CLK_SEL	C5 TRST/	C6 SD0–	C7 VDD_SCSI	C8 SD5–	C9 SD7–	C10 SATN+	C11 RBIAS–	C12 SBSY–	C13 SACK–
D1 A14	D2 A12	D3 A11	D4 VDD_CORE	D5 TESTIN	D6 SD0+	D7 SD2–	D8 SD6+	D9 SDP0+	D10 SBSY+	D11 SACK+	D12 SRST+	D13 SRST–
E1 ALE	E2 PSEN/	E3 A15	E4 A13	E5 A9	E6 VDD_SCSI	E7 SD2+	E8 SD4+	E9 RBIAS+	E10 VDD_SCSI	E11 SMSG–	E12 SSEL+	E13 SSEL–
F1 AD5	F2 AD6	F3 AD7	F4 VDD_IO	F5 AD4	F6 CLK	F7 VSS_IO	F8 SMSG+	F9 SCD+	F10 SCD–	F11 VDD_SCSI	F12 SREQ–	F13 SREQ+
G1 AD1	G2 AD2	G3 AD3	G4 AD0	G5 SCL0	G6 VSS_IO	G7 VSS_IO	G8 VSS_IO	G9 SIO+	G10 SIO–	G11 SHID1+	G12 SHID0–	G13 SHID0+
H1 VDD_IO	H2 SDA0	H3 MPIO0_0	H4 MPIO0_1	H5 MPIO0_2	H6 MPIO0_6	H7 VSS_IO	H8 MPIO2_6	H9 SHID1–	H10 TDI	H11 DIFFSENS	H12 SHID2–	H13 SHID2+
J1 MPIO0_3	J2 MPIO0_4	J3 MPIO0_5	J4 MPLED0_1	J5 MPLED0_7	J6 MPLED1_3	J7 MPIO2_0	J8 VDD_CORE	J9 MPLED2_7	J10 MPIO3_3	J11 TDO	J12 TMS	J13 TCK
K1 MPIO0_7	K2 MPLED0_0	K3 MPLED0_3	K4 MPLED0_5	K5 MPIO1_2	K6 MPIO1_7	K7 MPLED1_7	K8 MPIO2_3	K9 MPLED2_1	K10 MPLED2_5	K11 MPIO3_1	K12 MPIO3_2	K13 VDD_IO
L1 MPLED0_2	L2 MPLED0_4	L3 MPLED0_6	L4 MPIO1_0	L5 MPIO1_4	L6 MPLED1_0	L7 MPLED1_4	L8 MPIO2_2	L9 VDD_IO	L10 MPLED2_3	L11 MPLED2_6	L12 NC	L13 MPIO3_0
M1 NC	M2 NC	M3 NC	M4 MPIO1_1	M5 MPIO1_5	M6 MPLED1_1	M7 MPLED1_5	M8 MPIO2_1	M9 MPIO2_5	M10 MPLED2_0	M11 MPLED2_4	M12 NC	M13 NC
N1 NC	N2 NC	N3 VDD_IO	N4 MPIO1_3	N5 MPIO1_6	N6 MPLED1_2	N7 MPLED1_6	N8 VSS_CORE	N9 MPIO2_4	N10 MPIO2_7	N11 MPLED2_2	N12 NC	N13 NC

Table 3.3 169-Ball BGA List (Alphabetically by Ball Grid Location)

Ball #	Signal	Ball #	Signal	Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	NC	C9	SD7–	F4	VDD_IO	H12	SHID2–	L7	MPLED1_4
A2	RD/	C10	SATN+	F5	AD4	H13	SHID2+	L8	MPIO2_2
A3	VSS_CORE	C11	RBIAS–	F6	CLK	J1	MPIO0_3	L9	VDD_IO
A4	RESET/	C12	SBSY–	F7	VSS_IO	J2	MPIO0_4	L10	MPLED2_3
A5	SCL1	C13	SACK–	F8	SMSG+	J3	MPIO0_5	L11	MPLED2_6
A6	SD1+	D1	A14	F9	SCD+	J4	MPLED0_1	L12	NC
A7	SD3+	D2	A12	F10	SCD-	J5	MPLED0_7	L13	MPIO3_0
A8	SD4–	D3	A11	F11	VDD_SCSI	J6	MPLED1_3	M1	NC
A9	SD6–	D4	VDD_CORE	F12	SREQ–	J7	MPIO2_0	M2	NC
A10	VDD_SCSI	D5	TESTIN	F13	SREQ+	J8	VDD_CORE	M3	NC
A11	SATN–	D6	SD0+	G1	AD1	J9	MPLED2_7	M4	MPIO1_1
A12	NC	D7	SD2–	G2	AD2	J10	MPIO3_3	M5	MPIO1_5
A13	NC	D8	SD6+	G3	AD3	J11	TDO	M6	MPLED1_1
B1	NC	D9	SDP0+	G4	AD0	J12	TMS	M7	MPLED1_5
B2	NC	D10	SBSY+	G5	SCL0	J13	TCK	M8	MPIO2_1
B3	WR/	D11	SACK+	G6	VSS_IO	K1	MPIO0_7	M9	MPIO2_5
B4	VDD_IO	D12	SRST+	G7	VSS_IO	K2	MPLED0_0	M10	MPLED2_0
B5	SDA1	D13	SRST–	G8	VSS_IO	K3	MPLED0_3	M11	MPLED2_4
B6	SD1–	E1	ALE	G9	SIO+	K4	MPLED0_5	M12	NC
B7	SD3–	E2	PSEN/	G10	SIO–	K5	MPIO1_2	M13	NC
B8	SD5+	E3	A15	G11	SHID1+	K6	MPIO1_7	N1	NC
B9	SD7+	E4	A13	G12	SHID0–	K7	MPLED1_7	N2	NC
B10	SDP0–	E5	A9	G13	SHID0+	K8	MPIO2_3	N3	VDD_IO
B11	NC	E6	VDD_SCSI	H1	VDD_IO	K9	MPLED2_1	N4	MPIO1_3
B12	NC	E7	SD2+	H2	SDA0	K10	MPLED2_5	N5	MPIO1_6
B13	NC	E8	SD4+	H3	MPIO0_0	K11	MPIO3_1	N6	MPLED1_2
C1	A10	E9	RBIAS+	H4	MPIO0_1	K12	MPIO3_2	N7	MPLED1_6
C2	NC	E10	VDD_SCSI	H5	MPIO0_2	K13	VDD_IO	N8	VSS_CORE
C3	A8	E11	SMSG–	H6	MPIO0_6	L1	MPLED0_2	N9	MPIO2_4
C4	CLK_SEL	E12	SSEL+	H7	VSS_IO	L2	MPLED0_4	N10	MPIO2_7
C5	TRST/	E13	SSEL–	H8	MPIO2_6	L3	MPLED0_6	N11	MPLED2_2
C6	SD0–	F1	AD5	H9	SHID1–	L4	MPIO1_0	N12	NC
C7	VDD_SCSI	F2	AD6	H10	TDI	L5	MPIO1_4	N13	NC
C8	SD5–	F3	AD7	H11	DIFFSENS	L6	MPLED1_0		

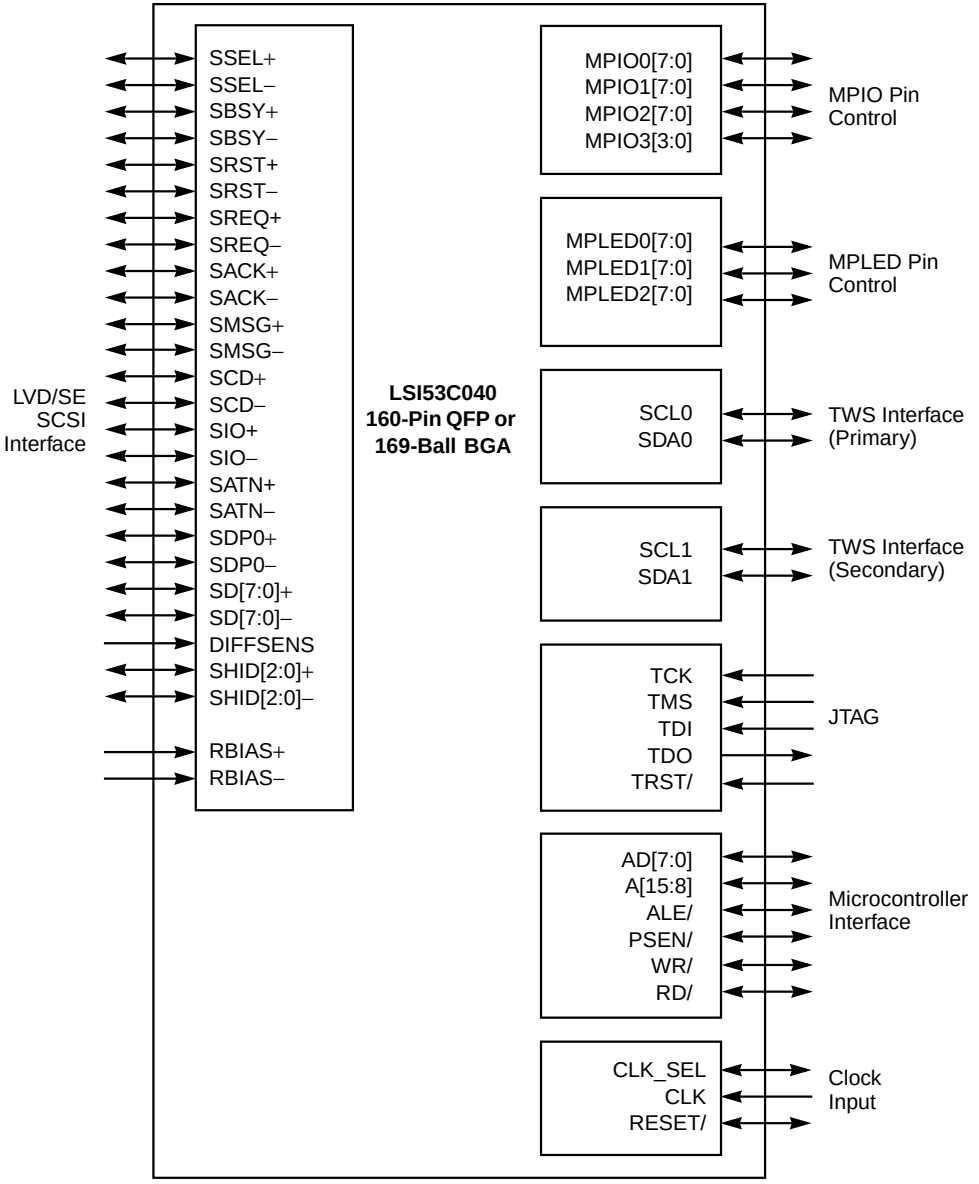
1. *NC* pins are not connected.

Table 3.4 169-Ball BGA List (Alphabetically by Signal Name)

Signal	Ball #	Signal	Ball #	Signal	Ball #	Signal	Ball #	Signal	Ball #
A8	C3	MPIO1_6	N5	MPLED2_4	M11	SCD–	F10	SREQ–	F12
A9	E5	MPIO1_7	K6	MPLED2_5	K10	SCD+	F9	SREQ+	F13
A10	C1	MPIO2_0	J7	MPLED2_6	L11	SCL0	G5	SRST–	D13
A11	D3	MPIO2_1	M8	MPLED2_7	J9	SCL1	A5	SRST+	D12
A12	D2	MPIO2_2	L8	NC	A1	SD0–	C6	SSEL–	E13
A13	E4	MPIO2_3	K8	NC	A12	SD0+	D6	SSEL+	E12
A14	D1	MPIO2_4	N9	NC	A13	SD1–	B6	TCK	J13
A15	E3	MPIO2_5	M9	NC	B1	SD1+	A6	TDI	H10
AD0	G4	MPIO2_6	H8	NC	B2	SD2–	D7	TDO	J11
AD1	G1	MPIO2_7	N10	NC	B11	SD2+	E7	TESTIN	D5
AD2	G2	MPIO3_0	L13	NC	B12	SD3–	B7	TMS	J12
AD3	G3	MPIO3_1	K11	NC	B13	SD3+	A7	TRST/	C5
AD4	F5	MPIO3_2	K12	NC	C2	SD4–	A8	VDD_CORE	D4
AD5	F1	MPIO3_3	J10	NC	L12	SD4+	E8	VDD_CORE	J8
AD6	F2	MPLED0_0	K2	NC	M1	SD5–	C8	VDD_IO	B4
AD7	F3	MPLED0_1	J4	NC	M2	SD5+	B8	VDD_IO	F4
ALE	E1	MPLED0_2	L1	NC	M3	SD6–	A9	VDD_IO	H1
CLK	F6	MPLED0_3	K3	NC	M12	SD6+	D8	VDD_IO	K13
CLK_SEL	C4	MPLED0_4	L2	NC	M13	SD7–	C9	VDD_IO	L9
DIFFSENS	H11	MPLED0_5	K4	NC	N1	SD7+	B9	VDD_IO	N3
MPIO0_0	H3	MPLED0_6	L3	NC	N2	SDA0	H2	VDD_SCSI	A10
MPIO0_1	H4	MPLED0_7	J5	NC	N12	SDA1	B5	VDD_SCSI	C7
MPIO0_2	H5	MPLED1_0	L6	NC	N13	SDP0–	B10	VDD_SCSI	E6
MPIO0_3	J1	MPLED1_1	M6	PSEN/	E2	SDP0+	D9	VDD_SCSI	E10
MPIO0_4	J2	MPLED1_2	N6	RBIAS–	C11	SHID0–	G12	VDD_SCSI	F11
MPIO0_5	J3	MPLED1_3	J6	RBIAS+	E9	SHID0+	G13	VSS_CORE	A3
MPIO0_6	H6	MPLED1_4	L7	RD/	A2	SHID1–	H9	VSS_CORE	N8
MPIO0_7	K1	MPLED1_5	M7	RESET/	A4	SHID1+	G11	VSS_IO	F7
MPIO1_0	L4	MPLED1_6	N7	SACK–	C13	SHID2–	H12	VSS_IO	G6
MPIO1_1	M4	MPLED1_7	K7	SACK+	D11	SHID2+	H13	VSS_IO	G7
MPIO1_2	K5	MPLED2_0	M10	SATN–	A11	SIO–	G10	VSS_IO	G8
MPIO1_3	N4	MPLED2_1	K9	SATN+	C10	SIO+	G9	VSS_IO	H7
MPIO1_4	L5	MPLED2_2	N11	SBSY–	C12	SMSG–	E11	WR/	B3
MPIO1_5	M5	MPLED2_3	L10	SBSY+	D10	SMSG+	F8		

1. *NC* pins are not connected.

Figure 3.3 LSI53C040 Functional Pin Description



3.1 Safety Mode Signals

The Safety Mode Signals section contains tables describing the signals for the following signal groups: Miscellaneous Signals, SCSI Signals, JTAG Signals, and Power and Ground Signals.

3.1.1 Miscellaneous Signals

Table 3.5 describes the signals for the Miscellaneous Signals group.

Table 3.5 Miscellaneous Signals

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
A8 A9 A10 A11 A12 A13 A14 A15	2 3 4 5 6 7 8 9	C3 E5 C1 D3 D2 E4 D1 E3	High byte of the microcontroller address bus. An external pull-up on the A11 pin causes the serial ROM download to use the 2-wire serial interface 1. If no external pull-up is used the download will use the 2-wire serial interface 0. A[10:8] are used to select a chip address for the serial ROM. For more information on the possible addresses, see Table 2.4. For more information on these power-up options, see Chapter 2.	4 mA, 5 V tolerant TTL bidirectional	100 µA pull-down
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	20 19 18 17 16 15 14 13	G4 G1 G2 G3 F5 F1 F2 F3	Low byte of the microcontroller multiplexed address/data bus. An external pull-up on AD[1:0] enables automatic branch generation. For information on the branch values, see Table 2.3. An external pull-up on AD5 causes the LSI53C040 to download firmware from a serial ROM at power on. For more information on these power-up options, see Chapter 2.	4 mA, 5 V tolerant TTL bidirectional	100 µA pull-down

Table 3.5 Miscellaneous Signals (Cont.)

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
PSEN/	10	E2	Active LOW microcontroller Program Space Enable output.	4 mA, 5 V tolerant TTL bidirectional	None
WR/	158	B3	Active LOW microcontroller write output.	4 mA, 5 V tolerant TTL bidirectional	None
RD/	160	A2	Active LOW microcontroller read output.	4 mA, 5 V tolerant TTL bidirectional	None
ALE	11	E1	Address latch enable for microcontroller bus.	4 mA, 5 V tolerant TTL bidirectional	None
SCL0 SCL1	22 149	G5 A5	Two-Wire Serial Port 0 Clock Two-Wire Serial Port 1 Clock	2 mA, 5 V tolerant TTL Schmitt open drain bidirectional	None (external pull-up required)
SDA0 SDA1	23 150	H2 B5	Two-Wire Serial Port 0 Data Two-Wire Serial Port 1 Data	2 mA, 5 V tolerant TTL Schmitt open drain bidirectional	None (external pull-up required)
MPIO0_ [7:0]	32, 31, 30, 29, 28, 27, 26, 25	K1, H6, J3, J2, J1, H5, H4, H3	Multipurpose I/O bank 0	4 mA, 5 V tolerant TTL bidirectional	25 µA pull-down
MPIO1_ [7:0]	52, 51, 49, 48, 47, 46, 45, 44	K6, N5, M5, L5, N4, K5, M4, L4	Multipurpose I/O bank 1	4 mA, 5 V tolerant TTL bidirectional	25 µA pull-down
MPIO2_ [7:0]	73, 72, 70, 69, 67, 66, 64, 63	N10, H8, M9, N9, K8, L8, M8, J7	Multipurpose I/O bank 2	4 mA, 5 V tolerant TTL bidirectional	25 µA pull-down

Table 3.5 Miscellaneous Signals (Cont.)

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
MPIO3_ [3:0]	87 86 85 84	J10 K12 K11 L13	Multipurpose I/O bank 3 MPIO3_0 = INT0/ to microcontroller, if 0xFF05 bit 0 is set (active low). MPIO3_1 = INT1/ to microcontroller, if 0xFF05 bit 0 is set (active low). MPIO3_2 = TXD from microcontroller, if 0xFF05 bit 1 is set. MPIO3_3 = RXD to microcontroller, if 0xFF05 bit 1 is set.	4 mA, 5 V tolerant TTL bidirectional	25 µA pull-down
MPLED 0_ [7:0]	42, 41, 40, 39, 37, 36, 35, 34	J5, L3, K4, L2, K3, L1, J4, K2	Open drain multipurpose LED bank 0 outputs. Any unused LED outputs must be tied to V_{SS} or resistively pulled HIGH.	16 mA, 5 V tolerant TTL open drain bidirectional	None
MPLED 1_ [7:0]	61, 60, 59, 58, 56, 55, 54, 53	K7, N7, M7, L7, J6, N6, M6, L6	Open drain multipurpose LED bank 1 outputs. Any unused LED outputs must be tied to V_{SS} HIGH.	16 mA, 5 V tolerant TTL open drain bidirectional	None
MPLED 2_ [7:0]	82, 81, 80, 79, 78, 77, 75, 74	J9, L11, K10, M11, L10, N11, K9, M10	Open drain multipurpose LED bank 2 outputs. Any unused LED outputs must be tied to V_{SS} or resistively pulled HIGH.	16 mA, 5 V tolerant TTL open drain bidirectional	None
TESTIN	155	D5	This pin should be tied LOW during normal operation.	5 V tolerant TTL input	None
CLK_S EL	157	C4	When this signal is tied HIGH, the internal clock will be the same as the external. When LOW, the external frequency is divided by 2.	5 V tolerant with TTL input bidirectional	100 A pull-up
CLK	152	F6	40 MHz system clock input.	5 V tolerant TTL input	None

Table 3.5 Miscellaneous Signals (Cont.)

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
RESET/	153	A4	Active low chip reset input. The LSI53C040 has an internal power-on reset circuit which can be relied upon for initializing the chip. If the LSI53C040 watchdog timer is used and it expires, it can force an internal chip reset and assert the RESET/ pin LOW to reset external devices (if bit 7 in register 0xFF05 is set).	4 mA open drain output, 5 V tolerant with TTL input bidirectional	None

3.1.2 SCSI Signals

Table 3.6 describes the signals for the SCSI Signals group.

Table 3.6 SCSI Signals

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
DIFFSENS	93	H11	SCSI DIFFSENS signal. A low level input enables SCSI SE mode. A mid-range level input enables SCSI LVD mode. A high level input enables SFF-8067 Mode. Tie this pin to V_{DD} to enable SFF-8067 mode.	Analog input	–
SHID2– SHID2+	94 95	H12 H13	SCSI High ID 2. This LVD SCSI pair may be connected to any of the SCSI data signals from data bit 8 through 15. This provides the means for the SCSI core to respond to selection as a device with an ID greater than 7. In SE mode, the SHID2– pin is the SE signal pin, and the SHID2+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SHID1– SHID1+	96 97	H9 G11	SCSI High ID 1. This LVD SCSI pair may be connected to any of the SCSI data signals from data bit 8 through 15. This enables the SCSI core to respond to selection as a device with an ID greater than 7. In SE mode, the SHID1– pin is the SE signal pin, and the SHID1+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SHID0– SHID0+	98 99	G12 G13	SCSI High ID 0. This LVD SCSI pair may be connected to any of the SCSI data signals from data bit 8 through 15. This enables the SCSI core to respond to selection as a device with an ID greater than 7. In SE mode, the SHID0– pin is the SE signal pin, and the SHID0+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None

Table 3.6 SCSI Signals (Cont.)

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
SIO– SIO+	101 102	G10 G9	SCSI I/O signal. In SE mode, the SIO– pin is the SE signal pin, and the SIO+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SREQ– SREQ+	103 104	F12 F13	SCSI REQ signal. In SE mode, the SREQ– pin is the SE signal pin, and the SREQ+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SCD– SCD+	106 107	F10 F9	SCSI C/D signal. In SE mode, the SCD– pin is the SE signal pin, and the SCD+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SSEL– SSEL+	108 109	E13 E12	SCSI SEL signal. In SE mode, the SSEL– pin is the SE signal pin, and the SSEL+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SMSG– SMSG+	111 112	E11 F8	SCSI MSG signal. In SE mode, the SMSG– pin is the SE signal pin, and the SMSG+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SRST– SRST+	113 114	D13 D12	SCSI RST signal. In SE mode, the SRST– pin is the SE signal pin, and the SRST+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SACK– SACK+	116 117	C13 D11	SCSI ACK signal. In SE mode, the SACK– pin is the SE signal pin, and the SACK+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SBSY– SBSY+	118 119	C12 D10	SCSI BSY signal. In SE mode, the SBSY– pin is the SE signal pin, and the SBSY+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None

Table 3.6 SCSI Signals (Cont.)

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
RBIAS– RBIAS+	121 122	C11 E9	Bias resistor for LVD operation. See Figure 2.4 for a suggested implementation.	Custom Input	None
SATN– SATN+	124 125	A11 C10	SCSI ATN signal. In SE mode, the SATN– pin is the SE signal pin, and the SATN+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SDP0– SDP0+	126 127	B10 D9	SCSI low data byte parity signal. In SE mode, the SDP0– pin is the SE signal pin, and the SDP0+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None
SD7–, SD7+, SD6–, SD6+, SD5–, SD5+, SD4–, SD4+, SD3–, SD3+, SD2–, SD2+, SD1–, SD1+, SD0–, SD0+	129,130, 131,132, 134,135, 136,137, 139,140, 141,142, 144,145, 146,147	C9, B9, A9, D8, C8, B8, A8, E8, B7, A7, D7, E7, B6, A6, C6, D6	SCSI low data byte signals. In SE mode, the SDx– pin is the SE signal pin, and the SDx+ pin should be connected as a virtual ground on the SCSI connector.	SE or LVD SCSI I/O	None

3.1.3 JTAG Signals

Table 3.7 describes the signals for the JTAG Signals group.

Table 3.7 JTAG Signals

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
TCK	91	J13	Test Clock. The Test Clock pin provides clocking for the JTAG test logic and boundary scan.	5 V tolerant TTL input	100 µA pull-up
TMS	90	J12	Test Mode Select. The Test Mode Select pin receives a signal to control the JTAG test operations and boundary scans.	5 V tolerant TTL input	100 µA pull-up
TDI	92	H10	Test Data In. The Test Data In pin receives serial input data and commands for JTAG test operations and boundary scans.	5 V tolerant TTL input	100 µA pull-up
TDO	89	J11	Test Data Out. The Test Data Out pin provides serial output data for JTAG test operations and boundary scans.	4 mA Output	None
TRST/	151	C5	Test Reset. The Test Reset pin receives a signal to reset the JTAG TAP controller. It also simulates a power-on reset for core logic (NOTE: not JTAG compliant).	5 V tolerant TTL input	100 µA pull-up

3.1.4 Power and Ground Signals

Table 3.8 describes the signals for the Power and Ground Signals group.

Table 3.8 Power and Grounds Signals[1]

Name	Pin Number	BGA Ball Number	Description	Pad Type	Internal Resistor
VSS_IO	1, 21, 33, 38, 50, 57, 62, 76, 83	F7, G6, G7, G8, H7	V_{SS} supply for I/O signal pins. Must be connected to ground.	V_{SS}	–
VDD_IO	12, 24, 43, 71, 88, 154	B4, F4, H1, K13, L9, N3	V_{DD} supply for I/O signal pins. Must be connected to +3.3 V power supply.	V_{DD}	–
VSS_ SCSI	100, 110, 120, 123, 133, 143		V_{SS} supply for SCSI I/O signal pins. Must be connected to ground.	V_{SS}	–
VDD_ SCSI	105, 115, 128, 138, 148	A10, C7, E6, E10, F11	V_{DD} supply for SCSI I/O signal pins. Must be connected to +3.3 V power supply.	V_{DD}	–
VSS_ CORE	65, 156	A3, N8	V_{SS} supply for core logic. Must be connected to ground.	V_{SS}	–
VDD_ CORE	68, 159	J8, D4	V_{DD} supply for core logic. Must be connected to +3.3 V power supply.	V_{DD}	–

1. For optimal operation, the power pins should be powered up at the same time or in this order: VDD_CORE, VDD_IO, VDD_SCSI.

3.2 SFF-8067 Mode

The SFF-8067 interface is enabled when the DIFFSENS pin is tied to V_{DD}. The SCSI pin functions are reassigned to SFF-8067 port functions as indicated in Table 3.9.

Table 3.9 Pin Assignments for SFF-8067 Mode

Name	Pin/Ball No.	Description	8067 Port	Pad Configuration
D0, SEL_0	147/D6	When PARALLEL_ESI/ is asserted, this signal contains bit 0 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_0 signal, included for compatibility with SFF-8045.	Port 0	4 mA open drain bidirectional
D1, SEL_1	146/C6	When PARALLEL_ESI/ is asserted, this signal contains bit 1 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_1 signal, included for compatibility with SFF-8045.	Port 0	4 mA open drain bidirectional
D2, SEL_2	145/A6	When PARALLEL_ESI/ is asserted, this signal contains bit 2 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_2 signal, included for compatibility with SFF-8045.	Port 0	4 mA open drain bidirectional
D3, SEL_3	144/B6	When PARALLEL_ESI/ is asserted, this signal contains bit 3 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_3 signal, included for compatibility with SFF-8045.	Port 0	4 mA open drain bidirectional

Table 3.9 Pin Assignments for SFF-8067 Mode (Cont.)

Name	Pin/Ball No.	Description	8067 Port	Pad Configuration
ENCL_ACK/, SEL_4	142/E7	When PARALLEL_ESI/ is asserted, this is an active low acknowledge signal sourced by the LSI53C040 back to the Fibre Channel device. When PARALLEL_ESI/ is deasserted, this signal is the SEL_4 signal, included for compatibility with SFF-8045.	Port 0	4 mA open drain bidirectional
DSK_RD/, SEL_5	141/D7	When PARALLEL_ESI/ is asserted, this is an active low control signal sourced by the drive to the LSI53C040 to indicate the device is ready to read data. When PARALLEL_ESI/ is deasserted, this signal is the SEL_5 signal, included for compatibility with SFF-8045.	Port 0	4 mA open drain bidirectional
DSK_WR/, SEL_6	140/A7	When PARALLEL_ESI/ is asserted, this is an active low control signal sourced by the drive to the LSI53C040 to indicate the device is ready to write data. When PARALLEL_ESI/ is deasserted, this signal is the SEL_6 signal, included for compatibility with SFF-8045.	Port 0	4 mA open drain bidirectional
PARALLEL_ ESI/	139/B7	Used to select between the SEL_ID and the bidirectional interface. Pull-up resistors on the interface are 3.3 kΩ minimum. When this pin is asserted, the drive begins the discovery process and prepares to read or write data. When this pin is deasserted, the drive is presented with SEL_ID. All SFF-8067 transactions are terminated, regardless of the state of the protocol.	Port 0	4 mA open drain bidirectional
D0, SEL_0	137/E8	When PARALLEL_ESI/ is asserted, this signal contains bit 0 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_0 signal, included for compatibility with SFF-8045.	Port 1	4 mA open drain bidirectional

Table 3.9 Pin Assignments for SFF-8067 Mode (Cont.)

Name	Pin/Ball No.	Description	8067 Port	Pad Configuration
D1, SEL_1	136/A8	When PARALLEL_ESI/ is asserted, this signal contains bit 1 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_1 signal, included for compatibility with SFF-8045.	Port 1	4 mA open drain bidirectional
D2, SEL_2	135/B8	When PARALLEL_ESI/ is asserted, this signal contains bit 2 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_2 signal, included for compatibility with SFF-8045.	Port 1	4 mA open drain bidirectional
D3, SEL_3	134/C8	When PARALLEL_ESI/ is asserted, this signal contains bit 3 of a data nibble for read and write operations. When PARALLEL_ESI/ is deasserted, this signal is the SEL_3 signal, included for compatibility with SFF-8045.	Port 1	4 mA open drain bidirectional
ENCL_ACK/, SEL_4	132/D8	When PARALLEL_ESI/ is asserted, this is an active low acknowledge signal sourced by the LSI53C040 back to the Fibre Channel device. When PARALLEL_ESI/ is deasserted, this signal is the SEL_4 signal, included for compatibility with SFF-8045.	Port 1	4 mA open drain bidirectional
DSK_RD/, SEL_5	131/A9	When PARALLEL_ESI/ is asserted, this is an active low control signal sourced by the drive to the LSI53C040 to indicate the device is ready to read data. When PARALLEL_ESI/ is deasserted, this signal is the SEL_5 signal, included for compatibility with SFF-8045.	Port 1	4 mA open drain bidirectional

Table 3.9 Pin Assignments for SFF-8067 Mode (Cont.)

Name	Pin/Ball No.	Description	8067 Port	Pad Configuration
DSK_WR/, SEL_6	130/B9	When PARALLEL_ESI/ is asserted, this is an active low control signal sourced by the drive to the LSI53C040 to indicate the device is ready to write data. When PARALLEL_ESI/ is deasserted, this signal is the SEL_6 signal, included for compatibility with SFF-8045.	Port 1	4 mA open drain bidirectional
PARALLEL_ ESI/	129/C9	Used to select between the SEL_ID and the bidirectional interface. Pull-up resistors on the interface are 3.3 kΩ minimum. When this pin is asserted, the drive begins the discovery process and prepares to read or write data. When this pin is deasserted, the drive is presented with SEL_ID. All SFF-8067 transactions are terminated, regardless of the state of the protocol.	Port 1	4 mA open drain bidirectional
PA0	127/D9	This pin contains bit 0 of the physical address of the enclosure.	Port 0	Input
PA1	126/B10	This pin contains bit 1 of the physical address of the enclosure.	Port 0	Input
PA2	125/C10	This pin contains bit 2 of the physical address of the enclosure.	Port 0	Input
PA3	124/A11	This pin contains bit 3 of the physical address of the enclosure.	Port 0	Input
PA4	119/D10	This pin contains bit 4 of the physical address of the enclosure.	Port 0	Input
PA5	118/C12	This pin contains bit 5 of the physical address of the enclosure.	Port 0	Input
PA6	117/D11	This pin contains bit 6 of the physical address of the enclosure.	Port 0	Input
tied to V_{DD}	116/C13	–	N/A	Input
tied to V_{DD}	114/D12	–	N/A	Input
tied to V_{DD}	113/D3	–	N/A	Input

Table 3.9 Pin Assignments for SFF-8067 Mode (Cont.)

Name	Pin/Ball No.	Description	8067 Port	Pad Configuration
PA0	112/F8	This pin contains bit 0 of the physical address of the enclosure.	Port 1	Input
PA1	111/E11	This pin contains bit 1 of the physical address of the enclosure.	Port 1	Input
PA2	109/E12	This pin contains bit 2 of the physical address of the enclosure.	Port 1	Input
PA3	108/E13	This pin contains bit 3 of the physical address of the enclosure.	Port 1	Input
PA4	107/F9	This pin contains bit 4 of the physical address of the enclosure.	Port 1	Input
PA5	106/F10	This pin contains bit 5 of the physical address of the enclosure.	Port 1	Input
PA6	104/F13	This pin contains bit 6 of the physical address of the enclosure.	Port 1	Input
Tied to V_{DD}	103/F12	–	N/A	Input
Tied to V_{DD}	102/G9	–	N/A	Input
Tied to V_{DD}	101/G10	–	N/A	Input
Tied to V_{DD}	99/G13	–	N/A	Input
Tied to V_{DD}	98/G12	–	N/A	Input
Tied to V_{DD}	97/G11	–	N/A	Input
Tied to V_{DD}	96/H9	–	N/A	Input
Tied to V_{DD}	95/H13	–	N/A	Input
Tied to V_{DD}	94/H12	–	N/A	Input

Chapter 4
SCSI and DMA Registers

This chapter contains descriptions of the LSI53C040 SCSI and DMA registers. The SFF-8067 registers, Two-Wire Serial registers, Miscellaneous registers, and System registers are described in Chapter 5 through Chapter 8. The term “set” is used to refer to bits that are programmed to a binary one, while the terms “reset” or “clear” are used to refer to bits that are programmed to binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Reserved bit functions may change at any time. Unless otherwise indicated, all bits in registers are active high; that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default bit values, which are enabled after the chip is powered on or reset.

Figure 4.1 summarizes the entire LSI53C040 register set.

Figure 4.1 Register Set Overview

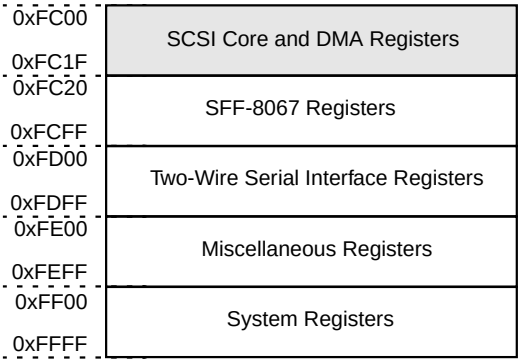


Table 4.1, the register map, summarizes the SCSI and DMA registers in graphical form.

Table 4.1 SCSI and DMA Registers

31 — 16	15 — 0	Address
Current SCSI Data (CSD) (Read)	Output Data (ODR) (Write)	0xFC00
Initiator Command (ICR)		0xFC01
Mode (MR)		0xFC02
Target Command (TC)		0xFC03
Current SCSI Bus Status (CSBS) (Read)	Select Enable (SER) (Write)	0xFC04
Bus and Status (BSR) (Read)	DMA Send (DSR) (Write)	0xFC05
Start DMA Target Receive (SDTR)		0xFC06
Reset Parity/Interrupt (RPI) (Read)	Start DMA Initiator Receive (SDIR) (Write)	0xFC07
Current SCSI Data High (CSDHI)		0xFC08
Reserved		0xFC09–0xFC0B
Select Enable High (SENHI)		0xFC0C
Reserved		0xFC0D–0xFC0F
DMA Status (DS)		0xFC10
DMA Transfer Length (DTL)		0xFC11
DMA Source/Destination Low (DSDL)		0xFC12
DMA Source/Destination High (DSDH)		0xFC13
DMA Interrupt (DMAI)		0xFC14
Reserved		0xFC15–0xFC1F

Register: 0xFC00

Current SCSI Data (CSD)

Read Only

7						1
DB						
x	x	x	x	x	x	x

DB **Current SCSI Data** **[7:0]**

The Current SCSI Data register is a read only register that allows the microcontroller to read the active SCSI data bus. Whenever a 1 is read in one of these bits, the corresponding data signal is asserted on the SCSI bus. If parity checking is enabled, the SCSI bus parity is checked at the beginning of the read cycle. This register is used during arbitration to check for higher priority arbitrating devices. Parity is not guaranteed valid during arbitration.

Register: 0xFC00

Output Data (ODR)

Write Only

7						1
DB						
x	x	x	x	x	x	x

DB **SCSI Output Data** **[7:0]**

The Output Data register is a write only register that is used to send data to the SCSI bus. This register is also used to assert the proper ID bits on the SCSI bus during the arbitration and selection phases. Writing a 1 to one of these bits causes the corresponding data signal to be asserted on the SCSI bus. This register is only asserted on the SCSI bus when the ADB bit (0xFC01, bit 0) is set.

Register: 0xFC01

Initiator Command (ICR)

Read/Write

7	6	5	4	3	2	1	0
ARST	AIP	LA	AACK	ABSY	ASEL	AATN	ADB
0	0	0	0	0	0	0	0

ARST **Assert SRST** **7**

Whenever a 1 is written to this bit, the SRST signal is asserted on the SCSI bus. The SRST signal will remain asserted until this bit is reset or until an external chip reset occurs. After this bit is set, the IRQ output goes active and all internal logic and control registers are reset (except for the interrupt latch and the Assert SRST bit). Writing a 0 to this bit deasserts the SRST signal. Reading this register bit simply reflects the status of this bit.

AIP **Arbitration In Progress (read only)** **6**

This bit is used to determine if arbitration is in progress. For this bit to be active, the ARB bit (Mode Register 0xFC02, bit 0) must have been set previously. It indicates that a bus free condition has been detected and that the chip has asserted BSY/ and the contents of the Output Data (ODR) register (0xFC00) onto the SCSI bus. The AIP bit will remain active until the Arbitrate bit is reset.

LA **Lost Arbitration** **5**

When active, this read only bit indicates that the SCSI core has detected a bus free condition, arbitrated for use of the bus by asserting BSY/ and its ID on the data bus, and lost arbitration due to SEL/ being asserted by another bus device. For this bit to be active, the ARB bit (Mode register 0xFC02, bit 0) must be active.

AACK **Assert ACK/** **4**

This bit is used by the bus initiator to assert the ACK/ pin on the SCSI bus. In order to assert ACK/, the Target Mode bit (Mode register 0xFC02, bit 6) must be false. Writing a zero to this bit resets ACK/ on the SCSI bus. Reading this register bit simply reflects the status of this bit.

ABSY **Assert BSY/** **3**

Writing a 1 into this bit asserts the BSY/ pin onto the SCSI bus. Conversely, a 0 resets the BSY/ signal. Asserting BSY/ indicates a successful selection or reselection, and resetting this bit creates a bus disconnect condition. Reading this bit reflects the status of this bit without changing the value.

ASEL **Assert SEL/** **2**

Writing a 1 into this bit asserts the SEL/ pin onto the SCSI bus. SEL/ is normally asserted after arbitration has been successfully completed. SEL/ may be deasserted by resetting this bit to a zero. A read of this register bit simply reflects the status of this bit.

AATN **Assert ATN/** **1**

The ATN/ pin may be asserted on the SCSI bus by setting this bit to a 1 if the Target Mode bit (Mode register 0xFC02, bit 6) is false. ATN/ is normally asserted by the initiator to request a Message Out bus phase. Note that since Assert SEL/ and Assert ATN/ are in the same register, a select with ATN/ may be implemented with one MPU write. ATN/ may be deasserted by resetting this bit to a 0. A read of this register bit simply reflects the status of this bit.

ADB **Assert Data Bus** **0**

When set, the Assert Data Bus bit allows the contents of the Output Data (ODR) register to be enabled as chip outputs on the signals DB0/–DB7/. Parity is also generated and asserted on DBP/. Resetting this bit disables the output data bus.

When the LSI53C040 is connected as an Initiator, the outputs are only enabled if the Target Mode bit (Mode register 0xFC02, bit 6) is false, the received SCSI I/O signal is false, and the phase signals (C/D, I/O, and MSG) match the contents of the Assert C_D/, Assert I_O/, and Assert MSG/ in the Target Command (TC) register (0xFC03).

This bit should also be set during DMA send operations.

Register: 0xFC02

Mode (MR)
Read/Write

7	6	5	4	3	2	1	0
AS_LVD	TGTM	EPC	EPI	R	MB	DM	ARB
0	0	0	0	0	0	0	0

AS_LVD **Arbitration/Selection LVD** **7**

This bit must be set to perform arbitration, selection, and reselection, and must be cleared upon successful completion of selection or reselection prior to asserting the data bus for any information transfer phases. When set, this bit causes the SCSI data bus to operate in open drain mode, which is a requirement of LVD SCSI as defined in the SPI-2 draft standard. Operation of this bit does not effect SCSI SE mode.

TGTM **Target Mode** **6**

The Target Mode bit allows the SCSI core to operate as either a SCSI bus initiator (bit reset to 0) or as a SCSI bus target device (bit set to 1). In order for the signals ATN/ and ACK/ to be asserted on the SCSI bus, the Target Mode bit must be reset (0). In order for the signals C_D/, I_O/, MSG/ and REQ/ to be asserted on the SCSI bus, the Target Mode bit must be set (1).

EPC **Enable Parity Checking** **5**

The Enable Parity Checking bit determines whether parity errors will be ignored or saved in the parity error latch. If this bit is reset (0), parity will be ignored. Conversely, if this bit is set (1), parity errors will be saved.

EPI **Enable Parity Interrupt** **4**

The Enable Parity Interrupt bit, when set to a 1, causes an interrupt to occur if a parity error is detected. A parity interrupt will only be generated if the Enable Parity Checking bit (bit 5) is also enabled.

R **Reserved** **3**

This bit must be cleared to 0.

MB **Monitor Busy** **2**

The Monitor Busy bit, when set to a 1, causes an interrupt to be generated for an unexpected loss of BSY/.

When the interrupt is generated due to loss of BSY/, the lower 6 bits of the Initiator Command (ICR) register (0xFC01) are reset and all signals are removed from the SCSI bus.

DM **DMA Mode** **1**

The DMA Mode bit is used to enable a DMA transfer and must be set to 1 prior to writing SCSI registers 0xFC05 through 0xFC07 to start DMA transfers. The Target Mode bit (Mode register 0xFC02, bit 6) must be consistent with writes to registers 0xFC06 and 0xFC07 (i.e., set to 1 for a write to register 0xFC06 and reset for a write to register 0xFC07). The Assert Data Bus bit (register 0xFC01, bit 0) must be set to 1 for all DMA send operations. In the DMA mode, REQ/ and ACK/ are automatically controlled.

The DMA Mode bit is not reset at the end of a DMA transfer; DMA mode must be turned off by writing a 0 into this bit location. However, care must be taken not to write to any SCSI register during a DMA byte transfer.

Note: The BSY/ signal must be active in order to set the DMA Mode bit.

ARB **Arbitrate** **0**

The Arbitrate bit is set to 1 to start the arbitration process. Prior to setting this bit, the Output Data (ODR) register should contain the proper SCSI device ID value. Only one data bit should be active for SCSI bus arbitration. The SCSI core will wait for a bus free condition for entering the arbitration phase. The results of the arbitration phase may be determined by reading the status bits LA and AIP (ICR register 0xFC01, bits 5 and 6 respectively). Write a 0 to this bit after completion of the arbitration phase.

Register: 0xFC03
Target Command (TC)
Read/Write

7	6		4	3	2	1	0
LBS	R			AREQ	AMSG	ACD	AIO
0	0	0	0	0	0	0	0

When connected as a target device, the Target Command register allows the microcontroller to control the SCSI bus information transfer phase and/or to assert REQ/ simply by writing this register. The Target Mode bit (register 0xFC02, bit 6) must be set (1) for bus assertion to occur. When connected as an initiator with DMA Mode true, if the phase lines (I_O/, C_D/, and MSG/) do not match the phase bits in this register, a phase mismatch interrupt is generated when REQ/ goes active. In order to send data as an initiator, the Assert I_O/, Assert C_D/ and Assert MSG/ bits must match the corresponding bits in the Current SCSI Bus Status (CSBS) register (0xFC04). The Assert REQ/ bit (bit 3) has no meaning when the LSI53C040 is operating as an initiator.

LBS **Last Byte Sent** **7**

In initiator mode, the SCSI core uses this bit to determine when the last byte of a DMA transfer is sent to the SCSI bus. This flag is necessary since the End of DMA bit in the Bus and Status (BSR) register only reflects when the last byte was received from the DMA function.

R **Reserved** **[6:4]**

AREQ **Assert REQ/** **3**

AMSG **Assert MSG/** **2**

ACD **Assert C_D/** **1**

AIO **Assert I_O/** **0**

These bits, when read together, give the current SCSI bus phase. Table 4.2 describes the SCSI bus phases that correspond to all possible values of these bits.

Table 4.2 SCSI Phase Bit Values

Bus Phase	Assert MSG/	Assert CD/	Assert IO/
Data Out	0	0	0
Undefined	1	0	0
Command	0	1	0
Message Out	1	1	0
Data In	0	0	1
Undefined	1	0	1
Status	0	1	1
Message In	1	1	1

Register: 0xFC04

Current SCSI Bus Status (CSBS)
Read Only

7	6	5	4	3	2	1	0
RST	BSY	REQ	MSG	C_D	I_O	SEL	DBP
x	x	x	x	x	x	x	x

The Current SCSI Bus Status register is a read only register that monitors seven SCSI bus control signals plus the data bus parity bit. For example, an initiator device can use this register to determine the current bus phase and to poll REQ/ for pending data transfers. The SCSI bus status information in this register may also help determine why a particular interrupt occurred.

RST **SCSI Reset** **7**

BSY **Busy** **6**

REQ **Request** **5**

MSG **Message** **4**

C_D **Command/Data** **3**

I_O **Input/Output** **2**

SEL	**Select**	**1**
DBP	**Data Bus Parity**	**0**

Register: 0xFC04

Select Enable (SER)
Write Only

7							0
SE							
x	x	x	x	x	x	x	x

SE **Selection ID bits** **[7:0]**

The Select Enable register is a write only register that is used as a mask to monitor a single ID during a selection attempt. The simultaneous occurrence of the corresponding ID bit, BSY/ false and SEL/ true will cause an interrupt. This interrupt can be disabled by resetting all bits in this register and in the Select Enable High (SENHI) register (0xFC0C). If the Enable Parity Checking bit (register 0xFC02, bit 5) is active (1), parity will be checked during selection.

Register: 0xFC05

Bus and Status (BSR)
Read Only

7	6	5	4	3	2	1	0
EOD	R	PERR	IRA	PMATCH	BERR	ATN	ACK
0	0	0	0	x	0	SATN/	SACK/

The Bus and Status register is a read only register that can be used to monitor the remaining SCSI control signals not found in the Current SCSI Bus Status (CSBS) register (ATN/ and ACK/), as well as six other status bits.

EOD **End of DMA Transfer** **7**

The End of DMA Transfer bit is set when a DMA transfer completes. The REQ/ and ACK/ signals should be monitored to ensure that the last byte has been transferred. This bit is reset when the DMA Mode bit is reset (0) in the Mode (MR) register (0xFC02).

The SCSI core contains a true End of DMA Status bit (last byte sent) in bit 7 of the Target Command (TC) register.

R **Reserved** **6**

PERR **Parity Error** **5**
This bit is set if a parity error occurs during a data receive or a device selection. The Parity Error bit can only be set (1) if the Enable Parity Check bit (register 0xFC02, bit 5) is active (1). This bit may be cleared by reading the Reset Parity/Interrupt (RPI) register (0xFC07).

IRA **Interrupt Request Active** **4**
This bit is set if an enabled interrupt condition occurs. It can be cleared by reading the Reset Parity/Interrupt (RPI) register (0xFC07).

PMATCH **Phase Match** **3**
The SCSI signals MSG/, C_D/, and I_O/ represent the current information transfer phase. The Phase Match bit indicates whether the current SCSI bus phase matches the lower three bits of the Target Command (TC) register. Phase Match is continuously updated and is only significant when the LSI53C040 is operating as a bus initiator. A phase match is required for data transfers to occur on the SCSI bus.

BERR **Busy Error** **2**
The Busy Error bit is active if an unexpected loss of the BSY/ signal has occurred. This level sensitive latch is set whenever the Monitor Busy bit (register 0xFC02, bit 2) is true and BSY/ is asserted. An unexpected loss of BSY/ will disable any SCSI outputs and will reset the DMA Mode bit (register 0xFC02, bit 1).

ATN **Attention** **1**
This bit reflects the condition of the SCSI bus control signal ATN/. This signal is normally monitored by a target device.

ACK **Acknowledge** **0**
This bit reflects the condition of the SCSI bus control signal ACK/. This signal is normally monitored by a target device.

Register: 0xFC05

DMA Send (DSR)
Write Only

This register does not have individual bit definitions. Any write to this register will initiate a DMA send, from the DMA core to the SCSI bus, for either initiator or target role operations. The DMA Mode bit (register 0xFC02, bit 1) must be set prior to writing this register.

Register: 0xFC06

Start DMA Target Receive (SDTR)
Write Only

This register does not have individual bit definitions. Any write to this register will initiate a DMA receive, from the SCSI bus to the DMA core, for target operation only. The DMA Mode bit (register 0xFC02, bit 1) and the Target Mode bit (register 0xFC02, bit 6) must both be set prior to writing this register.

Register: 0xFC07

Reset Parity/Interrupt (RPI)
Read Only

This register does not have individual bit definitions. Any read to this register resets the Parity Error bit (register 0xFC05, bit 5), the Interrupt Request Active bit (register 0xFC05, bit 4), and the Busy Error bit (register 0xFC05, bit 2).

Register: 0xFC07

Start DMA Initiator Receive (SDIR)
Write Only

This register does not have individual bit definitions. Any write to this register will initiate a DMA receive from the SCSI bus, for initiator operation only. The DMA Mode bit (register 0xFC02, bit 1) must be set (1) and the Target Mode bit (register 0xFC02, bit 6) must be clear (0) prior to writing this register.

Register: 0xFC08

Current SCSI Data High (CSDHI)
Read Only

7	6	5	4				0
SHID2	SHID1	SHID0	R				
0	0	0	0	0	0	0	0

SHID[2:0] **Current SCSI Data High** **[7:5]**
The Current SCSI Data High register is a read only register that allows the microcontroller to read the active SCSI High ID data bus. This register is used during arbitration to check for higher priority arbitrating devices. No parity is generated because only three of the lines are valid.

R **Reserved** **[4:0]**

Register: 0xFC0C

Select Enable High (SENHI)
Write Only

7	6	5	4				0
SHID2	SHID1	SHID0	R				
x	x	x	0	0	0	0	0

SHID[2:0] **SCSI High ID** **[7:5]**
The Select Enable Register High for the SCSI High ID lines is a write only register that is used as a mask to monitor a single ID during a selection attempt. The simultaneous occurrence of BSY/ false and SEL/ true and the correct ID bit, will cause an interrupt. This interrupt

can be disabled by resetting all bits in this register and in the Select Enable (SER) register (0xFC04). No parity is generated because only three of the lines are valid.

R **Reserved** **[4:0]**

Register: 0xFC10

DMA Status (DS)
Read/Write

7		5	4	3	2	1	0
R			IOD	TC	R	IEN	TIP
0	0	0	x	x	0	x	x

The DMA function in the LSI53C040 provides the capability of transferring up to 256 bytes from memory to the SCSI port or vice versa. The DMA function is designed to handshake automatically with the SCSI core, to offload the microcontroller and increase SCSI throughput. The DS register provides basic control of the DMA function, the DMA Transfer Length (DTL) register sets the 8-bit transfer length (1 to 256), and the DMA Source/Destination Low (DSDL) (0xFC12) and DMA Source/Destination High (DSDH) (0xFC13) registers set the 16-bit source or destination address for the data to be transferred. The DMA function does not provide any additional capability for handling SCSI protocol, so all phase changes and error conditions must still be handled manually by the microcontroller. The DMA direction is based solely on the SCSI I/O phase lines.

R **Reserved** **[7:5]**

IOD **I/O Direction** **4**
This status bit will indicate the current DMA direction. This bit is written by the microcontroller. A high on this bit indicates the DMA is reading bytes from the SCSI core and writing them to memory. A low on this bit indicates the DMA is reading bytes from memory and writing them to the SCSI core.

TC **Transfer Complete** **3**
This read only status bit will read a 1 following the normal completion of a DMA transfer.

R	**Reserved**	**2**

IEN **Interrupt Enable** **1**

When this bit is set to a 1, the DMA function will generate an interrupt whenever the TIP bit transitions from a 1 to a 0. This signifies that (1) the transfer completed normally, or (2) the TIP bit was written to a 0, which manually interrupted the transfer.

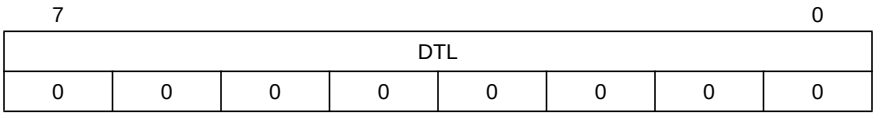
TIP **Transfer in Progress** **0**

When this bit is written to a 1, the DMA function will begin a transfer. The transfer length is specified in the DMA Transfer Length (DTL) register (0xFC11) and the data source or destination addresses are specified in the DMA Source/Destination Low (DSDL) (0xFC12) and DMA Source/Destination High (DSDH) (0xFC13) registers. The read value of this bit will stay 1 until either (1) the transfer completes normally, or (2) this bit is written to a 0, which can only be done when the DMA is not active. While this bit is 0, the other status bits in this register will be valid and the DTL register will hold the remaining transfer count. Conditions for which the SCSI core will interrupt are discussed in Chapter 2.

Register: 0xFC11

DMA Transfer Length (DTL)

Read/Write



DTL **Data Transfer Length** **[7:0]**

These register bits store the 8-bit transfer length for the DMA function. This register should be set to a value between 0x00 and 0xFF prior to setting bit 0 (TIP) of the DMA Status (DS) register to initiate a transfer. Setting this register to a value of 0 corresponds to a desired transfer length of 256 bytes. When the transfer ends or is interrupted, this register will read the value of the number of bytes remaining in the transfer.

Register: 0xFC12

DMA Source/Destination Low (DSDL)
Read/Write

7							0
DSDL							
0	0	0	0	0	0	0	0

DSDL **DMA Source/Destination Low** **[7:0]**
These register bits store the least significant byte of the DMA function's source address for send transfers and destination address for receive transfers. The read value of the DSDL and DMA Source/Destination High (DSDH) registers tracks the current source/destination address of the transfer. If the transfer is interrupted for any reason, the DSDL and DSDH registers will hold the next address required, in case the interrupted transfer resumes.

Register: 0xFC13

DMA Source/Destination High (DSDH)
Read/Write

7							0
DSDH							
0	0	0	0	0	0	0	0

DSDH **DMA Source/Destination High** **[7:0]**
These register bits store the most significant byte of the DMA function's source address for send transfers and destination address for receive transfers. The read value of the DMA Source/Destination Low (DSDL) and DSDH registers tracks the current source/destination address of the transfer. If the transfer is interrupted for any reason, the DSDL and DSDH registers hold the next address required, in case the interrupted transfer resumes.

Register: 0xFC14

DMA Interrupt (DMAI)

Read/Write

7						1	0
R							INT
0	0	0	0	0	0	0	

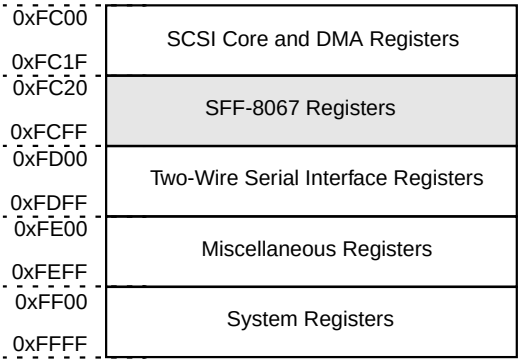
R	**Reserved**	**[7:1]**
INT	**DMA Interrupt** This register bit is the interrupt value for the DMA. This interrupt will only be enabled if the IEN bit in the DMA Status register is set.	**0**

Chapter 5
SFF-8067 Registers

This chapter contains descriptions of the LSI53C040 SFF-8067 registers. The SCSI/DMA registers, Two-Wire Serial registers, Miscellaneous registers, and System registers are described in Chapter 4 and Chapter 6 through Chapter 8. The term “set” is used to refer to bits that are programmed to a binary one, while the terms “reset” or “clear” are used to refer to bits that are programmed to binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Reserved bit functions may change at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default bit values, which are enabled after the chip is powered on or reset.

Figure 5.1 summarizes the entire LSI53C040 register set.

Figure 5.1 Register Set Overview



The SFF-8067 Interface register set allows observation and control of the two SFF-8067 interface ports which are designated as port 0 and port 1. The registers associated with port 0 occupy addresses 0xFC20 through 0xFC27 and the registers associated with port 1 occupy addresses 0xFC28 through 0xFC2F. To conserve space, the register descriptions only appear once in this chapter. The two applicable locations are separated by a slash (/), with the port 0 address listed first.

Table 5.1, the register map, summarizes the SFF-8067 registers in graphical form.

Table 5.1 SFF-8067 Interface Registers

31 16 15 0	Port	Address
Read Data (RDATA0)	0	0xFC20
Write Data (WDATA0)	0	0xFC21
Port Control/Status (PCST0)	0	0xFC22
Physical Address (PHAD0)	0	0xFC23
Live ESI (LESI0)	0	0xFC24
Manual Data Output (MDATA0)	0	0xFC25
Reserved	–	0xFC26–0xFC27
Read Data (RDATA1)	1	0xFC28
Write Data (WDATA1)	1	0xFC29
Port Control/Status (PCST1)	1	0xFC2A
Physical Address (PHAD1)	1	0xFC2B
Live ESI (LESI1)	1	0xFC2C
Manual Data Output (MDATA1)	1	0xFC2D
Reserved	–	0xFC2E–0xFC2F

Register: 0xFC20/0xFC28

Read Data (RDATA0/RDATA1)
Read/Write

7							0
DB							
0	0	0	0	0	0	0	0

DB **8067 Read Data** **[7:0]**

The Read Data bits are read/write bits that contain data to be transferred out on the associated 8067 port in response to a read request at that port.

Register: 0xFC21/0xFC29

Write Data (WDATA0/WDATA1)
Read/Write

7							0
DB							
0	0	0	0	0	0	0	0

DB **8067 Write Data** **[7:0]**

The Write Data registers are read/write registers that contain data which is transferred in on the associated 8067 port in response to a write request at that port.

Register: 0xFC22/0xFC2A

Port Control/Status (PCST0/PCST1)
Read/Write

7	6	5	4	3	2	1	0
PME	R		BSY	RRF	WRF	RINT	WINT
0	0	0	0	0	0	0	0

PME **Port Manual Enable** **7**

The microcontroller sets this bit to enable 8067 manual mode for the associated port. When manual mode is enabled the microcontroller has direct control over the associated 8067 port using the MDATA (0xFC25/0xFC2D) register, which contains output data,

and the LESI (0xFC24/0xFC2C) register, which is used to read the port pins. Setting this bit disables automatic receive or transmit over the 8067 interface.

R **Reserved (read only)** **[6:5]**

BSY **Port Busy Flag** **4**
This bit is set to a 1 when the associated 8067 port is in any state other than idle. Writing a 0 to this bit will remove the lockout to the other 8067 port. This bit should only be cleared when the device connected to this port is not responding. Therefore, a 0x10 should be written to this register when clearing interrupts.

RRF **Read Register Full (read only)** **3**
This read only bit is written to a 1 when a read request has been made from the associated 8067 port and the microcontroller loads the RDATAx (0xFC20/0xFC28) register. This bit is cleared by the associated 8067 port when the register data has been transferred onto the associated 8067 port and acknowledged.

WRF **Write Register Full (read only)** **2**
This bit is written to a 1 by the associated 8067 port when a byte of data has been loaded into the WDATAx (0xFC21/0xFC29) register from the associated 8067 port. When the microcontroller reads the WDATAx (0xFC21/0xFC29) register this bit will be automatically cleared. This bit is read only.

RINT **Read Interrupt** **1**
This bit is written to a 1 by the associated 8067 port when a read request has been made from the associated 8067 port. This notifies the microcontroller to load the RDATAx (0xFC20/0xFC28) register. The WINT and the RINT bits are ORed together to generate the port interrupt, which goes to the microcontroller using the Interrupt Status (ISR) register (0xFE04).

WINT **Write Interrupt** **0**
This bit is written to a 1 by the associated 8067 port when a byte of data has been loaded into the WDATAx (0xFC21/0xFC29) register from the associated 8067 port. This notifies the microcontroller to read the WDATAx (0xFC21/0xFC29) register. The WINT and the RINT bits

are ORed together to generate the port interrupt, which goes to the microcontroller using the Interrupt Status (ISR) register.

Note: The RINT and WINT bits are not self-clearing, so the microcontroller must clear this bit if the port is interrupt driven.

Register: 0xFC23/0xFC2B

Physical Address (PHAD0/PHAD1)
Read Only

7							0
PA							
x	x	x	x	x	x	x	x

PA **Physical Address** **[7:0]**
The Physical Address registers are read only registers that contain values of the PA inputs.

Register: 0xFC24/0xFC2C

Live ESI (LESI0/LESI1)
Read Only

7	6	5	4	3	2	1	0
PESI/	DWR/	RD/	ACK/	D3	D2	D1	D0
x	x	x	x	x	x	x	x

PESI/ **PARALLEL_ESI/ Value** **7**
Reading this active low bit gives the state of the PESI/ signal, which is used to select between the SEL_ID and the bidirectional interface that distinguishes the SFF-8067 interface from SFF-8045.

DWR/ **DSK_WR/ Value** **6**
Reading this active low bit gives the state of the DSK_WR/ signal on the SFF-8067 interface. When this active low bit is cleared, the drive is ready to write data to the LSI53C040. It will be cleared (0) if the PESI/ bit is cleared (0). If PESI/ is 1, this bit reflects the value of the PA6 signal.

RD/ **DSK_RD/ Value** **5**
Reading this active low bit gives the state of the DSK_RD/ signal on the SFF-8067 interface. When this active low bit is cleared, the drive is ready to read data from the LSI53C040. It will be cleared (0) if the PESI/ bit is cleared (0). If PESI/ is 1, this bit reflects the value of the PA5 signal.

ACK/ **ENCL_ACK/ Value** **4**
Reading this active low bit gives the state of the ENCL_ACK/ signal on the SFF-8067 interface. It will be cleared (0) if the PESI/ bit is cleared (0). If PESI/ is 1, this bit reflects the value of the PA4 signal.

D[3:0] **8067 Interface Data Nibble Bits** **[3:0]**
Reading these bits gives the contents of the D[3:0] signals on the SFF-8067 interface. If PESI/ is 1, these bits reflect the value of the PA[3:0] signals.

Register: 0xFC25/0xFC2D

Manual Data Output (MDATA0/MDATA1)
Read/Write

7	6	5	4	3	2	1	0
PESI/	DWR/	RD/	ACK/	D3	D2	D1	D0
1	1	1	1	1	1	1	1

The values in these registers are asserted onto the SFF-8067 bus when the PME bit is set in the PCSTx registers (0xFC22/0xFC2A). These signals are open drain on the SFF-8067 bus. Therefore, a 1 written to this register is considered a “soft” value and can be pulled low by another device on the bus.

PESI/ **PARALLEL_ESI/ Value** **7**
This active low bit is used to change the state of the PESI/ signal, which is used to select between the SEL_ID and the bidirectional interface that distinguishes the SFF-8067 interface from SFF-8045.

DWR/ **DSK_WR/ Value** **6**
When this active low bit is cleared, the drive is ready to write data to the LSI53C040.

RD/ **DSK_RD/ Value** **5**
When this active low bit is cleared, the drive is ready to read data from the LSI53C040.

ACK/ **ENCL_ACK/ Value** **4**
This active low bit is cleared as an acknowledge signal driven by the LSI53C040 in discovery, read, and write operations.

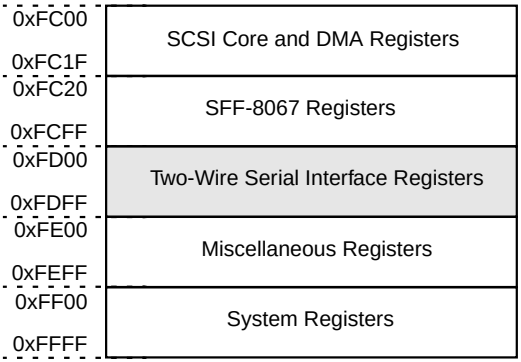
D[3:0] **8067 Interface Data Nibble Bits** **[3:0]**
These bits contain the current data nibble for the D[3:0] signals in read/write operations.

Chapter 6
Two-Wire Serial Registers

This chapter contains descriptions of the LSI53C040 Two-Wire Serial interface registers. The SCSI/DMA registers, SFF-8067 registers, Miscellaneous registers, and System registers are described in Chapter 4, Chapter 5, Chapter 7, and Chapter 8. The term “set” is used to refer to bits that are programmed to a binary one, while the terms “reset” or “clear” are used to refer to bits that are programmed to binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default bit values, which are enabled after the chip is powered on or reset.

Figure 6.1 summarizes the entire LSI53C040 register set.

Figure 6.1 Register Set Overview



All registers for the Two-Wire Serial interface 0, other than the Control register, are accessed through Register 0xFD00. All registers for the Two-Wire Serial interface 1, other than the Control register, are accessed through Register 0xFD02. To select one of the three registers available at address 0xFD00 or 0xFD02, write the desired value to the ES[0:2] bits in the Control register (0xFD01 or 0xFD03). To conserve space, the register descriptions only appear once in this chapter. The two applicable locations are separated by a slash, with the Two-Wire Serial interface 0 address listed first.

Table 6.1, the register map, summarizes the Two-Wire Serial registers in graphical form.

Table 6.1 Two-Wire Serial Registers

31 16 15 0	ES[0:2]	Definition	Address
Two-Wire Serial Interface 0 Register Access	000	Own Address	0xFD00
	010	Clock	
	100	Data	
Two-Wire Serial Interface 0 Control/Status	N/A	Control and Status Write	0xFD01
	0xx (ES0 = 0)	Control Reads	
	1xx (ES0 = 1)	Status Reads	
Two-Wire Serial Interface 1 Register Access	000	Own Address	0xFD02
	010	Clock	
	100	Data	
Two-Wire Serial Interface 1 Control/Status	N/A	Control and Status Write	0xFD03
	0xx (ES0 = 0)	Control Reads	
	1xx (ES0 = 1)	Status Reads	
MISC	N/A	Miscellaneous	0xFD04
Two-Wire Serial Interface 0 Manual Control	N/A	TWS Manual Control	0xFD05
Two-Wire Serial Interface 1 Manual Control	N/A	TWS Manual Control	0xFD06

Register: 0xFD00/0xFD02

Own Address (ES0, ES1, ES2 = 000)
Read/Write

7	6						0
R	A[6:0]						
1	0	1	0	1	0	1	0

R **Reserved** **7**

A[6:0] **Own Address** **[6:0]**
This register contains the address that is used for slave mode operation. If the first byte of transmission matches this bit pattern, then the AAS bit in the Two-Wire Serial interface 0 Control/Status register (0xFD01/0xFD03) will be made active. Note that the data in this register is shifted by one bit for comparisons, as the read/write bit is transmitted along with the slave address. This register should be programmed even if slave mode is not supported by the firmware. If this register is not programmed to a value other than zero, then the interface will be in a monitor state and will only provide bus status.

Register: 0xFD00/0xFD02

Clock (ES0, ES1, ES2 = 010)
Read/Write

7		5	4		2	1	0
R			ICF[2:0]			ASF[1:0]	
0	0	0	0	0	0	0	0

R **Reserved** **[7:5]**

ICF **Intermediate Clock Frequency** **[4:2]**

ASF **Active SCL Frequency** **[1:0]**
This register contains a value used to control the Two-Wire Serial bus clock frequency based upon the following tables and equation:

$$IIC\_Frequency(SLC) = \frac{f_{clk}}{(D0 \bullet D1)}$$

ICF2	ICF1	ICF0	D0
0	x	x	2
1	0	0	3
1	0	1	4
1	1	0	5
1	1	1	8

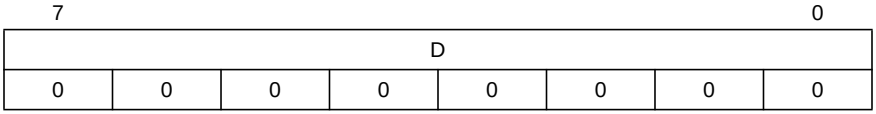
ASF1	ASF0	D1
0	0	16
0	1	32
1	0	128
1	1	1024

Examples:

1. A 40 MHz input clock and a maximum 400 kHz SCL output would require D1*D0 to be greater than 100. A best fit would be for D1 to be 32 and D0 to be 4. The value written into the register would be 0x15. This will yield a 312.5 kHz SCL output clock speed.
2. A 40 MHz input clock and a maximum 100 kHz SCL output would require D1*D0 to be greater than 400. A best fit would be for D1 to be 128 and D0 to be 4. The value written into the register would be 0x16. This would yield a 78.125 kHz SCL output clock speed.

Register: 0xFD00/0xFD02

Data (ES0, ES1, ES2 = 100)
Read/Write



D **Data** **[7:0]**

This register is used for data transmission to and reception from the Two-Wire Serial bus. During a transmit operation, the data is sent out onto the Two-Wire Serial bus after writing this register. During a receive operation, this register must be read to request a byte from the slave device. This prescribes a dummy read of this register to

start data flowing. Each operation will activate the PIN bit located in the Two-Wire Control register [0xFD01/0xFD03 (ES0=1)].

Register: 0xFD01/0xFD03

Control Register Writes

Write Only

7	6	5	4	3	2	1	0
PIN	ES0	ES[1:2]		ENI	STA	STO	ACK
0	0	0	0	0	0	0	0

PIN **Pending Interrupt** **7**

Setting this bit clears the interrupt and all of the status bits.

ES0 **Enable Serial Output** **6**

This bit enables the Two-Wire Serial bus I/O. When low (0), register access is available for initialization. If high (1), then communication with the serial shift register S0 and status register S1 are accessible.

ES[1:2] **Register Selection Bits** **[5:4]**

These bits select the Two-Wire Serial register that is read/written by accessing the Two-Wire Serial interface 0 register location.

ES0	ES1	ES2	Description
0	0	0	R/W Own Register
0	1	0	R/W Clock Register
1	0	0	R/W Data Register

ENI **External Interrupt Enable** **3**

Setting this bit enables the interrupt output to the microcontroller when the PIN bit (0xFD01/0xFD03, bit 7) is cleared (0). It causes the corresponding bit to be set in the Interrupt Status (ISR) register, if the Two-Wire Serial interrupt is not masked in the Interrupt Mask (IMR) register.

STA **Start** **2**

When set, this bit signifies that the byte located in the Two-Wire Register 0xFD00/0xFD02 [(ES0, ES1, ES2 =

100] - Data Register) will be sent out on the Two-Wire Serial bus with a start condition as defined in the Inter-Integrated Circuit specification.

STO **Stop** **1**
When set, this bit signifies that a stop condition (as described in the Inter-Integrated Circuit specification) will be sent out onto the interface.

ACK **Acknowledge** **0**
When set, this bit will enable an ACK to be transmitted during the ninth clock cycle of the transfer after receiving a data byte.

Register: 0xFD01/0xFD03

Control Register Reads (ES0 = 0)
Read Only

7	6	5	4	3	2	1	0
PIN	ES0	ES[1:2]		ENI	STA	STO	ACK
0	0	0	0	0	0	0	0

PIN **Pending Interrupt** **7**
Setting this bit clears the interrupt and all of the status bits.

ES0 **Enable Serial Output** **6**
This bit enables the Two-Wire Serial bus I/O. When low (0), register access is available for initialization. If high (1), then the serial shift register S0 and status register S1 are accessible.

ES[1:2] **Register Selection Bits** **[5:4]**
These bits select the Two-Wire Serial register that is read/written by accessing the Two-Wire Serial interface 0 register location.

ES0	ES1	ES2	Description
0	0	0	R/W Own Register
0	1	0	R/W Clock Register
1	0	0	R/W Data Register

ENI **External Interrupt Enable** **3**

Setting this bit enables the interrupt output to the microcontroller when the PIN bit (0xFD01/0xFD03, bit 7) is cleared (0). It causes the corresponding bit to be set in the Interrupt Status (ISR) register, if the Two-Wire Serial interrupt is not masked in the Interrupt Mask (IMR) register.

STA **Start** **2**

When set, this bit signifies that the byte located in the Data register [0xFD00/0xFD02 (ES0, ES1, ES2 = 100] will be sent out on the Two-Wire Serial bus with a start condition as defined in the Inter-Integrated Circuit specification.

STO **Stop** **1**

When set, this bit signifies that a stop condition as defined in the Inter-Integrated Circuit specification will be sent out onto the interface.

ACK **Acknowledge** **0**

When set, this bit will enable an ACK to be transmitted during the ninth clock cycle of the interface after receiving a data byte.

Register: 0xFD01/0xFD03

Status Register Reads (ES0 = 1)
Read Only

7	6	5	4	3	2	1	0
PIN	RPSS	STS	BER	LRB/AD0	AAS	LAB	BB_N
0	0	0	0	0	0	0	0

PIN **Pending Interrupt Not** **7**

This active low bit is cleared when the Data register has completed an operation and requires microcontroller intervention to continue operation.

RPSS **Repeated Start** **6**

This bit indicates that a repeated start condition occurred on the bus, but only when this interface was involved in the original transfer.

STS **Slave Mode Stop** **5**
This bit is set if the STOP condition is detected when the LSI53C040 is in slave receive mode.

BER **Bus Error Detection** **4**
This bit is set if a bus error is detected by the LSI53C040, (i.e., Misplaced Start or Stop). Setting this bit clears the BB_N bit and resets the PIN bit.

LRB/AD0 **Last Received Bit/Address 0 Bit** **3**
This bit specifies one of the following, depending on the state of the protocol when this bit is set (for more information, refer to Figure 2.11, page 2-19).

- If the slave selection address was the preprogrammed Own Address register value (logic 0) or the General Call address (logic 1) during Slave Selection operation, this bit indicates a read (1) or write (0) request.
- The last bit received during data transfer. Useful for testing ACK reception from a slave device.

AAS **Addressed as Slave** **2**
When active (1), this bit signifies that an address was received across the two-wire data register interface that matches the programmed Own Address (ES0, ES1, ES2 = 000) register (0xFD00/0xFD02) setting. When this bit is cleared, the address matches the general call address.

LAB **Lost Arbitration Bit** **1**
In a multiple master environment, if the LSI53C040 loses arbitration to another master on the bus, then it will relinquish control to the other master and set this bit. It should be noted that if two masters are simultaneously active on the Data register interface requesting the exact same operation, then the two masters will not observe each other and a parallel operation has occurred.

BB_N **Bus Busy** **0**
When active (logic 0), this active low bit signifies that the Data register interface is currently in use and access is not possible. It is activated upon detection of a start condition and deactivated upon detection of a stop condition.

Register: 0xFD04

Miscellaneous

Read Only

7						1	0
R							CKSUM
0	0	0	0	0	0	0	0

R **Reserved** **[7:1]**

CKSUM **Checksum Error** **0**
This bit is set if an error was detected when checking the checksum value after download.

Register: 0xFD05

UC Control ITF1

Read/Write

7		5	4	3	2	1	0
R			SDAI1	SCLI1	SDAO1	SCLO1	CTL1
0	0	0	1	1	1	1	1

R **Reserved** **[7:5]**

SDAI1 **ITF1 SDA Input** **4**
This bit indicates the current value on the SDA1 pin.

SCLI1 **ITF1 SCL Input** **3**
This bit indicates the current value on the SCL1 pin.

SDAO1 **ITF1 SDA Output** **2**
When the CTL1 bit is low, this bit will be the value output on the SDA1 pin.

SCLO1 **ITF1 SCL Output** **1**
When the CTL1 bit is low, this bit will be the value output on the SCL1 pin.

CTL1 **ITF1 Control** **0**
When this bit is high, the microcontroller does not have control over the TWS interface #1 SCL and SCA output lines. When low, the values for SCLO1 and SDAO1 will be output on the TWS interface #1 bus.

Register: 0xFD06

UC Control ITF0

Read/Write

7		5	4	3	2	1	0
R			SDAI0	SCLI0	SDAO0	SCLO0	CTL0
0	0	0	1	1	1	1	1

R **Reserved** **[7:5]**

SDAI0 **ITF0 SDA Input** **4**
This bit indicates the current value on the SDA0 pin.

SCLI0 **ITF0 SCL Input** **3**
This bit indicates the current value on the SCL0 pin.

SDAO0 **ITF0 SDA Output** **2**
When the CTL0 bit is low, this bit will be the value output on the SDA0 pin.

SCLO0 **ITF0 SCL Output** **1**
When the CTL0 bit is low, this bit will be the value output on the SCL0 pin.

CTL0 **ITF0 Control** **0**
When this bit is high, the microcontroller does not have control over the TWS interface #0 SCL and SCA output lines. When low, the values for SCLO0 and SDAO0 will be output on the TWS interface #0 bus.

Chapter 7
Miscellaneous Registers

This chapter contains descriptions of the LSI53C040 Miscellaneous registers. The SCSI/DMA registers, SFF-8067 registers, Two-Wire Serial registers, and System registers are described in Chapter 4 through Chapter 7, and Chapter 8. The term “set” is used to refer to bits that are programmed to a binary one, while the terms “reset” or “clear” are used to refer to bits that are programmed to binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default bit values, which are enabled after the chip is powered on or reset.

Figure 7.1 summarizes the entire LSI53C040 register set.

Figure 7.1 Register Set Overview

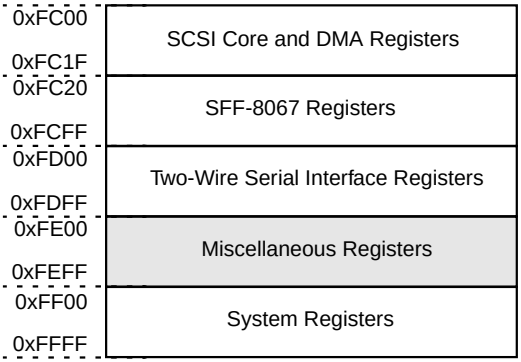


Table 7.2, the register map, summarizes the Miscellaneous registers in graphical form.

Table 7.1 Miscellaneous Registers

31 16 15 0	Address
Watchdog Timer Control (WDTC)	0xFE00
Watchdog Secondary Chain (WDSC)	0xFE01
Watchdog Final Chain (WDFC)	0xFE02
Miscellaneous Control (MCR)	0xFE03
Interrupt Status (ISR)	0xFE04
Timer 1 Control (T1C)	0xFE05
Timer 1 Threshold (T1TH)	0xFE06
Timer 1 Secondary Chain (T1SC)	0xFE07
Timer 1 Final Chain (T1FC)	0xFE08
Timer 2 Control (T2C)	0xFE09
Timer 2 Threshold (T2T)	0xFE0A
Timer 2 Secondary Chain (T2SC)	0xFE0B
Timer 2 Final Chain (T2FC)	0xFE0C
Interrupt Mask (IMR)	0xFE0D
Interrupt Destination (IDR)	0xFE0E
Reserved	0xFEF0–0xFEF5

Register: 0xFE00

Watchdog Timer Control (WDTC)
Read/Write

7	6		4	3	2	1	0
WDRBT	R			WTHR[3:0]			
0	0	0	0	0	0	0	0

The LSI53C040 includes a built-in watchdog timer, which causes a soft reset when it expires. If the watchdog timer expires and forces a chip reset, the reset pad will also assert a low output for resetting other external functions if the Enable Reset Output bit is set (0xFF05, bit 7). If the watchdog timer is used, the LSI53C040 firmware needs to periodically clear the watchdog timer. The watchdog timer reinitializes the LSI53C040 if the firmware does not clear the timer before time-out. The watchdog timer is cleared with any write to the Watchdog Timer Control (WDTC) register. This register is not affected by a soft reset.

In hardware, the timer consists of three divider chains. The primary divider divides the system clock by a factor of 4000, yielding a 10 kHz clock to the secondary chain when the internal system clock is 40 MHz. The secondary chain divides the primary chain output by a factor of 100, yielding a 100 Hz clock. The final chain divides the secondary chain by the programmable value in the Watchdog Timer Control (WDTC), represented by bits 3 through 0.

WDRBT **Watchdog Reboot** **7**
This read/write register bit, when set, indicates that the LSI53C040 has performed a soft reset, or reboot, due to expiration of the watchdog timer. This bit can be cleared or set by firmware.

R **Reserved** **[6:4]**

WTHR[3:0] **Watchdog Timer Threshold** **[3:0]**
The 4-bit value stored in bits 3 through 0 of the WDTC register define the watchdog timer threshold. A value of 0 in all bits disables the watchdog timer. The watchdog timer can be programmed for 15 different time-out values between 10 ms and 150 ms, in steps of 10 ms. Table 7.3 shows the possible time-out values.

Table 7.3 Possible Watchdog Timer Values (40 MHz Internal Clock)

WTHR3	WTHR2	WTHR1	WTHR0	Time-out Value[1]
0	0	0	0	Timer disable
0	0	0	1	10 ms
0	0	1	0	20 ms
0	0	1	1	30 ms
0	1	0	0	40 ms
0	1	0	1	50 ms
0	1	1	0	60 ms
0	1	1	1	70 ms
1	0	0	0	80 ms
1	0	0	1	90 ms
1	0	1	0	100 ms
1	0	1	1	110 ms
1	1	0	0	120 ms
1	1	0	1	130 ms
1	1	1	0	140 ms
1	1	1	1	150 ms

1. $$T_{OUT} = \frac{(\text{Decimal value of WTHR[3:0]}) \times 4000 \times 100}{f_{clk}}$$

Register: 0xFE01

Watchdog Secondary Chain (WDSC)
Read Only

7	6						0
R	WDSC[6:0]						
x	0	0	0	0	0	0	0

The values in this register are not affected by a soft reset.

R **Reserved** **7**

WDSC[6:0] **Watchdog Secondary Chain** **[6:0]**
These register bits provide the ability to read the 7-bit value in the secondary watchdog timer divider chain. With a 40 MHz external clock, this divider chain is clocked at 10 kHz (100 µs per count).

Register: 0xFE02

Watchdog Final Chain (WDFC)
Read Only

7			4	3			0
R				WDFC[3:0]			
Defaults:							
x	x	x	x	0	0	0	0

The values in this register are not affected by a soft reset.

R **Reserved** **[7:4]**

WDFC[3:0] **Watchdog Final Chain** **[3:0]**
These register bits provide the ability to read the 4-bit value in the final watchdog timer divider chain. With a 40 MHz external clock, this divider chain is clocked at 100 Hz (10 ms per count). The value in this register is compared to the 4-bit value in bits 0 through 3 of the Watchdog Timer Control (WDTC) register to determine the time-out value of the watchdog timer.

Register: 0xFE03

Miscellaneous Control (MCR)

Read/Write

7	6	5	4	3	2	1	0
REV[3:0]			REV0	LVD_PWRDWN	SISO	TE	ZMODE
0	0	0	0	0	0	0	0

REV[3:0] **Chip Revision (read only)** **[7:4]**

These bits define the hardware revision number for the LSI53C040.

LVD_PWRDWN

LVD Power Down **3**

A value of 1 in this bit powers down the input LVD transceivers for operation when not in LVD mode.

SISO **SCSI Isolation** **2**

When set, this bit 3-states and logically disconnects the LSI53C040 SCSI port from the SCSI bus when in SE mode (DIFFSENS = V_{SS}).

TE **TolerANT® Enable** **1**

This bit is used in LVD mode only. Refer to Figure 2.3 for information regarding when to set this bit.

ZMODE **High Impedance Mode** **0**

Setting this bit to 1 effectively 3-states all output and bidirectional pads.

Register: 0xFE04

Interrupt Status (ISR)
Read/Write

7	6	5	4	3	2	1	0
SCSI_INT	TW1_INT	TW0_INT	DMA_INT	TMR2_INT	TMR1_INT	EXS1_INT	EXS0_INT
0	0	0	0	0	0	0	0

The individual bits of this register may be written to force an interrupt on the corresponding bit. Clearing these bits does not clear the interrupt, unless it was originally set in this register.

SCSI_INT **SCSI Interrupt (read only)** **7**
A value of 1 in this bit indicates an interrupt pending from the SCSI block. The bit goes to 0 when the interrupt is cleared from the SCSI block.

TW1_INT **Two-Wire Interface 1 Interrupt (read only)** **6**
A value of 1 in this bit indicates an interrupt pending from the two-wire serial port_1 block. The bit goes to 0 when the interrupt is cleared from the two-wire serial port_1 block.

TW0_INT **Two-Wire Interface 0 Interrupt (read only)** **5**
A value of 1 in this bit indicates an interrupt pending from the two-wire serial port_0 block. The bit goes to 0 when the interrupt is cleared from the two-wire serial port_0 block.

DMA_INT **DMA Interrupt (read only)** **4**
A value of 1 in this bit indicates an interrupt pending from the DMA block. The bit goes to 0 when the interrupt is cleared from the DMA block.

TMR2_INT **Timer 2 Interrupt (read only)** **3**
A value of 1 in this bit indicates an interrupt pending from the timer2 block. The bit goes to 0 when the interrupt is cleared from the Timer2 block.

TMR1_INT **Timer 1 Interrupt (read only)** **2**
A value of 1 in this bit indicates an interrupt pending from the timer1 block. The bit goes to 0 when the interrupt is cleared from the Timer1 block.

EXS1_INT **8067 Port 1 Interrupt or MPIO3_1 Interrupt** **1**
A value of 1 in this bit indicates an interrupt pending from the SFF-8067 port 1 block or an external interrupt received on MPIO3(1). The bit goes to 0 when the interrupt is cleared from MPIO3(1) or cleared from the SFF-8067 port 1 block.

EXS0_INT **8067 Port 0 Interrupt or MPIO3_0 Interrupt** **0**
A value of 1 in this bit indicates an interrupt pending from the SFF-8067 port 0 block or a external interrupt received on MPIO3(0). The bit goes to 0 when the interrupt is cleared from MPIO3(0) or cleared from the SFF-8067 port 0 block.

Register: 0xFE05

Timer 1 Control (T1C)
Read/Write

7	6	5	4	3		1	0
T1EXP	T1RUN	T1CLR	T1PS	R			T1IEN
0	0	0	0	x	x	x	0

The LSI53C040 includes two built-in timers that run independently of the microcontroller core. Each timer can be programmed to generate one of the two possible interrupts to the microcontroller core, as long as these interrupts are not masked in the Interrupt Mask (IMR) register. Any DMA operation will also be suspended if either timer expires and generates an interrupt to the microcontroller. This frees the internal memory bus to allow access by the microcontroller after the interrupt awakens the microcontroller core.

T1EXP **Timer 1 Expired** **7**
A value of 1 in the T1EXP bit indicates that the timer has expired and an interrupt has been generated, if the T1IEN bit was set at the time the timer expired. The interrupt can be cleared by setting the T1CLR bit.

T1RUN **Timer 1 Run** **6**
A value of 1 in the T1RUN bit allows the timer to advance. A value of 0 stops timer advancement.

T1CLR **Timer 1 Clear** **5**

A value of 1 in the T1CLR bit clears the timer. A value of 0 allows the timer to advance beyond the clear state.

T1PS **Timer 1 Prescaler** **4**

A value of 1 in the T1PS bit selects the additional divide by 100 secondary divider chain, yielding a timer range of 0.5 ms to 128 ms with a resolution of 0.5 ms per step (with a 40 MHz clock). A value of 0 bypasses the secondary divider chain, yielding a timer range of 5 µs to 1.280 ms with a resolution of 5 µs per step.

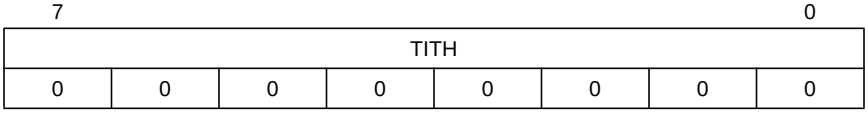
R **Reserved** **[3:1]**

T1IEN **Timer 1 Interrupt Enable (read only)** **0**

A value of 1 in the T1IEN bit enables the timer to interrupt the microcontroller core when the timer expires. This bit is cleared upon chip reset.

Register: 0xFE06

Timer 1 Threshold (T1TH)
Read/Write



T1TH **Timer 1 Threshold** **[7:0]**

These register bits select the time-out threshold for timer 1. The 8-bit number programmed in this register corresponds to a multiple of the selected timer resolution, which is selected by the T1PS bit (0xFE05, bit 4). A value of 0x00 in this register selects the maximum time-out value of 256 times the selected timer resolution.

Register: 0xFE07

Timer 1 Secondary Chain (T1SC)
Read Only

7	6						0
R	T1SC[6:0]						
x	0	0	0	0	0	0	0

R **Reserved** **7**

T1SC[6:0] **Timer 1 Secondary Chain** **[6:0]**
These register bits provide the ability to read the secondary divide by 100 chain of timer 1. This chain is enabled with the T1PS bit (0xFE05, bit 4). When enabled, a value of 100 (decimal) in this register triggers advancement of the final timer 1 divider chain.

Register: 0xFE08

Timer 1 Final Chain (T1FC)
Read Only

7							0
T1FC							
0	0	0	0	0	0	0	0

T1FC **Timer 1 Final Chain** **[7:0]**
These register bits provide the ability to read the final timer 1 divider chain. The timer expires when the value of this divider chain is equal to the value of the Timer 1 Threshold (T1TH) register (0xFE06). When this happens, the T1EXP bit (0xFE05, bit 7) will be set and an interrupt will be generated to the microcontroller, through the Interrupt Status (ISR) register, if the T1IEN bit (0xFE05, bit 0) is set.

Register: 0xFE09

Timer 2 Control (T2C)

Read/Write

7	6	5	4	3		1	0
T2EXP	T2RUN	T2CLR	T2PS	R			T2IEN
0	0	0	0	x	x	x	0

T2EXP **Timer 2 Expired (read only)** **7**

A value of 1 in the T2EXP bit indicates that the timer has expired and an interrupt has been generated if the T2IEN bit was set when the timer expired. The interrupt can be cleared by setting the T2CLR bit.

T2RUN **Timer 2 Run** **6**

A value of 1 in the T2RUN bit allows the timer to advance. A value of 0 stops timer advancement.

T2CLR **Timer 2 Clear** **5**

A value of 1 in the T2CLR bit clears the timer. A value of 0 allows the timer to advance beyond the clear state.

T2PS **Timer 2 Prescaler** **4**

A value of 1 in the T2PS bit selects the additional divide by 100 secondary divider chain, yielding a timer range of 0.5 ms to 128 ms with a resolution of 0.5 ms per step (with a 40 MHz clock). A value of 0 bypasses the secondary divider chain, yielding a timer range of 5 µs to 1.280 ms with a resolution of 5 µs per step.

R **Reserved** **[3:1]**

T2IEN **Timer 2 Interrupt Enable** **0**

A value of 1 in the T2IEN bit enables the timer's ability to interrupt the microcontroller core (through the Interrupt Status (ISR) register, 0xFE04) upon expiration. This bit is cleared upon chip reset.

Register: 0xFE0A

Timer 2 Threshold (T2T)
Read/Write

7							0
T2TH							
0	0	0	0	0	0	0	0

T2TH **Timer 2 Threshold** **[7:0]**

These register bits select the time-out threshold for timer 2. The 8-bit number programmed in this register corresponds to a multiple of the selected timer resolution, which is selected by the T2PS bit (0xFE09, bit 4). A value of 0x00 in this register selects the maximum time-out value of 256 times the selected timer resolution.

Register: 0xFE0B

Timer 2 Secondary Chain (T2SC)
Read Only

7	6						0
R	T2SC[6:0]						
x	0	0	0	0	0	0	0

R **Reserved** **7**

T2SC[6:0] **Timer 2 Secondary Chain** **[6:0]**

These register bits provide the ability to read the secondary divide by 100 chain of timer 2. This chain is enabled with the T2PS bit (0xFE09, bit 4). When enabled, a value of 100 (decimal) in this register triggers advancement of the final timer 2 divider chain.

Register: 0xFE0C
Timer 2 Final Chain (T2FC)
Read Only

7							0
T2FC							
0	0	0	0	0	0	0	0

T2FC **Timer 2 Final Chain** **[7:0]**
These register bits provide the ability to read the final timer 2 divider chain. The expiration condition for this timer is when the value of this divider chain is equal to the value of the Timer 2 Threshold (T2T) register (0xFE0A). When this happens, the T2EXP bit (0xFE09, bit 7) will be set and an interrupt will be generated to the microcontroller, through the Interrupt Status (ISR) register (0xFE04), if the T2IEN bit (0xFE09, bit 0) is set.

Register: 0xFE0D
Interrupt Mask (IMR)
Read/Write

7	6	5	4	3	2	1	0
IMR7	IMR6	IMR5	IMR4	IMR3	IMR2	IMR1	IMR0
0	0	0	0	0	0	0	0

These register bits provide the ability to mask the corresponding interrupts in the Interrupt Status (ISR) register (0xFE04). Writing a 1 to a bit in this register enables the corresponding interrupt in the ISR register.

IMR7 **SCSI Interrupt** **7**
Clearing this bit masks this interrupt. Setting this bit enables the interrupt.

IMR6 **Two-Wire Interface 1 Interrupt** **6**
Clearing this bit masks this interrupt. Setting this bit enables the interrupt.

IMR5 **Two-Wire Interface 0 Interrupt** **5**
Clearing this bit masks this interrupt. Setting this bit enables the interrupt.

IMR4	**DMA Interrupt** Clearing this bit masks this interrupt. Setting this bit enables the interrupt.	**4**
IMR3	**Timer 2 Interrupt** Clearing this bit masks this interrupt. Setting this bit enables the interrupt.	**3**
IMR2	**Timer 1 Interrupt** Clearing this bit masks this interrupt. Setting this bit enables the interrupt.	**2**
IMR1	**8067 Port 1 Interrupt or MPIO3_1 Interrupt** Clearing this bit masks this interrupt. Setting this bit enables the interrupt.	**1**
IMR0	**8067 Port 0 Interrupt or MPIO3_0 Interrupt** Clearing this bit masks this interrupt. Setting this bit enables the interrupt.	**0**

Register: 0xFE0E

Interrupt Destination (IDR)
Read/Write

7	6	5	4	3	2	1	0
IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
0	0	0	0	0	0	0	0

These register bits provide the ability to route the corresponding interrupts of the Interrupt Status (ISR) register (0xFE04) to either of the two external interrupt inputs of the microcontroller core. A value of 1 written to a bit in this register will route the corresponding interrupt in the ISR register to the external interrupt 1 input of the microcontroller, and a value of 0 written to a given bit will route the corresponding interrupt of the ISR register to the external interrupt 0 input of the microcontroller.

IDR7	**SCSI Interrupt**	**7**
IDR6	**Two-Wire Interface 1 Interrupt**	**6**
IDR5	**Two-Wire Interface 0 Interrupt**	**5**
IDR4	**DMA Interrupt**	**4**
IDR3	**Timer 2 Interrupt**	**3**
IDR2	**Timer 1 Interrupt**	**2**
IDR1	**8067 Port 1 Interrupt or MPIO3_1 Interrupt**	**1**
IDR0	**8067 Port 0 Interrupt or MPIO3_0 Interrupt**	**0**

Chapter 8
System Registers

This chapter contains descriptions of the LSI53C040 System registers. The SCSI/DMA registers, SFF-8067 registers, Two-Wire Serial registers, and Miscellaneous registers are described in Chapter 4 through Chapter 7. The term set is used to refer to bits that are programmed to a binary one, while the term reset or clear is used to refer to bits that are programmed to binary zero. Any bits marked as reserved should always be written to zero; mask all information read from them. Reserved bit functions may be changed at any time. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default bit values, which are enabled after the chip is powered on or reset.

Figure 8.1 summarizes the entire LSI53C040 register set.

Figure 8.1 Register Set Overview

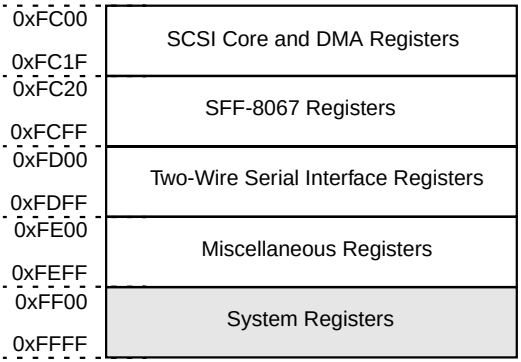


Table 8.1, the register map, summarizes the System registers in graphical form.

Table 8.1 System Registers

31 16 15 0	Address
Reserved	0xFF00
Power-On Configuration Zero (POC0)	0xFF01
Reserved	0xFF02
Power-On Configuration One (POC1)	0xFF03
LED Blink Rate (LBR)	0xFF04
System Control (SYSCTRL)	0xFF05
Reserved	0xFF06–0xFF07
Multipurpose I/O Bank 0 Output (MPO0)	0xFF08
Multipurpose I/O Bank 0 Enable (MPE0)	0xFF09
Multipurpose I/O Bank 0 Input (MPI0)	0xFF0A
Multipurpose I/O Bank 0 Latch Mask (MPLM0)	0xFF0B
Multipurpose I/O Bank 0 Latch (MPL0)	0xFF0C
Multipurpose I/O Bank 0 Pull-down Enable (MPPE0)	0xFF0D
Reserved	0xFF0E–0xFF0F
Multipurpose I/O Bank 1 Output (MPO1)	0xFF10
Multipurpose I/O Bank 1 Enable (MPE1)	0xFF11
Multipurpose I/O Bank 1 Input (MPI1)	0xFF12
Multipurpose I/O Bank 1 Latch Mask (MPLM1)	0xFF13
Multipurpose I/O Bank 1 Latch (MPL1)	0xFF14
Multipurpose I/O Bank 1 Pull-down Enable (MPPE1)	0xFF15
Reserved	0xFF16–0xFF17
Multipurpose I/O Bank 2 Output (MPO2)	0xFF18
Multipurpose I/O Bank 2 Enable (MPE2)	0xFF19
Multipurpose I/O Bank 2 Input (MPI2)	0xFF1A
Multipurpose I/O Bank 2 Latch Mask (MPLM2)	0xFF1B
Multipurpose I/O Bank 2 Latch (MPL2)	0xFF1C
Multipurpose I/O Bank 2 Pull-down Enable (MPPE2)	0xFF1D
Reserved	0xFF1E–0xFF1F
Multipurpose I/O Bank 3 Output (MPO3)	0xFF20
Multipurpose I/O Bank 3 Enable (MPE3)	0xFF21
Multipurpose I/O Bank 3 Input (MPI3)	0xFF22

Table 8.1 System Registers (Cont.)

Multipurpose I/O Bank 3 Latch Mask (MPLM3)	0xFF23
Multipurpose I/O Bank 3 Latch (MPL3)	0xFF24
Multipurpose I/O Bank 3 Pull-down Enable (MPPE3)	0xFF25
Reserved	0xFF26–0xFF29
Multipurpose LED Bank 0L Output (MLO0L)	0xFF30
Multipurpose LED Bank 0H Output (MLO0H)	0xFF31
Multipurpose LED Bank 0L Input (MLI0L)	0xFF32
Multipurpose LED Bank 0H Input (MLI0H)	0xFF33
Multipurpose LED Bank 0L Latch Mask (MLLM0L)	0xFF34
Multipurpose LED Bank 0H Latch Mask (MLLM0H)	0xFF35
Multipurpose LED Bank 0L Latch (MLL0L)	0xFF36
Multipurpose LED Bank 0H Latch (MLL0H)	0xFF37
Multipurpose LED Bank 1L Output (MLO1L)	0xFF38
Multipurpose LED Bank 1H Output (MLO1H)	0xFF39
Multipurpose LED Bank 1L Input (MLI1L)	0xFF3A
Multipurpose LED Bank 1H Input (MLI1H)	0xFF3B
Multipurpose LED Bank 1L Latch Mask (MLLM1L)	0xFF3C
Multipurpose LED Bank 1H Latch Mask (MLLM1H)	0xFF3D
Multipurpose LED Bank 1L Latch (MLL1L)	0xFF3E
Multipurpose LED Bank 1H Latch (MLL1H)	0xFF3F
Multipurpose LED Bank 2L Output (MLO2L)	0xFF40
Multipurpose LED Bank 2H Output (MLO2H)	0xFF41
Multipurpose LED Bank 2L Input (MLI2L)	0xFF42
Multipurpose LED Bank 2H Input (MLI2H)	0xFF43
Multipurpose LED Bank 2L Latch Mask (MLLM2L)	0xFF44
Multipurpose LED Bank 2H Latch Mask (MLLM2H)	0xFF45
Multipurpose LED Bank 2L Latch (MLL2L)	0xFF46
Multipurpose LED Bank 2H Latch (MLL2H)	0xFF47

Register: 0xFF01

Power-On Configuration Zero (POC0)
Read Only

7	6	5	4	3	2	1	0
POC0_7	POC0_6	DLCFG	POC0_4	POC0_3	POC0_2	FIBD1	FIBD0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

POC0_7 **Power-On Configuration 7** **7**
The reset value of this bit matches the TTL voltage level on the AD7 pin at reset.

POC0_6 **Power-On Configuration 6** **6**
The reset value of this bit matches the TTL voltage level on the AD6 pin at reset.

DLCFG **Download Serial ROM** **5**
When this bit is set, the LSI53C040 attempts to download from a serial ROM at power-on or after reset. When cleared, the LSI53C040 will skip the serial ROM download. The reset value of this bit matches the TTL voltage level on the AD5 pin at reset. The AD5 pin has an internal pull-down resistor; if no external pull-up resistor is used, the reset value will be 0 (do not perform serial ROM download). If an external pull-up resistor is used, the reset value will be 1 (perform serial ROM download).

POC0_4 **Power-On Configuration 4** **4**
The reset value of this bit tracks the TTL voltage level of the AD4 pin at reset.

POC0_3 **Power-On Configuration 3** **3**
The reset value of this bit tracks the TTL voltage level on the AD3 pin on reset.

POC0_2 **Power-On Configuration 2** **2**
The reset value of this bit tracks the TTL voltage level on the AD2 pin on reset.

FIBD[1:0] **First Instruction Branch Destination (read only)** **[1:0]**
The microcontroller always fetches its first instruction from address 0x0000. In order to accommodate different power-on memory mapping configurations, the

LSI53C040 address decode logic will automatically provide the first branch instruction to the microcontroller whenever it fetches from address 0x0000 through 0x0002. The values in bits 0 and 1 define the destination address for this branch instruction, according to Table 8.2. For more information on automatic branch addressing, see Chapter 2.

Table 8.2 Automatic Branch Destination Address

FIBD1	FIBD0	Branch Destination
1	1	0x8000
1	0	0x4000
0	1	0x0033
0	0	Fetched from 0x0000

The reset value of these bits matches the TTL voltage levels on the AD0 and AD1 pins on reset. These pins have internal pull-down resistors, so if no external pull-up resistor is used, the reset value is 0, and the first microcontroller instruction will be fetched from address 0x0000. If an external pull-up resistor is used, the reset value is 1.

Register: 0xFF03

Power-On Configuration One (POC1)

Read Only

7	6	5	4	3	2	1	0
R	POC1_6	POC1_5	POC1_4	DLSEL	DLADR2	DLADR1	DLADR0
A15	A14	A13	A12	A11	A10	A9	A8

This register is not affected by a soft reset.

R **Reserved** **7**
This bit should remain clear (0) for normal operation.

POC1_6 **Power-On Configuration 1_6** **6**
The reset value of this bit matches the TTL voltage level on the A14 pin on reset.

POC1_5 **Power-On Configuration 1_5** **5**
The reset value of this bit matches the TTL voltage level on the A13 pin on reset.

POC1_4 **Power-On Configuration 1_4** **4**
The reset value of this bit matches the TTL voltage level on the A12 pin on reset. If high, the download speed will be increased to an SCL of 1250 kHz. This bit is for test purposes only, and should remain clear for normal operation.

DLSEL **Download Configuration Select** **3**
Chooses between the 2 two-wire serial ports for the initial download. The reset value of this bit matches the TTL voltage level on the A11 pin at reset. A value of 0 selects two-wire serial port 0, a value of 1 selects two-wire serial port 1.

DLADR[2:0] **Download ROM Address** **[2:0]**
The chip address of the serial ROM to be used in the power-on download is defined by using pull-downs on the A8, A9, and A10 pins. (See Chapter 2.)

Register: 0xFF04
LED Blink Rate (LBR)
Read/Write

7	6	5	4	3	2	1	0
R		FBR[1:0]		R		SBR[1:0]	
0	0	0	0	0	0	0	0

Each of the LED output pins, controlled by the LED registers defined later in this register block, can be programmed to be constantly on, constantly off, or to blink at one of two different blink rates. The blink rates for all LED pins are defined globally in this register.

R **Reserved** **[7:6]**

FBR[1:0] **Fast Blink Rate** **[5:4]**

These bits define the fast blink rate for the LED output pins, as shown in Table 8.3.

Table 8.3 Fast LED Blink Rates (40 MHz Internal Clock)

FBR1	FBR0	Fast Blink Rate	Fast Blink Period
0	0	8 Hz	0.0625 s on/0.0625 s off
0	1	4 Hz	0.125 s on/0.125 s off
1	0	2 Hz	0.25 s on/0.25 s off
1	1	1 Hz	0.5 s on/0.5 s off

R **Reserved** **[3:2]**

SBR[1:0] **Slow Blink Rate** **[1:0]**

These bits define the slow blink rate for the LED output pins, as shown in Table 8.4.

Table 8.4 Slow LED Blink Rates (20 MHz Internal Clock)

SBR1	SBR0	Slow Blink Rate	Slow Blink Period
0	0	2 Hz	0.25 s on/0.25 s off
0	1	1 Hz	0.5 s on/0.5 s off
1	0	0.5 Hz	1 s on/1 s off
1	1	0.25 Hz	2 s on/2 s off

Register: 0xFF05

System Control (SYSCTRL)

Read/Write

7	6			3	2	1	0
ERO	R				LVD	SPEN	EIEN
0	0	0	0	0	0	0	0

ERO **Enable Reset Output** **7**

When set, this bit enables the internally generated watchdog time-out reset to be driven on the external reset pin. This bit is not affected by a soft reset.

R	**Reserved**	**[6:3]**
LVD	**SCSI LVD Mode (read only)** This read only bit is set when the SCSI interface is in LVD mode.	**2**
SPEN	**Serial Port Enable** When this bit is set to 1, the MPIO3_2 pin is mapped to the TXD serial port function of the microcontroller core and the MPIO3_3 pin is mapped to the RXD serial port function of the microcontroller core. When cleared (0), the MPIO3_2 and MPIO3_3 pins are controlled as standard multipurpose I/O pins. The Multipurpose I/O Bank 3 Enable (MPE3) register (0xFF21) and other control registers for MPIO bank 3 are not used in controlling the serial port function of the microcontroller core.	**1**
EIEN	**External Interrupt Enable** When this bit is set to a 1, the MPIO3_0 pin is mapped to the INT0/ external interrupt function of the microcontroller core and the MPIO3_1 pin is mapped to the INT1/ external interrupt function of the microcontroller core. When cleared (0), the MPIO3_0 and MPIO3_1 pins are controlled as a standard multipurpose I/O pin. The Multipurpose I/O Bank 3 Enable (MPE3) register (0xFF21) and other control registers for MPIO bank 3 are not used in controlling the serial port function of the microcontroller core.	**0**

Register: 0xFF08

Multipurpose I/O Bank 0 Output (MPO0)
Read/Write

7							0
MPO0_							
0	0	0	0	0	0	0	0

MPO0_	**Multipurpose I/O Bank 0 Output** The values stored in these register bits are driven on the I/O pins MPIO0_0, MPIO0_1, MPIO0_2, MPIO0_3, MPIO0_4, MPIO0_5, MPIO0_6, and MPIO0_7 when the corresponding pin enable in register 0xFF09 is set.	**[7:0]**

Register: 0xFF09

Multipurpose I/O Bank 0 Enable (MPE0)
Read/Write

7							0
MPE0_							
0	0	0	0	0	0	0	0

MPE0_ **Multipurpose I/O Bank 0 Enable** **[7:0]**
These bits control the output enables on the I/O pins MPIO0_0, MPIO0_1, MPIO0_2, MPIO0_3, MPIO0_4, MPIO0_5, MPIO0_6, and MPIO0_7. A value of 1 turns on the pin driver, and a value of 0 3-states the pin. Because the value in this register powers up to all zeros, the pins will initially be 3-stated at power-up. These pins also have internal 100 µA pull-down resistors, which can be disabled with the Multipurpose I/O Bank 3 Pull-down Enable (MPPE3) register (0xFF25).

Register: 0xFF0A

Multipurpose I/O Bank 0 Input (MPI0)
Read Only

7							0
MPI0_							
0	0	0	0	0	0	0	0

MPI0_ **Multipurpose I/O Bank 0 Input** **[7:0]**
These read only bits read the live input values on the I/O pins MPIO0_0, MPIO0_1, MPIO0_2, MPIO0_3, MPIO0_4, MPIO0_5, MPIO0_6, and MPIO0_7.

Register: 0xFF0B

Multipurpose I/O Bank 0 Latch Mask (MPLM0)
Read/Write

7							0
MPLM0_							
1	1	1	1	1	1	1	1

MPLM0_ **Multipurpose I/O Bank 0 Latch Mask** **[7:0]**
These read/write register bits define the write mask for the Multipurpose I/O Bank 0 Latch (MPL0) register (0xFF0C). A value of 1 in any of these bits allows the corresponding bit in the MPL0 to be modified.

Register: 0xFF0C

Multipurpose I/O Bank 0 Latch (MPL0)
Read/Write

7							0
MPL0_							
x	x	x	x	x	x	x	x

MPL0_ **Multipurpose I/O Bank 0 Latch** **[7:0]**
These read/write register bits store the power-on value of the I/O pins MPIO0_0, MPIO0_1, MPIO0_2, MPIO0_3, MPIO0_4, MPIO0_5, MPIO0_6, and MPIO0_7. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF0D

Multipurpose I/O Bank 0 Pull-down Enable (MPPE0)
Read/Write

7							0
MPPE0_							
1	1	1	1	1	1	1	1

MPPE0_ **Multipurpose I/O Bank 0 Pull-down Enable** **[7:0]**
These read/write register bits determine if pull-downs are active on the I/O pins MPIO0_0, MPIO0_1, MPIO0_2, MPIO0_3, MPIO0_4, MPIO0_5, MPIO0_6, and MPIO0_7. A value of 1 indicates the pull-down is active, a value of 0 indicates the pull-down is inactive.

Register: 0xFF10

Multipurpose I/O Bank 1 Output (MPO1)
Read/Write

7							0
MPO1_							
0	0	0	0	0	0	0	0

MPO1_ **Multipurpose I/O Bank 1 Output** **[7:0]**
The values stored in these register bits are driven on the I/O pins MPIO1_0, MPIO1_1, MPIO1_2, MPIO1_3, MPIO1_4, MPIO1_5, MPIO1_6, and MPIO1_7 when the corresponding pin enable in register 0xFF11 is set.

Register: 0xFF11

Multipurpose I/O Bank 1 Enable (MPE1)
Read/Write

7							0
MPE1_							
0	0	0	0	0	0	0	0

MPE1_ **Multipurpose I/O Bank 1 Enable** **[7:0]**
These bits control the output enables on the I/O pins MPIO1_0, MPIO1_1, MPIO1_2, MPIO1_3, MPIO1_4, MPIO1_5, MPIO1_6, and MPIO1_7. A value of 1 turns on the pin driver, and a value of 0 3-states the pin. Because this register powers up to all zeros, the pins will initially be 3-stated at power-up. These pins also have internal 100 µA pull-down resistors, which can be disabled with the Multipurpose I/O Bank 3 Pull-down Enable (MPPE3) register (0xFF25).

Register: 0xFF12

Multipurpose I/O Bank 1 Input (MPI1)
Read Only

7							0
MPI1_							
0	0	0	0	0	0	0	0

MPI1_ **Multipurpose I/O Bank 1 Input** **[7:0]**
These read only bits read the live input values on the I/O MPIO1_0, MPIO1_1, MPIO1_2, MPIO1_3, MPIO1_4, MPIO1_5, MPIO1_6, and MPIO1_7.

Register: 0xFF13

Multipurpose I/O Bank 1 Latch Mask (MPLM1)
Read/Write

7							0
MPLM1_							
1	1	1	1	1	1	1	1

MPLM1_ **Multipurpose I/O Bank 1 Latch Mask** **[7:0]**
These read/write register bits define the write mask for the Multipurpose I/O Bank 1 Latch (MPL1) register (0xFF14). A value of 1 in any of these bits allows the corresponding bit in the MPL1 to be modified.

Register: 0xFF14

Multipurpose I/O Bank 1 Latch (MPL1)
Read/Write

7							0
MPL1_							
x	x	x	x	x	x	x	x

MPL1_ **Multipurpose I/O Bank 1 Latch** **[7:0]**
These read/write register bits store the power-on value of the I/O pins MPIO1_0, MPIO1_1, MPIO1_2, MPIO1_3, MPIO1_4, MPIO1_5, MPIO1_6, and MPIO1_7. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF15

Multipurpose I/O Bank 1 Pull-down Enable (MPPE1)
Read/Write

7							0
MPPE1_							
1	1	1	1	1	1	1	1

MPPE1_ **Multipurpose I/O Bank 1 Pull-down Enable** **[7:0]**
These read/write register bits determine if pull-downs are active on the I/O pins MPIO1_0, MPIO1_1, MPIO1_2, MPIO1_3, MPIO1_4, MPIO1_5, MPIO1_6, and MPIO1_7. A value of 1 indicates the pull-down is active, a value of 0 indicates the pull-down is inactive.

Register: 0xFF18

Multipurpose I/O Bank 2 Output (MPO2)
Read/Write

7							0
MPO2_							
0	0	0	0	0	0	0	0

MPO2_ **Multipurpose I/O Bank 2 Output** **[7:0]**
The values stored in these register bits are driven on the I/O pins MPIO2_0, MPIO2_1, MPIO2_2, MPIO2_3, MPIO2_4, MPIO2_5, MPIO2_6, and MPIO2_7 when the corresponding pin enable in register 0xFF19 is set.

Register: 0xFF19

Multipurpose I/O Bank 2 Enable (MPE2)
Read/Write

7							0
MPE2_							
0	0	0	0	0	0	0	0

MPE2_ **Multipurpose I/O Bank 2 Enable** **[7:0]**
These bits control the output enables on the I/O pins MPIO2_0, MPIO2_1, MPIO2_2, MPIO2_3, MPIO2_4, MPIO2_5, MPIO2_6, and MPIO2_7. A value of 1 turns on the pin driver, and a value of 0 3-states the pin. Because this register powers up to all zeros, the pins will initially be 3-stated at power-up. These pins also have internal 100 µA pull-down resistors, which can be disabled with the Multipurpose I/O Bank 3 Pull-down Enable (MPPE3) register (0xFF25).

Register: 0xFF1A

Multipurpose I/O Bank 2 Input (MPI2)
Read Only

7							0
MPI2_							
0	0	0	0	0	0	0	0

MPI2_ **Multipurpose I/O Bank 2 Input** **[7:0]**
These read only bits read the live input values on the I/O MPIO2_0, MPIO2_1, MPIO2_2, MPIO2_3, MPIO2_4, MPIO2_5, MPIO2_6, and MPIO2_7.

Register: 0xFF1B

Multipurpose I/O Bank 2 Latch Mask (MPLM2)
Read/Write

7							0
MPLM2_							
1	1	1	1	1	1	1	1

MPLM2_ **Multipurpose I/O Bank 2 Latch Mask** **[7:0]**
These read/write register bits define the write mask for the Multipurpose I/O Bank 2 Latch (MPL2) register (0xFF1C). A value of 1 in any of these bits allows the corresponding bit in the MPL2 to be modified.

Register: 0xFF1C

Multipurpose I/O Bank 2 Latch (MPL2)
Read/Write

7							0
MPL2_							
x	x	x	x	x	x	x	x

MPL2_ **Multipurpose I/O Bank 2 Latch** **[7:0]**
These read/write register bits store the power-on value of the I/O pins MPIO2_0, MPIO2_1, MPIO2_2, MPIO2_3, MPIO2_4, MPIO2_5, MPIO2_6, and MPIO2_7. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF1D

Multipurpose I/O Bank 2 Pull-down Enable (MPPE2)
Read/Write

7							0
MPPE2_							
1	1	1	1	1	1	1	1

MPPE2_ **Multipurpose I/O Bank 2 Pull-down Enable** **[7:0]**
These read/write register bits determine if pull-downs are active on the I/O pins MPIO2_0, MPIO2_1, MPIO2_2, MPIO2_3, MPIO2_4, MPIO2_5, MPIO2_6, and MPIO2_7. A value of 1 indicates the pull-down is active, a value of 0 indicates the pull-down is inactive.

Register: 0xFF20

Multipurpose I/O Bank 3 Output (MPO3)
Read/Write

7				4	3			0
R					MPO_[3:0]			
0	0	0	0		0	0	0	0

R **Reserved** **[7:4]**

MPO3_[3:0] **Multipurpose I/O Bank 3 Output** **[3:0]**
The values stored in these register bits are driven on the I/O pins MPIO3_0, MPIO3_1, MPIO3_2, and MPIO3_3 when the corresponding pin enable in register 0xFF21 is set.

Register: 0xFF21

Multipurpose I/O Bank 3 Enable (MPE3)
Read/Write

7			4	3			0
R				MPE3_[3:0]			
0	0	0	0	0	0	0	0

R **Reserved** **[7:4]**

MPE3_[3:0] **Multipurpose I/O Bank 3 Enable** **[3:0]**
These bits control the output enables on the I/O pins MPIO3_0, MPIO3_1, MPIO3_2, and MPIO3_3. A value of 1 turns on the pin driver, and a value of 0 3-states the pin. Because the value in this register powers up to all zeros, the pins will initially be 3-stated at power-up. These pins also have internal 100 µA pull-down resistors, which can be disabled with the Multipurpose I/O Bank 3 Pull-down Enable (MPPE3) register (0xFF25).

When the SPEN bit (0xFF05, bit 1) is set, the MPIO3_2 pin is mapped to the TXD serial port function of the microcontroller core, and the MPIO3_3 pin is mapped to the RXD serial port function of the microcontroller core. When the EIEN bit (0xFF05, bit 0) is set, the MPIO3_0 pin is mapped to the EXS0_INT external interrupt function of the microcontroller core and the MPIO3_1 pin is mapped to the EXS1_INT external interrupt function of the microcontroller core.

Register: 0xFF22

Multipurpose I/O Bank 3 Input (MPI3)
Read Only

7				4	3			0
R					MPI3_[3:0]			
0	0	0	0		0	0	0	0

R **Reserved** **[7:4]**

MPI3_[3:0] **Multipurpose I/O Bank 3 Input** **[3:0]**
These read only bits read the live input values on the I/O pins MPIO3_0, MPIO3_1, MPIO3_2, and MPIO3_3.

Register: 0xFF23

Multipurpose I/O Bank 3 Latch Mask (MPLM3)
Read/Write

7				4	3			0
R					MPLM3_[3:0]			
1	1	1	1		1	1	1	1

R **Reserved** **[7:4]**

MPLM3_[3:0] **Multipurpose I/O Bank 3 Latch Mask** **[3:0]**
These read/write register bits define the write mask for the Multipurpose I/O Bank 3 Latch (MPL3) register (0xFF24). A value of 1 in any of these bits allows the corresponding bit in the MPL3 to be modified.

Register: 0xFF24

Multipurpose I/O Bank 3 Latch (MPL3)
Read/Write

7			4	3			0
R				MPL3_[3:0]			
x	x	x	x	x	x	x	x

R **Reserved** **[7:4]**

MPL3_[3:0] **Multipurpose I/O Bank 3 Latch** **[3:0]**
These read/write register bits store the power-on value of the I/O pins MPIO3_0, MPIO3_1, MPIO3_2, and MPIO3_3. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF25

Multipurpose I/O Bank 3 Pull-down Enable (MPPE3)
Read/Write

7			4	3			0
R				MPPE3_[3:0]			
1	1	1	1	1	1	1	1

R **Reserved** **[7:4]**

MPPE3_[3:0] **Multipurpose I/O Bank 3 Pull-down Enable** **[3:0]**
These read/write register bits determine if pull-downs are active on the I/O pins MPIO3_0, MPIO3_1, MPIO3_2, and MPIO3_3. A value of 1 indicates the pull-down is active, a value of 0 indicates the pull-down is inactive.

Register: 0xFF30

Multipurpose LED Bank 0L Output (MLO0L)
Read/Write

7	6	5	4	3	2	1	0
MLO0_3A	MLO0_3B	MLO0_2A	MLO0_2B	MLO0_1A	MLO0_1B	MLO0_0A	MLO0_0B
0	0	0	0	0	0	0	0

MLO0_[3A:0A], [3B:0B]

Multipurpose LED Bank 0L Output **[7:0]**

The bits in this register control the Multipurpose LED Bank 0 pins MPLED0_3, MPLED0_2, MPLED0_1, and MPLED0_0. Two bits are used to control each LED, according to Table 8.5.

Table 8.5 LED Behavior

MLOx_xA	MLOx_xB	LED Behavior
0	0	Off
0	1	Slow blink
1	0	Fast blink
1	1	Constant on

The slow blink and fast blink rates are defined in the LED Blink Rate (LBR) register (0xFF04). All LED pins have 16 mA open drain drivers. Turning the LED off (MLOx_xA = 0 and MLOx_xB = 0) effectively 3-states the driver.

Register: 0xFF31

Multipurpose LED Bank 0H Output (MLO0H)
Read/Write

7	6	5	4	3	2	1	0
MLO0_7A	MLO0_7B	MLO0_6A	MLO0_6B	MLO0_5A	MLO0_5B	MLO0_4A	MLO0_4B
Defaults:							
0	0	0	0	0	0	0	0

MLO0_[7A:4A], [7B:4B] **Multipurpose LED Bank 0H Output** **[7:0]**

The bits in this register control the Multipurpose LED Bank 0 pins MPLED0_7, MPLED0_6, MPLED0_5, and MPLED0_4. Two bits are used to control each LED, according to Table 8.5.

The slow blink and fast blink rates are defined in the LED Blink Rate (LBR) register (0xFF04). All LED pins have 16 mA open drain drivers. Turning the LED off (MLOx_xA = 0 and MLOx_xB = 0) effectively 3-states the driver.

Register: 0xFF32

Multipurpose LED Bank 0L Input (MLI0L)
Read Only

7	6	5	4	3	2	1	0
R	MLL0_3	R	MLL0_2	R	MLL0_1	R	MLLO_0
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLL0_[3:0] **Multipurpose LED Bank 0L Input** **[6, 4, 2, 0]**

The bits in this read only register read the live input value on the MPLED0_0, MPLED0_1, MPLED0_2, and MPLED0_3 pins. If these pins are 3-stated using the Multipurpose LED Bank 0 Output registers (0xFF30, 0xFF31), they can be used as input pins.

Register: 0xFF33

Multipurpose LED Bank 0H Input (MLI0H)
Read Only

7	6	5	4	3	2	1	0
R	MLL0_7	R	MLL0_6	R	MLL0_5	R	MLL0_4
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLL0_[7:4] **Multipurpose LED Bank 0H Input** **[6, 4, 2, 0]**
The bits in this read only register read the live input value on the MPLED0_4, MPLED0_5, MPLED0_6, and MPLED0_7 pins. If these pins are 3-stated using the Multipurpose LED Bank 0 Output registers (0xFF30, 0xFF31), they can be used as input pins.

Register: 0xFF34

Multipurpose LED Bank 0L Latch Mask (MLLM0L)
Read/Write

7	6	5	4	3	2	1	0
R	MLLM0_3	R	MLLM0_2	R	MLLM0_1	R	MLLM0_0
Default:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLLM0_[3:0] **Multipurpose LED Bank 0L Latch Mask** **[6, 4, 2, 0]**
The bits in this read/write register define the write mask for the Multipurpose LED Bank 0L Latch (MLL0L) register (0xFF36) and the Multipurpose LED Bank 0H Latch (MLL0H) register (0xFF37). A value of 1 in any of these bits allows the corresponding bit in MLL0L and MLL0H to be modified.

Register: 0xFF35

Multipurpose LED Bank 0H Latch Mask (MLLM0H)
Read/Write

7	6	5	4	3	2	1	0
R	MLLM0_7	R	MLLM0_6	R	MLLM0_5	R	MLLM0_4
Default:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLLM0_[7:4] **Multipurpose LED Bank 0H Latch Mask** **[6, 4, 2, 0]**
The bits in this read/write register define the write mask for the Multipurpose LED Bank 0L Latch (MLL0L) register (0xFF36) and the Multipurpose LED Bank 0H Latch (MLL0H) register (0xFF37). A value of 1 in any of these bits allows the corresponding bit in MLL0L and MLL0H to be modified.

Register: 0xFF36

Multipurpose LED Bank 0L Latch (MLL0L)
Read/Write

7	6	5	4	3	2	1	0
R	MLL0_3	R	MLL0_2	R	MLL0_1	R	MLL0_0
Defaults:							
0	x	0	x	0	x	0	x

R **Reserved** **[7, 5, 3, 1]**

MLL0_[3:0] **Multipurpose LED Bank 0L Latch** **[6, 4, 2, 0]**
The bits in this read/write register store the power-on value of the I/O pins MPLED0_0, MPLED0_1, MPLED0_2, and MPLED0_3. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF37

Multipurpose LED Bank 0H Latch (MLL0H)
Read/Write

7	6	5	4	3	2	1	0
R	MLL0_7	R	MLL0_6	R	MLL0_5	R	MLL0_4
Defaults:							
0	x	0	x	0	x	0	x

R **Reserved** **[7, 5, 3, 1]**

MLL0_[7:4] **Multipurpose LED Bank 0H Latch** **[6, 4, 2, 0]**
The bits in this read/write register store the power-on value of the I/O pins MPLED0_4, MPLED0_5, MPLED0_6, and MPLED0_7. The values on these pins are latched into this register on the deasserting edge of the RESET input signal or the internal power-on reset.

Register: 0xFF38

Multipurpose LED Bank 1L Output (MLO1L)
Read/Write

7	6	5	4	3	2	1	0
MLO1_3A	MLO1_3B	MLO1_2A	MLO1_2B	MLO1_1A	MLO1_1B	MLO1_0A	MLO1_0B
Defaults:							
0	0	0	0	0	0	0	0

MLO1_[3A:0A], [3B:0B]
Multipurpose LED Bank 1L Output **[7:0]**
These bits control the Multipurpose LED Bank 1 pins MPLED1_0, MPLED1_1, MPLED1_2, and MPLED1_3. One pair of bits controls each LED, according to Table 8.6.

Table 8.6 LED Bank 1 Behavior

MLOx_xA	MLOx_xB	LED Behavior
0	0	Off
0	1	Slow blink
1	0	Fast blink
1	1	Constant on

The slow blink and fast blink rates are defined in the LED Blink Rate (LBR) register (0xFF04). All LED pins have 16 mA open drain drivers. Turning the LED off (MLOx_xA = 0 and MLOx_xB = 0) effectively 3-states the driver.

Register: 0xFF39

Multipurpose LED Bank 1H Output (MLO1H)
Read/Write

7	6	5	4	3	2	1	0
MLO1_7A	MLO1_7B	MLO1_6A	MLO1_6B	MLO1_5A	MLO1_5B	MLO1_4A	MLO1_4B
Defaults:							
0	0	0	0	0	0	0	0

MLO1_[7A:4A], [7B:4B]

Multipurpose LED Bank 1H Output **[7:0]**

These bits control the Multipurpose LED Bank 1 pins MPLED1_4, MPLED1_5, MPLED1_6, and MPLED1_7. One pair of bits controls each LED, according to Table 8.6.

The slow blink and fast blink rates are defined in the LED Blink Rate (LBR) register (0xFF04). All LED pins have 16 mA open drain drivers. Turning the LED off (MLOx_xA = 0 and MLOx_xB = 0) effectively 3-states the driver.

Register: 0xFF3A

Multipurpose LED Bank 1L Input (MLI1L)
Read Only

7	6	5	4	3	2	1	0
R	MLI1_3	R	MLI1_2	R	MLI1_1	R	MLI1_0
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLI1_[3:0] **Multipurpose LED Bank 1L Input** **[6, 4, 2, 0]**
The bits in this read only register read the live input value on the MPLED1_0, MPLED1_1, MPLED1_2, and MPLED1_3 pins. If these pins are 3-stated using the Multipurpose LED Bank 2 Output registers (0xFF38, 0xFF39), they can be used as input pins.

Register: 0xFF3B

Multipurpose LED Bank 1H Input (MLI1H)
Read Only

7	6	5	4	3	2	1	0
R	MLI1_7	R	MLI1_6	R	MLI1_5	R	MLI1_4
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLI1_[7:4] **Multipurpose LED Bank 1H Input** **[6, 4, 2, 0]**
The bits in this read only register read the live input value on the MPLED1_4, MPLED1_5, MPLED1_6, and MPLED1_7 pins. If these pins are 3-stated using the Multipurpose LED Bank 2 Output registers (0xFF38, 0xFF39), they can be used as input pins.

Register: 0xFF3C

Multipurpose LED Bank 1L Latch Mask (MLLM1L)
Read/Write

7	6	5	4	3	2	1	0
R	MLLM1_3	R	MLLM1_2	R	MLLM1_1	R	MLLM1_0
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLLM1_[3:0] **Multipurpose LED Bank 1L Latch Mask** **[6, 4, 2, 0]**
These read/write register bits define the write mask for the Multipurpose LED Bank 1L Latch Mask (MLLM1L) register (0xFF3E) and the Multipurpose LED Bank 1H Latch Mask (MLLM1H) register (0xFF3F). A value of 1 in any of these bits allows the corresponding bit in MLL1L and MLL1H to be modified.

Register: 0xFF3D

Multipurpose LED Bank 1H Latch Mask (MLLM1H)
Read/Write

7	6	5	4	3	2	1	0
R	MLLM1_7	R	MLLM1_6	R	MLLM1_5	R	MLLM1_4
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLLM1_[7:4] **Multipurpose LED Bank 1H Latch Mask** **[6, 4, 2, 0]**
These read/write register bits define the write mask for the Multipurpose LED Bank 1L Latch (MLL1L) register (0xFF3E) and the Multipurpose LED Bank 1H Latch (MLL1H) register (0xFF3F). A value of 1 in any of these bits allows the corresponding bit in MLL1L and MLL1H to be modified.

Register: 0xFF3E

Multipurpose LED Bank 1L Latch (MLL1L)
Read/Write

7	6	5	4	3	2	1	0
R	MLL1_3	R	MLL1_2	R	MLL1_1	R	MLL1_0
Defaults:							
0	x	0	x	0	x	0	x

R **Reserved** **[7, 5, 3, 1]**

MLL1_[3:0] **Multipurpose LED Bank 1L Latch Mask** **[6, 4, 2, 0]**
The bits in these read/write registers store the power-on value of the I/O pins MPLED1_0, MPLED1_1, MPLED1_2, and MPLED1_3. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF3F

Multipurpose LED Bank 1H Latch (MLL1H)
Read/Write

7	6	5	4	3	2	1	0
R	MLL1_7	R	MLL1_6	R	MLL1_5	R	MLL1_4
Defaults:							
0	x	0	x	0	x	0	x

R **Reserved** **[7, 5, 3, 1]**

MLL1_[7:4] **Multipurpose LED Bank 1H Latch** **[6, 4, 2, 0]**
The bits in these read/write registers store the power-on value of the I/O pins MPLED1_4, MPLED1_6, MPLED1_5, and MPLED1_7. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF40

Multipurpose LED Bank 2L Output (MLO2L)
Read/Write

7	6	5	4	3	2	1	0
MLO2_3A	MLO2_3B	MLO2_2A	MLO2_2B	MLO2_1A	MLO2_1B	ML02_0A	MLO2_0B
Default:							
0	0	0	0	0	0	0	0

MLO2_[3A:0A], [3B:0B]

Multipurpose LED Bank 2L Output **[7:0]**

These bits control the Multipurpose LED Bank 2 pins MPLED2_0, MPLED2_1, MPLED2_2, and MPLED2_3. Two bits control each LED, according to Table 8.7.

Table 8.7 LED Bank 2 Behavior

MLOx_xA	MLOx_xB	LED Behavior
0	0	Off
0	1	Slow blink
1	0	Fast blink
1	1	Constant on

The slow blink and fast blink rates are defined in the LED Blink Rate (LBR) register (0xFF04). All LED pins have 16 mA open drain drivers. Turning the LED off (MLOx_xA = 0 and MLOx_xB = 0) effectively 3-states the driver.

Register: 0xFF41

Multipurpose LED Bank 2H Output (MLO2H)
Read/Write

7	6	5	4	3	2	1	0
ML02_7A	MLO2_7B	MLO2_6A	MLO2_6B	MLO2_5A	MLO2_5B	ML02_4A	MLO2_4B
Default:							
0	0	0	0	0	0	0	0

MLO2_[7A:4A], [7B:4B]

Multipurpose LED Bank 2H Output **[7:0]**

These bits control the Multipurpose LED Bank 2 pins MPLED2_4, MPLED2_5, MPLED2_6, and MPLED2_7. Two bits control each LED, according to Table 8.7.

The slow blink and fast blink rates are defined in the LED Blink Rate (LBR) register (0xFF04). All LED pins have 16 mA open drain drivers. Turning the LED off (MLOx_xA = 0 and MLOx_xB = 0) effectively 3-states the driver.

Register: 0xFF42

Multipurpose LED Bank 2L Input (MLI2L)
Read Only

7	6	5	4	3	2	1	0
R	MLI2_3	R	MLI2_2	R	MLI2_1	R	MLI2_0
Default:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLI2_[3:0] **Multipurpose LED Bank 2L Input** **[6, 4, 2, 0]**

The bits in this read only register read the live input value on the MPLED2_0, MPLED2_1, MPLED2_2, and MPLED2_3 pins. If these pins are 3-stated using the Multipurpose LED Bank 2 Output Registers (0xFF38, 0xFF39), they can be used as input pins.

Register: 0xFF43

Multipurpose LED Bank 2H Input (MLI2H)
Read Only

7	6	5	4	3	2	1	0
R	MLI2_7	R	MLI2_6	R	MLI2_5	R	MLI2_4
Default:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLI2_[7:4] **Multipurpose LED Bank 2H Input** **[6, 4, 2, 0]**
The bits in this read only register read the live input value on the MPLED2_4, MPLED2_5, MPLED2_6, and MPLED2_7 pins. If these pins are 3-stated using the Multipurpose LED Bank 2 Output Registers (0xFF38, 0xFF39), they can be used as input pins.

Register: 0xFF44

Multipurpose LED Bank 2L Latch Mask (MLLM2L)
Read/Write

7	6	5	4	3	2	1	0
R	MLLM2_3	R	MLLM2_2	R	MLLM2_1	R	MLLM2_0
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLLM2_[3:0] **Multipurpose LED Bank 2L Latch Mask** **[6, 4, 2, 0]**
The bits in this read/write register define the write mask for the Multipurpose LED Bank 2L Latch (MLL2L) register (0xFF3E) and the Multipurpose LED Bank 2H Latch (MLL2H) register (0xFF3F). A value of 1 in any of these bits allows the corresponding bit in MLL2L and MLL2H to be modified.

Register: 0xFF45

Multipurpose LED Bank 2H Latch Mask (MLLM2H)
Read/Write

7	6	5	4	3	2	1	0
R	MLLM2_7	R	MLLM2_6	R	MLLM2_5	R	MLLM2_4
Defaults:							
0	0	0	0	0	0	0	0

R **Reserved** **[7, 5, 3, 1]**

MLLM2_[7:4] **Multipurpose LED Bank 2H Latch Mask** **[6, 4, 2, 0]**
The bits in this read/write register define the write mask for the Multipurpose LED Bank 2L Latch (MLL2L) register (0xFF3E) and the Multipurpose LED Bank 2H Latch (MLL2H) register (0xFF3F). A value of 1 in any of these bits allows the corresponding bit in MLL2L and MLL2H to be modified.

Register: 0xFF46

Multipurpose LED Bank 2L Latch (MLL2L)
Read/Write

7	6	5	4	3	2	1	0
R	MLL2_3	R	MLL2_2	R	MLL2_1	R	MLL2_0
Defaults:							
0	x	0	x	0	x	0	x

R **Reserved** **[7, 5, 3, 1]**

MLL2_[3:0] **Multipurpose LED Bank 2L Latch** **[6, 4, 2, 0]**
These read/write register bits store the power-on value of the I/O pins MPLED2_0, MPLED2_1, MPLED2_2, and MPLED2_3. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Register: 0xFF47

Multipurpose LED Bank 2H Latch (MLL2H)
Read/Write

7	6	5	4	3	2	1	0
R	MLL2_7	R	MLL2_6	R	MLL2_5	R	MLL2_4
Defaults:							
0	x	0	x	0	x	0	x

R **Reserved** **[7, 5, 3, 1]**

MLL2_[7:4] **Multipurpose LED Bank 2H Latch** **[6, 4, 2, 0]**
These read/write register bits store the power-on value of the I/O pins MPLED2_4, MPLED2_6, and MPLED2_7. The values on these pins are latched into this register on the deasserting edge of the RESET/ input signal or the internal power-on reset.

Chapter 9
Electrical Characteristics

This chapter presents the DC characteristics and AC specifications for the LSI53C040, using tables and timing diagrams. Timings for Two-Wire Serial and SFF-8067 operation are compliant with current published standards, and are only discussed briefly in this technical manual. Please refer to the appropriate standards documentation for the latest information.

9.1 Operating Requirements

Table 9.1 Absolute Maximum Stress Ratings

Symbol	Parameter[1]	Min	Max	Units	Test Conditions
T_{stg}	Storage temperature	–55	150	°C	–
V_{dd}	Supply voltage	–0.5	5.0	V	–
V_{in}	Input voltage	V_{SS} –0.3	V_{DD} +0.3	V	–
V_{in5V}	Input voltage (5 V tolerant pins)	V_{SS} –0.3	5.25	V	–
I_{lp}[2]	Latch-up current	150	–	mA	–
ESD[3]	Electrostatic discharge	–	2 K	V	Mil-STD 883C, Method 3015.7

1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed in the Operating Conditions section of this manual is not implied.
2. –2 V < Vpin < 8 V.
3. SCSI pins only.

Table 9.2 Operating Conditions

Symbol	Parameter[1]	Min	Max	Units	Test Conditions
V_{dd}	Supply voltage	3.13	3.47	V	–
I_{dd}	Supply current (dynamic) Supply current (static)	– –	200 1	mA mA	–
$I_{dd\text{-}SCSI}$	LVD pad supply current	–	600	mA	RBIAS = 9.76 kΩ, Vdd = 3.3 V
T_a	Operating free air	–	70	°C	–
θ_{ja}	Thermal resistance (junction to ambient air)	–	67	°C/W	–

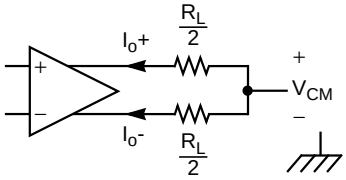
1. Conditions that exceed the operating limits may cause the device to function incorrectly.

9.2 3.3 Volt DC Specifications

Table 9.3 LVD Driver SCSI Signals—SD[7:0]+ SD[7:0]–, SDP0+, SDP0–, SREQ+, SREQ–, SACK/+, SACK/–, SHID[2:0]+, SHID[2:0]–, SMSG/+, SMSG/–, SIO/+, SIO/–, SCD/+, SCD/–, SATN/+, SATN/–, SBSY/+, SBSY/–, SSEL/+, SSEL/–, SRST/+, SRST/–

Symbol	Parameter	Min	Max	Units	Test Conditions
I_O+	Source (+) current	7	13	mA	Asserted state
I_O-	Sink (–) current	–7	–13	mA	Asserted state
I_O+	Source (+) current	–3.5	–6.5	mA	Negated state
I_O-	Sink (–) current	3.5	6.5	mA	Negated state
I_{OZ}	3-state leakage	–20	20	µA	V_{PIN} = 0 V, 3.47 V
I_{OZ} (SRST+, SRST– only)	3-state leakage	–500	–50	µA	–

Figure 9.1 LVD Driver



V_{CM} = 0.7–1.8 V

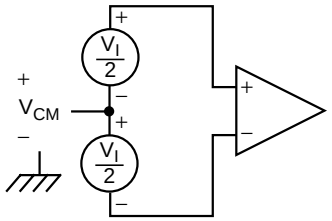
R_L = 0–110 Ω

RBIAS = 9.76 Ω

Table 9.4 LVD Receiver SCSI Signals—SD[7:0]+, SD[7:0]–, SDP0+, SDP0–, SREQ/+, SREQ/–, SACK/+, SACK/–, SMSG/+, SMSG/–, SIO/+, SIO/–, SCD/+, SCD/–, SATN/+, SATN/–, SBSY/+, SBSY/–, SSEL/+, SSEL/–, SRST/+, SRST/–, SHID[2:0]+, SHID[2:0]–

Symbol	Parameter	Min	Max	Units
V_I	LVD receiver voltage asserting	60	–	mV
V_I	LVD receiver voltage negating	–	–60	mV

Figure 9.2 LVD Receiver



V_{CM} = 0.7 - 1.8 V

Table 9.5 SE SCSI and SFF-8067 Signals—SD[7:0]+, SD[7:0]–, SHID[2:0]+, SHID[2:0]–, SDP0+, SDP0–, SREQ+, SREQ–, SACK+, SACK–

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{ih}	Input high voltage	2.0	V_{DD} +0.3	V	–
V_{il}	Input low voltage	V_{SS} –0.3	0.8	V	Referenced to V_{SS}
V_{oh}	Output high voltage	2.0	V_{DD}	V	I_{OH} = 7 mA
V_{ol}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{ol}	Output low voltage (SFF-8067 mode)	V_{SS}	0.5	V	4 mA

Table 9.6 SCSI Signals—DIFFSENS

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{ih}	High differential sense voltage (indicates SFF-8067 mode)	2.4	5.0	V	–
V_{il}	Low differential sense voltage (indicates SE SCSI operation)	V_{SS} –0.3	0.5	V	–
V_{im}	Mid-level differential sense voltage (indicates LVD mode)	0.7	1.9	V	–
I_{in}	Input leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

Table 9.7 Bidirectional 80C32 Signals—AD[7:0], A[15:8], ALE, PSEN/, RD/, WR/

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{ih}	Input high voltage	2.0	5.0	V	–
V_{il}	Input low voltage	V_{SS} –0.3	0.8	V	–
V_{oh}	Output high voltage	2.4	V_{dd}	V	–4 mA
V_{ol}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{oz}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{pull}	Pull-down current	100	–	µA	–

Table 9.8 Input Signals—CLK, TCK, TMS, TDI, TRST/, TESTIN

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{ih}	Input high voltage	2.0	5.0	V	–
V_{il}	Input low voltage	V_{SS} –0.3	0.8	V	–
V_{oh}	Output high voltage	2.4	V_{dd}	V	–4 mA
V_{ol}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{in}	Input leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

Table 9.9 Bidirectional Signals—RESET/, TESTOUT, CL0, SDA0, SCL1, SDA1

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{ih}	Input high voltage	2.0	5.0	V	–
V_{il}	Input low voltage	V_{SS} –0.3	0.8	V	–
V_{oh}	Output high voltage	2.4	V_{dd}	V	–4 mA
V_{ol}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{oz}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

Table 9.10 Bidirectional Signals—MPIO0[7:0], MPIO1[7:0], MPIO2[7:0], MPIO3[3:0]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{ih}	Input high voltage	2.0	5.0	V	–
V_{il}	Input low voltage	V_{SS} –0.3	0.8	V	–
V_{oh}	Output high voltage	2.4	V_{dd}	V	–4 mA
V_{ol}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{oz}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V
I_{pull}	Pull-down current	25	–	µA	–

Table 9.11 Bidirectional Signals—MPLED0[7:0], MPLED1[7:0], MPLED2[7:0]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{ih}	Input high voltage	2.0	5.0	V	–
V_{il}	Input low voltage	V_{SS} –0.5	0.8	V	–
V_{ol}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{oz}	3-state leakage	–10	10	µA	V_{PIN} = 0 V, 5.25 V

9.3 TolerANT Technology Electrical Characteristics

The LSI53C040 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation actively drives the SCSI Request, Acknowledge, Data, and Parity signals HIGH rather than allowing them to be passively pulled up by terminators. Table 9.12 provides electrical characteristics for SE SCSI signals. Figure 9.3 through Figure 9.7 provide reference information for testing SCSI signals.

Table 9.12 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[2]	Output high voltage	2.0	V_{DD}	V	I_{OH} = –7 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	V_{DD} +0.3	V	–
V_{IL}	Input low voltage	V_{SS} –0.3	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	V_{DD} = 4.75;I_I = –20 mA
V_{TH}	Threshold, high to low	1.0	1.2	V	–
V_{TL}	Threshold, low to high	1.4	1.6	V	–
V_{TH}– V_{TL}	Hysteresis	300	500	mV	–
I_{OH}[2]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply[3]
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	20	µA	V_{DD} 5%,V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–20	–	µA	V_{DD} 5%,V_{PIN} = 0 V
I_{PD}	Power down leakage	–	20	µA	V_{DD} = 0 V, V_{PIN} = 1.2 V
R_I	Input resistance	20	–	MΩ	SCSI pins[4]

Table 9.12 TolerANT Technology Electrical Characteristics for SE SCSI Signals[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
C_P	Capacitance per pin	–	15	pF	PQFP
t_R[2]	Rise time, 10% to 90%	4.0	18.5	ns	Figure 9.3
t_F	Fall time, 90% to 10%	4.0	18.5	ns	Figure 9.3
dV_H/dt	Slew rate, low to high	0.15	0.50	V/ns	Figure 9.3
dV_L/dt	Slew rate, high to low	0.15	0.50	V/ns	Figure 9.3
ESD	Electrostatic discharge	2	–	KV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	Figure 9.4
	Ultra filter delay	10	15	ns	Figure 9.4
	Ultra2 filter delay	5	8	ns	Figure 9.4
	Extended filter delay	40	60	ns	Figure 9.4

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, SACK/. (Minus Pins) SCSI mode only.
3. Single pin only; irreversible damage may occur if sustained for one second.
4. SCSI RESET pin has 10 KΩ pull-up resistor.

Figure 9.3 Rise and Fall Time Test Condition

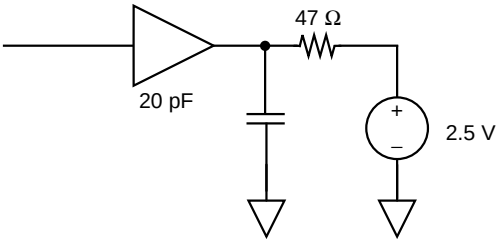
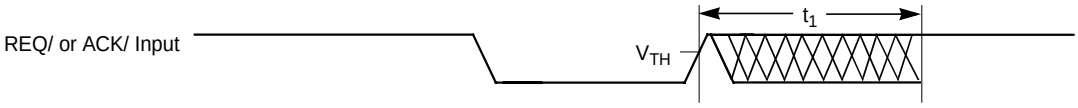


Figure 9.4 SCSI Input Filtering



Note: t_1 is the input filtering period.

Figure 9.5 Hysteresis of SCSI Receivers

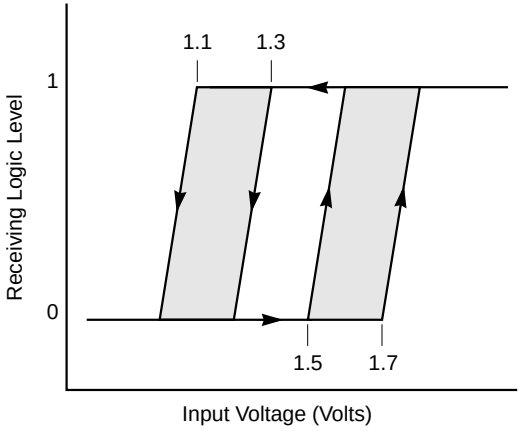


Figure 9.6 Input Current as a Function of Input Voltage

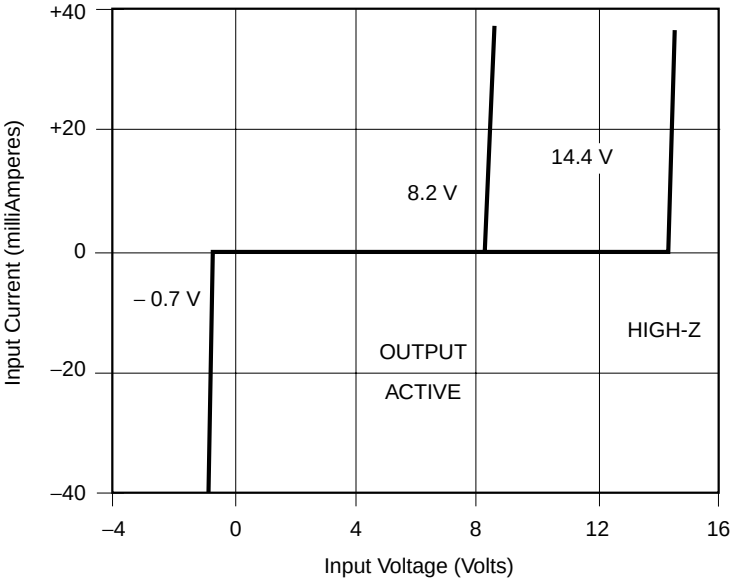
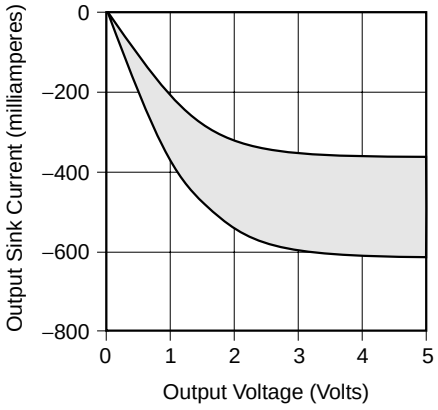
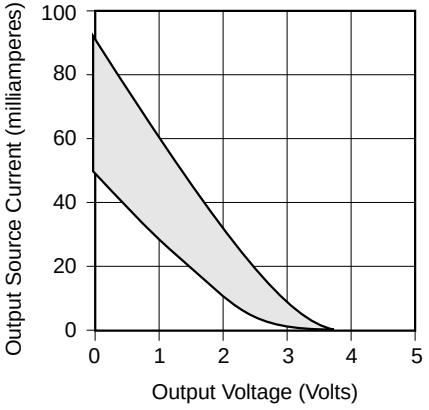


Figure 9.7 Output Current as a Function of Output Voltage





9.4 AC Characteristics

9.4.1 Clock Timing

Figure 9.8 LSI53C040 Clock Waveforms

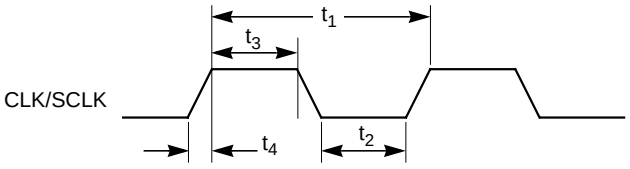


Table 9.13 LSI53C040 Clock Timings[1]

Symbol	Parameter	Min	Max	Units
t_1	CLK clock period	25	DC	ns
t_2	CLK low time	10	–	ns
t_3	CLK high time	10	–	ns
t_4	CLK slew rate	1	–	V/ns

1. Duty cycle not to exceed 60/40.

9.4.2 Reset Signal

Figure 9.9 Reset Waveforms

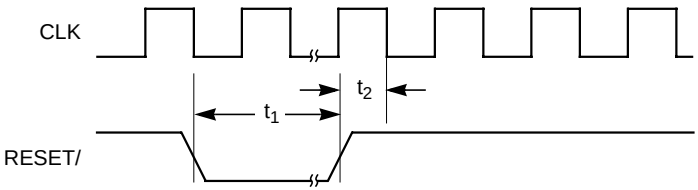


Table 9.14 Reset Timings

Symbol	Parameter	Min	Max	Units
t_1	Reset Input Pulse Width	10 tclk	–	ns
t_1	Reset Output Pulse Width	15 tclk	–	ns
t_2	Reset deasserted setup to CLK high	0	–	ns

9.5 Microcontroller Interface Timings

This section provides timing information for the microcontroller interface. The AC characteristics described in this section apply over the entire range of operating conditions for the LSI53C040.

9.5.1 External Memory Interface

Figure 9.10 External Memory Interface Waveforms

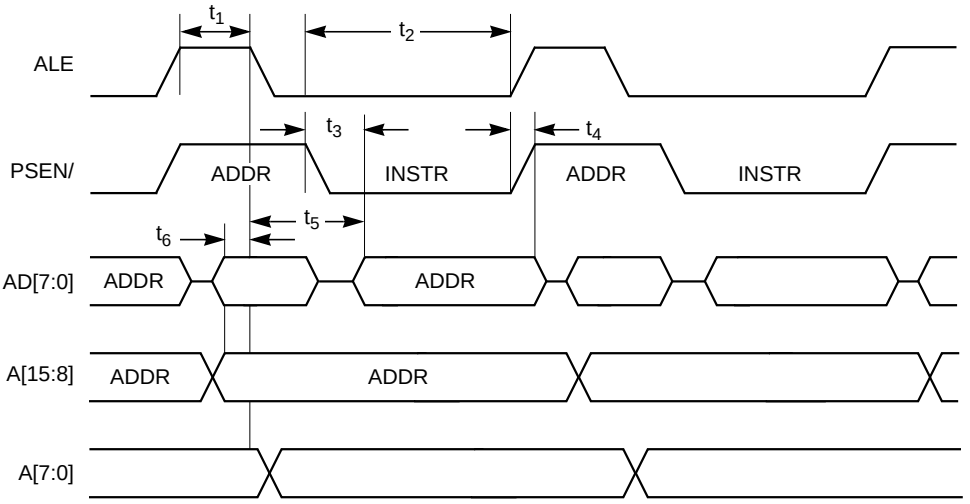


Table 9.15 External Memory Interface Timings

Symbol	Parameter	Min	Max	Units
T_1	ALE pulse width = duration of positive ALE pulse	23	–	ns
T_2	PSEN/ pulse width = duration of negative PSEN/ pulse	75	–	ns
T_3	PSEN/ falling to instruction valid = maximum delay from PSEN/ falling to input data valid	–	55	ns
T_4	Data hold to PSEN/ rising = minimum hold time for data after PSEN/ rises	0	–	ns
T_5	ALE falling to instruction valid = maximum delay from ALE falling to input data valid	–	80	ns
T_6	Address valid to ALE falling = minimum setup time for A[15:8] and AD[7:0] to ALE falling	20	–	ns

9.5.2 External Data Read Cycle

Figure 9.11 External Data Read Waveforms

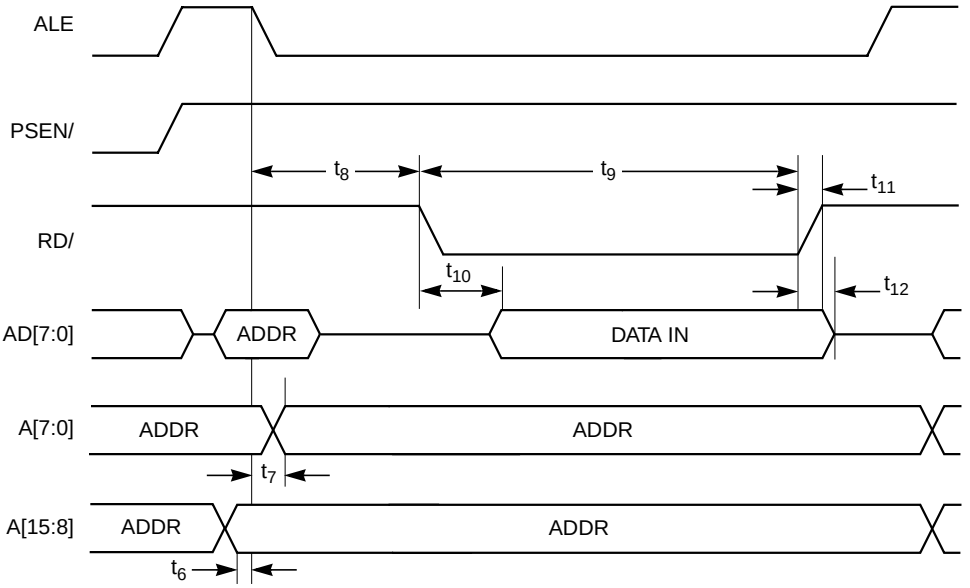


Table 9.16 External Data Read Timings

Symbol	Parameter	Min	Max	Units
t_8	ALE to RD/ = Minimum delay from ALE falling to RD/ falling	50	–	ns
t_9	RD/ pulse width = Minimum time RD/ is low	50	–	ns
t_{10}	RD/ to valid data in = Maximum delay from RD/ falling to data valid	–	48	ns
t_{11}	Data hold after RD/	0	–	ns
t_{12}	Data float after RD/	–	5	ns
t_6	Address Valid to ALE Falling = Minimum setup time for A[15:8] and AD[7:0] to ALE falling	20	–	ns
t_7	ALE Falling to Lower Address Valid = Maximum delay from ALE falling to A[7:0] valid	–	10	–

9.5.3 External Data Write Cycle

Figure 9.12 External Data Write Waveforms

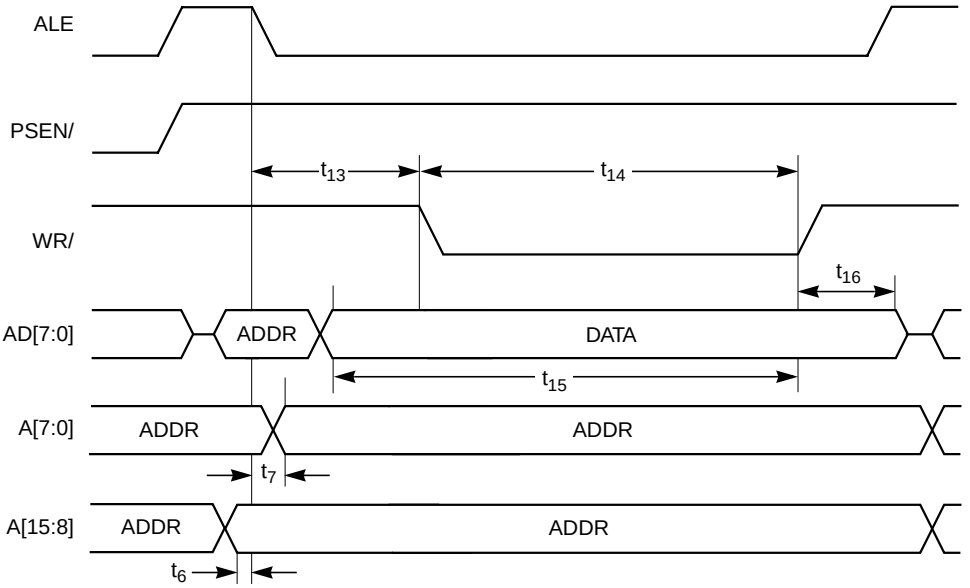


Table 9.17 External Data Write Timings

Symbol	Parameter	Min	Max	Units
t_{13}	ALE to WR/ = Minimum delay from ALE falling to WR/ falling	50	–	ns
t_{14}	WR/ pulse width = Minimum time WR/ is low	50	–	ns
t_{15}	Data setup to WR/ = Minimum time data is valid prior to WR/ rising	50	–	ns
t_{16}	Data hold after WR/ = Minimum time data is valid after WR/ rising	20	–	ns
t_6	Address Valid to ALE Falling = Minimum setup time for A[15:8] and AD[7:0] to ALE falling	20	–	ns
t_7	ALE Falling to Lower Address Valid = Maximum delay from ALE falling to AD[7:0] valid	–	10	ns

9.6 Multipurpose Register Access

The timings in Table 9.18 apply to register accesses to control the MPIO and MPLED pins. Please refer to Chapter 2 for more information on specifying the operation of these pins.

Table 9.18 Multipurpose I/O and LED Timings

Parameter	Min	Max	Units
Shared input setup	20	–	ns
Shared input hold	10	–	ns
CLK to output valid	20	–	ns

9.7 Two-Wire Serial Timings

The LSI53C040 Two-Wire Serial interface timings comply with the Inter-Integrated Circuit specification. Please refer to the specification for more information.

Figure 9.13 Two-Wire Serial Bus Timings

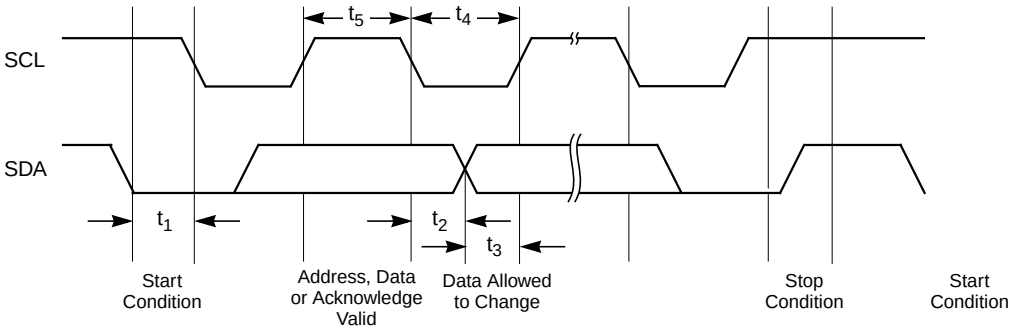


Table 9.19 Two-Wire Serial Interface Timings, Normal Mode (100 KHz Clock)

Symbol	Description	Min	Max	Units
t_1	Hold time after start condition	4.0	–	µs
t_2	Data hold	0	–	µs
t_3	Data setup	250	–	ns
t_4	SCL low period	4.7	–	µs
t_5	SCL high period	4.0	–	µs

Table 9.20 Two-Wire Interface Timings, Fast Mode (400 KHz Clock)

Symbol	Description	Min	Max	Units
t_1	Hold time after start condition	0.6	–	µs
t_2	Data hold	0	0.9	µs
t_3	Data setup	100	–	ns
t_4	SCL low period	1.3	–	µs
t_5	SCL high period	0.6	–	µs

9.8 SFF-8067 Interface Timings

Figure 9.14 SFF-8067 Discovery Phase Waveforms

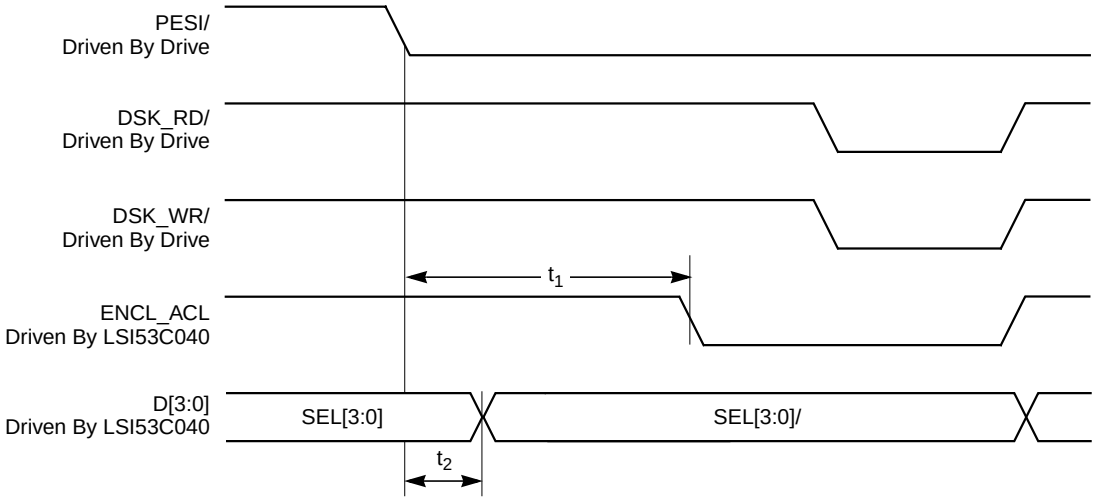


Figure 9.15 SFF-8067 Write Phase Waveforms

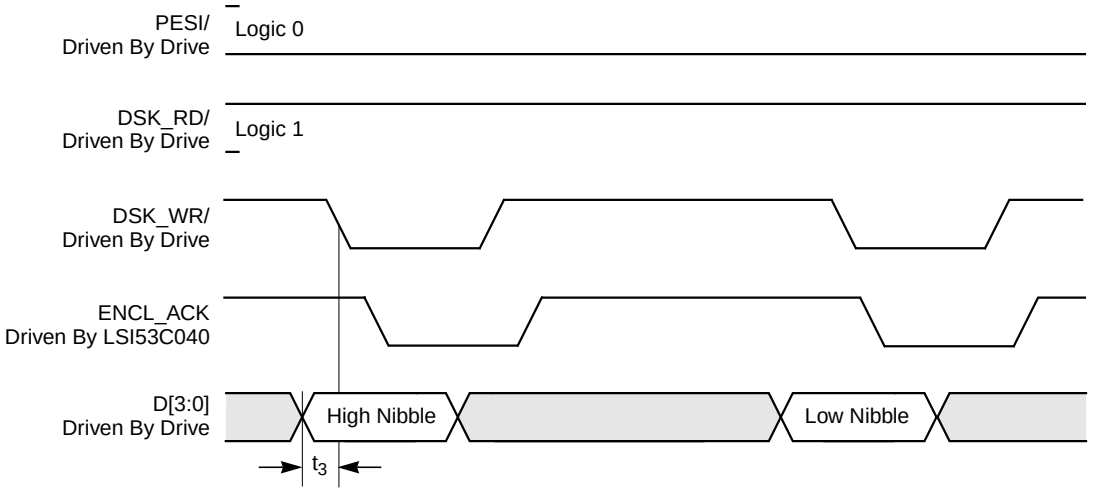


Figure 9.16 SFF-8067 Read Waveforms

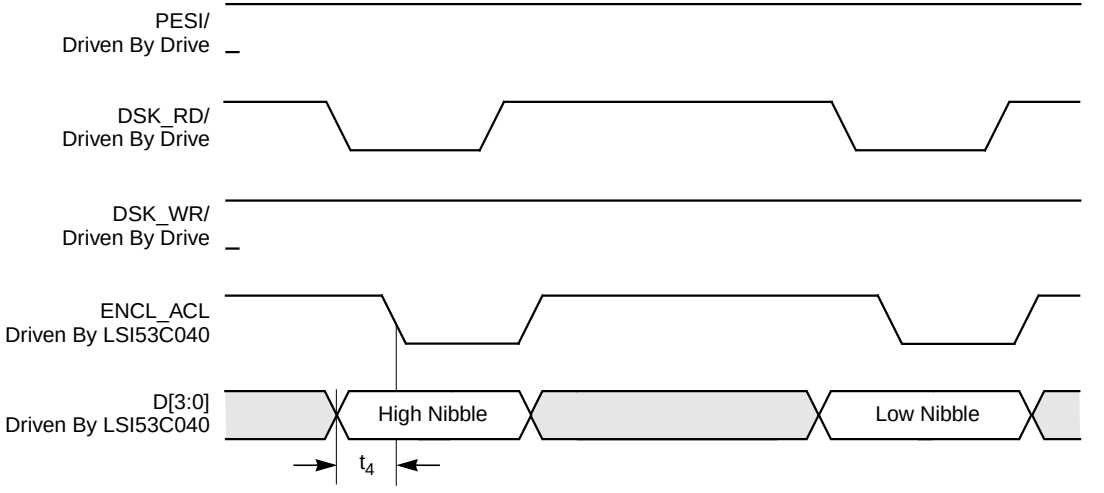


Table 9.21 SFF-8067 Interface Timings

Parameter	Description	Min	Max	Units
t_1	PESI/ LOW to ENCL_ACK/ LOW	–	1	s
t_2	Data hold from PESI/ LOW	–	1	µs
t_3	Data setup to DSK_WR/ LOW	100	–	ns
t_4	Data setup to ENCL_ACK/ LOW	100	–	ns

9.9 SCSI Timings

9.9.1 Initiator Asynchronous Send

Figure 9.17 Initiator Asynchronous Send Waveforms

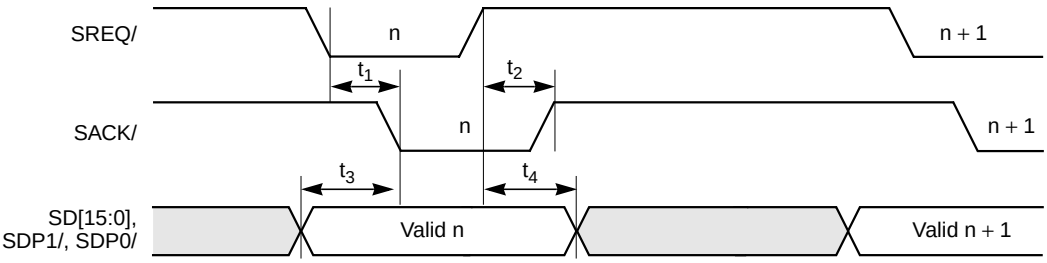


Table 9.22 Initiator Asynchronous Send Timings

Symbol	Description	Min	Max	Units
t_1	SACK asserted from SREQ deasserted	5	–	ns
t_2	SACK deasserted from SREQ deasserted	5	–	ns
t_3	Data setup to SACK asserted	55	–	–
t_4	Data hold from SREQ deasserted	20	–	–

9.9.2 Initiator Asynchronous Receive

Figure 9.18 Initiator Asynchronous Receive Waveforms

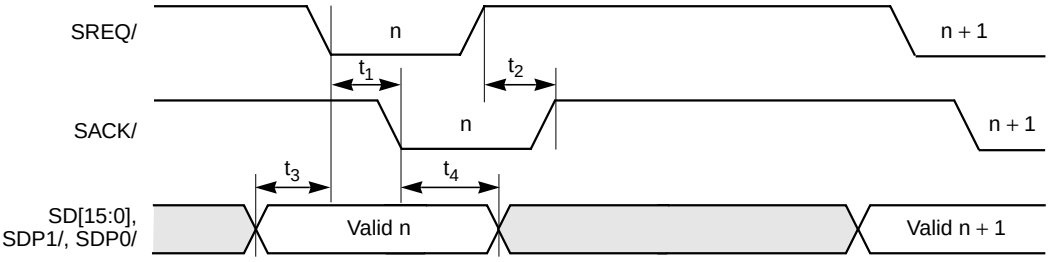


Table 9.23 Initiator Asynchronous Receive Timings

Symbol	Description	Min	Max	Units
t_1	ACK asserted from REQ deasserted	5	–	ns
t_2	ACK deasserted from REQ deasserted	5	–	ns
t_3	Data setup to REQ asserted	0	–	–
t_4	Data hold from ACK deasserted	0	–	–

9.9.3 Target Asynchronous Send

Figure 9.19 Target Asynchronous Send Waveforms

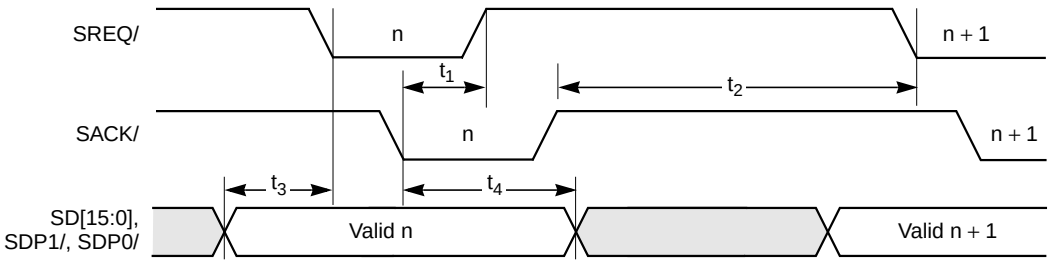


Table 9.24 Target Asynchronous Send Timings

Symbol	Description	Min	Max	Units
t_1	REQ deasserted from REACKQ asserted	5	–	ns
t_2	REQ asserted from ACK deasserted	5	–	ns
t_3	Data setup to REQ asserted	55	–	–
t_4	Data hold from ACK asserted	20	–	–

9.9.4 Target Asynchronous Receive

Figure 9.20 Target Asynchronous Receive Waveforms

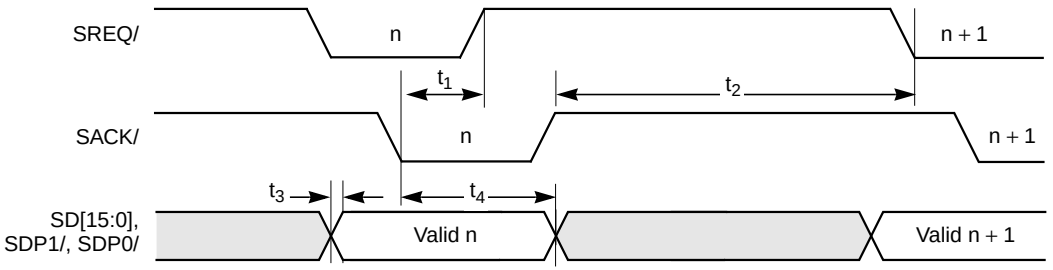


Table 9.25 Target Asynchronous Receive Timings

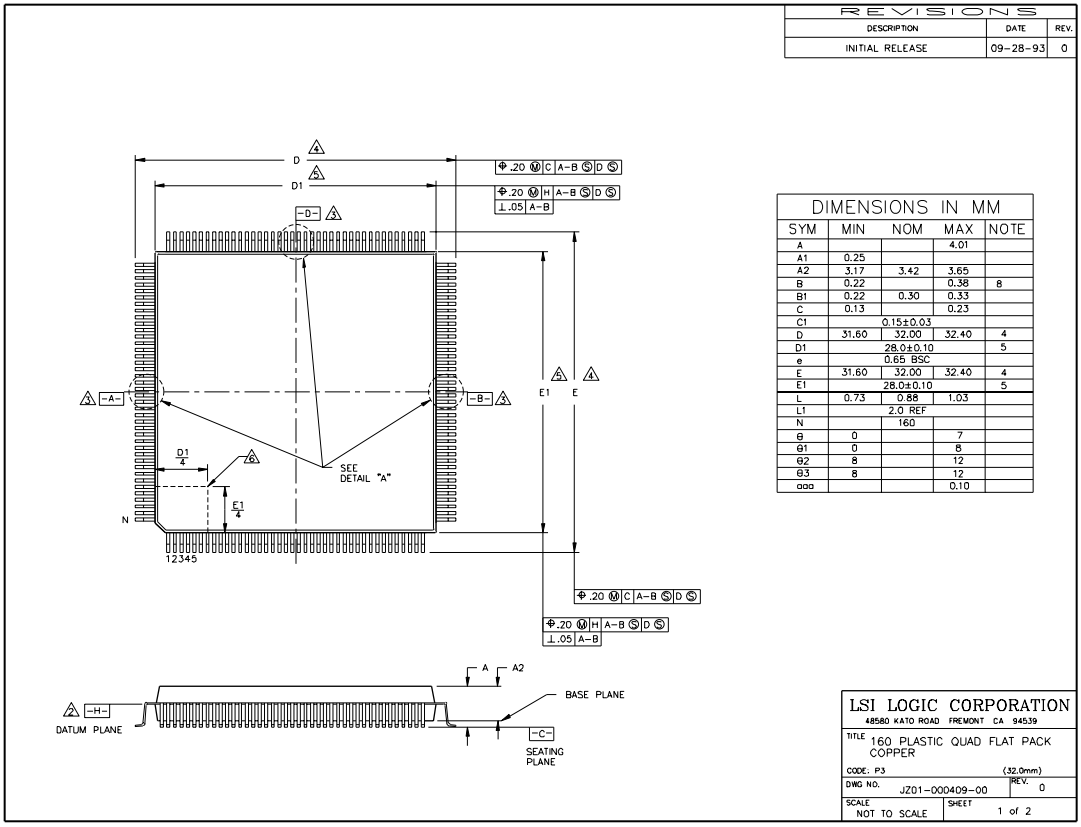
Symbol	Description	Min	Max	Units
t_1	REQ deasserted from ACK asserted	5	–	ns
t_2	REQ asserted from ACK deasserted	5	–	ns
t_3	Data setup to ACK asserted	0	–	–
t_4	Data hold from REQ deasserted	0	–	–

9.10 Mechanical Drawings

For printed circuit board land patterns that accept LSI Logic components, it is recommended that customers refer to the IPC standards (Institute for Interconnecting and Packaging Electronic Circuits). Specification IPC-SM-782, *Surface Mount Design and Land Pattern Standard* is an established method of designing land patterns. Feature size and tolerances are industry standards based on IPC assumptions.

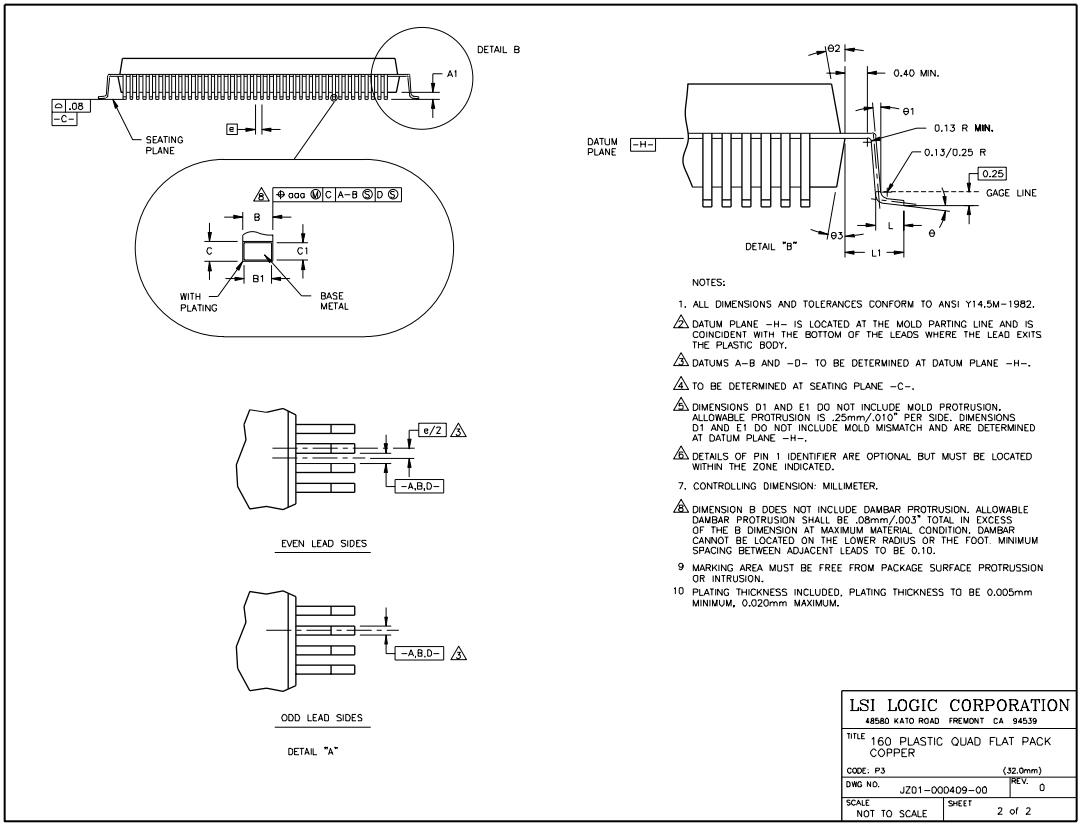
All package dimensions are in millimeters. Figure 9.21 and Figure 9.22 are the mechanical drawings of the two package options for the LSI53C040.

Figure 9.21 160-Lead PQFP (P3) Mechanical Drawing (Sheet 1 of 2)



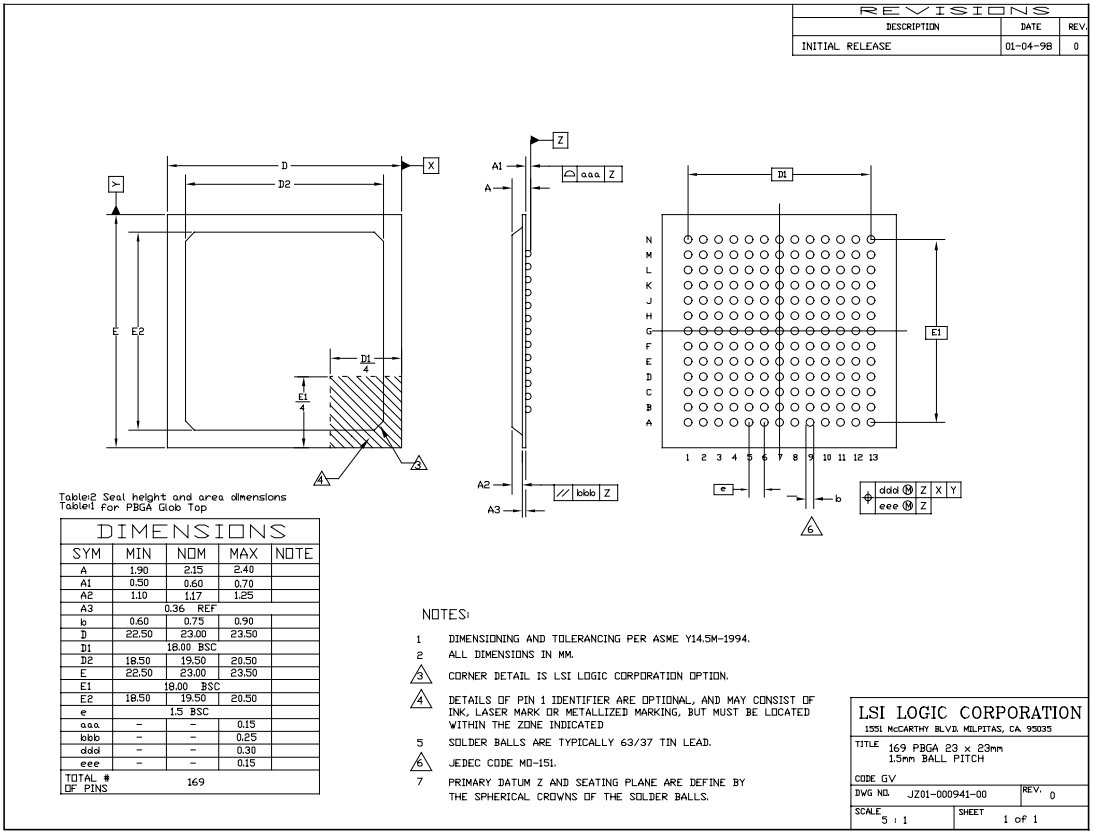
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code P3.**

Figure 9.21 160-Lead PQFP (P3) Mechanical Drawing (Sheet 2 of 2)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code P3.**

Figure 9.22 169-Pin PBGA (GV) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code GV.**

Appendix A
Register Summary

Table A.1 Register Summary by Description

Description	Address	R/W	Page #
Bus and Status (BSR)	0xFC05	Read Only	4-10
Clock (ES0, ES1, ES2 = 010)	0xFD00/0xFD02	Read/Write	6-3
Control Register Reads (ES0 = 0)	0xFD01/0xFD03	Read Only	6-6
Control Register Writes	0xFD01/0xFD03	Write Only	6-5
Current SCSI Bus Status (CSBS)	0xFC04	Read Only	4-9
Current SCSI Data (CSD)	0xFC00	Read Only	4-3
Current SCSI Data High (CSDHI)	0xFC08	Read Only	4-13
Data (ES0, ES1, ES2 = 100)	0xFD00/0xFD02	Read/Write	6-4
DMA Interrupt (DMAI)	0xFC14	Read/Write	4-17
DMA Send (DSR)	0xFC05	Write Only	4-12
DMA Source/Destination High (DSDH)	0xFC13	Read/Write	4-16
DMA Source/Destination Low (DSDL)	0xFC12	Read/Write	4-16
DMA Status (DS)	0xFC10	Read/Write	4-14
DMA Transfer Length (DTL)	0xFC11	Read/Write	4-15
Initiator Command (ICR)	0xFC01	Read/Write	4-4
Interrupt Destination (IDR)	0xFE0E	Read/Write	7-15
Interrupt Mask (IMR)	0xFE0D	Read/Write	7-13
Interrupt Status (ISR)	0xFE04	Read/Write	7-7
LED Blink Rate (LBR)	0xFF04	Read/Write	8-6

Table A.1 Register Summary by Description (Cont.)

Description	Address	R/W	Page #
Live ESI (LESI0/LESI1)	0xFC24/0xFC2C	Read Only	5-5
Manual Data Output (MDATA0/MDATA1)	0xFC25/0xFC2D	Read/Write	5-6
Miscellaneous	0xFD04	Read Only	6-9
Miscellaneous Control (MCR)	0xFE03	Read/Write	7-6
Mode (MR)	0xFC02	Read/Write	4-6
Multipurpose I/O Bank 0 Enable (MPE0)	0xFF09	Read/Write	8-9
Multipurpose I/O Bank 0 Input (MPI0)	0xFF0A	Read Only	8-9
Multipurpose I/O Bank 0 Latch (MPL0)	0xFF0C	Read/Write	8-10
Multipurpose I/O Bank 0 Latch Mask (MPLM0)	0xFF0B	Read/Write	8-10
Multipurpose I/O Bank 0 Output (MPO0)	0xFF08	Read/Write	8-8
Multipurpose I/O Bank 0 Pull-down Enable (MPPE0)	0xFF0D	Read/Write	8-11
Multipurpose I/O Bank 1 Enable (MPE1)	0xFF11	Read/Write	8-12
Multipurpose I/O Bank 1 Input (MPI1)	0xFF12	Read Only	8-12
Multipurpose I/O Bank 1 Latch (MPL1)	0xFF14	Read/Write	8-13
Multipurpose I/O Bank 1 Latch Mask (MPLM1)	0xFF13	Read/Write	8-13
Multipurpose I/O Bank 1 Output (MPO1)	0xFF10	Read/Write	8-11
Multipurpose I/O Bank 1 Pull-down Enable (MPPE1)	0xFF15	Read/Write	8-14
Multipurpose I/O Bank 2 Enable (MPE2)	0xFF19	Read/Write	8-15
Multipurpose I/O Bank 2 Input (MPI2)	0xFF1A	Read Only	8-15
Multipurpose I/O Bank 2 Latch (MPL2)	0xFF1C	Read/Write	8-16
Multipurpose I/O Bank 2 Latch Mask (MPLM2)	0xFF1B	Read/Write	8-16
Multipurpose I/O Bank 2 Output (MPO2)	0xFF18	Read/Write	8-14
Multipurpose I/O Bank 2 Pull-down Enable (MPPE2)	0xFF1D	Read/Write	8-17
Multipurpose I/O Bank 3 Enable (MPE3)	0xFF21	Read/Write	8-18
Multipurpose I/O Bank 3 Input (MPI3)	0xFF22	Read Only	8-19

Table A.1 Register Summary by Description (Cont.)

Description	Address	R/W	Page #
Multipurpose I/O Bank 3 Latch (MPL3)	0xFF24	Read/Write	8-20
Multipurpose I/O Bank 3 Latch Mask (MPLM3)	0xFF23	Read/Write	8-19
Multipurpose I/O Bank 3 Output (MPO3)	0xFF20	Read/Write	8-17
Multipurpose I/O Bank 3 Pull-down Enable (MPPE3)	0xFF25	Read/Write	8-20
Multipurpose LED Bank 0H Input (MLI0H)	0xFF33	Read Only	8-23
Multipurpose LED Bank 0H Latch (MLL0H)	0xFF37	Read/Write	8-25
Multipurpose LED Bank 0H Latch Mask (MLLM0H)	0xFF35	Read/Write	8-24
Multipurpose LED Bank 0H Output (MLO0H)	0xFF31	Read/Write	8-22
Multipurpose LED Bank 0L Input (MLI0L)	0xFF32	Read Only	8-22
Multipurpose LED Bank 0L Latch (MLL0L)	0xFF36	Read/Write	8-24
Multipurpose LED Bank 0L Latch Mask (MLLM0L)	0xFF34	Read/Write	8-23
Multipurpose LED Bank 0L Output (MLO0L)	0xFF30	Read/Write	8-21
Multipurpose LED Bank 1H Input (MLI1H)	0xFF3B	Read Only	8-27
Multipurpose LED Bank 1H Latch (MLL1H)	0xFF3F	Read/Write	8-29
Multipurpose LED Bank 1H Latch Mask (MLLM1H)	0xFF3D	Read/Write	8-28
Multipurpose LED Bank 1H Output (MLO1H)	0xFF39	Read/Write	8-26
Multipurpose LED Bank 1L Input (MLI1L)	0xFF3A	Read Only	8-27
Multipurpose LED Bank 1L Latch (MLL1L)	0xFF3E	Read/Write	8-29
Multipurpose LED Bank 1L Latch Mask (MLLM1L)	0xFF3C	Read/Write	8-28
Multipurpose LED Bank 1L Output (MLO1L)	0xFF38	Read/Write	8-25
Multipurpose LED Bank 2H Input (MLI2H)	0xFF43	Read Only	8-32
Multipurpose LED Bank 2H Latch (MLL2H)	0xFF47	Read/Write	8-34
Multipurpose LED Bank 2H Latch Mask (MLLM2H)	0xFF45	Read/Write	8-33
Multipurpose LED Bank 2H Output (MLO2H)	0xFF41	Read/Write	8-31
Multipurpose LED Bank 2L Input (MLI2L)	0xFF42	Read Only	8-31

Table A.1 Register Summary by Description (Cont.)

Description	Address	R/W	Page #
Multipurpose LED Bank 2L Latch (MLL2L)	0xFF46	Read/Write	8-33
Multipurpose LED Bank 2L Latch Mask (MLLM2L)	0xFF44	Read/Write	8-32
Multipurpose LED Bank 2L Output (MLO2L)	0xFF40	Read/Write	8-30
Output Data (ODR)	0xFC00	Write Only	4-3
Own Address (ES0, ES1, ES2 = 000)	0xFD00/0xFD02	Read/Write	6-3
Physical Address (PHAD0/PHAD1)	0xFC23/0xFC2B	Read Only	5-5
Port Control/Status (PCST0/PCST1)	0xFC22/0xFC2A	Read/Write	5-3
Power-On Configuration One (POC1)	0xFF03	Read Only	8-5
Power-On Configuration Zero (POC0)	0xFF01	Read Only	8-4
Read Data (RDATA0/RDATA1)	0xFC20/0xFC28	Read/Write	5-3
Reset Parity/Interrupt (RPI)	0xFC07	Read Only	4-12
Select Enable (SER)	0xFC04	Write Only	4-10
Select Enable High (SENHI)	0xFC0C	Write Only	4-13
Start DMA Initiator Receive (SDIR)	0xFC07	Write Only	4-13
Start DMA Target Receive (SDTR)	0xFC06	Write Only	4-12
Status Register Reads (ES0 = 1)	0xFD01/0xFD03	Read Only	6-7
System Control (SYSCTRL)	0xFF05	Read/Write	8-7
Target Command (TC)	0xFC03	Read/Write	4-8
Timer 1 Control (T1C)	0xFE05	Read/Write	7-8
Timer 1 Final Chain (T1FC)	0xFE08	Read Only	7-10
Timer 1 Secondary Chain (T1SC)	0xFE07	Read Only	7-12
Timer 1 Threshold (T1TH)	0xFE06	Read/Write	7-9
Timer 2 Control (T2C)	0xFE09	Read/Write	7-11
Timer 2 Final Chain (T2FC)	0xFE0C	Read Only	7-13
Timer 2 Secondary Chain (T2SC)	0xFE0B	Read Only	7-12

Table A.1 Register Summary by Description (Cont.)

Description	Address	R/W	Page #
Timer 2 Threshold (T2T)	0xFE0A	Read/Write	7-12
UC Control ITF0	0xFD06	Read/Write	6-10
UC Control ITF1	0xFD05	Read/Write	6-9
Watchdog Final Chain (WDFC)	0xFE02	Read Only	7-5
Watchdog Secondary Chain (WDSC)	0xFE01	Read Only	7-5
Watchdog Timer Control (WDTC)	0xFE00	Read/Write	7-3
Write Data (WDATA0/WDATA1)	0xFC21/0xFC29	Read/Write	5-3

Table A.2 Register Summary by Address

Address	Description	R/W	Page #
0xFC00	Current SCSI Data (CSD)	Read Only	4-3
0xFC00	Output Data (ODR)	Write Only	4-3
0xFC01	Initiator Command (ICR)	Read/Write	4-4
0xFC02	Mode (MR)	Read/Write	4-6
0xFC03	Target Command (TC)	Read/Write	4-8
0xFC04	Current SCSI Bus Status (CSBS)	Read Only	4-9
0xFC04	Select Enable (SER)	Write Only	4-10
0xFC05	Bus and Status (BSR)	Read Only	4-10
0xFC05	DMA Send (DSR)	Write Only	4-12
0xFC06	Start DMA Target Receive (SDTR)	Write Only	4-12
0xFC07	Reset Parity/Interrupt (RPI)	Read Only	4-12
0xFC07	Start DMA Initiator Receive (SDIR)	Write Only	4-13
0xFC08	Current SCSI Data High (CSDHI)	Read Only	4-13
0xFC0C	Select Enable High (SENHI)	Write Only	4-13
0xFC10	DMA Status (DS)	Read/Write	4-14

Table A.2 Register Summary by Address (Cont.)

Address	Description	R/W	Page #
0xFC11	DMA Transfer Length (DTL)	Read/Write	4-15
0xFC12	DMA Source/Destination Low (DSDL)	Read/Write	4-16
0xFC13	DMA Source/Destination High (DSDH)	Read/Write	4-16
0xFC14	DMA Interrupt (DMAI)	Read/Write	4-17
0xFC20/0xFC28	Read Data (RDATA0/RDATA1)	Read/Write	5-3
0xFC21/0xFC29	Write Data (WDATA0/WDATA1)	Read/Write	5-3
0xFC22/0xFC2A	Port Control/Status (PCST0/PCST1)	Read/Write	5-3
0xFC23/0xFC2B	Physical Address (PHAD0/PHAD1)	Read Only	5-5
0xFC24/0xFC2C	Live ESI (LESI0/LESI1)	Read Only	5-5
0xFC25/0xFC2D	Manual Data Output (MDATA0/MDATA1)	Read/Write	5-6
0xFD00/0xFD02	Clock (ES0, ES1, ES2 = 010)	Read/Write	6-3
0xFD00/0xFD02	Data (ES0, ES1, ES2 = 100)	Read/Write	6-4
0xFD00/0xFD02	Own Address (ES0, ES1, ES2 = 000)	Read/Write	6-3
0xFD01/0xFD03	Control Register Reads (ES0 = 0)	Read Only	6-6
0xFD01/0xFD03	Control Register Writes	Write Only	6-5
0xFD01/0xFD03	Status Register Reads (ES0 = 1)	Read Only	6-7
0xFD04	Miscellaneous	Read Only	6-9
0xFD05	UC Control ITF1	Read/Write	6-9
0xFD06	UC Control ITF0	Read/Write	6-10
0xFE00	Watchdog Timer Control (WDTC)	Read/Write	7-3
0xFE01	Watchdog Secondary Chain (WDSC)	Read Only	7-5
0xFE02	Watchdog Final Chain (WDFC)	Read Only	7-5
0xFE03	Miscellaneous Control (MCR)	Read/Write	7-6
0xFE04	Interrupt Status (ISR)	Read/Write	7-7
0xFE05	Timer 1 Control (T1C)	Read/Write	7-8

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