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# NET2272 USB 2.0 Interface Controller: DMA Transfer Performance Report

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**Revision:** 1.0  
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## **Purpose**

This document outlines and analyzes USB bandwidth measurement tests of the NET2272 with DMA transfer and their results.

## **Test Setup**

### USB Device

- NET2272 PCI-RDK
- Generic 80MHz EPLD DMA Controller

The [NET2272 PCI-RDK](#) is a PCI based development board for the NET2272. When plugged into a PC, the NET2272 PCI-RDK turns the PC into a USB Device.

For the NET2272 local bus interface, the NET2272 PCI-RDK uses an Altera EPLD part. The EPLD runs at 80 MHz and is programmed to perform DMA transactions as well as I/O transactions. DMA request from the NET2272 can be serviced by a simple DMA state machine in the EPLD, or can be passed to the PCI bus on the NET2272 PCI-RDK board. For this test, the simple DMA state machine is used to service DMA request from the NET2272.

### USB Host Machine

- Pentium 4, 2.0 GHz
- 512 MB RAM
- Chipset containing Intel® 82801DB I/O Controller Hub 4 (ICH4)
- Microsoft Windows XP

The ICH4 is the USB host controller in our host PC and is one of the fastest USB 2.0 host controllers currently available.

WinMon, NetChip's USB host debug user application, is used to initiate transfers. The host PC loads NcBulk, NetChip's general purpose USB client driver, when the NET2272 PCI-RDK is plugged into the host controller and enumerates.

## **Test Measurement**

### Local Bus

- Agilent 16702B Logic Analysis System
- 3ns sample period

For each DMA mode of the NET2272, DMA transaction timing is measured by the Agilent logic analyzer, with sample period of 3 ns.

### USB Bus

- CATC Advisor™ USB 2.0 Bus & Protocol Analyzer

In order to measure the USB transfer rate of the NET2272, the CATC USB analyzer is used. The microframe transfer rate\* is calculated by counting the number of

bytes transferred in one USB microframe and divide the number of bytes by the microframe period.

The microframe transfer rate, however, cannot be sustained by the host controller. WinMon can only initiate transfers of a finite size. When one transfer completes, the OS must make a context switch back to WinMon so that another transfer can be re-submitted. This results in approximately a 2 Megabyte/second penalty resulting in a sustained transfer rate<sup>\*\*</sup>.

## **Results**

Bus Mode	DMA Mode	Sample Period	IN Transfer Rate (MB/sec)	OUT Transfer Rate (MB/sec)
8 Bit	Slow	uFrame*	12.29	12.29
		Sustained**	10.29	10.29
	Fast	uFrame	20.48	20.48
		Sustained	18.48	18.48
	Burst	uFrame	26.62	24.58
		Sustained	24.62	22.58
16 Bit	Slow	uFrame	24.57	24.57
		Sustained	22.57	22.57
	Fast	uFrame	36.86	32.77
		Sustained	34.86	30.77
	Burst	uFrame	40.96	32.77
		Sustained	38.96	30.77

\* microframe transfer rate

\*\* sustained microframe transfer rate

Table 0.1 USB transfer rate

## **1. Slow DMA Mode**

As shown in the timing diagrams below (Figure 1.1.1 and Figure 1.1.2), in Slow DMA mode, the NET2272 de-asserts DREQ typically within 45 ns after DACK is asserted. Then it asserts DREQ again typically within 21 ns after the end of the previous transaction. The Table 1.1 summarizes the performance of DMA write and DMA read in Slow Mode.

	DREQ to DACK (ns)	DACK to ~DREQ (ns)	~DREQ to DREQ (ns)	Total (ns)
DMA Write	15 ~ 21	42 ~ 45	18 ~ 21	81
DMA Read	15 ~ 21	42 ~ 45	18 ~ 21	81

Table 1.1 Typical DMA timing for Slow Mode DMA transaction

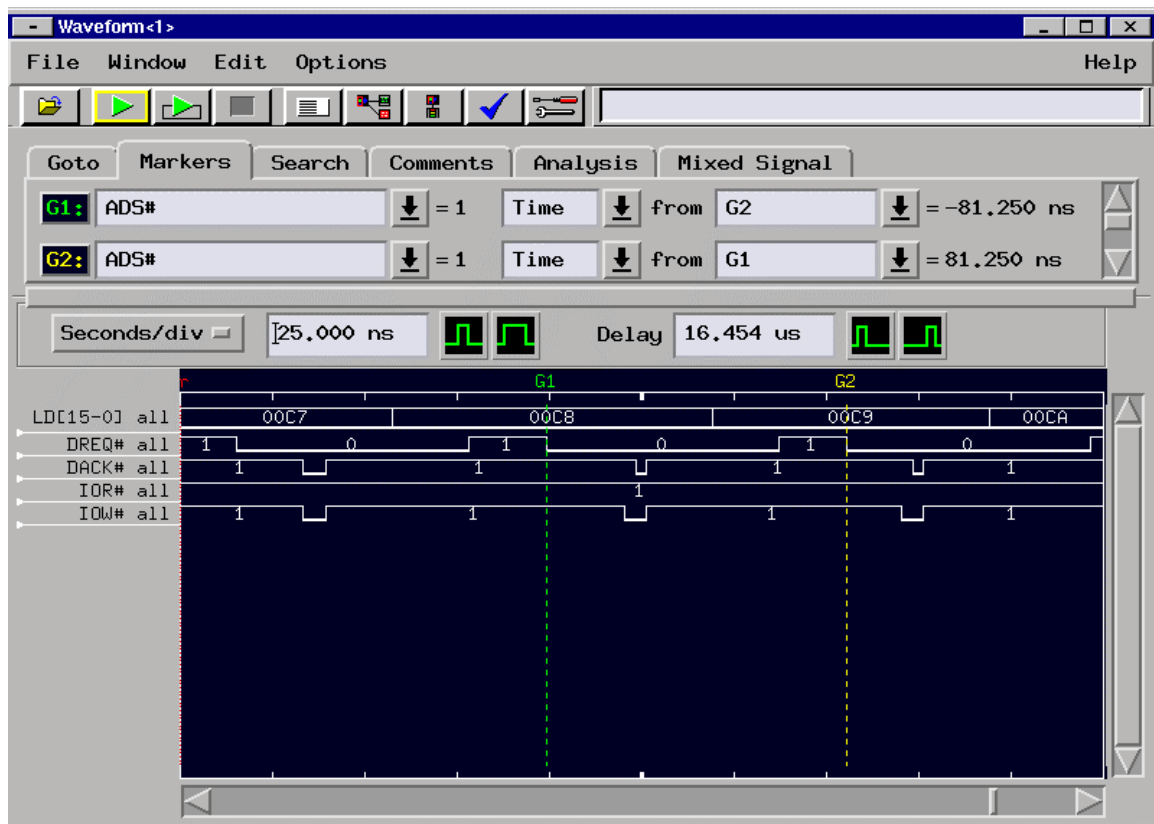


Figure 1.1.1 DMA write (IN transfer) in Slow Mode

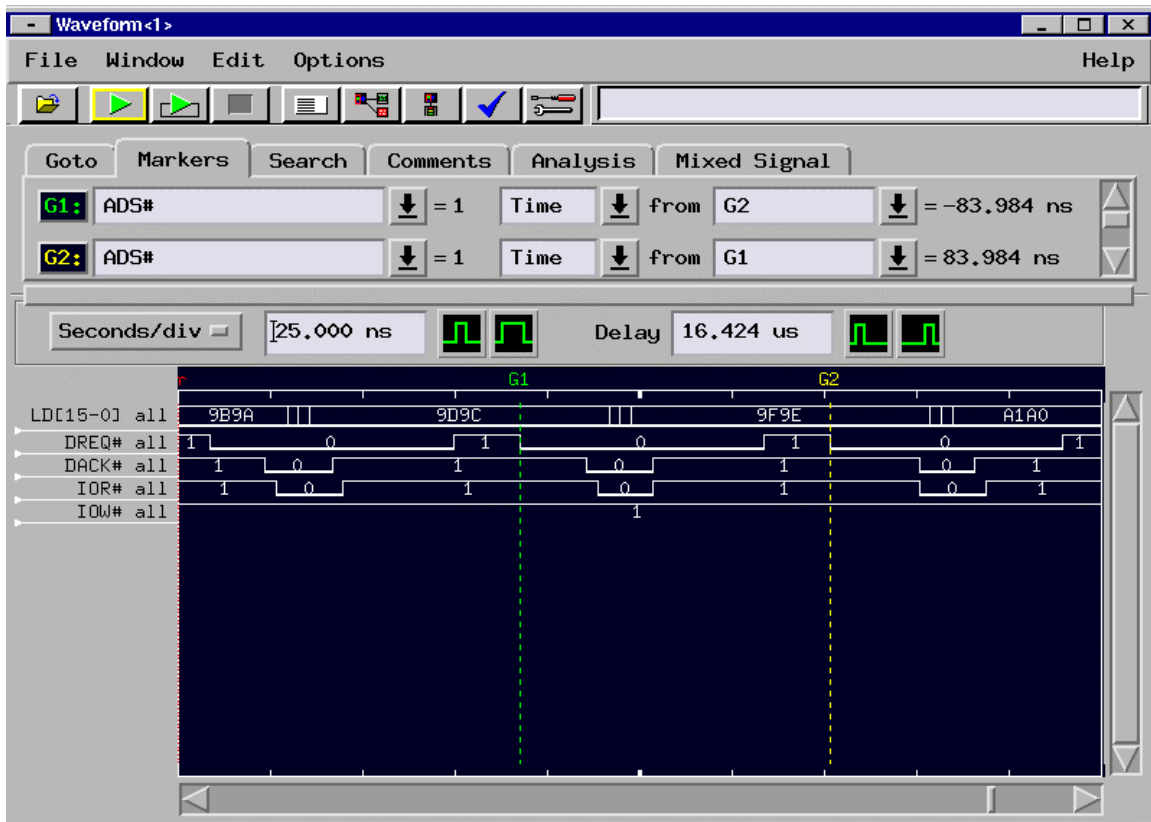


Figure 1.1.2 DMA read (OUT transfer) in Slow Mode

With the cycle period of 81 ns, both DMA write and DMA read transactions in Slow Mode result in  $1 \text{ byte} / 81 \text{ ns} = 12.3 \text{ Mbytes/sec}$  transfer rate in 8 Bit Bus Mode, and  $2 \text{ bytes} / 81 \text{ ns} = 24.7 \text{ Mbytes/sec}$  transfer rate in 16 Bit Bus Mode.

On the USB side, the IN and OUT transfer rates correspond to the DMA write and DMA read transfer rates, respectively. For 8 Bit Bus Mode, the NET2272 can consistently transmit three 512 byte packets in one microframe for IN transfer (Figure 1.2.1) and can consistently receive three 512 byte packets in one microframe for OUT transfer (Figure 1.2.2). Therefore, the microframe transfer rate for both IN and OUT transfers is  $(3 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 12.29 \text{ Mbytes/sec}$ , which corresponds to the DMA transfer rate of 12.3 Mbytes/sec.

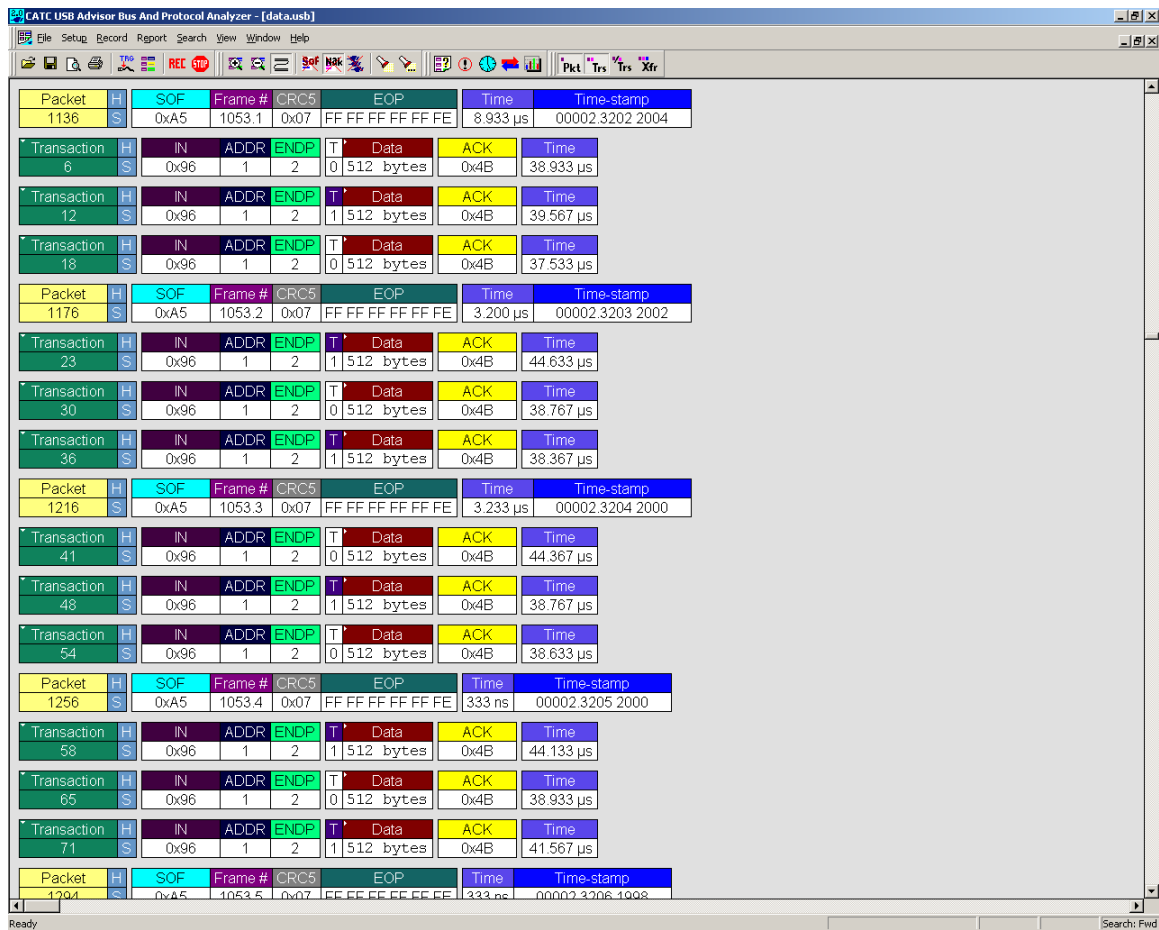


Figure 1.2.1 IN transfer with Slow DMA Mode in 8 Bit Bus Mode

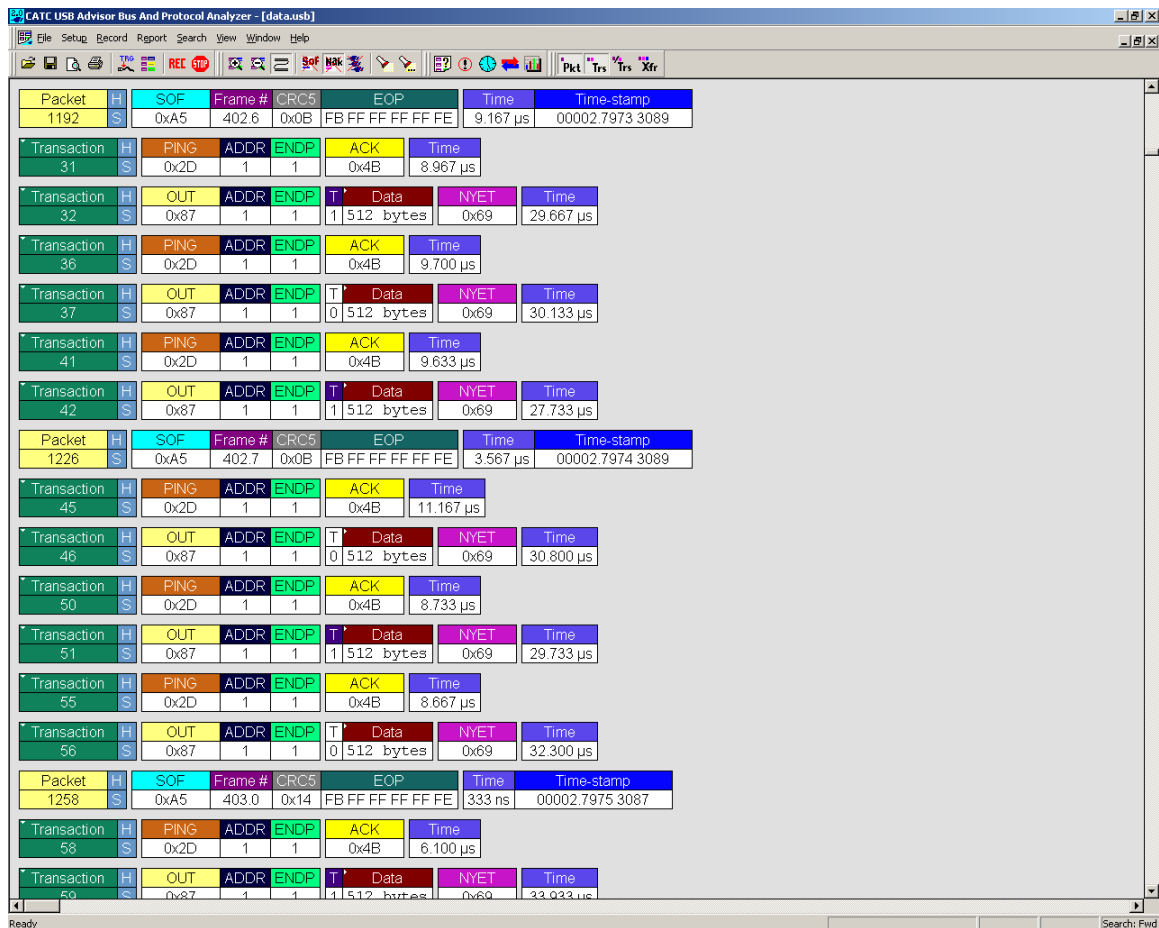


Figure 1.2.2 OUT transfer with Slow DMA Mode in 8 Bit Bus Mode

For 16 Bit Bus Mode, the NET2272 can consistently transmit six 512 byte packets in one microframe for IN transfer (Figure 1.3.1) and can consistently receive six 512 byte packets in one microframe for OUT transfer (Figure 1.3.2). Therefore, the microframe transfer rate for both IN and OUT transfers is  $(6 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 24.57 \text{ Mbytes/sec}$ , which corresponds to the DMA transfer rate of 24.7 Mbytes/sec.

CATC USB Advisor Bus And Protocol Analyzer - [datausb]									
File Setup Record Report Search View Window Help									
Pkt Trs Trs Xfr									
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1150	S	0xA5	1494.2	0x08	FF FF FF FF FE	3.233 µs	00002.0464.4957		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
10	S	0x96	1	2	1	512 bytes	0x4B	23.200 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
13	S	0x96	1	2	0	512 bytes	0x4B	17.100 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
15	S	0x96	1	2	1	512 bytes	0x4B	22.867 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
18	S	0x96	1	2	0	512 bytes	0x4B	22.800 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
21	S	0x96	1	2	1	512 bytes	0x4B	17.267 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
23	S	0x96	1	2	0	512 bytes	0x4B	18.533 µs	
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1187	S	0xA5	1494.3	0x08	FF FF FF FF FE	3.200 µs	00002.0465.4957		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
25	S	0x96	1	2	1	512 bytes	0x4B	22.267 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
28	S	0x96	1	2	0	512 bytes	0x4B	17.267 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
30	S	0x96	1	2	1	512 bytes	0x4B	22.433 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
33	S	0x96	1	2	0	512 bytes	0x4B	22.533 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
36	S	0x96	1	2	1	512 bytes	0x4B	17.300 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
38	S	0x96	1	2	0	512 bytes	0x4B	19.967 µs	
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1224	S	0xA5	1494.4	0x08	FF FF FF FF FE	333 ns	00002.0466.4955		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
39	S	0x96	1	2	1	512 bytes	0x4B	22.567 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
42	S	0x96	1	2	0	512 bytes	0x4B	22.533 µs	

Figure 1.3.1 IN transfer with Slow DMA Mode in 16 Bit Bus Mode



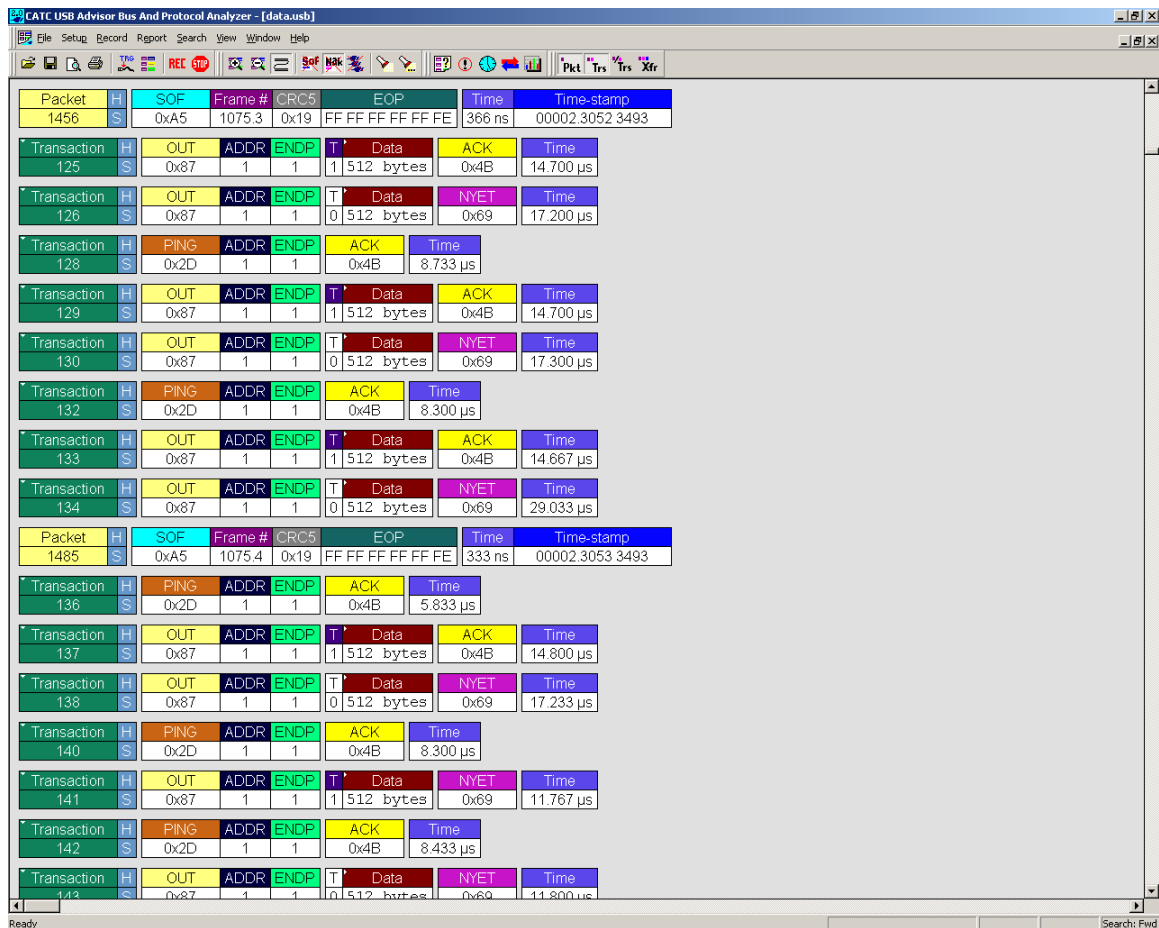


Figure 1.3.2 OUT transfer with Slow DMA Mode in 16 Bit Bus Mode

## 2. Fast DMA Mode

As shown in the timing diagrams below (Figure 2.1.1 and Figure 2.1.2), in Fast DMA mode, the NET2272 de-asserts DREQ typically within 12 ns after DACK is asserted. Then it asserts DREQ again typically within 18 ns after the end of the previous transaction. Table 2.1 summarizes the performance of DMA write and DMA read in Fast Mode.

	DREQ to DACK (ns)	DACK to ~DREQ (ns)	~DREQ to DREQ (ns)	Total (ns)
DMA Write	15 ~ 21	9 ~ 12	18 ~ 21	48
DMA Read	15 ~ 21	9 ~ 12	18 ~ 21	48

Table 2.1 Typical DMA timing for Fast Mode DMA transaction

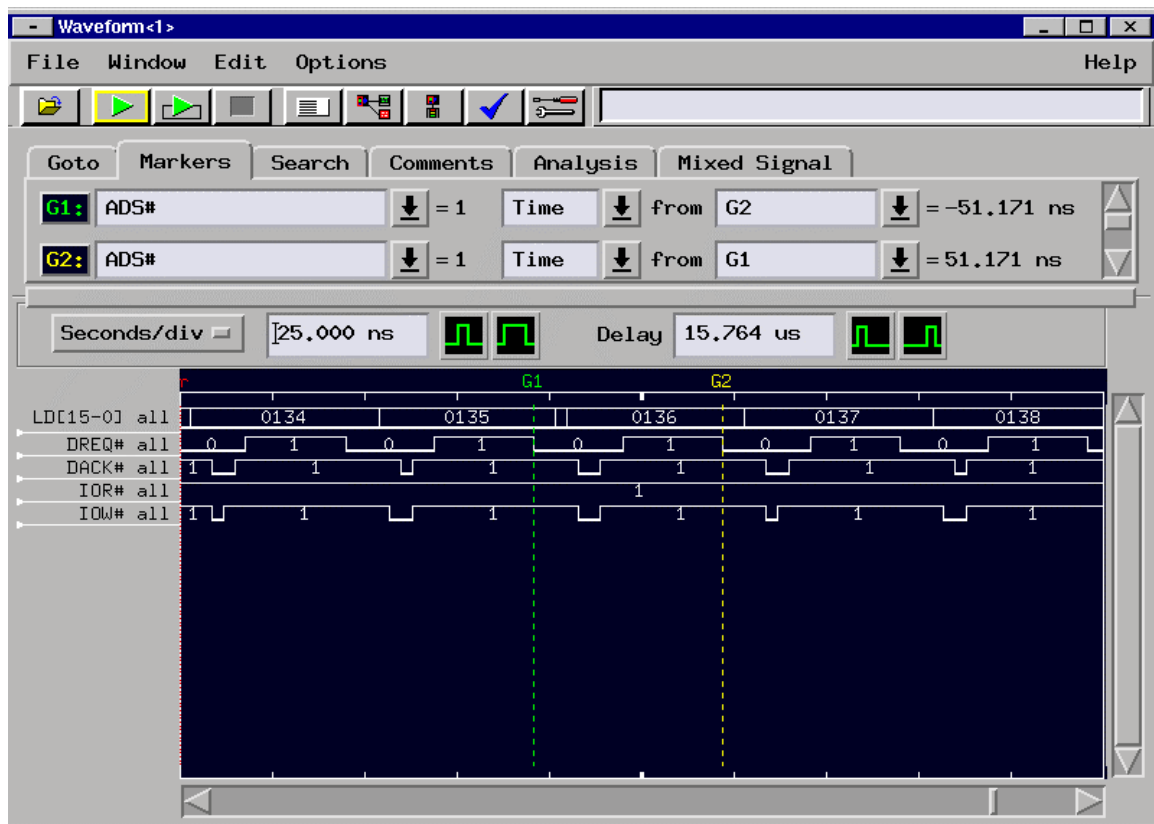


Figure 2.1.1 DMA write (IN transfer) in Fast Mode

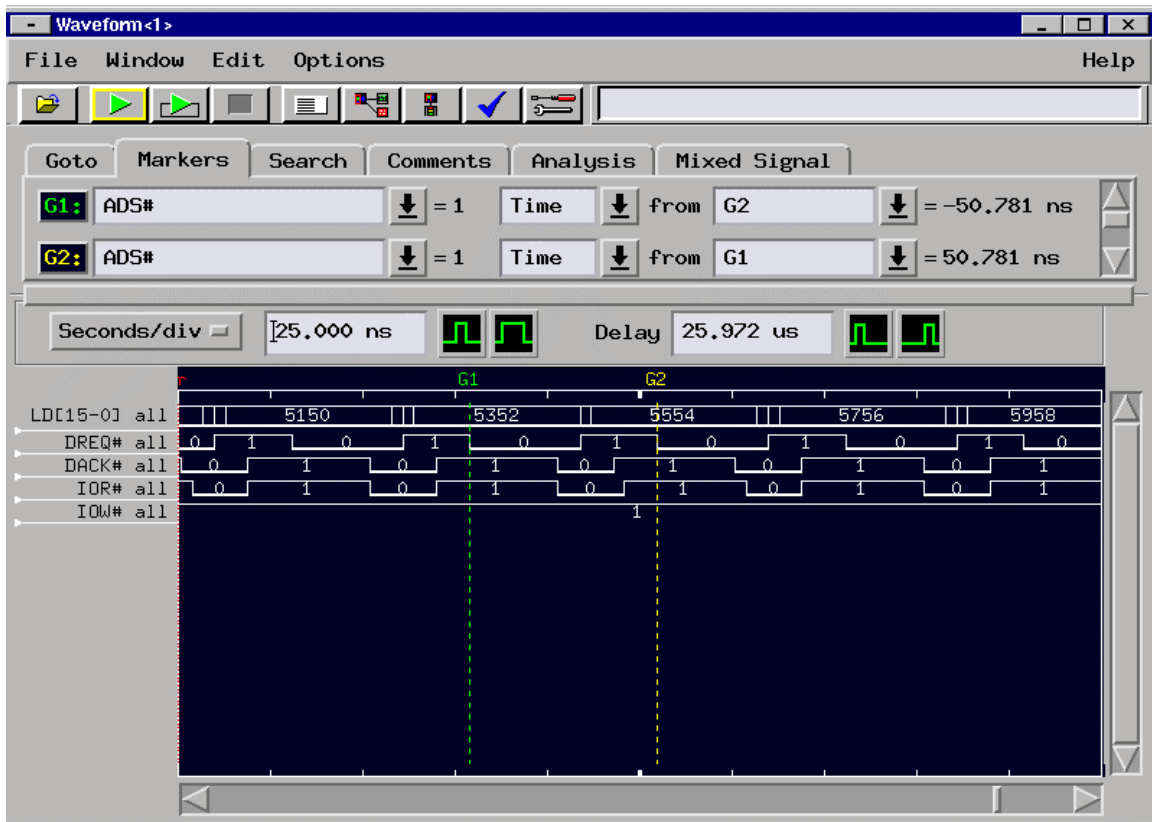


Figure 2.1.2 DMA Read (OUT transfer) in Fast Mode

With the cycle period of 48 ns, both DMA write and DMA read transactions in Fast Mode result in  $1 \text{ byte} / 48 \text{ ns} = 20.83 \text{ Mbytes/sec}$  transfer rate in 8 Bit Bus Mode, and  $2 \text{ bytes} / 48 \text{ ns} = 41.67 \text{ Mbytes/sec}$  transfer rate in 16 Bit Bus Mode.

On the USB side, the IN and OUT transfer rates correspond to the DMA write and DMA read transfer rates, respectively. For 8 Bit Bus Mode, the NET2272 can consistently transmit five 512 byte packets in one microframe for IN transfer (Figure 2.2.1) and can consistently receive five 512 byte packets in one microframe for OUT transfer (Figure 2.2.2). Therefore, the microframe transfer rate for both IN and OUT transfers is  $(5 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 20.48 \text{ Mbytes/sec}$ , which corresponds to the DMA transfer rate of 20.83 Mbytes/sec.

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Pkt Trs Trs Xfr									
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1159	S	0xA5	1186.0	0x0C	FF FF FF FF FF FE	333 ns	00002.0034 2466		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
13	S	0x96	1	2	1	512 bytes	0x4B	17.000 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
15	S	0x96	1	2	0	512 bytes	0x4B	22.600 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
18	S	0x96	1	2	1	512 bytes	0x4B	28.000 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
22	S	0x96	1	2	0	512 bytes	0x4B	27.800 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
26	S	0x96	1	2	1	512 bytes	0x4B	29.233 µs	
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1195	S	0xA5	1186.1	0x0C	FF FF FF FF FF FE	333 ns	00002.0035 2464		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
28	S	0x96	1	2	0	512 bytes	0x4B	22.400 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
31	S	0x96	1	2	1	512 bytes	0x4B	22.300 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
34	S	0x96	1	2	0	512 bytes	0x4B	27.767 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
38	S	0x96	1	2	1	512 bytes	0x4B	27.833 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
42	S	0x96	1	2	0	512 bytes	0x4B	24.367 µs	
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1231	S	0xA5	1186.2	0x0C	FF FF FF FF FF FE	333 ns	00002.0036 2464		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
43	S	0x96	1	2	1	512 bytes	0x4B	22.400 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
46	S	0x96	1	2	0	512 bytes	0x4B	28.200 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
50	S	0x96	1	2	1	512 bytes	0x4B	27.800 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
54	S	0x96	1	2	0	512 bytes	0x4B	22.233 µs	

Figure 2.2.1 IN transfer with Fast DMA Mode in 8 Bit Bus Mode

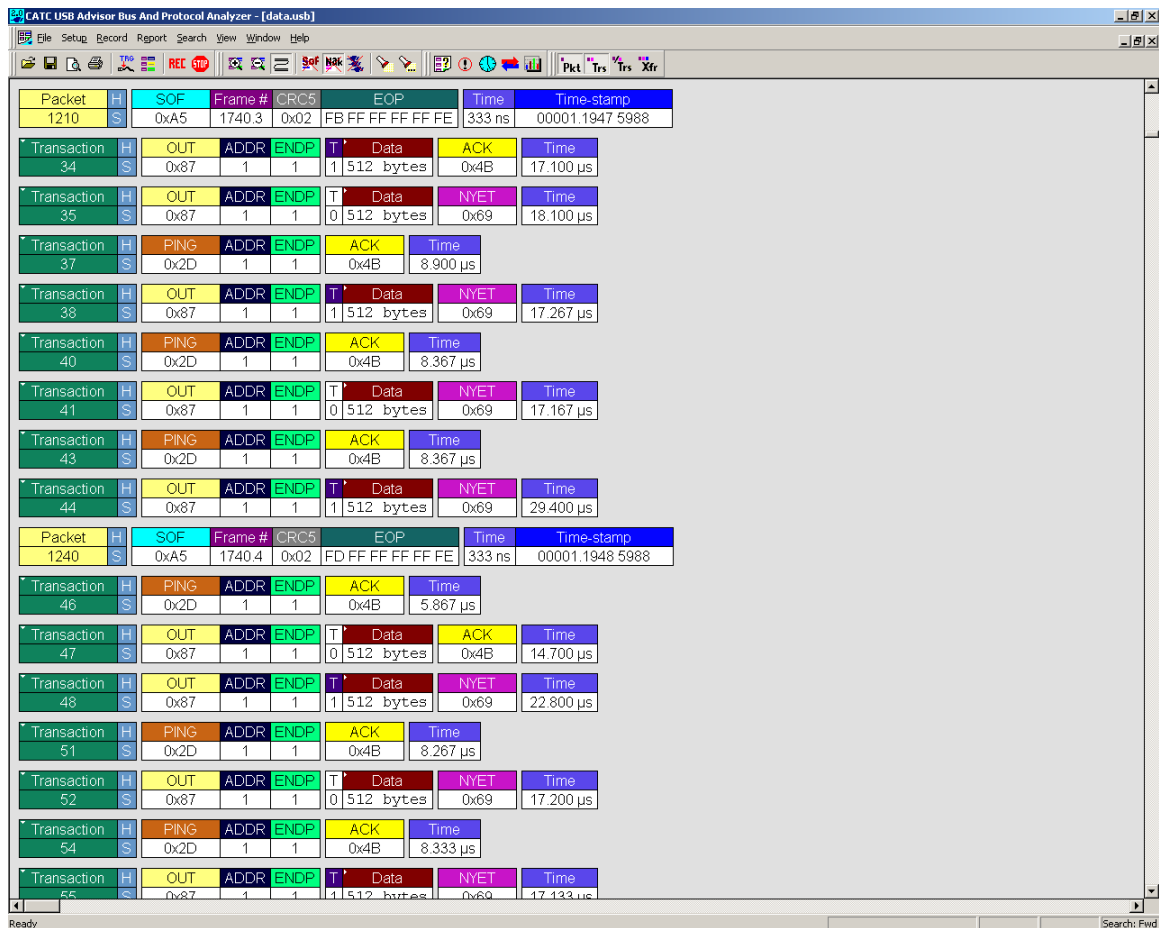


Figure 2.2.2 OUT transfer with Fast DMA Mode in 8 Bit Bus Mode

For 16 Bit Bus Mode, the NET2272 can transmit almost as fast as the maximum bandwidth of the USB host for IN transfer (Figure 2.3.1), and can maximize the bandwidth of the USB host for OUT transfer (Figure 2.3.3). Figure 2.3.2 is the same trace as the IN transfer trace in Figure 2.3.1 but without NAK filter option. As shown in the trace, there are only a couple of NAKs during the IN transfer. The fact that there are only a couple of NAK response indicates that the NET2272 can perform DMA write transactions and transmit the data to the host almost as fast as the USB host can receive. The microframe transfer rate is  $(9 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 36.86 \text{ Mbytes/sec}$ . As the OUT transfer trace in Figure 2.3.3 shows, the NET2272 can consistently receive eight 512 byte packets in one microframe without any NYET or NAK. This indicates that the NET2272 maximizes the USB bandwidth that the host can support. The microframe transfer rate is  $(8 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 32.77 \text{ Mbytes/sec}$  for OUT transfer, which is less than the DMA read transfer rate of 41.67 Mbytes/sec. Considering that the DMA read transfer rate is faster than the OUT transfer rate, the NET2272 would accept more OUT data without NAK if the host could transmit more OUT data.

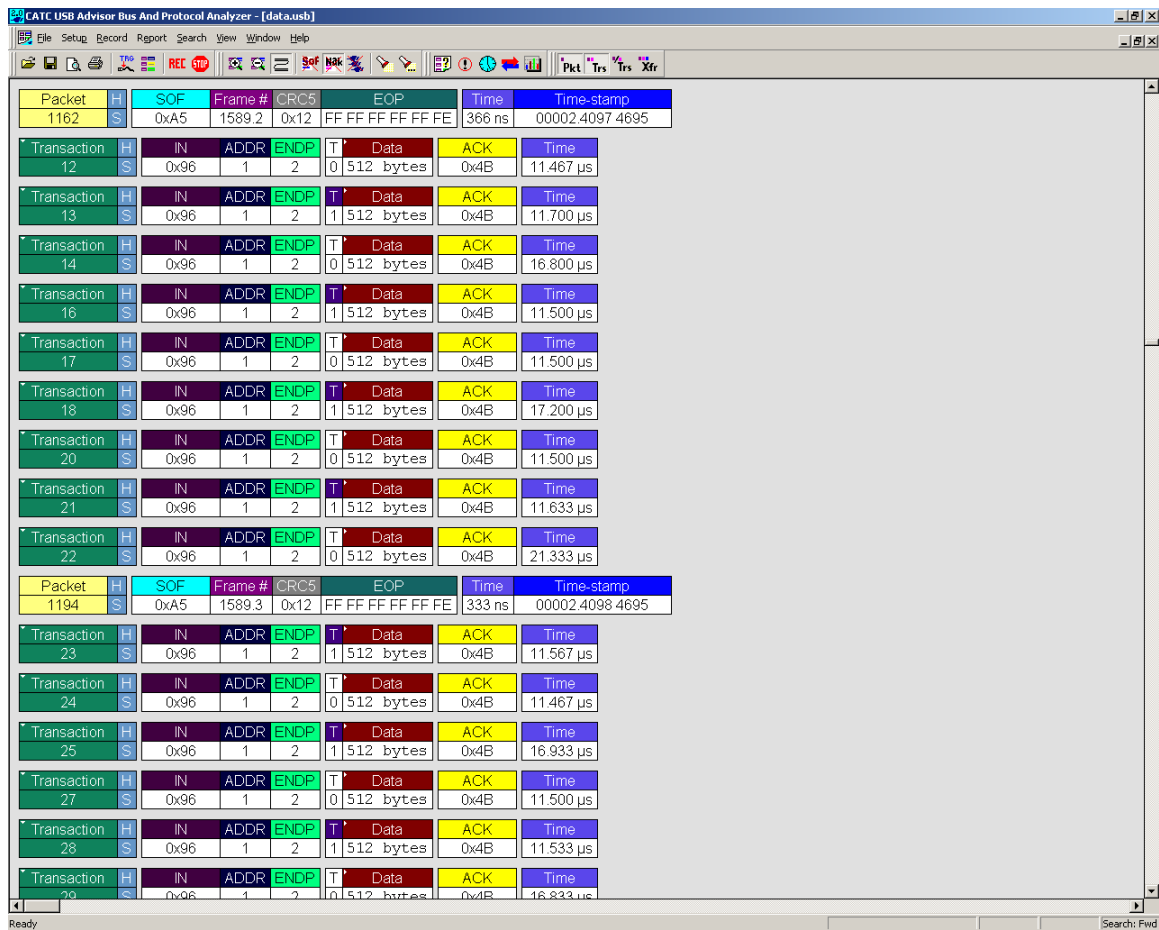


Figure 2.3.1 IN transfer with Fast DMA Mode in 16 Bit Bus Mode

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Pkt Trs Trs Xfr									
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1162	S	0xA5	1589.2	0x12	FF FF FF FF FE	366 ns	00002.4097 4695		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
12	S	0x96	1	2	0	512 bytes	0x4B	11.467 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
13	S	0x96	1	2	1	512 bytes	0x4B	11.700 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
14	S	0x96	1	2	0	512 bytes	0x4B	11.467 µs	
Transaction	H	IN	ADDR	ENDP	T	NAK	Time		
15	S	0x96	1	2	0x5A	5.333 µs			
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
16	S	0x96	1	2	1	512 bytes	0x4B	11.500 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
17	S	0x96	1	2	0	512 bytes	0x4B	11.500 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
18	S	0x96	1	2	1	512 bytes	0x4B	11.733 µs	
Transaction	H	IN	ADDR	ENDP	T	NAK	Time		
19	S	0x96	1	2	0x5A	5.467 µs			
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
20	S	0x96	1	2	0	512 bytes	0x4B	11.500 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
21	S	0x96	1	2	1	512 bytes	0x4B	11.633 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
22	S	0x96	1	2	0	512 bytes	0x4B	21.333 µs	
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1194	S	0xA5	1589.3	0x12	FF FF FF FF FE	333 ns	00002.4098 4695		
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
23	S	0x96	1	2	1	512 bytes	0x4B	11.567 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
24	S	0x96	1	2	0	512 bytes	0x4B	11.467 µs	
Transaction	H	IN	ADDR	ENDP	T	Data	ACK	Time	
25	S	0x96	1	2	1	512 bytes	0x4B	11.567 µs	
Transaction	H	IN	ADDR	ENDP	T	NAK	Time		
26	S	0x96	1	2	0x5A	5.367 µs			

Figure 2.3.2 IN transfer with Fast DMA Mode in 16 Bit Bus Mode (without NAK filter option)

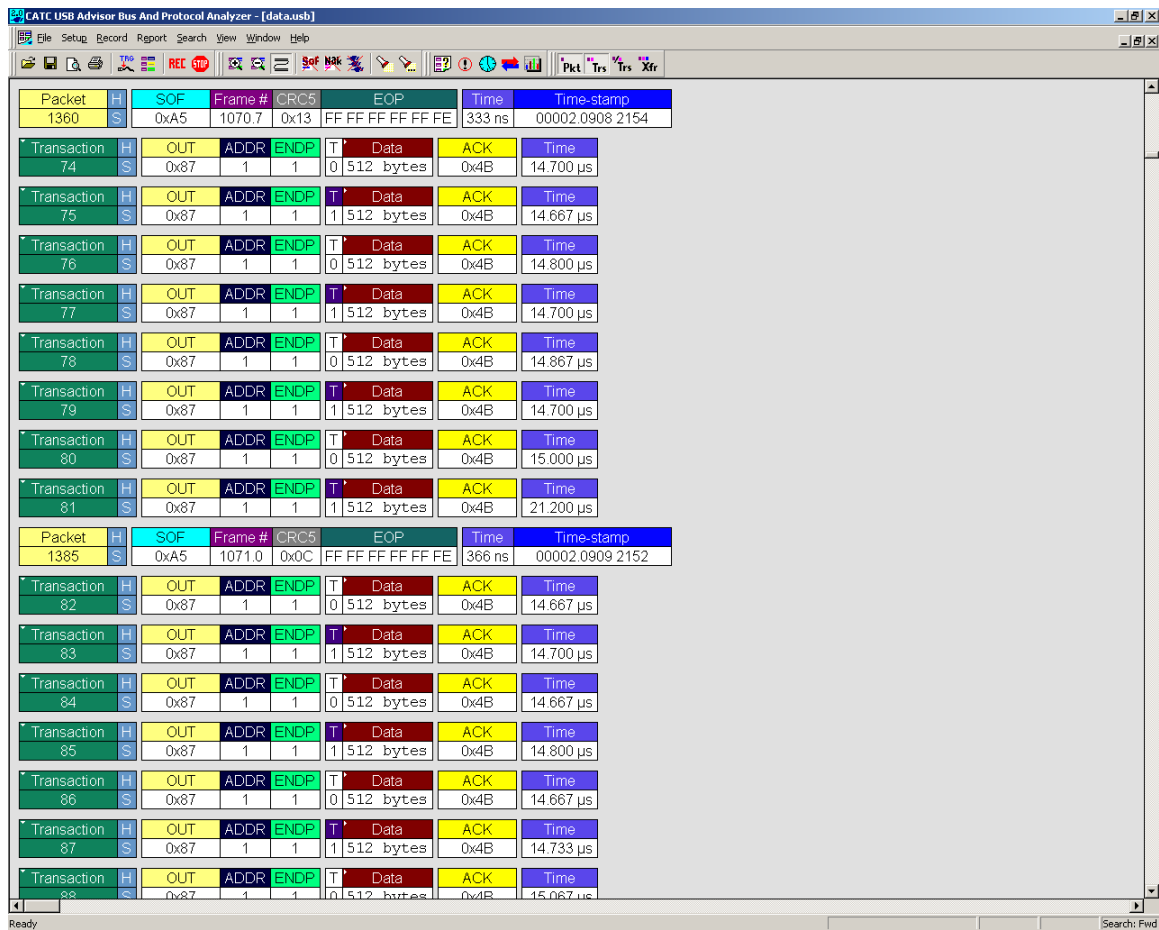


Figure 2.3.3 OUT transfer with Fast DMA Mode in 16 Bit Bus Mode (without NAK filter option)

### 3. Burst DMA Mode

As shown in the timing diagrams below (Figure 3.1.1 and Figure 3.1.2), in Burst DMA mode, the NET2272 keeps DREQ asserted until the end of the transaction. Table 3.1 summarizes the performance of DMA write and DMA read in Burst Mode.

	DACK width (ns)	~DACK to DACK (ns)	Total (ns)
DMA Write	6.25	30 ~ 33	37
DMA Read	18.25	21 ~ 24	40

Table 3.1 Typical DMA timing for Burst Mode DMA transaction



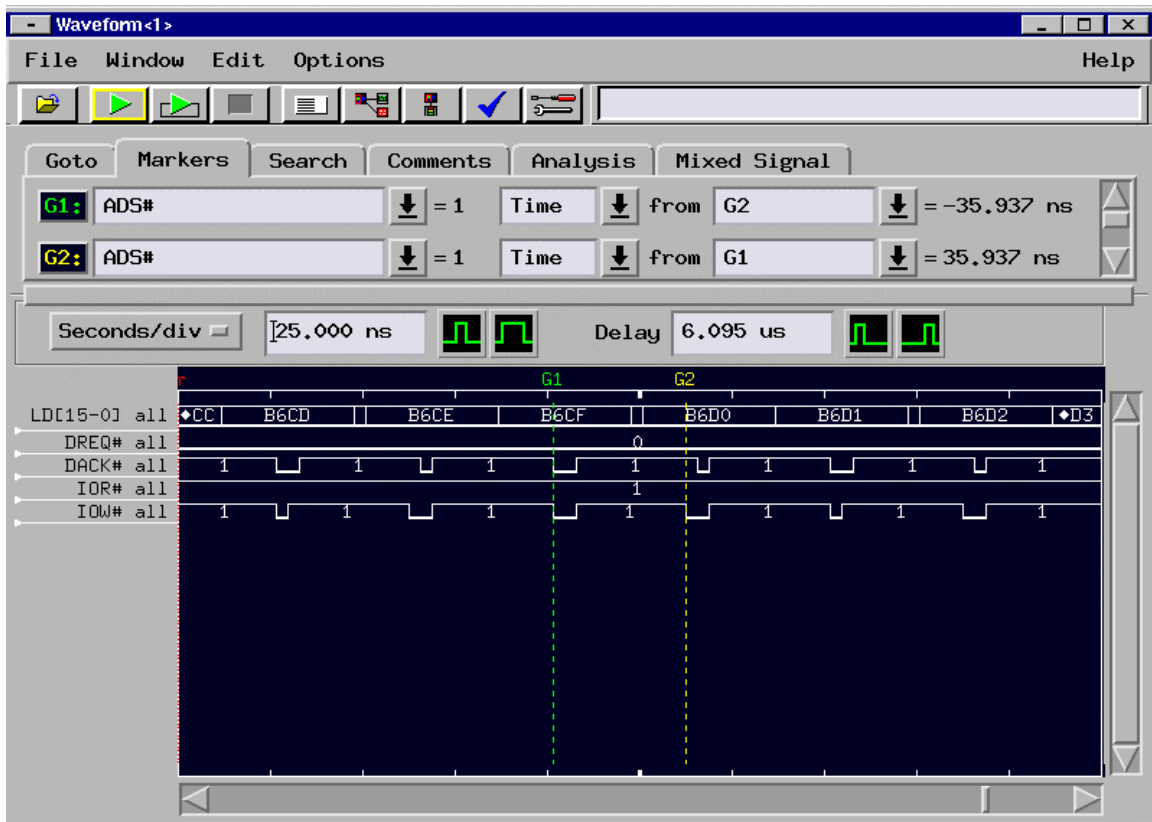


Figure 3.1.1 DMA write (IN transfer) in Burst Mode

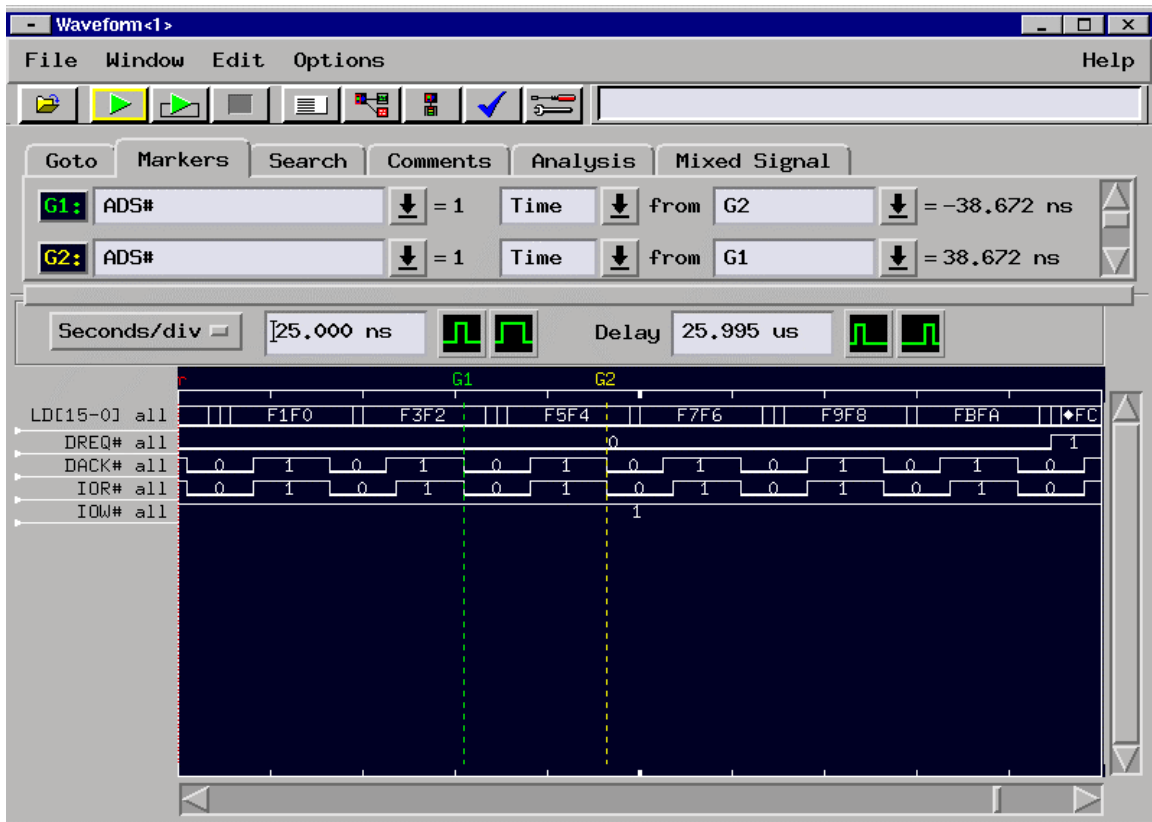


Figure 3.1.2 DMA read (OUT transfer) in Burst Mode

With the cycle period of 37 ns, DMA write transaction in Burst Mode results in  $1 \text{ byte} / 37 \text{ ns} = 27.03 \text{ Mbytes/sec}$  transfer rate in 8 Bit Bus Mode, and  $2 \text{ bytes} / 37 \text{ ns} = 54.05 \text{ Mbytes/sec}$  transfer rate in 16 Bit Bus Mode. For DMA read transaction in Burst Mode, with the cycle period of 40 ns, results in  $1 \text{ byte} / 40 \text{ ns} = 25.00 \text{ Mbytes/sec}$  transfer rate in 8 Bit Bus Mode, and  $2 \text{ bytes} / 40 \text{ ns} = 50.00 \text{ Mbytes/sec}$  transfer rate in 16 Bit Bus Mode.

On the USB side, the IN and OUT transfer rates correspond to the DMA write and DMA read transfer rates, respectively. For 8 Bit Bus Mode, the NET2272 can transmit an average of six and a half 512 byte packets in one microframe for IN transfer (Figure 3.2.1), and can consistently receive six 512 byte packets in one microframe for OUT transfer (Figure 3.2.2). The microframe transfer rate for IN transfer is  $(6.5 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 26.62 \text{ Mbytes/sec}$ , which corresponds to the DMA write transfer rate of 27.03 Mbytes/sec. For OUT transfer, the microframe transfer rate is  $(6 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 24.58 \text{ Mbytes/sec}$ , which corresponds to the DMA read transfer rate of 25.00 Mbytes/sec.

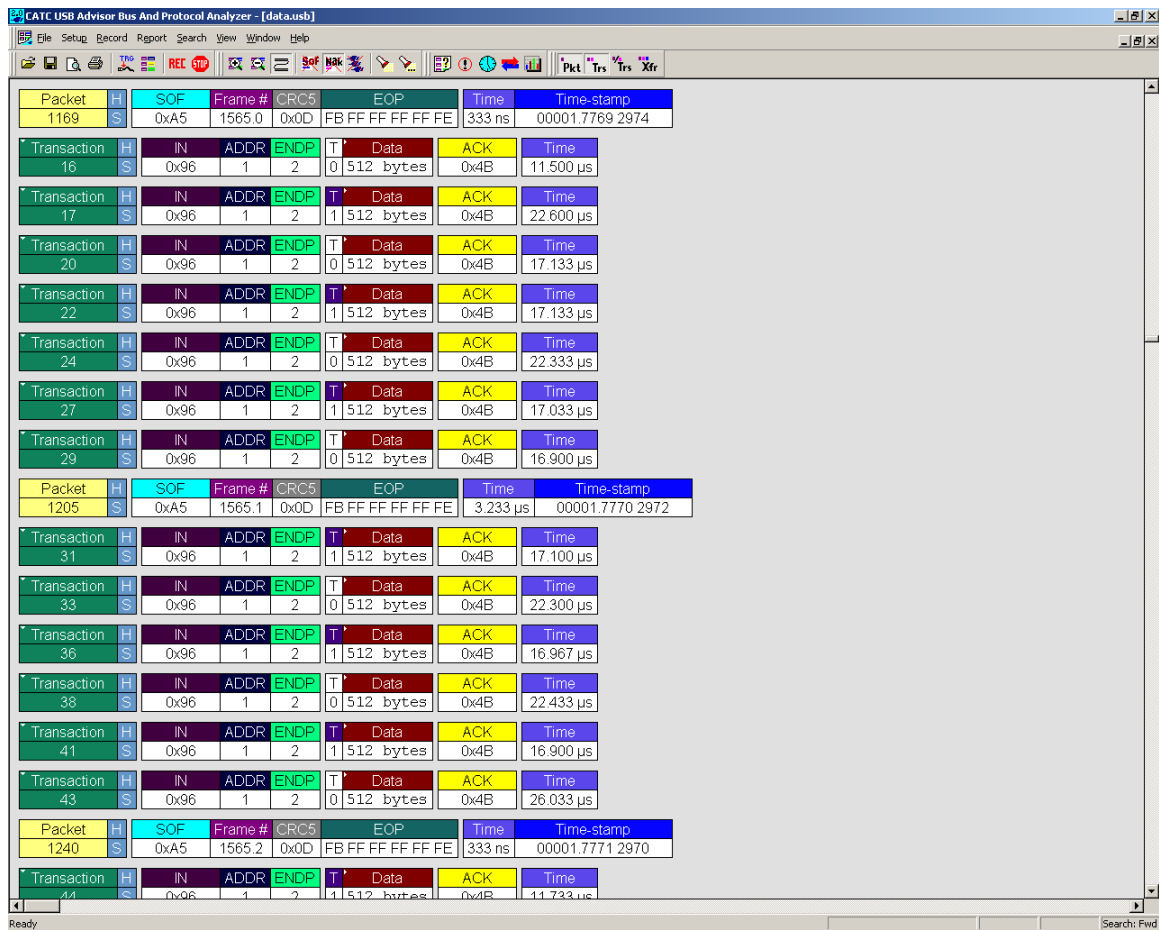


Figure 3.2.1 IN transfer with Burst DMA Mode in 8 Bit Bus Mode

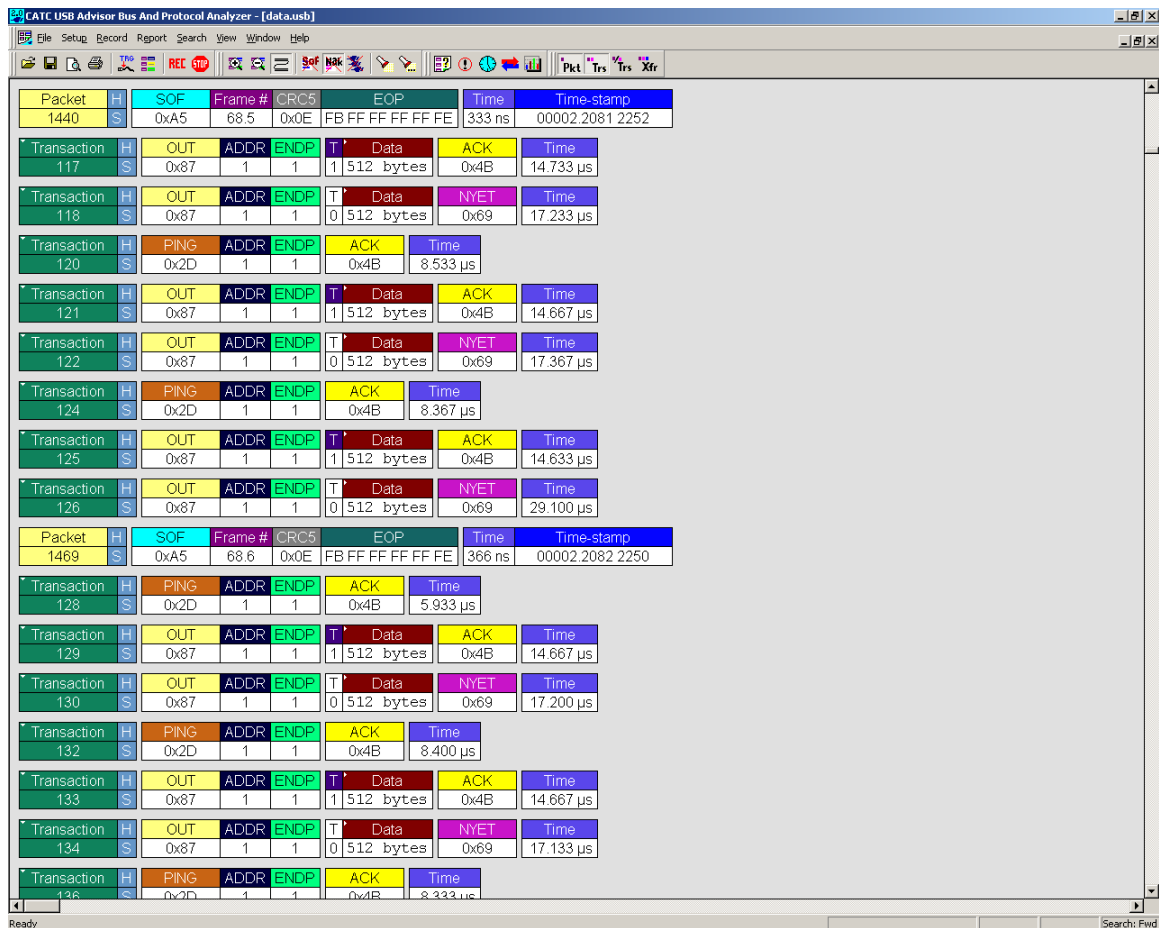


Figure 3.2.2 OUT transfer with Burst DMA Mode in 8 Bit Bus Mode

For 16 Bit Bus Mode, the NET2272 can maximize the USB bandwidth of the host for both IN and OUT transfers; there is no NAK response in both IN and OUT transfers (Figure 3.3.1 IN transfer and Figure 3.3.2 OUT transfer). The NET2272 can consistently transmit ten 512 byte packets in one microframe for IN transfer, which results in the microframe transfer rate of  $(10 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 40.96 \text{ Mbytes/sec}$ , and can consistently receive eight 512 byte packets in one microframe for OUT transfer, which results in the microframe transfer rate of  $(8 \text{ packets} * 512 \text{ bytes}) / 0.125 \text{ us} = 32.77 \text{ Mbytes/sec}$ .

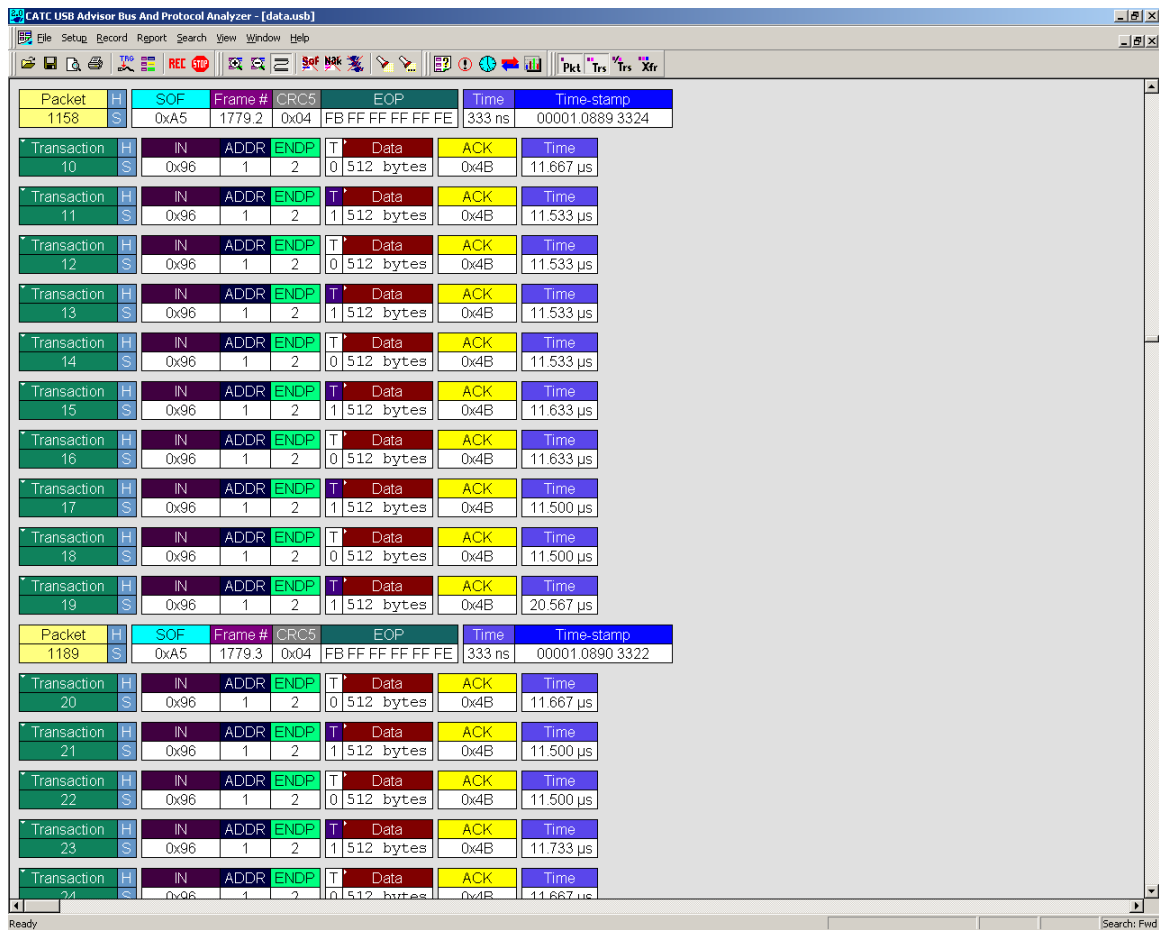


Figure 3.3.1 IN transfer with Burst DMA Mode in 16 Bit Bus Mode (without NAK filter option)

CATC USB Advisor Bus And Protocol Analyzer - [datausb]									
File Setup Record Report Search View Window Help									
Pkt Trs Trs Xfr									
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1173	S	0xA5	1612.0	0x0F	FB FF FF FF FE	333 ns	00004.0477 0327		
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
15	S	0x87	1	1	1	512 bytes	0x4B	14.733 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
16	S	0x87	1	1	0	512 bytes	0x4B	14.733 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
17	S	0x87	1	1	1	512 bytes	0x4B	14.733 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
18	S	0x87	1	1	0	512 bytes	0x4B	14.800 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
19	S	0x87	1	1	1	512 bytes	0x4B	14.800 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
20	S	0x87	1	1	0	512 bytes	0x4B	14.767 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
21	S	0x87	1	1	1	512 bytes	0x4B	14.667 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
22	S	0x87	1	1	0	512 bytes	0x4B	21.400 µs	
Packet	H	SOF	Frame #	CRC5	EOP	Time	Time-stamp		
1198	S	0xA5	1612.1	0x0F	FB FF FF FF FE	333 ns	00004.0478 0325		
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
23	S	0x87	1	1	1	512 bytes	0x4B	14.700 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
24	S	0x87	1	1	0	512 bytes	0x4B	14.833 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
25	S	0x87	1	1	1	512 bytes	0x4B	14.833 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
26	S	0x87	1	1	0	512 bytes	0x4B	14.733 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
27	S	0x87	1	1	1	512 bytes	0x4B	14.667 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
28	S	0x87	1	1	0	512 bytes	0x4B	14.667 µs	
Transaction	H	OUT	ADDR	ENDP	T	Data	ACK	Time	
29	S	0x87	1	1	1	512 bytes	0x4B	14.833 µs	

Figure 3.3.2 OUT transfer with Burst DMA Mode in 16 Bit Bus Mode (without NAK filter option)