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NET2272 USB 2.0 Interface Controller: DMA Transfer Performance Report



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<u>Purpose</u>

This document outlines and analyzes USB bandwidth measurement tests of the NET2272 with DMA transfer and their results.

Test Setup

USB Device

- NET2272 PCI-RDK
- Generic 80MHz EPLD DMA Controller

The <u>NET2272 PCI-RDK</u> is a PCI based development board for the NET2272. When plugged into a PC, the NET2272 PCI-RDK turns the PC into a USB Device.

For the NET2272 local bus interface, the NET2272 PCI-RDK uses an Altera EPLD part. The EPLD runs at 80 MHz and is programmed to perform DMA transactions as well as I/O transactions. DMA request from the NET2272 can be serviced by a simple DMA state machine in the EPLD, or can be passed to the PCI bus on the NET2272 PCI-RDK board. For this test, the simple DMA state machine is used to service DMA request from the NET2272.

USB Host Machine

- Pentium 4, 2.0 GHz
- 512 MB RAM
- Chipset containing Intel® 82801DB I/O Controller Hub 4 (ICH4)
- Microsoft Windows XP

The ICH4 is the USB host controller in our host PC and is one of the fastest USB 2.0 host controllers currently available.

WinMon, NetChip's USB host debug user application, is used to initiate transfers. The host PC loads NcBulk, NetChip's general purpose USB client driver, when the NET2272 PCI-RDK is plugged into the host controller and enumerates.

Test Measurement

Local Bus

- Agilent 16702B Logic Analysis System
- 3ns sample period

For each DMA mode of the NET2272, DMA transaction timing is measured by the Agilent logic analyzer, with sample period of 3 ns.

USB Bus

■ CATC AdvisorTM USB 2.0 Bus & Protocol Analyzer

In order to measure the USB transfer rate of the NET2272, the CATC USB analyzer is used. The microframe transfer rate^{*} is calculated by counting the number of

bytes transferred in one USB microframe and divide the number of bytes by the microframe period.

The microframe transfer rate, however, cannot be sustained by the host controller. WinMon can only initiate transfers of a finite size. When one transfer completes, the OS must make a context switch back to WinMon so that another transfer can be re-submitted. This results in approximately a 2 Megabyte/second penalty resulting in a sustained transfer rate^{**}.

Results

Bus Mode	DMA Mode	Sample Period	IN Transfer Rate (MB/sec)	OUT Transfer Rate (MB/sec)
Widde	Widde	uFrame*	12.29	12.29
	Slow			
		Sustained**	10.29	10.29
8 Bit	Fast	uFrame	20.48	20.48
o Dit	Fast	Sustained	18.48	18.48
	Burst	uFrame	26.62	24.58
		Sustained	24.62	22.58
	Slow	uFrame	24.57	24.57
	SIOW	Sustained	22.57	22.57
16 Bit	Fast	uFrame	36.86	32.77
10 Bit		Sustained	34.86	30.77
	Burst	uFrame	40.96	32.77
		Sustained	38.96	30.77

* microframe transfer rate

** sustained microframe transfer rate

Table 0.1 USB transfer rate

1. Slow DMA Mode

As shown in the timing diagrams below (Figure 1.1.1 and Figure 1.1.2), in Slow DMA mode, the NET2272 de-asserts DREQ typically within 45 ns after DACK is asserted. Then it asserts DREQ again typically within 21 ns after the end of the previous transaction. The Table 1.1 summarizes the performance of DMA write and DMA read in Slow Mode.

	DREQ to DACK (ns)	DACK to ~DREQ (ns)	~DREQ to DREQ (ns)	Total (ns)
DMA Write	15 ~ 21	42 ~ 45	18 ~ 21	81
DMA Read	15 ~ 21	42 ~ 45	18 ~ 21	81

Table 1.1 Typical DMA timing for Slow Mode DMA transaction

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G1: ADS#	↓ = 1 Time ↓ from	G2 ± = -	-81.250 ns
G2: ADS#	1 = 1 Time 1 from	G1 ± = 8	81.250 ns
Seconds/div = [25.000 r	ns 👖 🗖 Delay 16	.454 us	
P	G1	G2	
LD[15-0] all 00007 DREQ# all 1 0			
DACK# all 1			
IOW# all 1	1	1	1
K			

Figure 1.1.1 DMA write (IN transfer) in Slow Mode

File Window Edit Options Hel Hel
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0.05t $1 - 1$ Time 1 from C2 1 - 23 984 pc
G2: ADS#
Seconds/div = [25,000 ns] Delay 16.424 us
G1 G2 LD[15-0] all 9B9A 9D9C 9F9E 1 A1A0 DREQ# all 1 0 1 0 1 0 1 DACK# all 1 0 1 0 1 0 1 IOR# all 1 0 1 0 1 0 1 IOW# all 1 0 1 0 1 0 1

Figure 1.1.2 DMA read (OUT transfer) in Slow Mode

With the cycle period of 81 ns, both DMA write and DMA read transactions in Slow Mode result in 1 byte / 81 ns = 12.3 Mbytes/sec transfer rate in 8 Bit Bus Mode, and 2 bytes / 81 ns = 24.7 Mbytes/sec transfer rate in 16 Bit Bus Mode.

On the USB side, the IN and OUT transfer rates correspond to the DMA write and DMA read transfer rates, respectively. For 8 Bit Bus Mode, the NET2272 can consistently transmit three 512 byte packets in one microframe for IN transfer (Figure 1.2.1) and can consistently receive three 512 byte packets in one microframe for OUT transfer (Figure 1.2.2). Therefore, the microframe transfer rate for both IN and OUT transfers is (3 packets * 512 bytes) / 0.125 us = 12.29 Mbytes/sec, which corresponds to the DMA transfer rate of 12.3 Mbytes/sec.

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Packet H SOF Frame # CRC5 EOP Time Time-stamp	
Factor Soch France France Inne Inne	
Transaction H N ADDR ENDP T Data ACK Time 6 \$ 0x96 1 2 0 512 bytes 0x4B 38.933 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
12 S 0x96 1 2 1 512 bytes 0x4B 39.567 µs	
Transaction H N ADDR ENDP T Data ACK Time 18 \$ 0.96 1 2 0 512 bytes 0x4B 37.533 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp	
1176 S 0xA5 1053.2 0x07 FF FF FF FF FF FE 3.200 µs 00002.3203 2002	
Transaction H IN ADDR ENDP T Data ACK Time 23 S 0x96 1 2 1 512 bytes 0x4B 44.633 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
30 S 0x96 1 2 0 512 bytes 0x4B 38.767 µs Transaction H N ADDR ENDP T Data ACK Time	
36 S 0x96 1 2 1 512 bytes 0x4B 38.367 µs	
Packet H SOF Frame # CRC5 EOP Time - stamp 1216 S 0xA5 1053.3 0x07 FF FF FF FF FF FE 3.233 µs 00002.3204 2000	
Transaction H IN ADDR ENDP T Data ACK Time	
41 S 0x96 1 2 0 512 bytes 0x4B 44.367 µs	
Transaction H IN ADDR ENDP T Data ACK Time 48 S 0x96 1 2 1 512 bytes 0x4B 38:767 µs	
54 S 0x96 1 2 0 512 bytes 0x4B 38.633 µs Packet H SOF Frame # CRC5 EOP Time Time-stamp	
1256 S 0xA5 1053.4 0x07 FF FF FF FF FF FE 333 ns 00002.3205 2000	
Transaction H N ADDR ENDP T Data ACK Time 58 \$ 0x96 1 2 1 512 bytes 0x4B 44.133 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
65 S 0x96 1 2 0 512 bytes 0x4B 38.933 µs	
Transaction H IN ADDR ENDP T Data ACK Time 71 S 0x96 1 2 1 512 bytes 0x4B 41.567 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp	
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Figure 1.2.1 IN transfer with Slow DMA Mode in 8 Bit Bus Mode

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Packet H SOF Frame # CRC5 EOP Time Time-stamp 1192 S 0xA5 402.6 0x0B FB FF FF FF FF FF 9.167 µs 00002.7973 3089 1	
ansaction H PING ADDR ENDP ACK Time	
31 S 0x2D 1 1 0x4B 8.967 µs	
ansaction H OUT ADDR ENDP T Data NYET Time 32 S 0x87 1 1 1 1512 bytes 0x69 29.667 µs	
ansaction H PING ADDR ENDP ACK Time	
36 S 0x2D 1 1 0x4B 9.700 μs	
37 S 0x87 1 1 0 512 bytes 0x69 30.133 µs	
ADDR ENDP ACK Time 41 S 0x2D 1 1 0x4B 9.633 µs	
ansaction H OUT ADDR ENDP T Data NYET Time	
42 S 0x87 1 1 1 512 bytes 0x69 27.733 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp 1226 S 0xA5 402.7 0x0B FB FF FF FF FF FF 3.567 µs 00002.7974 3089	
ansaction H PING ADDR ENDP ACK Time	
45 S 0x2D 1 1 0x4B 11.167 μs	
ansaction H OUT ADDR ENDP T Data NYET Time	
46 S 0x87 1 1 0 512 bytes 0x69 30.800 µs	
ansaction H PING ADDR ENDP ACK Time 50 S 0x2D 1 1 0x4B 8.733 µs	
51 S 0x87 1 1 1 512 bytes 0x69 29.733 µs	
ansaction H PING ADDR ENDP ACK Time 55 S 0x2D 1 1 0x4B 8.667 µs	
ansaction H OUT ADDR ENDP T Data NYET Time	
Size Octor ADDR LNDF 1 Data NTE1 Time 56 S 0x87 1 1 0 512 bytes 0x69 32.300 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp	
1258 S 0xA5 403.0 0x14 FB FF FF FF FE 333 ns 00002.7975 3087	
ansaction H PING ADDR ENDP ACK Time 58 S 0x2D 1 1 0x4B 6.100 µs	
ansaction H OUT ADDR ENDP T Data NYET Time	
50 0 0v87 1 1 1 512 butes 0v60 33.033.us	

Figure 1.2.2 OUT transfer with Slow DMA Mode in 8 Bit Bus Mode

For 16 Bit Bus Mode, the NET2272 can consistently transmit six 512 byte packets in one microframe for IN transfer (Figure 1.3.1) and can consistently receive six 512 byte packets in one microframe for OUT transfer (Figure 1.3.2). Therefore, the microframe transfer rate for both IN and OUT transfers is (6 packets * 512 bytes) / 0.125 us = 24.57 Mbytes/sec, which corresponds to the DMA transfer rate of 24.7 Mbytes/sec.

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Packet H SOF Frame # CRC5 EOP Time Time-stamp 1150 S 0xA5 1494.2 0x08 FF FF FF FF FF FF 3.233 µs 00002.0464 4957	×
Transaction H IN ADDR ENDP T Data ACK Time 10 S 0x96 1 2 1 512 bytes 0x4B 23.200 µs	
Transaction H N ADDR ENDP T Data ACK Time 13 S 0x96 1 2 0 512 bytes 0x4B 17.100 µs Transaction H IN ADDR ENDP T Data ACK Time	
15 0x96 1 2 1 512 bytes 0x4B 22.867 µs Transaction IN ADDR ENDP T Data ACK Time	
18 S 0x96 1 2 0 512 bytes 0x4B 22.800 µs Transaction H N ADDR ENDP T Data ACK Time 21 S 0x96 1 2 1 512 bytes 0x4B 17.267 µs	-
Transaction I N ADDR ENDP T Data ACK Time 23 S 0x96 1 2 0 512 bytes 0x4B 18:533 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp 1187 S 0xA5 1494.3 0x08 FF FF FF FF FF FF 3 200 μs 00002.0465 4957	
Transaction H N ADDR ENDP T Data ACK Time 25 S 0x96 1 2 1 512 bytes 0x4B 22.267 µs	
Transaction H N ADDR ENDP T Data ACK Time 28 S 0x96 1 2 0 512 bytes 0x4B 17.267 µs Transaction H IN ADDR ENDP T Data ACK Time	
30 S 0x96 1 2 1 512 bytes 0x4B 22.433 µs Transaction N ADDR T Data ACK Time 22 0.6 4 2 0.475 0.475 0.475	
33 S 0x96 1 2 0 512 bytes 0x4B 22.533 µs Transaction H N ADDR ENDP T Data ACK Time 36 S 0x96 1 2 1 512 bytes 0x4B 17.300 µs	
Image: Transaction Image: Normal State Sta	
Packet H SOF Frame # CRC5 EOP Time Time-stamp 1224 S 0xA5 1494.4 0x08 FF FF FF FF FE 333 ns 00002.0466 4955	
Transaction H IN ADDR ENDP T Data ACK Time 39 S 0x96 1 2 1 512 bytes 0x4B 22.567 µs Transaction H IN ADDR ENDP T Data ACK Time	
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Figure 1.3.1 IN transfer with Slow DMA Mode in 16 Bit Bus Mode

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Packet H SOF Frame # CRC5 EOP Time Time-stamp 1456 S 0xA5 1075.3 0x19 FF FF FF FF FF FF FF and the stamp 366 ns 00002.3052 3493	
125 S 0x87 1 1 1 512 bytes 0x4B 14.700 µs	
ransaction H OUT ADDR ENDP T Data NYET Time	
126 S 0x87 1 1 0 512 bytes 0x69 17.200 µs	
ransaction H PING ADDR ENDP ACK Time	
128 S 0x2D 1 1 0x4B 8.733 μs	
ransaction H OUT ADDR ENDP T Data ACK Time 129 S 0x87 1 1 1 1512 bytes 0x4B 14.700 µs	
ransaction H OUT ADDR ENDR T' Data NYET Time	
130 S 0x87 1 1 0 512 bytes 0x69 17.300 µs	
ransaction H PING ADDR ENDP ACK Time	
132 S 0x2D 1 1 0x4B 8.300 μs	
ransaction H OUT ADDR ENDP T Data ACK Time	
133 S 0x87 1 1 1 1512 bytes 0x4B 14.667 µs	
ransaction H OUT ADDR ENDP T Data <u>NYET Time</u> 134 S 0x87 1 1 0 512 bytes 0x69 29.033 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp	
1485 S 0xA5 1075.4 0x19 FF FF FF FF FE 333 ns 00002.3053 3493	
ansaction H PING ADDR ENDP ACK Time	
136 S 0x2D 1 1 0x4B 5.833 µs	
ransaction H OUT ADDR ENDP T Data ACK Time	
137 S 0x87 1 1 1 1 512 bytes 0x4B 14.800 µs	
ransaction H OUT ADDR ENDP T Data <u>NYET</u> Time 138 S 0x87 1 1 0 512 bytes 0x69 17,233 µs	
ransaction H PING ADDR ENDP ACK Time	
140 S 0x2D 1 1 0x4B 8.300 µs	
ransaction H OUT ADDR ENDP T' Data NYET Time	
141 S 0x87 1 1 1 512 bytes 0x69 11.767μs	
ransaction H PING ADDR ENDP ACK Time	
142 S 0x2D 1 1 0x4B 8.433 µs	
ransaction H OUT ADDR ENDP T Data NYET Time	
	Search

Figure 1.3.2 OUT transfer with Slow DMA Mode in 16 Bit Bus Mode

2. Fast DMA Mode

As shown in the timing diagrams below (Figure 2.1.1 and Figure 2.1.2), in Fast DMA mode, the NET2272 de-asserts DREQ typically within 12 ns after DACK is asserted. Then it asserts DREQ again typically within 18 ns after the end of the previous transaction. Table 2.1 summarizes the performance of DMA write and DMA read in Fast Mode.

	DREQ to DACK (ns)	DACK to ~DREQ (ns)	~DREQ to DREQ (ns)	Total (ns)
DMA Write	15 ~ 21	9~12	18 ~ 21	48
DMA Read	15 ~ 21	9 ~ 12	18 ~ 21	48

Table 2.1 Typical DMA timing for Fast Mode DMA transaction

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G1: ADS# ± = 1 Time ± fr	rom G2
G2: ADS# ± = 1 Time ± fr	rom G1 = 51.171 ns
Seconds/div = 25,000 ns Delay	15.764 us
IOR# all 1	

Figure 2.1.1 DMA write (IN transfer) in Fast Mode

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File Window Edit Options	Help
Goto Markers Search Comments Analysis Mixed Signal	
G1: ADS# \blacksquare = 1 Time \blacksquare from G2 \blacksquare = -50	.781 ns
G2: ADS# $= 1$ Time $from$ G1 $= 50$.	781 ns 🛛
Seconds/div = [25.000 ns Delay 25.972 us	
LD[15-0] all 5150 5352 5554 5756 DREQ# all 0 1 0 1 0 DACK# all 0 1 0 1 0 IOR# all 0 1 0 1 0 IOW# all 1 0 1 0 1	

Figure 2.1.2 DMA Read (OUT transfer) in Fast Mode

With the cycle period of 48 ns, both DMA write and DMA read transactions in Fast Mode result in 1 byte / 48 ns = 20.83 Mbytes/sec transfer rate in 8 Bit Bus Mode, and 2 bytes / 48 ns = 41.67 Mbytes/sec transfer rate in 16 Bit Bus Mode.

On the USB side, the IN and OUT transfer rates correspond to the DMA write and DMA read transfer rates, respectively. For 8 Bit Bus Mode, the NET2272 can consistently transmit five 512 byte packets in one microframe for IN transfer (Figure 2.2.1) and can consistently receive five 512 byte packets in one microframe for OUT transfer (Figure 2.2.2). Therefore, the microframe transfer rate for both IN and OUT transfers is (5 packets * 512 bytes) / 0.125 us = 20.48 Mbytes/sec, which corresponds to the DMA transfer rate of 20.83 Mbytes/sec.

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Packet H SOF		
1159 S 0xA		
	N ADDR ENDP T Data ACK Time 0x96 1 2 1 512 bytes 0x4B 17.000 µs	
	IN ADDR ENDP T Data ACK Time	
	0x96 1 2 0 512 bytes 0x4B 22.600 µs	
	IN ADDR ENDP T Data ACK Time 0x96 1 2 1 512 bytes 0x4B 28.000 µs	
	0x96 1 2 0 512 bytes 0x4B 27.800 µs	
	IN ADDR ENDP T Data ACK Time 0x96 1 2 1 512 bytes 0x4B 29.233 µs	
Packet H SOF		
Transaction H	KA5 1186.1 0x0C FF FF FF FF FF FE 333 ns 00002.0035 2464	
	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	
	IN ADDR ENDP T Data ACK Time 0x96 1 2 1 512 bytes 0x4B 22.300 µs	
	0x96 1 2 0 512 bytes 0x4B 27.767 µs	
	IN ADDR ENDP T Data ACK Time 0x96 1 2 1 512 bytes 0x4B 27.833 µs	
	IN ADDR ENDP T Data ACK Time	
42 S Ox Packet H SOF	0x96 1 2 0 512 bytes 0x48 24.367 µs 0F Frame # CRC5 EOP Time Time-stamp	
1231 S OXA		
	IN ADDR ENDP T Data ACK Time 0x96 1 2 1 512 bytes 0x4B 22,400 µs	
	0x96 1 2 0 512 bytes 0x4B 28.200 µs	
	IN ADDR ENDP T Data ACK Time 0x96 1 2 1 512 bytes 0x4B 27.800 µs	
Transaction H		
	0x96 1 2 10512 butes 0x48 22234s	
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Figure 2.2.1 IN transfer with Fast DMA Mode in 8 Bit Bus Mode

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Packet H SOF Frame # 1210 S 0xA5 1740.3	# CRC5 EOP Time Time-stamp 0x02 FB FF FF FF FF FE 333 ns 00001.1947 5988	
ransaction H OUT ADDR 34 S 0x87 1	T Data ACK Time 1 1 512 bytes 0x4B 17.100 µs	
ransaction H OUT ADDR 35 S 0x87 1	1 0 512 bytes 0x69 18.100 µs	
37 S 0x2D 1	ENDP ACK Time 1 0x4B 8.900 μs	
ransaction H OUT ADDR 38 S 0x87 1 ransaction H PING ADDR	R ENDP T Data NYET Time 1 1 512 bytes 0x69 17.267 μs 2 ENDP ACK Time	
40 S 0x2D 1 ransaction H OUT ADDR	1 0x4B 8.367 µs	
41 S 0x87 1	1 0 512 bytes 0x69 17.167 μs ENDP ACK Time	
	1 0x4B 8.367 μs R ENDP Τ Data NYET Time	
44 S 0x87 1 Packet H SOF Frame # 1240 S 0xA5 1740.4	1 1 512 bytes 0x69 29.400 µs # CRC5 EOP Time Time-stamp 0x02 FD FF FF FF FE 333 ns 00001.1948 5988	
	ENDP ACK Time 1 0x4B 5.867 µs	
ransaction H OUT ADDR 47 S 0x87 1	CENDP T Data ACK Time 1 0 512 bytes 0x4B 14.700 µs	
48 S 0x87 1	Render Time 1 1512 bytes 0x89 22.800 µs	
51 S 0x2D 1	ENDP ACK Time 1 0x4B 8.267 µs	
ransaction H OUT ADDR 52 S 0x87 1 ransaction H PING ADDR	R ENDP T Data NYET Time 1 0 512 bytes 0x69 17.200 μs R ENDP ACK Time	
54 S 0x2D 1 ransaction H OUT ADDR	1 0x4B 8.333 µs	
55 C 0v87 1	1 1 512 hutes 0x60 17 133 lie	

Figure 2.2.2 OUT transfer with Fast DMA Mode in 8 Bit Bus Mode

For 16 Bit Bus Mode, the NET2272 can transmit almost as fast as the maximum bandwidth of the USB host for IN transfer (Figure 2.3.1), and can maximize the bandwidth of the USB host for OUT transfer (Figure 2.3.3). Figure 2.3.2 is the same trace as the IN transfer trace in Figure 2.3.1 but without NAK filter option. As shown in the trace, there are only a couple of NAKs during the IN transfer. The fact that there are only a couple of NAK response indicates that the NET2272 can perform DMA write transactions and transmit the data to the host almost as fast as the USB host can receive. The microframe transfer rate is (9 packets * 512 bytes) / 0.125 us = 36.86 Mbytes/sec.As the OUT transfer trace in Figure 2.3.3 shows, the NET2272 can consistently receive eight 512 byte packets in one microframe without any NYET or NAK. This indicates that the NET2272 maximizes the USB bandwidth that the host can support. The microframe transfer rate is (8 packets * 512 bytes) / 0.125 us = 32.77 Mbytes/sec for OUT transfer, which is less than the DMA read transfer rate of 41.67 Mbytes/sec. Considering that the DMA read transfer rate is faster than the OUT transfer rate, the NET2272 would accept more OUT data without NAK if the host could transmit more OUT data.

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Packet H SOF Frame # CRC5 EOP Time Time-stamp	
1162 S 0xA5 1589.2 0x12 FF FF FF FF FE 366 ns 00002.4097 4695	
Transaction H IN ADDR ENDP T Data ACK Time 12 S 0x96 1 2 0 512 bytes 0x4B 11.467 μs	
13 S 0x96 1 2 [1] 512 bytes 0x4B [11.700 µs] Transaction H IN ADDR ENDP T Data ACK Time	
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Transaction I N ADDR ENDP T Data ACK Time 16 S 0x96 1 2 1 512 bytes 0x4B 11.500 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
17 S 0x96 1 2 0 512 bytes 0x4B 11.500 µs	
Transaction H IN ADDR ENDP T Data ACK Time 18 S 0x96 1 2 1 512 bytes 0x4B 17.200 µs	
Transaction H N ADDR ENDP T Data ACK Time 20 S 0x96 1 2 0 512 bytes 0x4B 11.500 µs	
Transaction H IN ADDR ENDP T' Data ACK Time	
21 S 0x96 1 2 1 512 bytes 0x4B 11.633 µs	
Transaction H IN ADDR ENDP T Data ACK Time 22 S 0x96 1 2 0 512 bytes 0x4B 21.333 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp 1194 S 0xA5 1589.3 0x12 FF FF FF FF FE 333 ns 00002,4098 4695	
23 S 0x96 1 2 1 512 bytes 0x4B 11.567 µs	
Transaction H IN ADDR ENDP T Data ACK Time 24 S 0x96 1 2 0 512 bytes 0x4B 11.467 μs	
Transaction H IN ADDR ENDP T Data ACK Time	
25 S 0x96 1 2 1 512 bytes 0x4B 16.933 µs Transaction H IN ADDR ENDP T Data ACK Time	
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Transaction H N ADDR ENDP T Data ACK Time 28 S 0x96 1 2 1 512 bytes 0x4B 11.533 µs	
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Figure 2.3.1 IN transfer with Fast DMA Mode in 16 Bit Bus Mode

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Packet H SOF Frame # CRC5 EOP Time Time-stamp 1162 S 0xA5 1589.2 0x12 FF FF FF FF FE 366 ns 00002.4097 4695	
12 S 0x96 1 2 0 512 bytes 0x4B 11.467 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
13 S 0x96 1 2 1 512 bytes 0x4B 11.700 µs	
Transaction H N ADDR ENDP T Data ACK Time 14 S 0x96 1 2 0 512 bytes 0x4B 11.467 μs	
Transaction H IN ADDR ENDP NAK Time	
15 S 0x96 1 2 0x5A 5.333 µs	
Transaction H N ADDR ENDP T Data ACK Time 16 S 0x96 1 2 1 512 bytes 0x4B 11.500 µs	
17 S 0x96 1 2 0 512 bytes 0x4B 11.500 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
18 S 0x96 1 2 1 512 bytes 0x4B 11.733 µs	
Transaction H IN ADDR ENDP NAK Time 19 S 0x96 1 2 0x5A 5.467 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
20 S 0x96 1 2 0 512 bytes 0x4B 11.500 µs	
Transaction H N ADDR ENDP T Data ACK Time 21 S 0x96 1 2 1 512 bytes 0x4B 11.633 µs	
22 S 0x96 1 2 0 512 bytes 0x4B 21.333 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp	
1194 S 0xA5 1589.3 0x12 FF FF FF FF FE 333 ns 00002.4098 4695	
Transaction H N ADDR ENDP T Data ACK Time 23 S 0x96 1 2 1 512 bytes 0x4B 11.567 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
24 S 0x96 1 2 0 512 bytes 0x4B 11.467 µs	
Transaction H N ADDR ENDP T Data ACK Time 25 S 0x96 1 2 1 512 bytes 0x4B 11.567 μs	
Transaction H N ADDR ENDP NAK Time	
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Figure 2.3.2 IN transfer with Fast DMA Mode in 16 Bit Bus Mode (without NAK filter option)

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Packet H 1360 S	SOF Frame # CRC5 EOP Time Time-stamp 0xA5 1070.7 0x13 FF FF FF FF FF FF 333 ns 00002.0908 2154	
ansaction H 74 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 0 512 bytes 0x4B 14.700 µs	
nsaction H 75 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 1512 bytes 0x4B 14.667 µs	
nsaction H 76 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 0 512 bytes 0x4B 14.800 µs	
nsaction H 77 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 512 bytes 0x4B 14.700 µs	
nsaction H 78 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 0 512 bytes 0x4B 14.867 µs	
nsaction H 79 S	OUT ADDR ENDP T.* Data ACK Time 0x87 1 1 512 bytes 0x4B 14.700 μs	
insaction H 80 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 0 512 bytes 0x4B 15.000 µs	
nsaction H 81 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 512 bytes 0x4B 21.200 µs	
acket H 1385 S	SOF Frame # CRC5 EOP Time Time-stamp 0xA5 1071.0 0x0C FF FF FF FF FF FF 366 ns 00002.0909 2152	
nsaction H 82 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 0 512 bytes 0x4B 14.667 µs	
nsaction H 83 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 512 bytes 0x4B 14.700 µs	
nsaction H 84 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 0 512 bytes 0x4B 14.667 µs	
nsaction H 85 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 512 bytes 0x4B 14.800 µs	
nsaction H 86 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 0 512 bytes 0x4B 14.667 µs	
nsaction H 87 S	OUT ADDR ENDP T Data ACK Time 0x87 1 1 512 bytes 0x4B 14.733 µs	
nsaction H	OUT ADDR ENDP T Data ACK Time	

Figure 2.3.3 OUT transfer with Fast DMA Mode in 16 Bit Bus Mode (without NAK filter option)

3. Burst DMA Mode

As shown in the timing diagrams below (Figure 3.1.1 and Figure 3.1.2), in Burst DMA mode, the NET2272 keeps DREQ asserted until the end of the transaction. Table 3.1 summarizes the performance of DMA write and DMA read in Burst Mode.

	DACK width (ns)	~DACK to DACK (ns)	Total (ns)
DMA Write	6.25	30 ~ 33	37
DMA Read	18.25	21 ~ 24	40

Table 3.1 Typical DMA timing for Burst Mode DMA transaction

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G1: ADS#
62: ADS#
Seconds/div = [25,000 ns] Delay 6,095 us
LD[15-0] all CC B6CD B6CE B6CF B6D0 B6D1 B6D2 +D3
DREQ# all 0 DACK# all 1 1 1 1 1 1 1 1 1
IOR# all

Figure 3.1.1 DMA write (IN transfer) in Burst Mode

_ Waveform<1>
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File Window Edit Options Help Help Help
G2: ADS# ▲ = 1 Time ▲ from G1 ▲ = 38.672 ns
Seconds/div = [25.000 ns Delay 25.995 us
LD[15-0] all F1F0 F3F2 F5F4 F7F6 F9F8 FBFA • FC 1 DREQ# all 0 1 DACK# all 1 1 0 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0

Figure 3.1.2 DMA read (OUT transfer) in Burst Mode

With the cycle period of 37 ns, DMA write transaction in Burst Mode results in 1 byte / 37 ns = 27.03 Mbytes/sec transfer rate in 8 Bit Bus Mode, and 2 bytes / 37 ns = 54.05 Mbytes/sec transfer rate in 16 Bit Bus Mode. For DMA read transaction in Burst Mode, with the cycle period of 40 ns, results in 1 byte / 40 ns = 25.00 Mbytes/sec transfer rate in 8 Bit Bus Mode, and 2 bytes / 40 ns = 50.00 Mbytes/sec transfer rate in 16 Bit Bus Mode.

On the USB side, the IN and OUT transfer rates correspond to the DMA write and DMA read transfer rates, respectively. For 8 Bit Bus Mode, the NET2272 can transmit an average of six and a half 512 byte packets in one microframe for IN transfer (Figure 3.2.1), and can consistently receive six 512 byte packets in one microframe for OUT transfer (Figure 3.2.2). The microframe transfer rate for IN transfer is (6.5 packets * 512 bytes) / 0.125 us = 26.62 Mbytes/sec, which corresponds to the DMA write transfer rate of 27.03 Mbytes/sec. For OUT transfer, the microframe transfer rate is (6 packets * 512 bytes) / 0.125 us = 24.58 Mbytes/sec, which corresponds to the DMA read transfer rate of 25.00 Mbytes/sec.

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Packet H SOF Frame # CRC5 EOP Time Time-stamp	
1169 S 0xA5 1565.0 0x0D FF FF FF FF S 00001.7769 2974	
Transaction H N ADDR ENDP T Data ACK Time 16 S 0x96 1 2 0 512 bytes 0x4B 11.500 µs	
Transaction H IN ADDR ENDP T' Data ACK Time	
17 S 0x96 1 2 1 512 bytes 0x4B 22.600 µs	
Transaction H IN ADDR ENDP T Data ACK Time 20 S 0x96 1 2 0 512 bytes 0x4B 17.133 µs	
Transaction H IN ADDR ENDP T Data ACK Time	
22 S 0x96 1 2 1 512 bytes 0x4B 17.133 µs Transaction H IN ADDR ENDP T Data ACK Time	
24 S 0x96 1 2 0 512 bytes 0x4B 22.333 µs	
Transaction H N ADDR ENDP T Data ACK Time 27 IS 0x96 1 2 1 512 bytes 0x4B 17.033 µs	
Transaction H N ADDR ENDP T' Data ACK Time	
29 S 0x96 1 2 0 512 bytes 0x4B 16.900 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp 1205 S 0xA5 1565.1 0x0D FB FF FF FF FE 3.233 µs 00001.7770 2972	
Transaction H IN ADDR ENDP T' Data ACK Time	
31 S 0x96 1 2 1 512 bytes 0x4B 17.100 μs Transaction H N ADDR ENDP T Data ACK Time	
33 S 0x96 1 2 0 512 bytes 0x4B 22.300 µs	
Transaction H N ADDR ENDP T Data ACK Time 36 S 0x96 1 2 1 512 bytes 0x4B 16.967 µs	
Transaction H N ADDR ENDP T Data ACK Time	
38 S 0x96 1 2 0 512 bytes 0x4B 22.433 µs	
Transaction H N ADDR ENDP T Data ACK Time 41 S 0x96 1 2 1 512 bytes 0x4B 16.900 µs	
Transaction H IN ADDR ENDP T' Data ACK Time	
43 S 0x96 1 2 0 512 bytes 0x4B 26.033 µs Packet H SOF Frame # CRC5 EOP Time Time Time	
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Transaction H N ADDR ENDP T Data ACK Time	
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Figure 3.2.1 IN transfer with Burst DMA Mode in 8 Bit Bus Mode

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Packet H SOF Frame # CRC5 EOP Time Time-stamp 1440 S 0xA5 68.5 0x0E FB FF FF FF FE 333 ns 00002.2081 2252	
Construction OUT ADDR EDP T Data ACK Time 117 5 0x87 1 1 1512 bytes 0x4B 14.733 µs	
ransaction H OUT ADDR ENDP T Data NYET Time 118 S 0x87 1 1 0 512 bytes 0x69 17.233 µs	
ransaction H PING ADDR ENDP ACK Time 120 S 0x2D 1 1 0x4B 8.533 µs	
ransaction H OUT ADDR ENDP T' Data ACK Time 121 S 0x87 1 1 1 1512 bytes 0x4B 14.667 µs	
ransaction H OUT ADDR ENDP T Data NYET Time 122 S 0x87 1 1 0 512 bytes 0x69 17.367 µs	
ransaction Η PING ADDR ENDP ACK Time 124 S 0x2D 1 1 0x4B 8.367 μs	
ransaction H OUT ADDR ENDP T Data ACK Time 125 S 0x87 1 1 1 1512 bytes 0x4B 14.633 µs	
ransaction H OUT ADDR ENDP T Data NYET Time 126 S 0x87 1 1 0 512 bytes 0x69 29.100 µs	
Packet H SOF Frame # CRC5 EOP Time Time-stamp 1469 S 0xA5 68.6 0x0E FB FF FF FF FE 366 ns 00002.2082.2250	
ransaction H PING ADDR ENDP ACK Time 128 S 0x2D 1 1 0x4B 5.933 µs	
Image: Target action H OUT ADDR ENDP T Data ACK Time 129 S 0x87 1 1 1512 bytes 0x4B 14.667 µs	
ransaction H OUT ADDR ENDP T Data NYET Time 130 S 0x87 1 1 0 512 bytes 0x89 17.200 µs	
ransaction H PING ADDR ENDP ACK Time 132 S 0x2D 1 1 0x4B 8.400 μs ransaction H OUT ADDR ENDP T' Data ACK Time	
ransaction H OUT ADDR ENDP T Data ACK Time 133 S 0x87 1 1 1512 bytes 0x4B 14.667 µs ransaction H OUT ADDR ENDP T Data NYET Time	
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136 C 0/2D 1 1 0/1R 8.333.uc	

Figure 3.2.2 OUT transfer with Burst DMA Mode in 8 Bit Bus Mode

For 16 Bit Bus Mode, the NET2272 can maximize the USB bandwidth of the host for both IN and OUT transfers; there is no NAK response in both IN and OUT transfers (Figure 3.3.1 IN transfer and Figure 3.3.2 OUT transfer). The NET2272 can consistently transmit ten 512 byte packets in one microframe for IN transfer, which results in the microframe transfer rate of (10 packets * 512 bytes) / 0.125 us = 40.96 Mbytes/sec, and can consistently receive eight 512 byte packets in one microframe for OUT transfer, which results in the microframe transfer rate of (8 packets * 512 bytes) / 0.125 us = 32.77 Mbytes/sec.

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Packet H	SOF Frame # CRC			
		FB FF FF FF FF FE 333		
Transaction H 10 S	IN ADDR ENDI 0x96 1 2	T' Data ACk 0 512 bytes 0x4E		
Transaction H	IN ADDR END			
Transaction H	0x96 1 2	1 512 bytes 0x4E		
12 S	0x96 1 2	0 512 bytes 0x4E		
ransaction H	IN ADDR END	T Data ACK		
ransaction H				
14 S	0x96 1 2	0 512 bytes 0x4E		
ransaction H 15 S	IN ADDR END 0x96 1 2	T Data ACk 1 512 bytes 0x4E		
ransaction H	IN ADDR END			
16 S	0x96 1 2	0 512 bytes 0x4E		
17 S	0x96 1 2	1 512 bytes 0x4E		
ransaction H	IN ADDR END	T Data ACK		
ransaction H				
19 S	0x96 1 2	1 512 bytes 0x4E		
	SOF Frame # CRC 0xA5 1779.3 0x04	5 EOP Tir FBFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF		
ransaction H 20 S	IN ADDR END	T Data ACk		
zu S	IN ADDR END			
21 S	0x96 1 2	1 512 bytes 0x4E		
ransaction H 22 S	IN ADDR ENDI 0x96 1 2	P T Data ACK		
ransaction H				
23 S	0x96 1 2	1 512 bytes 0x4E		
ransaction H	IN ADDR END	T Data ACK		

Figure 3.3.1 IN transfer with Burst DMA Mode in 16 Bit Bus Mode (without NAK filter option)

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Packet H	SOF	Frame # CRC5	· 10	Time	Time-stamp	1		
1173 S	0xA5		FB FF FF FF FF FF		00004.0477 0327			
ransaction H	OUT	ADDR ENDP		ACK	Time			
15 S	0x87	1 1	1 512 bytes	0x4B	14.733 µs			
ransaction H 16 S	0UT 0x87	ADDR ENDP	T Data 0 512 bytes	ACK 0x4B	<u>Time</u> 14.733 μs			
ransaction H	OUT	ADDR ENDP		ACK	Time			
17 S	0x87	1 1	1 512 bytes	0x4B	14.733 µs			
ansaction H	TUO			ACK	Time			
	0x87	ADDR ENDP	0 512 bytes	0x4B	14.800 µs			
ansaction H 19 S	OUT 0x87	ADDR ENDP	T Data 1 512 bytes	0x4B	Time 14.800 µs			
ansaction H	OUT		T Data	ACK	Time			
20 S	0x87	1 1	0 512 bytes	0x4B	14.767 µs			
ansaction H	OUT 0x87	ADDR ENDP	T Data 1 512 bytes	ACK 0x4B	Time 14.667 µs			
ansaction H		ADDR ENDP		ACK	Time			
22 S	0x87	1 1	0 512 bytes	0x4B	21.400 µs			
Packet H	SOF	Frame # CRC5		Time	Time-stamp			
1198 S	0xA5		FB FF FF FF FF FF		00004.0478 0325			
ansaction H 23 S	OUT 0x87	ADDR ENDP	T Data 1 512 bytes	ACK 0x4B	Time 14.700 μs			
ansaction H	OUT	ADDR ENDP	T Data	ACK	Time			
24 S	0x87	1 1	0 512 bytes	0x4B	14.833 µs			
ansaction H 25 S	OUT 0x87	ADDR ENDP	T Data 1 512 bytes	ACK 0x4B	Time 14.833 μs			
ansaction H		ADDR ENDP		ACK	Time			
26 S	0x87	1 1	0 512 bytes	0x4B	14.733 µs			
ansaction H	OUT	ADDR ENDP		ACK	Time			
27 S	0x87	1 1	1 512 bytes	0x4B	14.667 µs			
ansaction H 28 S	OUT 0x87	ADDR ENDP	T Data 0 512 bytes	ACK 0x4B	<u>Time</u> 14.667 μs			
ansaction H	OUT	ADDR ENDP		ACK	Time			
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Figure 3.3.2 OUT transfer with Burst DMA Mode in 16 Bit Bus Mode (without NAK filter option)