USER MANUAL

BCM91125E

Evaluation Board

91125E-UM100-R

16215 Alton Parkway • P.O. Box 57013 • Irvine, CA 92619-7013 • Phone: 949-450-8700 • Fax: 949-450-8710

04/27/05

REVISION HISTORY

Revision	*Date*	*Change Description*
91125E-UM100-R	04/27/05	Initial release.

Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, CA 92619-7013

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Section 1: Product Overview

INTRODUCTION

The BCM91125E evaluation board is an evaluation platform for the BCM1125H processor. This user manual provides information on how to get the BCM91125E evaluation board up and running quickly. This manual also describes how to locate, configure, and observe the various connectors, switches, jumpers, and LEDs on the BCM91125E, allowing software development and evaluation of the BCM1125H processor.

PRODUCT OVERVIEW

The BCM91125E is a standard length PCI form factor board which can run in device mode on the PCI bus. It can be used in a standard PCI slot with a PCI host, or stand alone. In stand-alone mode, power is provided using a standard ATX type power supply. The BCM91125E block diagram is shown in Figure 1.

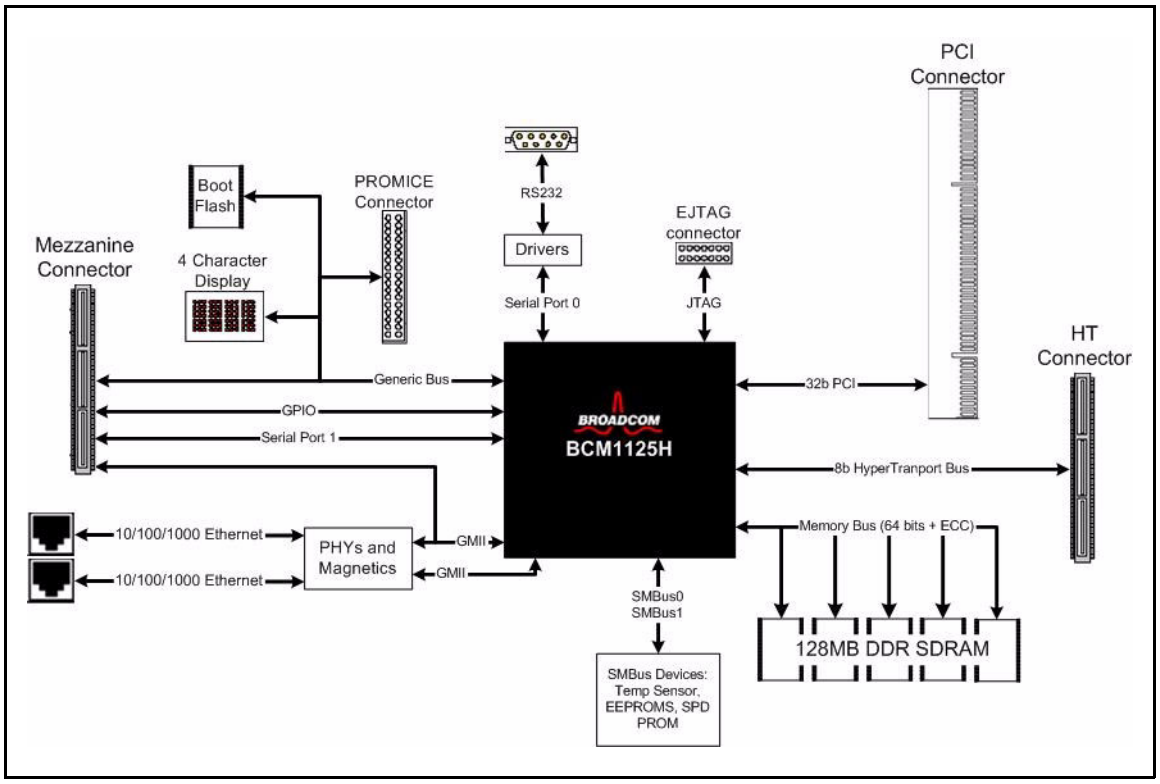

Figure 1: BCM91125E Block Diagram

The board contains 128MB of soldered down SDRAM. Both GMII ports are also brought out to standard connectors on the side of board. It has one 8 bit wide HyperTransport interface which the user can access by means of a standard connector. Another connector provides GPIO, generic bus address and data lines, and an alternate use of one of the GMII ports. Either or both connectors can be used as an interface to a mezzanine

card. The BCM1125H can boot from either an on board flash or a ROM emulator, to assist in code development. Debug features include a 4-character display and an EJTAG port. An RS232 port provides access to one of the BCM1125H UARTs.

For additional information on this board and the BCM1125H processor, go to:
http://sibyte.broadcom.com/public.

ITEMS INCLUDED WITH THE SHIPMENT

The following items are included with the BCM91125E evaluation board shipment:

- BCM91125E evaluation board
- This document

HARDWARE FEATURES

- BCM1125H processor
- Full length PCI card form factor
- 128MB DDR SDRAM
- Two 10/100/1000 Mbps Ethernet interfaces with RJ45 connectors
- One UART with RS232 interface
- Universal 32-bit, 33/66-MHz capable PCI connector
- 16MB Flash ROM
- Two SMBus channels with the following devices connected:
  - RTC
  - EEPROMs
  - Temperature sensor
  - SPD EEPROM
- EJTAG connector
- PROMICE connector
- Four character LED

FIRMWARE FEATURES

The Common Firmware Environment (CFE) is designed to be easily portable to designs incorporating current and future Broadcom MIPS64-compatible broadband processors. Supported platforms include Broadcom's SiByte processor family (containing the BCM1250, BCM1125H, and other processors), 32-bit and 64-bit memory models, and big and little-endian operation. There are many parameters configurable at build time that can be used to customize CFE to suit diverse customer requirements.

On the BCM91125E, CFE can load programs (such as S-records, raw binary, or ELF formatted) from bootstrap devices in a variety of ways, including:

- Via either Ethernet port, from a TFTP server
- Via the serial port (S-records only)

For additional information on CFE, refer to the *Common Firmware Environment (CFE) Specification* document that can be found in the CFE source code distribution at: http://sibyte.broadcom.com/public.

Section 2: Getting Started

Complete the following steps to get to a BCM91125E CFE (firmware) prompt.

1. Connect a 9-pin null modem cable to the serial port of the BCM91125E and to a serial port on a workstation/PC.
2. Use a terminal program and set it to 115200 bps, 8-bit data, 1-stop bit, no parity, and no flow control.
3. Power up the BCM91125E by plugging in a standard hard drive power connector.

   After a short delay, the CFE initialization output and serial console prompt should display. The following is an example of the output:

```
CFE version 1.0.37 for BCM91125E (64bit,SP,BE)
Build Date: Fri Jul 11 10:46:42 PDT 2003
Copyright (C) 2000,2001,2002,2003 Broadcom Corporation.

Initializing Arena.
Initializing PCI. [ldt_rev_017]
HyperTransport: 600 MHz
HyperTransport not initialized: InitDone not set
Initializing Devices.
BCM91125E board revision 1
PCIIDE: 0 controllers found
Config switch: 2
CPU: 1125H A1
L2 Cache: 256KB
SysCfg: 0080000020C20600 [PLL_DIV: 12, IOB0_DIV: CPUCLK/4, IOB1_DIV: CPUCLK/3]
CPU type 0x40103: 600MHz
Total memory: 0x8000000 bytes (128MB)

Total memory used by CFE:  0x87E8B300 - 0x88000000 (1527040)
Initialized Data:          0x87E8B300 - 0x87E95080 (40320)
BSS Area:                  0x87E95080 - 0x87E95770 (1776)
Local Heap:                0x87E95770 - 0x87F95770 (1048576)
Stack Area:                0x87F95770 - 0x87F97770 (8192)
Text (code) segment:       0x87F97780 - 0x87FFFFB8 (428088)
Boot area (physical):      0x07E4A000 - 0x07E8A000
Relocation Factor:         I:E8397780 - D:05F8B300
CFE>
```

4. At the prompt, a program can be run via the network from a TFTP server by doing the following:
   a. Connect the BCM91125E Ethernet port E0 with an Ethernet cable to a switch, repeater, or directly to the Ethernet port of the file server.

      

      Note: Because the Broadcom PHYs handle direct connects automatically, a crossover cable for direct connects is not needed.

   b. To initialize Ethernet port E0, type the following:

```
ifconfig eth0 -auto
```

      

      Note: The ifconfig eth0 -auto command can only be used with a DHCP server.

   c. To run a program, type the following:

```
boot -elf tftp_server:/path_to_software/program
```

Section 3: Physical Description

The BCM91125E is implemented in the standard full length PCI card form factor. Figure 2 shows a front view of the BCM91125E.

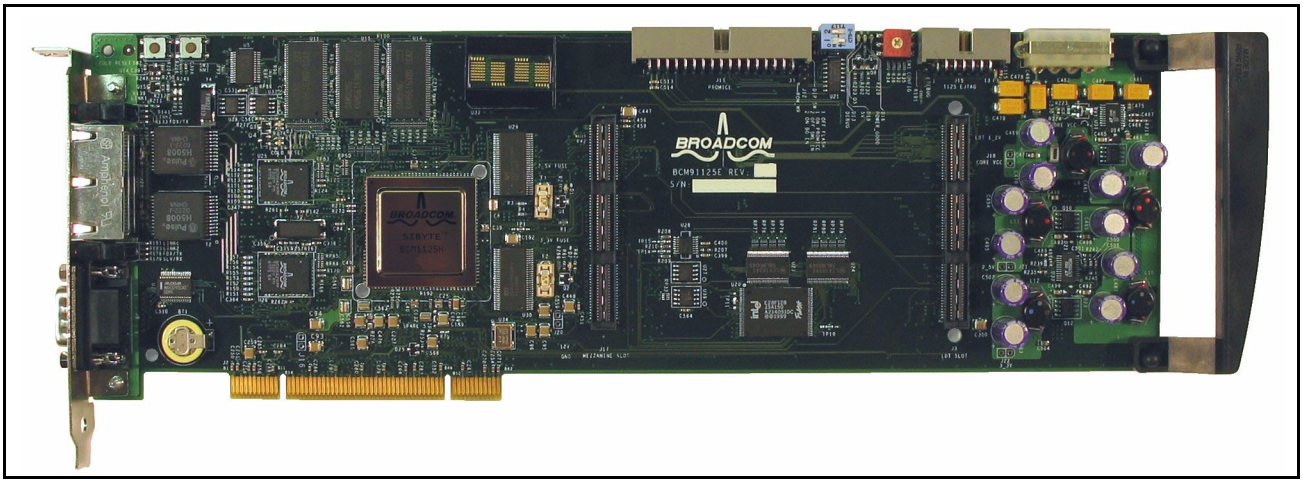

Figure 2: Front View

CONNECTORS

Figure 3 shows the location of each of the connectors on the board. These connectors are defined in Table 1. Exact pin descriptions for the more complex connectors are documented in “Supplemental Information” on page 15.

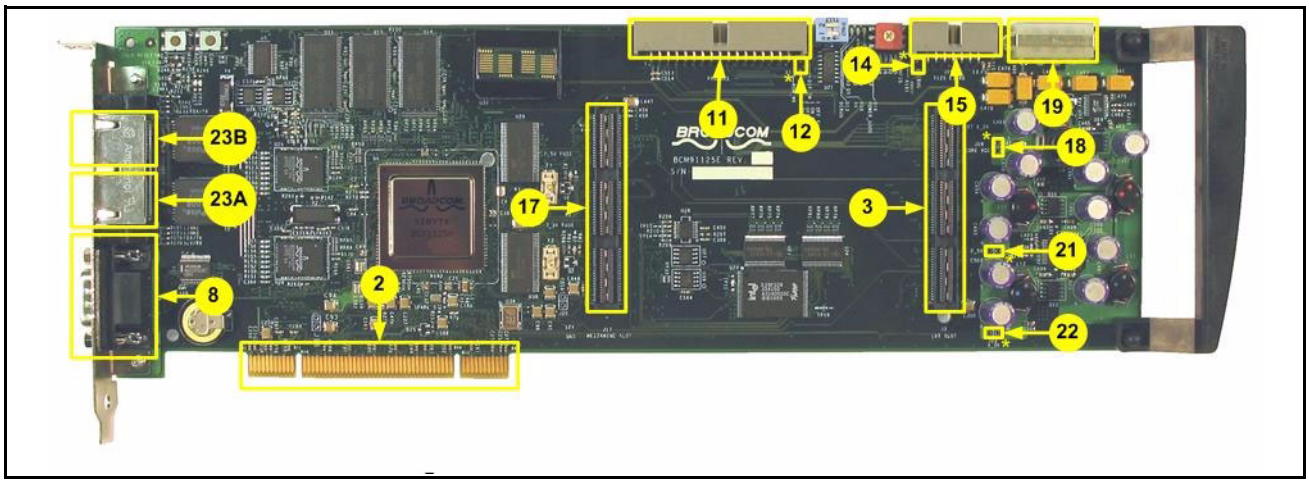

Figure 3: Connector Locations

Table 1: Connector Descriptions

Board ID	*Description*
J2	Dual-sided 62-pin edge finger PCI connector.
J3	HyperTransport socket for motherboards (see Table 14 on page 15).
J8	Serial port 0 RS-232 connector.
J11	ROM emulator connector (see Table 16 on page 19).
J12	ROM emulator write line (pin1* = IO_WR_L, pin2 = no connect).
J14	DEBUG_L trigger for scope (pin1* = GND, pin2 = DEBUG_L).
J15	EJTAG connector.
J17	Mezzanine connector (see Table 15 on page 17).
J18	1.2V core supply sense (pin1* = GND, pin2 = 1.2V).
J19	Standard hard drive power supply connector.
J21	2.5V supply sense (pin1* = GND, pin2 = 2.5V).
J22	3.3V supply sense (pin1* = GND, pin2 = 3.3V).
J23A	10/100/1000 Mbps Ethernet Port E1.
J23B	10/100/1000 Mbps Ethernet Port E0.

* = Pin1 located is indicated by the * on this figure. It can also be identified by viewing the back of the board for the square solder pad.

LEDs

Figure 4 shows the locations of the LEDs. The LEDs are described in Table 2.

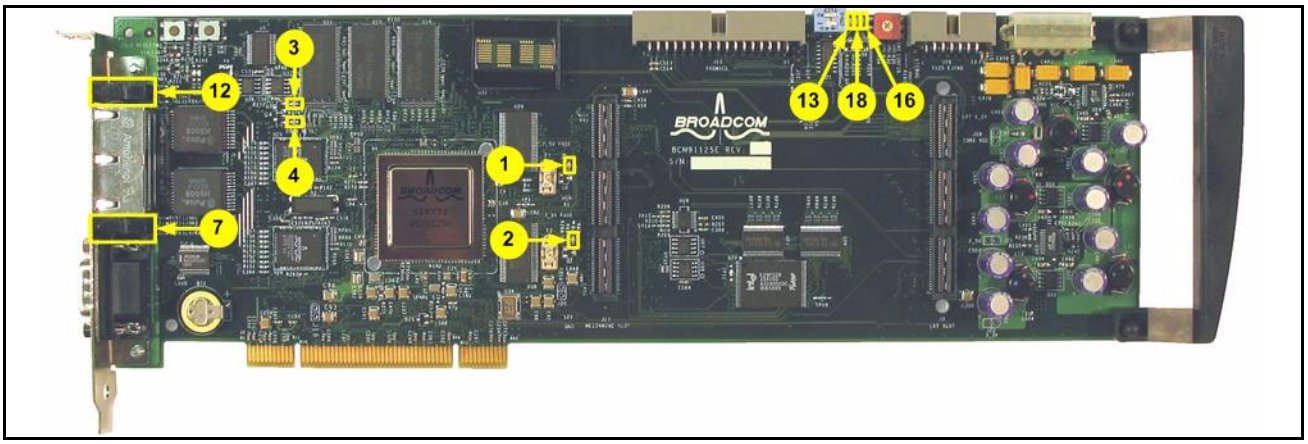

Figure 4: LED Locations

Table 2: LED Descriptions

Board ID	*Color*	*Description*
D1	Red	2.5V Fuse blown indicator.
D2	Red	3.3V Fuse blown indicator.
D3	Yellow	System reset.
D4	Yellow	Cold reset.
D7 *		**Ethernet Port E1 PHY LEDs**
	Red	Link2 = Speed indicator.
	Green	Link1 = Speed indicator.
	Yellow	Fdx = Full-duplex indicator.
	Green	Slv = Slave indicator.
	Yellow	Act = Transmit and receive activity indicator.
	Green	Link = Link quality indicator.
D12 *		**Ethernet Port E0 PHY LEDs**
	Red	Link2 = Speed indicator.
	Green	Link1 = Speed indicator.
	Yellow	Fdx = Full-duplex indicator.
	Green	Slv = Slave indicator.
	Yellow	Act = Transmit and receive activity indicator.
	Green	Link = Link quality indicator.
D13	Green	Debug LED.
D16	Green	3.3V power good.
D18	Green	5V.
* = LEDs visible from the board's side panel.		

FUSES AND BATTERY

Figure 5 shows the positions of the fuses and battery. Table 3 describes each fuse or battery.

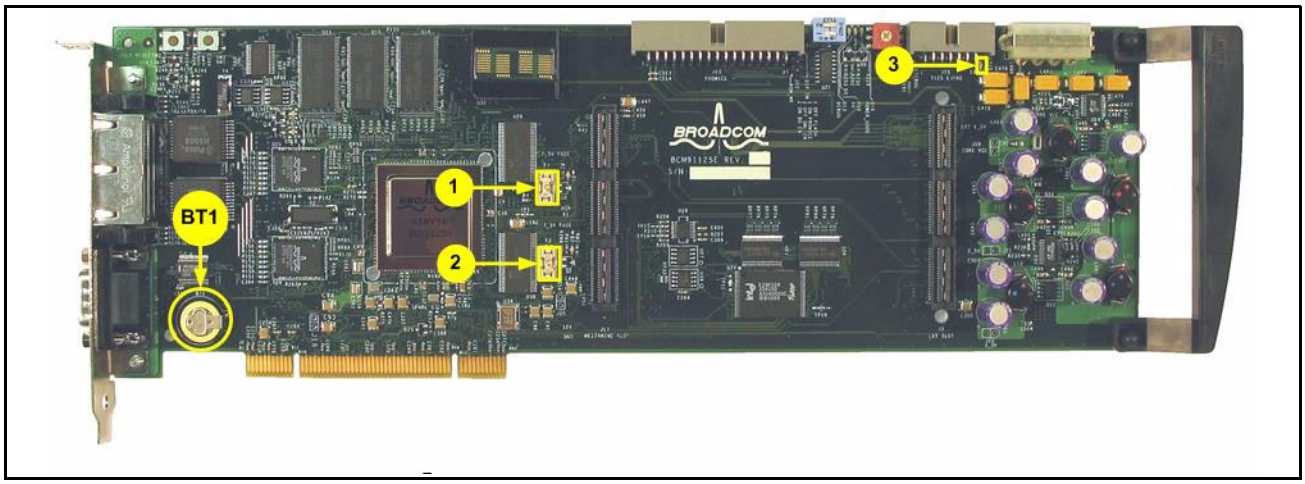

Figure 5: Fuses and Battery Callouts

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Table 3: Fuses and Battery Descriptions

Board ID	*Function*
F1	BCM1125H 2.5V current limit, 5A.
F2	BCM1125H 3.3V current limit, 1A.
F3	EJTAG 3.3V, 1A current limit fuse.
BT1	RTC battery.

SWITCHES AND PUSHBUTTONS

Figure 6 shows the locations of each of the switches and pushbuttons. Table 4 describes the function of each switch or pushbutton.

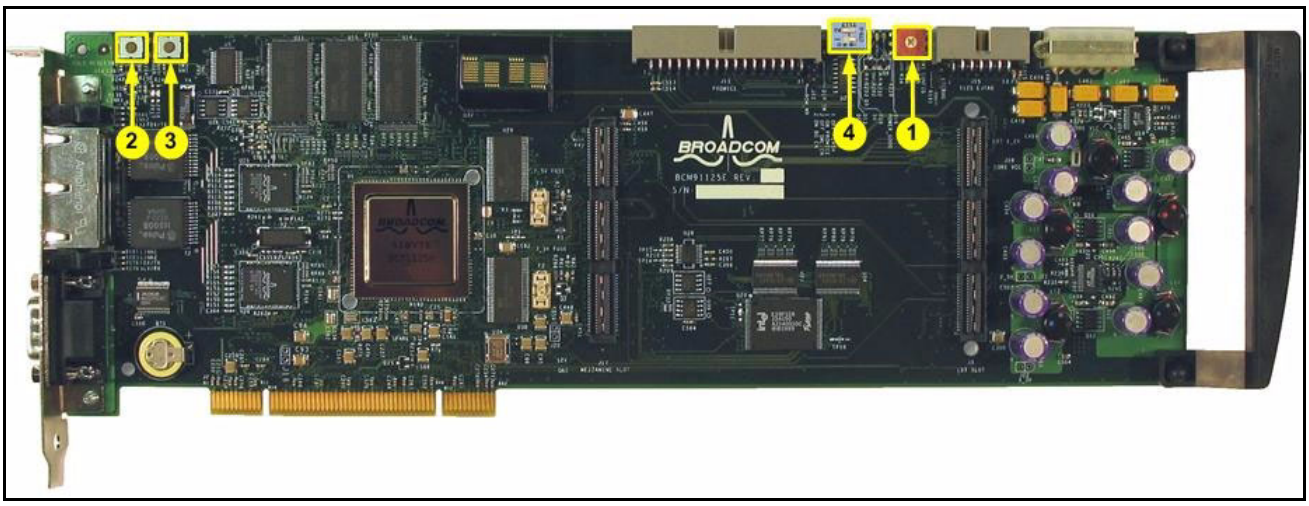

Figure 6: Switch Callouts

Table 4: Switch Descriptions

Board ID	*Function*	*Default*
SW1	16-position rotary switch to set the power-on state of IO_AD[31-28], which are captured in system_cfg[31:28], also called the config[5:2]. These bits are used by the CFE to select the firmware configuration according to Table 7, and could be used for other purposes according to customer software requirements.	0x2
SW2	Cold Reset is asserted when the button is pressed.	N/A
SW3	NMI (GPIO 8) is asserted when the button is pressed.	N/A
SW4	2-position DIP switch, for hardware configuration. These bits have dedicated purposes that do not change under firmware control.	
	Bit[2] = Big Endian enable (ON = big endian, OFF = little endian).	ON
	Bit[1] = Boot from ROM emulator (ON = ROM emulator, OFF = Flash). See also Table 5.	OFF

Section 4: Firmware Configuration

This section contains information that is useful to software and firmware developers working with the board.

ENDIANNESS

The firmware image in the flash is bi-endian, so it supports both big and little-endian operation. This can be selected by Switch 4, Bit 2.

GENERIC BUS CHIP SELECTS AND MEMORY MAP

Table 5 describes how the generic bus devices are connected to chip selects, and the default memory addresses and sizings used by CFE. Programmers can alter the sizing of the blocks and the location in memory of each chip select except CS0 by modifying CFE.

Table 5: Generic Bus Chip Selects and Memory Map

Chip Select	*Description*	*Physical Memory Address*	*Size*
CS0	Boot ROM *	0x1FC0_0000	16 MB
CS1	Alternate Boot ROM *	0x1EC0_0000	16 MB
CS6	HP HDLO-2416 LED display	0x1D0A_0000	64 KB

* Intel® E28F128J3A boot flash memory or ROM emulator, depending on Switch 4 bit 0 setting (see Table 4).

GPIO PINS

Table 6 lists the wiring and firmware configuration for the BCM1125H GPIO pins.

Table 6: GPIO Map

GPIO Pin #	*BCM1125H Pin Direction*	*Description*
0	Output	Debug LED.
1	Input	OUT from RTC.
6	Input	HyperTransport interrupt, HT_INT_L.
7	Input	PHY_INT_L (ORed PHY interrupt from both BCM5421 PHY chips).
8	Input	NMI_L from switch SW3.
9	Input	TEMP_ALERT_L from the temperature sensor.

Note: All GPIO[15:0] pins are routed to the mezzanine connector as well. See Table 15 for details.

SWITCH 1 FIRMWARE CONFIGURATION

Table 7 lists how the firmware interprets the software configuration bits indicated by Switch 1. Once the user determines a desired configuration, it can be hardcoded and the switch is available for other uses. It is read as bits 31-28 of the system_configuration register (field config[5:2]).

Table 7: Switch 1 Firmware Configuration

SW1 value	***Action***
0x0	UART console, no PCI initialization
0x1	PromICE console, no PCI initialization
0x2*	UART console, PCI initialization
0x3	PromICE console, PCI initialization
0x6	UART console, PCI initialization, Hypertransport (HT) slave mode
0x7	UART console, no PCI initialization, do not read CFE environment variables. Use of this setting is strongly discouraged.
0x8	UART console, PCI initialization, device download mode
0x9	UART console, PCI initialization, device reboot mode
0x14	UART console, program SPD EEPROM
* = recommended/default setting. All other settings are reserved.	

PCI INTERRUPT MAP

Table 8 shows the mapping of PCI interrupts from the BCM1125H to the connector.

Table 8: PCI Interrupt Map

Description	*Interrupt Map*
32-bit universal PCI connector.	BCM1125H PCI INTA = PCI Connector (J2) INTA

SMBUS PERIPHERALS

Table 9 shows how the SMBus peripherals are distributed over the two SMbus channels on the BCM1125H, as well as the addresses used by each of the peripherals.

Table 9: SMBus Peripherals

SMBus Channel	*SMBus Address*	*Description*
0	0x2A	Maxim MAX6654 temperature sensor.
0	0x50	Microchip 28LC128C EEPROM.
0	0x54	Atmel AT24C02 SPD EEPROM.
1	0x50	Microchip 28LC128C EEPROM.
1	0x68	ST Microelectronics M41T81 RTC.

Section 5: Troubleshooting

CORRECTIVE PROCEDURES

1. When CFE is not able to initialize the system and reach the console prompt, the four-character alphanumeric LED display may be used to help debug the initialization sequence. When the Cer2 message appears, a cache error has occurred. This frequently occurs when the BCM1125H is either undercooled or is in a low-voltage situation. Ensure that the correct voltage and cooling is being provided. For other LED message descriptions, refer to the *Common Firmware Environment (CFE) Specification* document.
2. There is no output coming from the serial boot console, but the four-character LED displays *CFE*. Because CFE uses serial port 0 by default, ensure that a standard 9-pin RS232 null-modem cable connection is being used. Also ensure that the terminal program is set to a baud rate of 115200, 8-bit, no parity, no flow control.

REPLACEMENT PARTS

Table 10: Replacement Parts

Board ID	*Description*	*Manufacturer*	*Manufacturer ID*	*Web Information*
F1	BCM1125H 2.5V power 5A current limit	Littelfuse®	154005	http://www.littelfuse.com
F2	BCM1125H 3.3V power 1A current limit	Littelfuse®	154001	http://www.littelfuse.com
F3	EJTAG connector 0.5A 32V surface mounted fuse.	Littelfuse®	434.500	http://www.littelfuse.com
BT1	RTC battery.	Panasonic	BR1225/1HC	www.panasonic.com

Section 6: Web Resources

SiByte

Table 11: SiByte Web Resources

Resource	Website
BCM1250 and BCM1125H User Manual	http://sibyte.broadcom.com/public/resources/
SB-1 Core User Manual	
General information	http://sibyte.broadcom.com/public/

Peripherals

Table 12: Peripheral Web Resources

Resource	Website
Maxim MAX6654 temperature sensor	www.maxim-ic.com
Microchip 24LC128C serial EEPROM	www.microchip.com
ST Microelectronics M41T81serial RTC	www.st.com
Samsung K4H561638D-TCA2 256Mb DDR SDRAM	www.samsung.com
HP HDLO-2416 four-character alphanumeric display	www.agilent.com
Atmel AT24C02 serial EEPROM (SPD for memory)	www.atmel.com
Broadcom BCM5421 10/100/1000BASE-T Gigabit Copper Transceiver	www.broadcom.com
Intel E28F128J3A 128 Mbit Strataflash® Memory	www.intel.com
Samtec connector QSE-060-01-FDA (J3 and J17)	www.samtec.com

Bus Interface

Table 13: Bus Interface Web Resources

Resource	Website
HyperTransport specification	www.hypertransport.org
EJTAG specification	www.mips.com
PCI specification	www.pcisig.com

Section 7: Supplemental Information

PINOUT FOR HYPERTRANSPORT SOCKET (J3)

Table 14 shows the location of the pins of the HyperTransport Socket, J3. The middle pins (121-132) are not shown though since they are all connected to ground (GND).

More information about these connectors can be found in “Web Resources” on page 14.

Table 14: Pinout For Hypertransport Socket (J3)

Odd Pin Name	*Odd Pin Number*	*Even Pin Number*	*Even Pin Name*
VDD33	1	2	VDD33
VDD33	3	4	VDD33
VDDLDT	5	6	VDDLDT
GND	7	8	GND
TCK	9	10	CLK100
TMS	11	12	GND
TDI	13	14	RDY
TDO	15	16	OE_L
TRST_L	17	18	WR_L
SCL	19	20	CS_L0
SDA	21	22	CS_L1
LDT_RESET_L	23	24	INT
LDT_PWROK	25	26	RESET_L
GND	27	28	GND
LDT_RX_CTLn	29	30	LDT_TX_CADp0
LDT_RX_CTLp	31	32	LDT_TX_CADn0
GND	33	34	GND
LDT_RX_CADn7	35	36	LDT_TX_CADp1
LDT_RX_CADp7	37	38	LDT_TX_CADn1
GND	39	40	GND
GND	41	42	GND
LDT_RX_CADn6	43	44	LDT_TX_CADp2
LDT_RX_CADp6	45	46	LDT_TX_CADn2
GND	47	48	GND
LDT_RX_CADn5	49	50	LDT_TX_CADp3
LDT_RX_CADp5	51	52	LDT_TX_CADn3
GND	53	54	GND
LDT_RX_CADn4	55	56	LDT_TX_CLKp

Table 14: Pinout For Hypertransport Socket (J3) (Cont.)

Odd Pin Name	Odd Pin Number	Even Pin Number	Even Pin Name
LDT_RX_CADp4	57	58	LDT_TX_CLKn
GND	59	60	GND
GND	61	62	GND
LDT_RX_CLKn	63	64	LDT_TX_CADp4
LDT_RX_CLKp	65	66	LDT_TX_CADn4
GND	67	68	GND
LDT_RX_CADn3	69	70	LDT_TX_CADp5
LDT_RX_CADp3	71	72	LDT_TX_CADn5
GND	73	74	GND
LDT_RX_CADn2	75	76	LDT_TX_CADp6
LDT_RX_CADp2	77	78	LDT_TX_CADn6
GND	79	80	GND
GND	81	82	GND
LDT_RX_CADn1	83	84	LDT_TX_CADp7
LDT_RX_CADp1	85	86	LDT_TX_CADn7
GND	87	88	GND
LDT_RX_CADn0	89	90	LDT_TX_CTLp
LDT_RX_CADp0	91	92	LDT_TX_CTLn
GND	93	94	GND
AD0	95	96	AD9
AD1	97	98	AD24
AD2	99	100	AD25
AD3	101	102	AD26
AD4	103	104	AD27
AD5	105	106	AD28
AD6	107	108	AD29
AD7	109	110	AD30
AD8	111	112	AD31
GND	113	114	GND
VDDLDT	115	116	VDDLDT
VDD33	117	118	VDD33
VDD33	119	120	VDD33

PINOUT FOR MEZZANINE CONNECTOR (J17)

Table 15 shows the location of the pins of the Mezzanine connector. The middle pins (121-132) are not shown though since they are all connected to ground (GND).

More information about these connectors can be found in “Web Resources” on page 14.

Table 15: Pinout For Mezzanine Connector (J17)

Odd Pin Name	*Odd Pin Number*	*Even Pin Number*	*Even Pin Name*
VDD33	1	2	VDD33
VDD33	3	4	VDD33
VDD50	5	6	VDD50
GND	7	8	GND
E1_RCLK	9	10	E1_TCLKI
GND	11	12	GND
E1_RXD7	13	14	E1_TCLKO
GND	15	16	GND
E1_RXD6	17	18	E1_TXD7
GND	19	20	GND
E1_RXD5	21	22	E1_TXD6
GND	23	24	GND
E1_RXD4	25	26	E1_TXD5
GND	27	28	GND
E1_RXD3	29	30	E1_TXD4
GND	31	32	GND
E1_RXD2	33	34	E1_TXD3
GND	35	36	GND
E1_RXD1	37	38	E1_TXD2
GND	39	40	GND
E1_RXD0	41	42	E1_TXD1
GND	43	44	GND
E1_RXDV	45	46	E1_TXD0
GND	47	48	GND
E1_RXER	49	50	E1_TXEN
GND	51	52	MEZ_MAC_PRSNT_L
E1_COL	53	54	E1_TXER
GND	55	56	GND
E1_CRS	57	58	E1_MDC
GND	59	60	GND
E1_MDIO	61	62	REFCLK02

Table 15: Pinout For Mezzanine Connector (J17) (Cont.)

Odd Pin Name	Odd Pin Number	Even Pin Number	Even Pin Name
GND	63	64	GND
IO_RD_WR	65	66	GPIO15
IO_CS_L3	67	68	GPIO14
IO_CS_L4	69	70	GPIO13
IO_ALE	71	72	GPIO12
GND	73	74	GPIO11
S1_DIN	75	76	GPIO10
S1_DIN_RCLKIN	77	78	GPIO9
S1_CTS_TCLKIN	79	80	GPIO8
S1_RIN	81	82	GND
GND	83	84	GPIO7
S1_TIN	85	86	GPIO6
S1_DOUT	87	88	GPIO5
S1_COUT	89	90	GPIO4
S1_RTS_TSTROBE	91	92	GPIO3
GND	93	94	GPIO2
IO_AD10	95	96	GPIO1
IO_AD11	97	98	GPIO0
IO_AD12	99	100	GND
IO_AD13	101	102	IO_AD14
GND	103	104	IO_AD16
IO_AD15	105	106	IO_AD18
IO_AD17	107	108	IO_AD20
IO_AD19	109	110	IO_AD22
IO_AD21	111	112	IO_AD23
GND	113	114	VDDN120
VDD50	115	116	VDD50
VDD33	117	118	VDD120
VDD33	119	120	VDD120

ROM EMULATOR PINOUT

Table 16 shows the location of the pins of the connector. All I/O signals on this connector are 3.3 V outputs that are tolerant of 5V inputs.

Table 16: ROM Emulator Pinout

Odd Pin Name	*Odd Pin Number*	*Even Pin Number*	*Even Pin Name*
GND	1	2	AD20
3.3 V PWR	3	4	AD19
AD18	5	6	AD16
AD17	7	8	AD15
AD14	9	10	AD12
AD13	11	12	AD7
AD8	13	14	AD6
AD9	15	16	AD5
AD11	17	18	AD4
OE_L	19	20	AD3
AD10	21	22	AD2
ROMEMUCS_L	23	24	AD1
AD31	25	26	AD0
AD30	27	28	AD24
AD29	29	30	AD25
AD28	31	32	AD26
AD27	33	34	GND

Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, CA 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710