EPSON

No. FQI 05-0245 B

PLX TECHNOLOGY INC

SEIKO EPSON RELIABILITY REPORT

DEVICE PART NUMBER: PCI9054-AC50PI (Sn-Pb)

PACKAGE TYPE: QFP-21 176 PIN

14/July/2005

IC CS QUALITY ASSURANCE DEPARTMENT
SEMICONDUCTOR OPERATIONS DIVISION
SEIKO EPSON CORPORATION

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TEST RESULTS OF RELIABILITY TEST

The followings are our reliability report for this device.

There is no anomaly, and we assure this device have enough reliability

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[RELIABILITY TEST RESULTS]

1. LIFE TEST

No	TEST ITEM	TEST CONDITION	SAMPLE SIZE	TEST DURATION	DEVICE HOURS	FAILURES	REMARKS
1	HIGH TEMPERATURE WITH BIAS	125℃, 4.0V, 7.0V, CLK	135	1,000 H	135,000 H	0	
2	TEMPERATURE/ HUMIDITY WITH BIAS	85℃, 85%RH, 4.0V, 7.0V	135	1,000 H	135,000 H	0	

2. ENVIRONMENTAL TEST

No	TEST ITEM	TEST CONDITION	SAMPLE SIZE	TEST DURATION	FAILURES	REMARKS
1	HIGH TEMPERATURE STORAGE	Ta=150℃	45	1,000 H	0	
2	TEMPERATURE CYCLING	-65℃ ～ 150℃ Each more than 10 minutes	45	200 cyc.	0	
3	PRESSURE COOKER	Ta=121℃、2.0E5 Pa	45	200 H	0	

2. ENVIRONMENTAL TEST (Cont'd)

No	TEST ITEM	TEST CONDITION	SAMPLE SIZE	TEST DURATION	FAILURES	REMARKS
4	TERHMAL SHOCK	0℃～100℃ Each 5 minutes	22	10 cyc.	0	
5	SALT ATMOSPHERE	Ta=35℃、NaCl=5%	22	48 H	0	
6	RESISTANCE TO SOLDERING HEAT	Pre-conditioning -> Reflow	45	2 Time	0	
7	RESISTANCE TO SOLVENT	Isopropyl Alcohol	22	1 Time	0	

3. MECHANICAL TEST

No	TEST ITEM	TEST CONDITION	SAMPLE SIZE	TEST DURATION	FAILURES	REMARKS
1	LEAD INTEGRITY (TENSION)	2.5N ,10 seconds	22	1 Time	0	
2	LEAD INTEGRITY (BEND)	90 °	22	2 Times	0	
3	SOLDERABILITY 1	Steam Aging 4H -> 215℃、5 seconds	22	1 Time	0	
4	SOLDERABILITY 2	150℃、16H -> 215℃、5 seconds	22	1 Time	0	

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[ESD/ LATCH-UP TEST RESULTS]

1. ESD TEST RESULTS (Broken Voltage)

(Sample Size: each n=3)

TEST CONDITION	PIN	VDD LINE - GND	VSS LINE - GND
C=200pF、R=0Ω、1 Time	PIN -	500V	>500V
	PIN +	350V	450V
C=100pF、R=1.5KΩ、3 Times	PIN -	>4000V	>4000V
	PIN +	>4000V	3500V

2. LATCH-UP TEST RESULTS

(Sample Size: each n=3)

TEST CONDITION	TRIGGER VOLTAGE (Vt)	TRIGGER CURRENT (It)	REMARK
+ Trigger	2. 0V<	476. 7mA<	*
- Trigger	1. 8V<	555. 8mA<	*

"*" on remark colum means that Latch-up was not occured.
The followings are our judgement level;
160mW ≦ [Tregger Voltage] × [Trigger Current]

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RELIABILITY TEST CONDITION AND CRITERIA (1)

No	TEST ITEM	TEST CONDITION	STANDARD	CRITERIA
1	HIGH TEMPERATURE WITH BIAS	Ta=125℃ (Absolute maximum rating) V、 (A certain frequency) Hz	EIAJ-ED-4701/100 Test Method 101 MIL-STD-883 1005	Must meet the electrical characteristics specification
2	TEMPERATURE/ HUMIDITY WITH BIAS	Ta=85℃、85%RH (Absolute maximum rating) V、 (A certain frequency) Hz	EIAJ-ED-4701/100 Test Method 102	Must meet the electrical characteristics specification
3	HIGH TEMEPERATURE STORAGE	Ta=150℃	EIAJ-ED-4701/200 Test Method 201 MIL-STD-883 1008	Must meet the electrical characteristics specification
4	TEMPERATURE CYCLING	-65℃ ～ 150℃ Each more than 10 minutes	EIAJ-ED-4701/100 Test Method 105 MIL-STD-883 1010	Must meet the electrical characteristics specification
5	PRESSURE COOKER	Ta=121℃、2.0E5 Pa	EIAJ-ED-4701/100 Test Method 103	Must meet the electrical characteristics specification
6	THERMAL SHOCK	0℃～100℃ Each 5 minutes	EIAJ-ED-4701/300 Test Method 307 MIL-STD-883 1011	Must meet the electrical characteristics specification
7	SALT ATMOSPHERE	Ta=35℃、NaCl=5%	EIAJ-ED-4701/200 Test Method 204 MIL-STD-883 1009	Must meet the electrical characteristics specification
8	RESISTANCE TO SOLDER HEAT	Pre-conditioning -> Reflow	EIAJ-ED-4701/300 Test Method 301,302	Must meet the electrical characteristics specification
9	RESISTANCE TO SOLVENT	Isopropyl Alcohol	EIAJ-ED-4701/500 Test Method 501 MIL-STD-883 2015	The marking shoud be read.

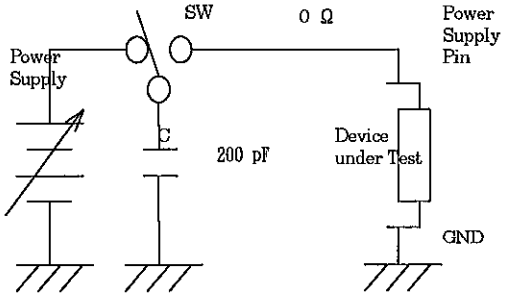
RELIABILITY TEST CONDITION AND CRITERIA (2)

No	TEST ITEM	TEST CONDITION	STANDARD	CRITERIA
10	LEAD INTEGRITY (Pull)	Pull: DIP - 10N, QFP - 2.5N 10 seconds	EIAJ-ED-4701/400 Test MethoD 401 MIL-STD-883 2004	No cut, breakage, and looseness is found. Also, there is no sliding between leads and package body.
11	LEAD INTEGRITY (BEND)	90 °	EIAJ-ED-4701/400 Test Method 401 MIL-STD-883 2004	No cut, breakage, and looseness is found. Also, there is no sliding between leads and package body.
12	SOLDERABILITY	Steam Aging 4H -> 215℃, 5 seconds	EIAJ-ED-4701/300 Test Method 303 MIL-STD-883 2003	The specimen shoud have 95% or more of the dipped portion object of evaluation covered with solder, shoud have no concentration of pin holes, coids and other defects at one place, and more over these defects should not account for more than 5% of the overall surface.
13	VIBRATION FATIGUE (Vibration Frequency) * Only for hollow package	100Hz ~ 2000Hz Sweeping Time: 4 minutes, Acceleration: 200m/S^2 X·Y·Z each 4 time, 48 minutes	EIAJ-ED-4701/400 Test Method 403 MIL-STD-883 2007	Must meet the electrical characteristics specification.
14	VIBRATION FATIGUE (Fixed Frequency) * Only for hollow package	60Hz, Acceleration: 200m/S^2 X·Y·Z 96 Hours	EIAJ-ED-4701/400 Test Method 403 MIL-STD-883 2005	Must meet the electrical characteristics specification.

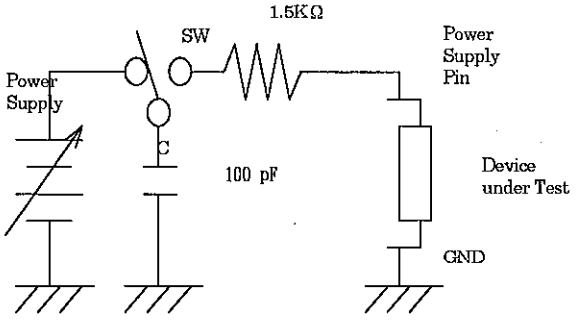
[ESD/LATCH-UP TEST PROCEDURE]

<ESD Test Procedure>

In order to determine the susceptibility levels of our device to ESD potential, testing is performed using the test circuit shown in following figures.



C= 200pF, 0Ω, 1 Time
Reference Standard : EIAJ ED-4701/300-(304)

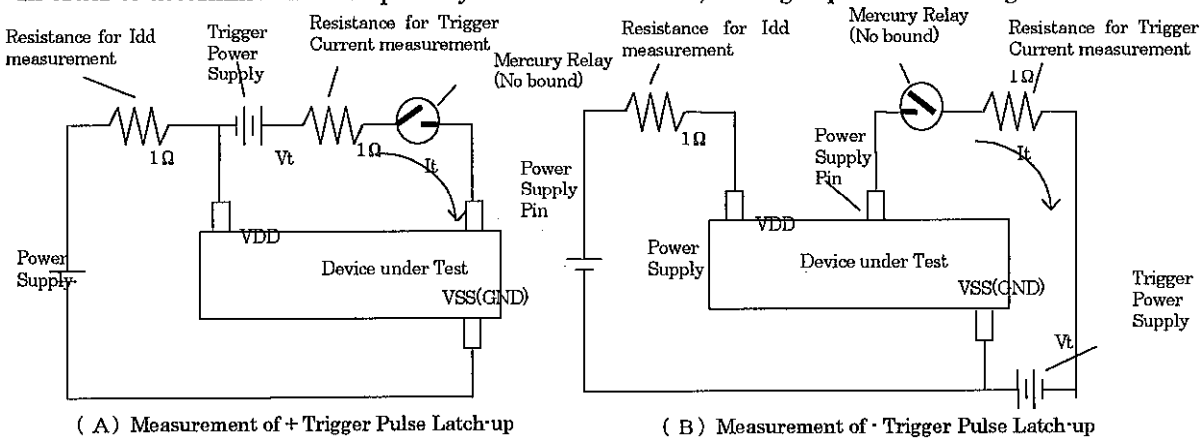


C= 100pF, 1.5KΩ, 3 Time
Reference Standard: EIAJ ED-4701/300-(304), MIL-STD-883, 3015

(1) After charging the condenser, switch the "SW" and apply the test voltage on each pins.
(2) Measure the all electrical parameters and the functions.
(3) If no failure is found, increase the voltage in steps. Continue testing until failure occurs.

<Latch-up Test Procedure>

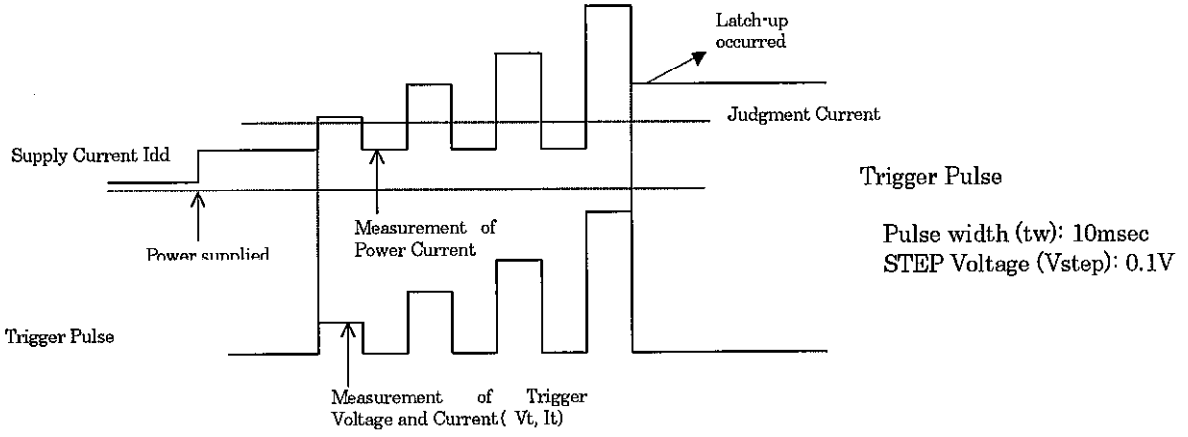
In order to determine the susceptibility levels of our device, testing is performed using the test circuit as follows;



(A) Measurement of + Trigger Pulse Latch-up

(B) Measurement of - Trigger Pulse Latch-up

The triggering pulse is applied as shown in Figure 2-2.



Trigger Pulse

Pulse width (tw): 10msec
STEP Voltage (Vstep): 0.1V

After increasing 0.1 volts Trigger Pulse step by step, the supply current are measured at each time. When the supply current is found to increase anomaly comparing with the current before stressing, we judge the latch up is occurred and the trigger voltage and trigger current just before latch up occurring is recorded.

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ESTIMATION OF FAILURE RATE

We estimate the failure rate of our device using the following method.

1. Acceleration Factor
The acceleration factor is estimated from the following equation;

$$\text{Acceleration Factor } A = \frac{F1}{F0} = \frac{C \cdot \exp(\beta \cdot VDD1 - Ea/KT1)}{C \cdot \exp(\beta \cdot VDD0 - Ea/KT0)}$$

Ea: Activation Energy (0.5 eV)
K: Boltzman's constant (8.62×10^{-5}eV・deg K)
β:Voltage Acceleration factor;
Empirical constant minimum
β= 3
C: Constant
F1: TTF at T0 (deg K)
F0: TTF at T1 (deg K)
VDD1: Voltage at acceleration test
VDD0: Voltage at use point
T1: Temperature at acceleration test
T0: Temperature at use point

The acceleration factor between 125 deg C/ 4.0 V and 40 deg C/ 3.3 V is;

A = 427.44

2. Intrinsic Failure Rate (IFR) Estimation
The failure rate of device in the field under normal operating condition is estimated by following equation.

$$\text{Intrinsic Failure Rate } F = \frac{r \times \alpha}{\Sigma (n \times T \times A)}$$

$$= \frac{0.92}{135 \times 1000 \times 427.44}$$

= 15.94 Fit (C.L. = 60 %)

r: Number of Failures α: Coefficient of Kai square low n: Sample Size
T: Test Duration A: Acceleration Factor r:Failures (If r=0, $r \times \alpha$= 0.92)

As a result of the above estimation, the IFR is estimated less than 16 FIT.